Design and Development of a Low Cost, Manufacturable High Voltage Power Module for Energy Storage Systems

Phase I SBIR

September 27, 2012

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Acknowledgements

• I would like to thank Dr. Imre Gyuk of the DOE Energy Storage Systems Program and Dr. Stan Atcitty for technical support.

• I would also like to thank
APEI, Inc. Manufacturing Facilities

• APEI, Inc. Class 1000 Manufacturing
• ISO 9001 Certified
• AS 9100 Certified

Engineering Samples

APE XT-1000 series SiC Power Modules
APE XT-254 SiC Discretes
APE T-2000 series SiC Gate Drivers
APE HT-2000 series SiC Power Modules
APE HT-DH series SiC Gate Drivers
APE XT- series SiC Gate Drivers
SBIR Program Goals

Design and develop a high performance, high voltage SiC multi-chip power module (MCPM) that targets energy storage applications.

Phase I
- 2012: Start Program
- 2013: Develop HV packaging approach and demonstrate it via hardware testing

Phase II
- 2014: Design HV SiC MCPM based on hardware demonstrator
- 2015: Build and perform electrical, thermal, and reliability testing for the HV SiC half-bridge MCPM

Phase III
- APEI, Inc. will work with its partners to transition this HV MCPM technology to a commercial product

Key Deliverables:
- Discrete HV hardware demonstrator and MCPM design
- High Performance HV Half-bridge SiC MCPMs
HV SiC Power Modules Reduce Energy Storage System Size and Complexity

Multi-level converters reduce voltage stress on power devices:

Two-Level Phase Leg
\[ V_{DS,\text{max}} = V_{dc} \]

Three-Level Phase Leg
\[ V_{DS,\text{max}} = V_{dc}/2 \]

ABB’s SVC Light energy storage system

Comparison of solutions for a 11 kV 600 kW ESS

<table>
<thead>
<tr>
<th>Technology</th>
<th>Power Electronics</th>
<th>Relative Size/Mass</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( V_{BD} )</td>
<td>( T_j (°C) )</td>
</tr>
<tr>
<td>Si Device</td>
<td>6.5 kV</td>
<td>125</td>
</tr>
<tr>
<td>SiC Device</td>
<td>12 kV</td>
<td>175</td>
</tr>
<tr>
<td>SiC Device</td>
<td>12 kV</td>
<td>225</td>
</tr>
</tbody>
</table>

Other Targeted Applications

Solid State Transformers

- Replace passive transformers with power electronic converters to reduce size
- Isolation transformer size proportional to frequency

Solid State Transformer²

Comparison of solutions for a 13.8 kV / 480 V 100 kVA substation transformer

<table>
<thead>
<tr>
<th>Technology</th>
<th>Power Electronics</th>
<th>Isolation Transformer</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_{BD}$</td>
<td>$T_j$ (°C)</td>
</tr>
<tr>
<td>Passive</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Si Device</td>
<td>6.5 kV</td>
<td>125</td>
</tr>
<tr>
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# Existing HV Power Modules vs. Next Generation HV Power Modules

<table>
<thead>
<tr>
<th>Existing HV Silicon (Si) Power Modules</th>
<th>APEI’s HV Silicon Carbide (SiC) Power Module Developed in this SBIR Program</th>
</tr>
</thead>
<tbody>
<tr>
<td>Larger volume/weight than desired</td>
<td>Reduced volume/weight =&gt; Simplify system</td>
</tr>
<tr>
<td>Limited voltage blocking capability (&lt; 5kV)</td>
<td>High voltage (&gt; 15 kV) capable</td>
</tr>
<tr>
<td>Lower switching frequency</td>
<td>Demonstrated high switching frequency</td>
</tr>
<tr>
<td>Lower efficiency</td>
<td>Higher efficiency due to low conduction losses</td>
</tr>
<tr>
<td>Requires bulky magnetics and filter capacitors</td>
<td>Small magnetics and filter capacitors</td>
</tr>
<tr>
<td>Maximum operation temperature is below &lt; 125°C</td>
<td>High operation temperature &gt; 200°C</td>
</tr>
<tr>
<td>Higher thermal resistance</td>
<td>Low thermal resistance due to high thermal conductivity of SiC</td>
</tr>
</tbody>
</table>

Simply increasing the size of existing Si power modules does not take advantage of the superior properties of SiC.

![HV Si Single Switch IGBT Module](image)

6.5 kV / 750 A, 78 in³, 1.8 kg
APEI’s SiC Power Module Package Design Dramatically Improves Performance

If the power module design is not optimized, switching losses are exacerbated at high voltage

HT-2000
- 22 × reduction in turn off losses
- 17% reduction in on-state resistance
- 20% improvement in thermal resistance
- 50% increase in current capability

MSK (MOSFET)
- \( V_{DS} = 300\text{VDC} \)
- \( I_{DS} = 45 \text{Amps} \)
- \( \text{Turn On} = 47\text{ns} \)
- \( E_{on} = 2700 \mu\text{J} @ 300\text{V} / 90\text{A} \)

PowerEx (MOSFET)
- \( V_{DS} = 300\text{VDC} \)
- \( I_{DS} = 60 \text{Amps} \)
- \( \text{Turn On} = 22\text{ns} \)
- \( E_{on} = 1600 \mu\text{J} @ 300\text{V} / 90\text{A} \)

APEI HT-2000 (MOSFET)
- \( V_{DS} = 600\text{VDC} \)
- \( I_{DS} = 120 \text{Amps} \)
- \( \text{Turn On} = 14\text{ns} \)
- \( E_{on} = 70 \mu\text{J} @ 300\text{V} / 120\text{A} \)
- \( E_{on} = 300 \mu\text{J} @ 600\text{V} / 120\text{A} \)
Key Benefits of APEI’s HV MCPM Package Design

- Low junction-to-case thermal resistance => reduces size of cooling system
- Low module parasitics due to wire bondless interconnections => enables high switching frequency
- Ease of manufacturing
- Reliability
- Reworkability
- Reduction in volume/weight
Discrete Package Will Demonstrate High Performance, HV Package Design

- Device neutral
- High temperature capable (>200°C)
- Low volume
- Low profile
- Wire bondless interconnections
- Improved reliability
- Low resistance and inductance
- Reworkable
Discrete Package Thermal Simulations Demonstrate High Thermal Performance for Passive Cooling

- Passive cooling is possible for 200 W of thermal loss due to the low thermal resistance of the package
- Passive cooling significantly simplifies system
Summary

• Completed HV conceptual discrete package design
• Developed thermal model and confirmed high thermal performance using advanced packaging materials and techniques
• Developed HV design rules
• Targeted applications were identified and analyzed in more detail
Phase I Future Tasks

- Further investigate ESS applications and work with customers to develop target specs
- Finalize HV discrete package design
- Perform full thermal-mechanical stress analysis on packaging approach
- Fabricate, assemble, and test feasibility of packaging concepts
- Perform high voltage electrical parasitic design and analysis and compare with other conventional packaging approaches
- Half-bridge Power Module Mechanical and thermal Design
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