Large Area SiC Gate Turn Off (GTO) Thyristor Development

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## Why Silicon Carbide Power Devices?

<table>
<thead>
<tr>
<th>Property - Silicon Carbide vs Silicon</th>
<th>Performance of SiC Power Device</th>
<th>Impact AC-DC/DC-AC circuits</th>
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</thead>
<tbody>
<tr>
<td>Breakdown Field (10X)</td>
<td>Lower On-state Voltage drop for 5-20 kV Devices (2-3X)</td>
<td>Higher Efficiency of circuits</td>
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<tr>
<td>Smaller Epitaxial Layers (10-20X)</td>
<td>Faster Switching speeds (100-1000X)</td>
<td>Compact circuits</td>
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<tr>
<td>Higher Thermal Conductivity (3.3-4.5 W/cmK vs 1.5 W/cmK)</td>
<td>Higher Chip Temperatures (250-300°C instead of 125°C)</td>
<td>Higher continuous current densities, Higher pulsed power</td>
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<tr>
<td>Melting Point (2X)</td>
<td>High Temperature Operation (3X)</td>
<td>Simple Heat Sink</td>
</tr>
<tr>
<td>Bandgap (3X) (10^{16}X smaller n_i)</td>
<td>High Intrinsic Adiabatic Pulsed Current Level (3-10X?)</td>
<td>Higher Current Capability</td>
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SiC Thyristors – Wide Applicability

- Grid-Tied Energy Storage Power Conditioning – AC/DC; DC-AC; DC-DC
- FACTS Elements
  - Static VAR Comp.
  - STATCOM
  - TCSC (Series Comp.)
  - Static Sync. SC
  - Univ. Power Flow C.
  - Interline PFC
- HVDC

![Graph showing Forward Voltage Drop (Vf) vs. Line Voltage (kV)]

*Courtesy: Princeton Power Systems*
Goals: Specs for Devices/Modules

- Voltage: 15 kV (Phase II Target)
- Current: >100 Amp
- Frequency: >20 kHz
- Fully Soldered Packaging on all terminals
Forward blocking characteristics

Forward blocking voltages in excess of 8000 V were achieved.
On-state performance

- Gate trigger currents as low as 50 mA
- Von as low as 3.8 V @ 100 A/cm²
- Differential Ron,sp as low as 5 mΩ-cm²
Device Designs

Involute

Cellular
Device Layout

Test Structures

<table>
<thead>
<tr>
<th>Pattern</th>
<th>W_A(µm)</th>
<th>W_G(µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Involute</td>
<td>24</td>
<td>21</td>
</tr>
<tr>
<td>Involute</td>
<td>48</td>
<td>21</td>
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<tr>
<td>Involute</td>
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<tr>
<td>Cellular</td>
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<td>Cellular</td>
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<td>24</td>
</tr>
<tr>
<td>Cellular</td>
<td>42</td>
<td>15</td>
</tr>
</tbody>
</table>
Device Processing – metallization, surface planarization

No surface planarization

With surface planarization
Device Packaging

Custom designed package capable of >10kV operation

Soldered contacts are being worked upon, but metallization integrity was good for multiple wire bonds
On-state performance – influence of anode width

For involute devices, gate trigger current decreases with increasing anode width, due to smaller number of parallel gate fingers originating from central gate pad.

Ron,sp is the range of 5-6 mΩ-cm² for all designs implying negligible resistance contribution from ohmic contacts.
Pulsed Measurements conducted to test failure limits of Thyristors

- 3400V
- 3200V
- 2400V
- 1600V
Optical micrographs after failure

With metallization intact

After metallization was etched off
Optically Controlled SiC Thyristors for stacked serial operation

- Higher Electromagnetic Noise Immunity
- Enhanced Electrical Isolation
- Rapid Turn on due to Direct Photogeneration

![Diagram showing circuit components and waveforms.](image)

- Peak gate current ~ 3A
- Peak gate current ~ 4A

Courtesy: Univ. Illinois (Prof. Mazumder)
Conclusions

- First Batch of 8000 V GTO Thyristors show exceptional performance – near theoretical blocking voltages and low on-state losses
- Significant device design, processing and characterization developed at UHV levels
- In pulsed mode, over 600 A of current was conducted through a single 4 x 4 mm device
- Next Steps:
  - Build 12 kV Thyristors
  - Finish switching characterization
  - Determine high temperature limits
  - Find Strategic Partners for insertion for commercialization