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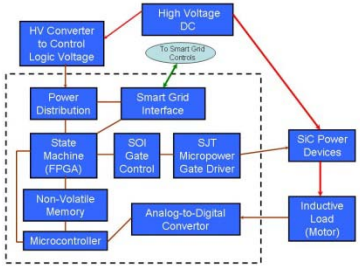
Development of an Integrated Power Controller Based on HT SOI and SiC

Joseph A. Henfling, Stan Atcitty, Frank Maldonado, Sandia National Laboratories
Randy Normann, PermaWorks
Nicholas Summers, Trevor Thornton, ASU



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Overview

- **Program Goals for HT Power Controller**
  - **Ultimately a single module solution**
- **Power Controller Design Details**
  - **PWM options (Microcontroller, FPGA)**
  - **High side gate control**
  - **HT MESFET demonstrated to drive SiC JFET in low side applications**
- **Test Results**
- **Future work**
- **Conclusions**

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Project Goals

- Design HT power controller that can be integrated into a single module
  - Benefits include:
    - Size reduction of power controllers
      - Integration of the SOI based controller with (near) SiC power devices
    - Eases thermal management requirements
    - Increase reliability
      - Designed using HT components and elimination of board-level interconnects
    - Increase efficiency
      - Optimized to fully exploit the benefits of using SiC technology in power controllers
        - Higher breakdown voltage coupled with a lower “ON” resistance can reduce energy losses by 3-4%
    - High voltage capable designs (SiC JFET’s rated at 1200 Volts)
- Demonstrate HT power controller using discrete devices
  - Using HT devices:
    - SOI control circuits – 240 C
    - SiC Power devices – 300 C
- Establish commercialization path to quicken the adaptation of energy-saving SiC technology

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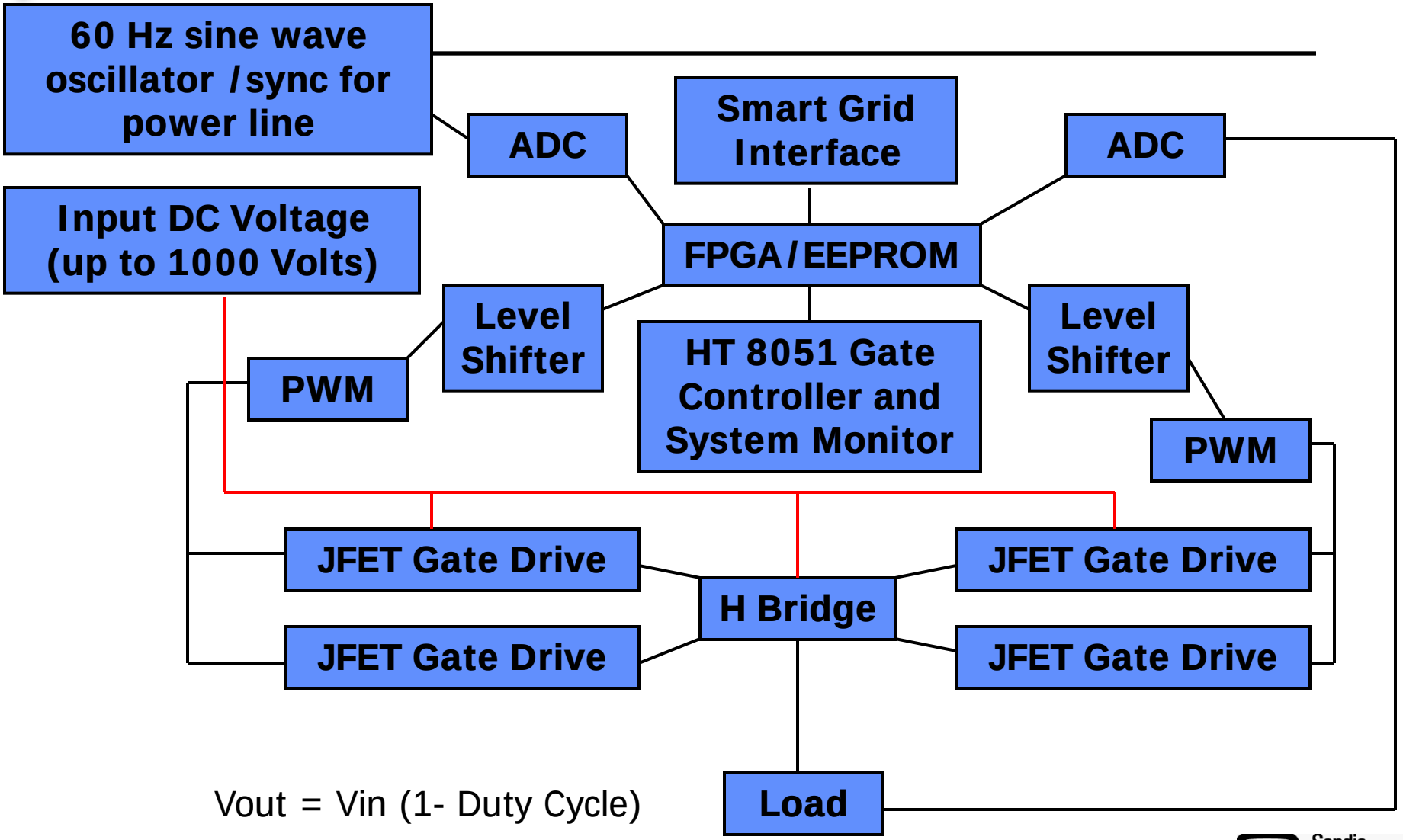
Block Diagram of the Power Controller



Vout = Vin (1- Duty Cycle)

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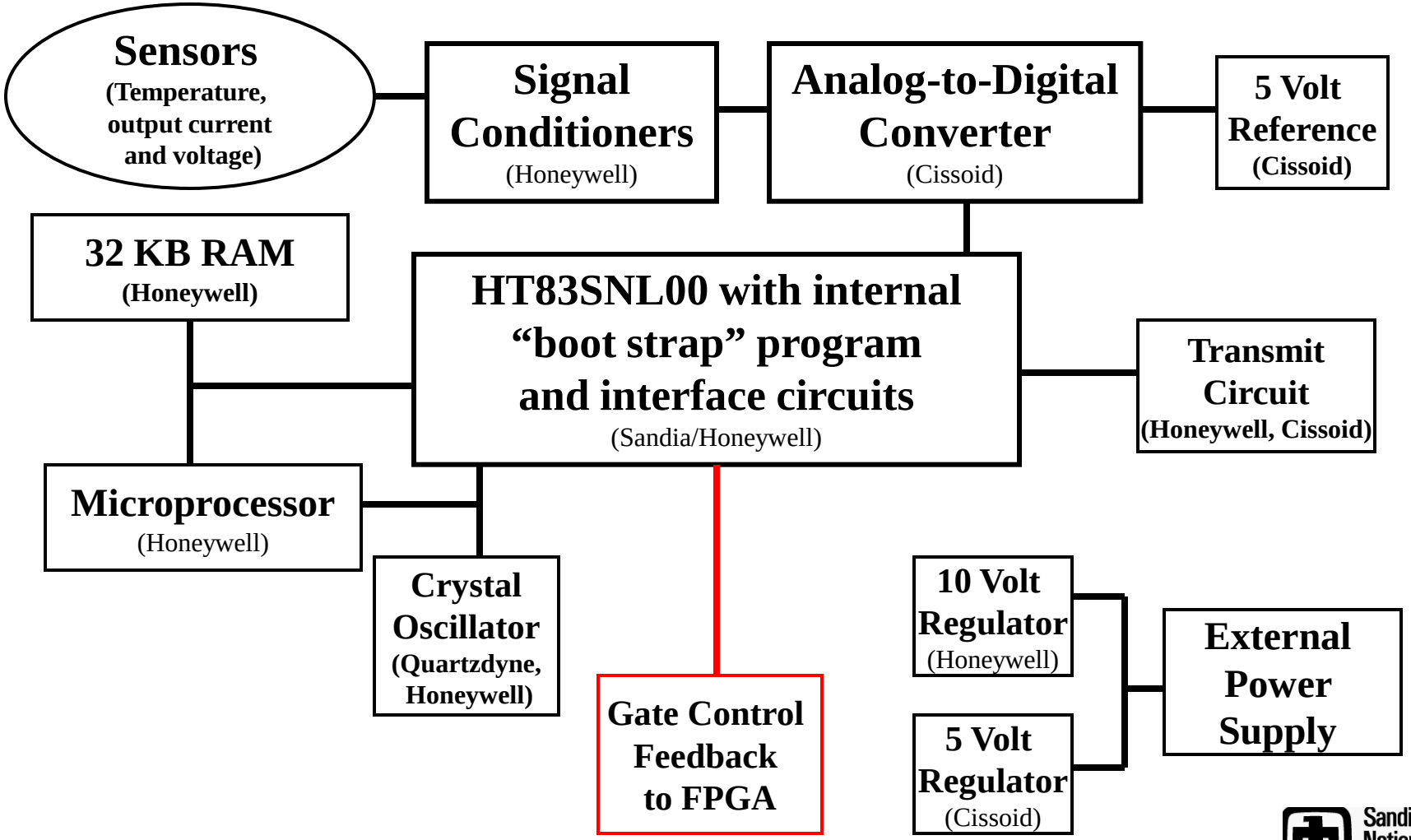
Block Diagram of the System Monitor



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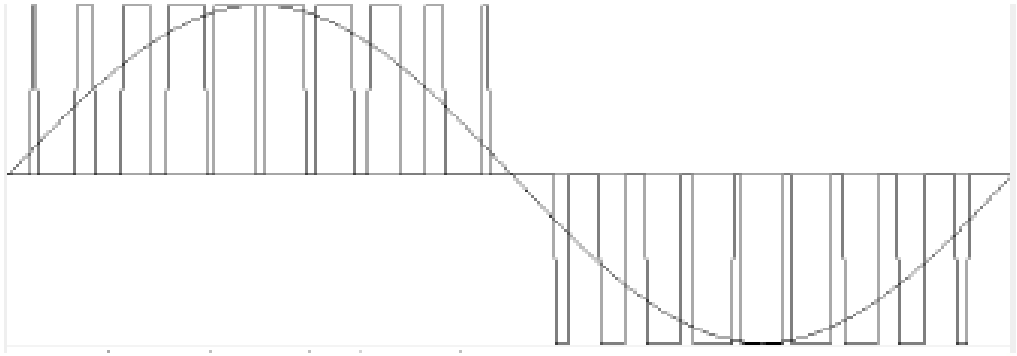
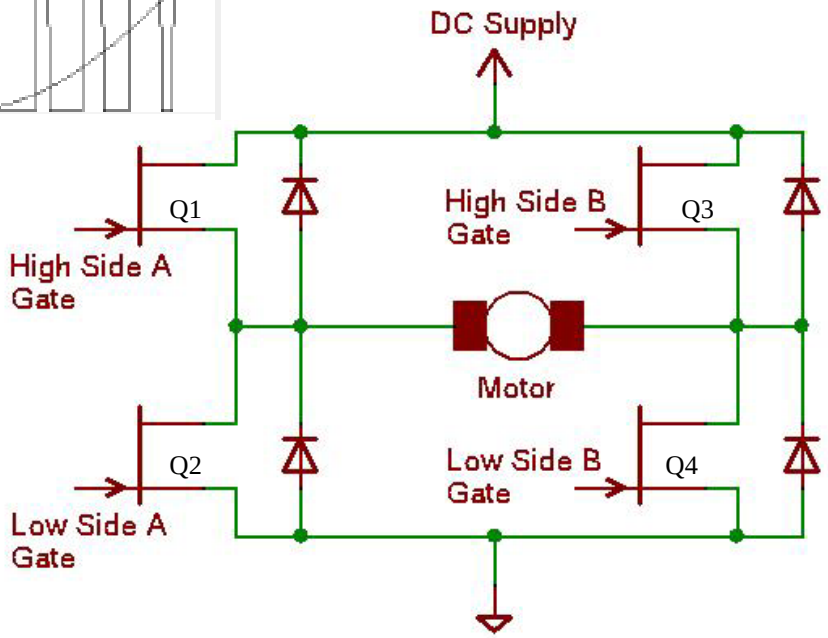
H-Bridge PWM Drive



PWM Gate Drive Waveform



PWM Gate Drive at Q1 and Q3; 60Hz at Q2 and Q4

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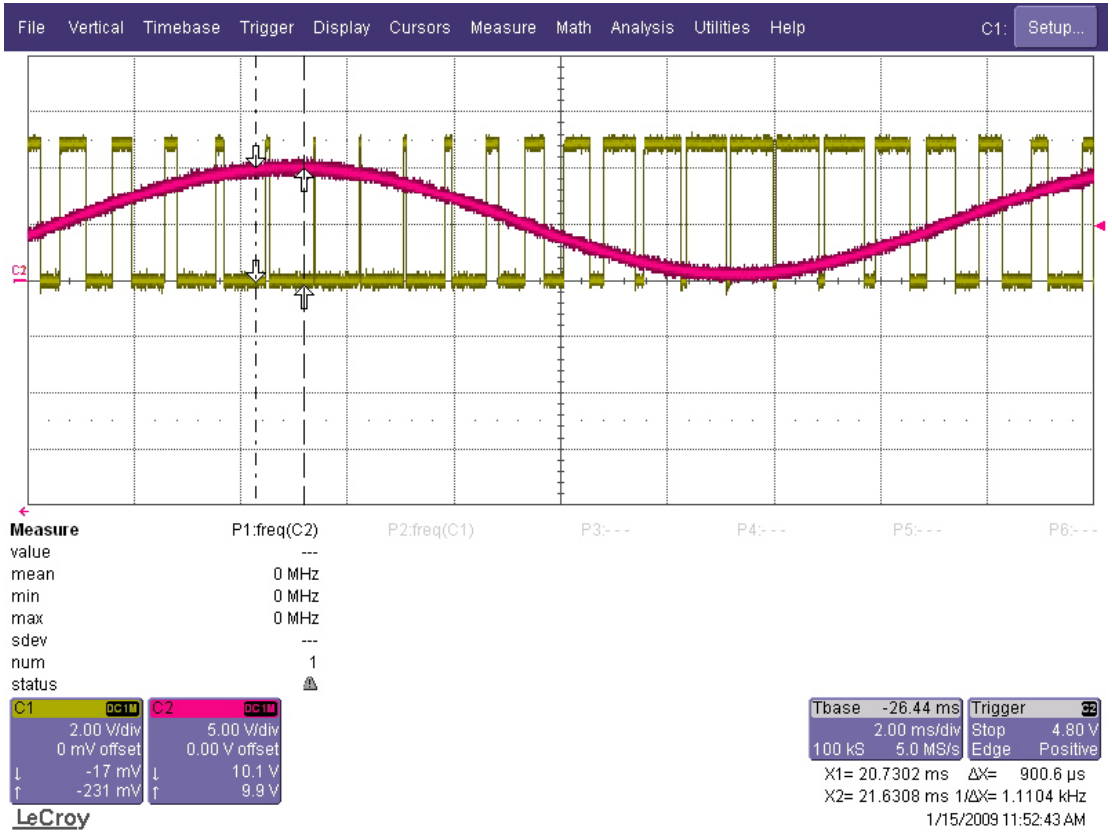
Microcontroller-Based PWM



Probably not fast enough

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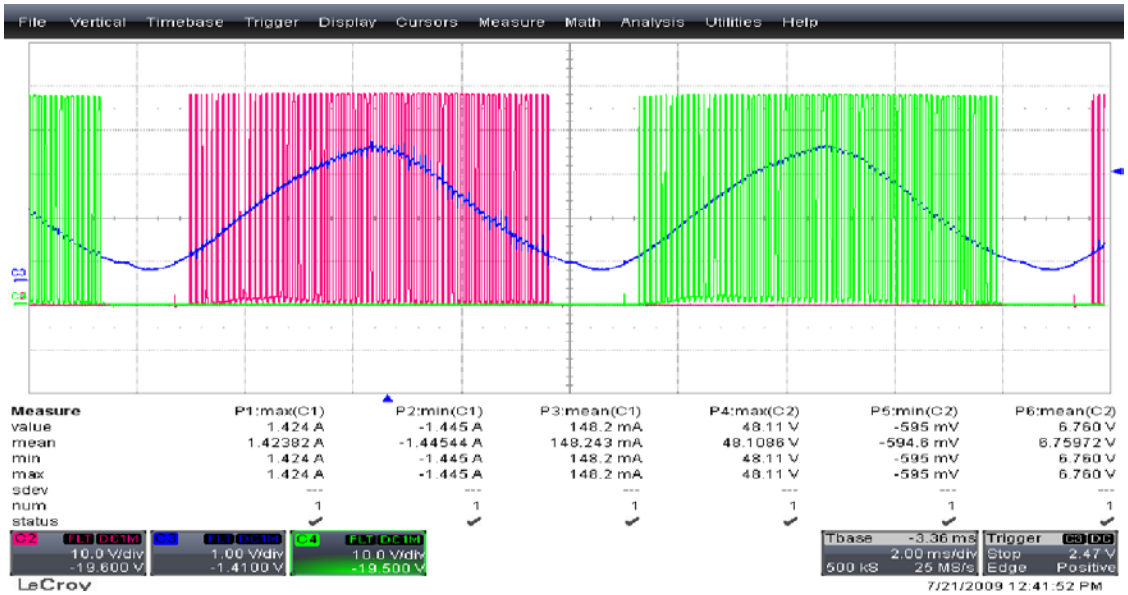
FPGA-Based PWM

- FPGA generated a square wave
- Square wave was filtered and measured using a 10 bit A/D converter by the FPGA
- FPGA adjusted the pulse width based on the reference sine wave



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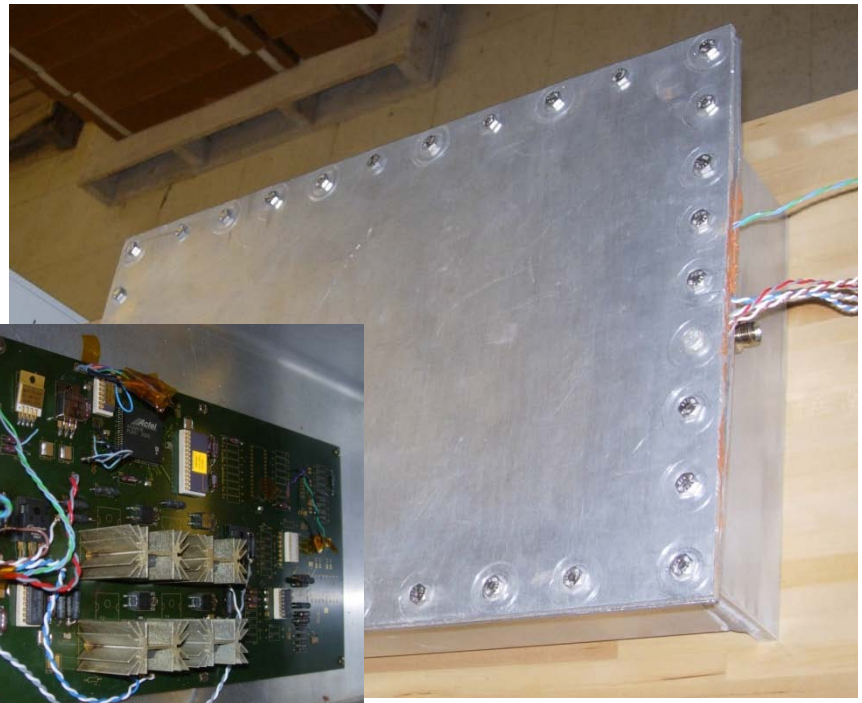
Test Setup



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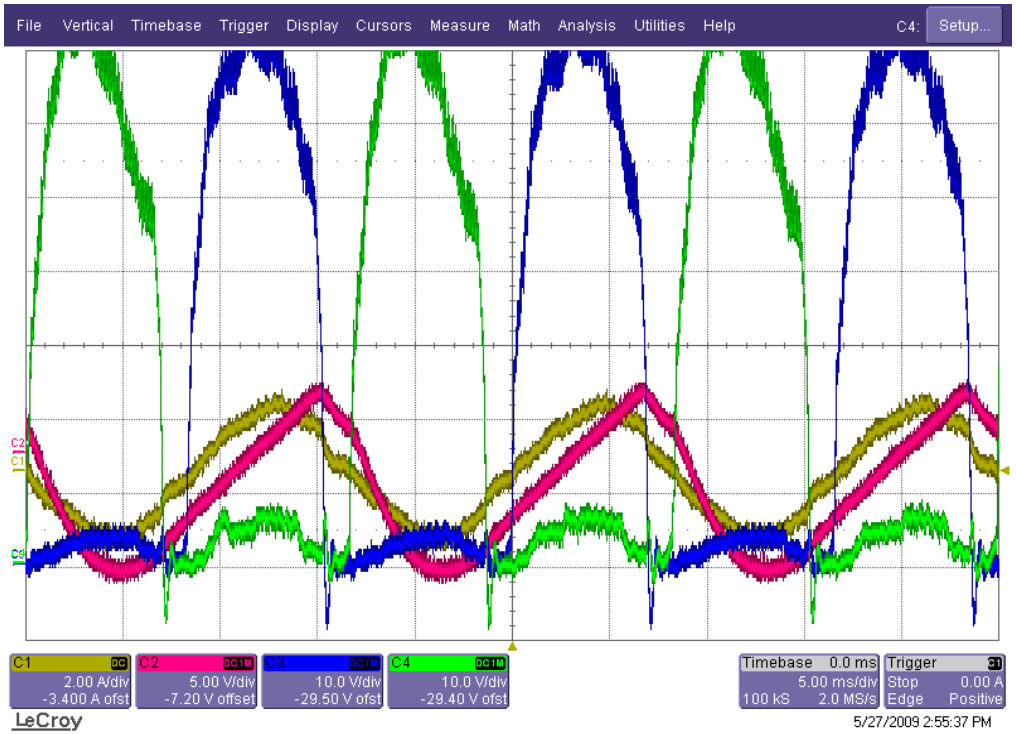
Test Results



Green and blue traces are the voltages at the load. Yellow trace is the current measurement and the red is the differential voltage across the load (divided down)

- This graph shows the output waveform during one of the lab tests. Test conditions were:
  - 240 C ambient temperature
  - JFET case temperature approximately 280 C
  - Supply voltage was 100 Volts

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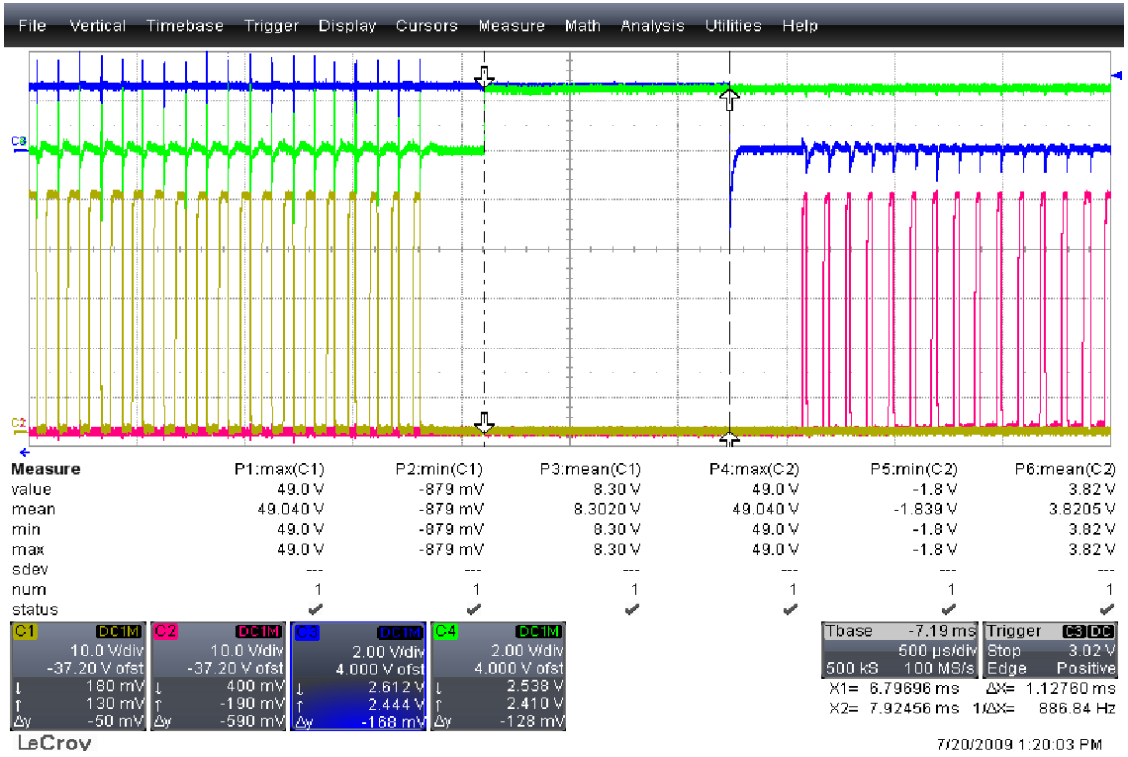
Test Results (continued)



Note: Prototype design exaggerated the dead band between cycles to ensure the JFETs were not damaged due to timing issues. This substantially reduced the overall efficiency. Future work will eliminate the excessive dead band.

Scope image depicting the gate drive for the H bridge: Yellow trace is high side A, blue is low-side B, red is high-side B and green is low-side A

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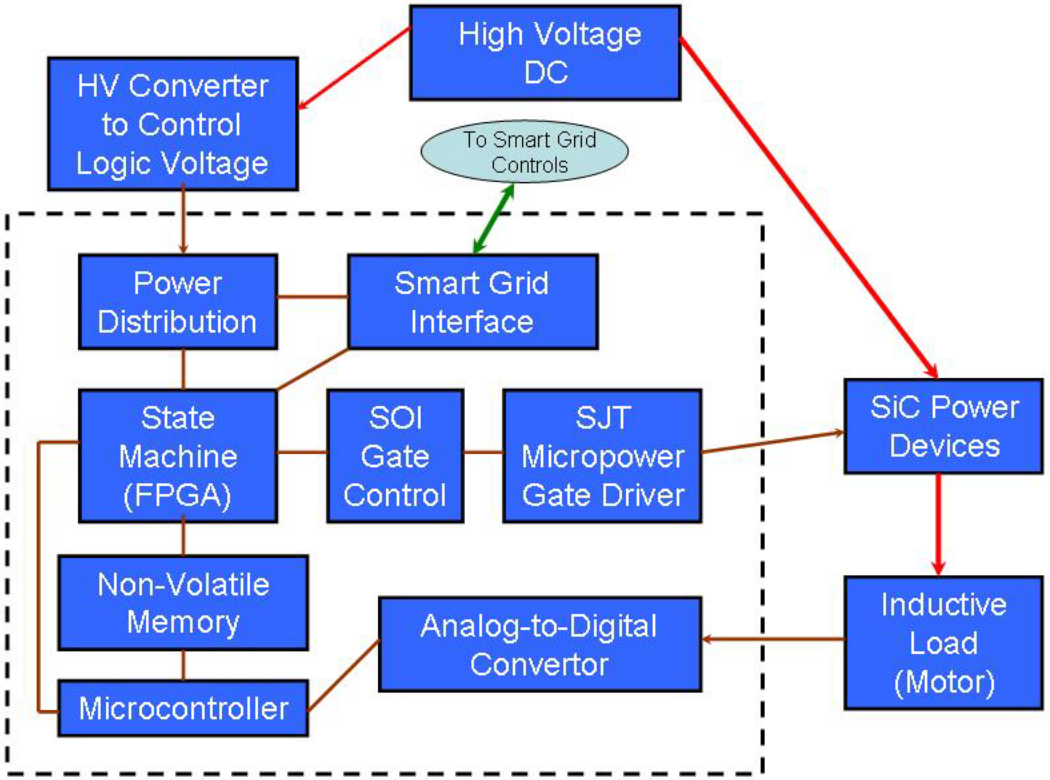
Proposed Integrated Power Controller



Dotted line represents components of the proposed MCM

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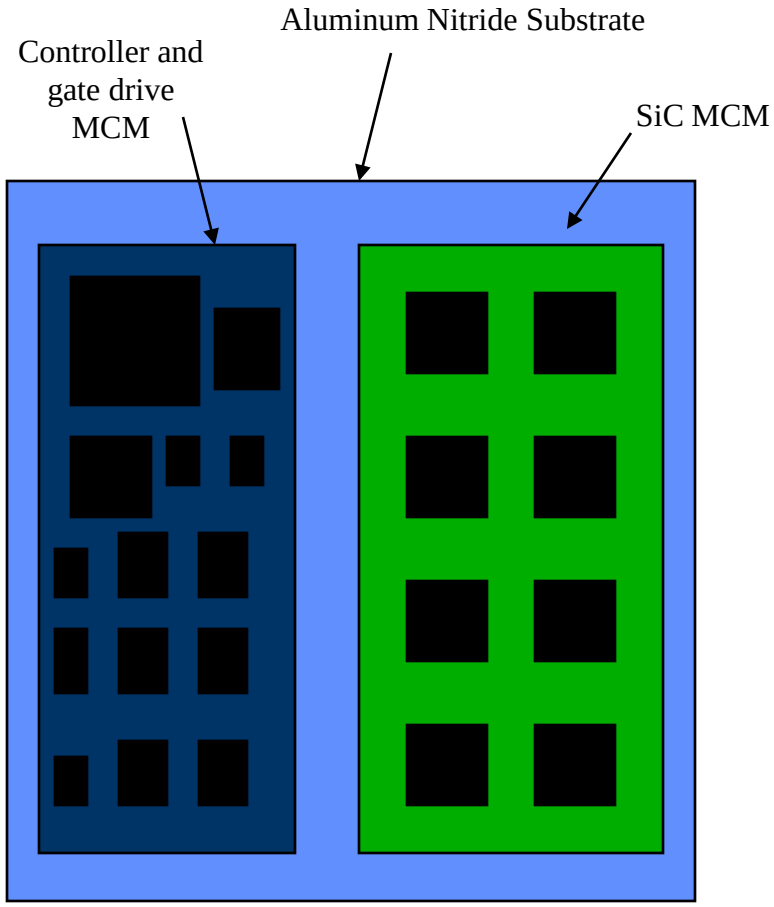
Potentially Same Substrate for MCM's



Aluminum Nitride			
Mechanical	**Units of Measure**	**SI/Metric**	**(Imperial)**
Density	gm/cc (lb/ft^3)	3.26	(203.5)
Porosity	% (%)	0	(0)
Color	—	gray	—
Flexural Strength	MPa (lb/in^{2}x10^3)	320	(46.4)
Elastic Modulus	GPa (lb/in^{2}x10^6)	330	(47.8)
Shear Modulus	GPa (lb/in^{2}x10^6)	—	—
Bulk Modulus	GPa (lb/in^{2}x10^6)	—	—
Poisson's Ratio	—	0.24	(0.24)
Compressive Strength	MPa (lb/in^{2}x10^3)	2100	(304.5)
Hardness	Kg/mm^2	1100	—
Fracture Toughness K_{IC}	MPa•m$^{1/2}$	2.6	—
Maximum Use Temperature (no load)	°C (°F)	—	—
Thermal			
Thermal Conductivity	W/m•°K (BTU•in/ft^2•hr•°F)	140–180	(970–1250)
Coefficient of Thermal Expansion	10^{-6}/°C (10^{-6}/°F)	4.5	(2.5)
Specific Heat	J/Kg•°K (Btu/lb•°F)	740	(0.18)
Electrical			
Dielectric Strength	ac-kv/mm (volts/mil)	17	(425)
Dielectric Constant	@ 1 MHz	9	(9)
Dissipation Factor	@ 1 MHz	0.0003	(0.0003)
Loss Tangent	@ 1 MHz	—	—
Volume Resistivity	ohm•cm	>10^{14}	—

http://www.accuratus.com/index.htm

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Future Work

- **“Fine-Tune” prototype design**
  - **Design, fabricate and test a version 2 board to optimize system efficiency. Improvements include:**
    - **Enhancing the high side gate drive of the H bridge**
    - **Mitigating the current spikes**
    - **Minimizing the switching “dead time”**
    - **Optimizing the output filter**
    - **Improving microcontroller design.**
      - **Better control of the power devices.**
      - **Active feedback**
- **White paper on future packaging options to enhance commercial viability.**

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Conclusion

- A prototype microcontroller-based HT power controller was successfully demonstrated at 240 C
- It had basic control capabilities including monitoring the JFET case temperature and safely shutting the system down if a programmed temperature was exceeded
- High side / Low side SOI gate drive for the JFET power devices was demonstrated
- SOI MESFET gate drive was also successfully tested
- In summary, by combining SOI control and drive circuits with SiC, an intelligent system capable of operation up to 240 C (JFET junction temperature approaching 300 C) was successfully demonstrated.

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Collaborative Effort with Academia and Industry

- **DOE Funded**
  - **Participants include:**
    - **Sandia (Lead)**
    - **ASU (Circuit simulation, fabrication of test circuits using HT MESFET – JFET gate drive)**
    - **PermaWorks (Inverter design simulation and fabrication of HV supply)**
  - **Commercial-of-the-Shelf suppliers**
    - **Honeywell SSEC**
    - **Cissoid**
    - **SemiSouth**

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