Solid-State Fault Current Limiters (SSFCL)

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Fault Current Management

• Growth in the generation of electrical energy, increased penetration of distributed resources and increased interconnection of the networks leads to higher fault currents

• The growth in capacity requires replacing existing circuit breakers with higher fault current ratings. Major cost and down time.

• Higher fault causes more stress on the system reducing the life of critical components such as transformers
EPRI’s Smart Grid Power
Electronic based Technologies

- **DSTATCOM**
- **ENERGY STORAGE**
- **SOLID-STATE BREAKER**
- **SSCL**
- **DVR**
- **ENERGY STORAGE**
- **SSTS**
- **REDUCED SAGS, TRANSIENTS, HARMONICS**
- **SOLID-STATE BREAKER**
- **COMPENSATED VOLTAGE, POWER FACTOR HARMONICS**
- **DYNAMIC NON-LINEAR LOAD**
- **SENSITIVE LOAD**
- **UNINTERRUPTED SUPPLY**
- **SENSITIVE LOAD**
- **CRITICAL LOAD**
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Project Overview

• SSFCL will provide solution to allow delivery system to grow its capacity with increased reliability and power quality

• DOE awarded Contract to EPRI to develop under instrument DE-FC02-06CH11354 a 69kV Class Solid State Current Limiter. The project period is from 07/01/2006 through 06/30/2009

• Silicon Power Corporation, Malvern, PA is sub-contracted by EPRI to develop the SSFSCL
Current Limiting Effect

2007 R&D100 Award Winner

SGTO Device

- Performance Driver
Deliverables

Outline of 69kV, 1000A, 1Ph Unit

- SSFCL looks like a Transformer
  - Tank Size - 12’h x 12’w x 12’d
- OFAF Cooling System
  - Size - 10’h x 5’w x 7’d
- Total weight – 80,000 lbs
- Local / Remote Control
Program Team

- DOE / Washington HQ - Gil Bindewald
- DOE / Chicago - Stephen Waslo
- EPRI Project manager - Ashok Sundaram
- SSCL Developer - Silicon Power Corp.
- SSCL Commercializer - Howard Industries
- Technical Consultant - Dr. Laszlo Guygyi
- Utility Advisor’s - Pat Duggan (ConEd)
- - Pat Dilillo (ConEd)
  - Sanjay Bose (ConEd)

EPRI P37D Task Force on Advanced Solid-State Substations Techniques
Project Structure & Schedule

1. Select Switch technology and Demonstration 9/’06 – 7/’07
2. Develop & test the Standard Building Block 2/’07 – 8/’08
3. Design the Power Stack 7/’07 – 7/’08
4. Complete the design of 69kV 1Ph 1000A SSCL 10/’07 – 9/’08
5. Build & test the Power Stack 1/’08 – 2/’09
6. Build & test the 69kV 1Ph 1000A SSCL 3/’08 – 6/’09
7. Final Report - 9/’09
Project Status

1. Select Switch technology and Demonstration - Completed
2. Develop & test the Standard Building Block - Completed
3. Design a Power Stack - Completed
4. Complete the design of 69kV 1ph 1000A SSCL - Completed
5. Build & test the Power Stack - In progress
   • Completion by Dec. ‘08
6. Build & test the 69kV 1Ph 1000A SSCL - In progress
   • Completion by 6/’09
7. Final Report - Deliver by 3QCY09
**SSFCL Concept**

- **Features:**
  - No cryogenics
  - Immediate recovery
  - Fail safe
  - No current distortions
  - SuperGTO
    - Lower losses
    - Reduced Overall size and weight
  - Modular design expandable to desired Voltage & Current Ratings

![SSFCL Diagram](image-url)
Standard Building Block (SBB) Assembly

- Comm. Cap.
- Aux Switch Module
- Main Switch Module
- Control Boards
- Varistors
- Cold plates

- Size – 44”l x 13”w x 10”h, Weight – 100 lbs
SBB Assembly In Progress
Control Hardware

- Gate Drive
- VLC Interface Board
- FPGA
- Cap Charging
- Aux. PS
- Master Controller
69kV 1Ph SSCL Assembly

- Bushing
- Inlet Manifold
- CLR
- Power Stack
SBB in Test
Test Results

Module current sharing

V-Cres: +1400V $\rightarrow$ -2500V

I-ratio = 1.54

t-rec = [26. 26] us

Main: +2390A $\rightarrow$ -1790A, 2380V

Res: +3680A $\rightarrow$ -1320A,
CLR Testing

CLR under Let-thru test

CLR under DC Res. test

CLR under Inductance test

- Inductance measurement:
  - 1.5 V at 10 A = 310 uH
- DC Resistance measurement:
  - At 10 A = 4.285 mOhm
- Let-thru current withstand:
  - 2.9 kA rms sym for 0.5sec = Ok
  - 7.5 kA peak Asym for 0.5sec = Ok
• SGTO Devices demonstrated the desired performance for SSFCL.

• SSFCL Design is modular and is based on Standard Building Block.

• Standard Building Block testing demonstrated the desired current interruption and current sharing.

• Power Stack is being built.

• Design of 69kV 1ph 1000A SSCL is completed. Thermal Management design is verified by NOVA-Therm Lab, Villanova University.

• Manufacturability of the design is reviewed by Commercialization Partner – Howard Industries. Parts and components are being procured.
Future Tasks

- Complete building 69kV 1000A 1ph SSFCL by 3’09.
- Test 69kV 1000A 1ph SSFCL for design Verification at KEMA by 6’09.
- Deliver Final Report by 9’09.