OAK RIDGE National Laboratory

Highly Integrated Power Module (Keystone Project #1)

Emre Gurpinar

Email: gurpinare@ornl.gov

Phone: 865-341-1286

Oak Ridge National Laboratory

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ORNL is managed by UT-Battelle, LLC
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U.S. DEPARTMENT OF ENERGY

Overview

Timeline

- Start – FY19
- End – FY21
- 25% complete

Barriers

- Availability and the limited field reliability data of wide band-gap (WBG) power devices
- Meeting DOE ELT 2025 High Voltage Power Electronics Targets
  - Power Density: 100kW/L
  - Cost: $2.7/kW
  - Peak Efficiency: > 97%
  - Reliability: 300,000 mile lifetime or 15 years

Budget

- Total project funding
  - DOE share – 100%
- Funding for FY19: $600K

Partners

- NREL and SNL
- Momentive, Henkel, Indiana IC, and DuPont
- ORNL team members: Emre Gurpinar, Shajjad Chowdhury, Steven Campbell, Randy Wiles, Alfonso Tarditi, and Burak Ozpineci

Relevance – Project Objectives

- Overall Objective
  - Develop technologies for next generation advanced integrated power electronic systems enabling high power density and reliability to achieve DOE ELT 2025 technical targets (100kW/L, $2.7/kW, and 300,000 mile lifetime)
- FY19 Objectives
  - Power Module Design
    - Evaluate electrical and thermal characteristics, and design challenges of Insulated Metal Substrate (IMS) and Organic Direct Bonded Copper (ODBC) with Thermal Pyrolytic Graphite (TPG) insert as a substrate solution
    - Evaluate feasibility of Quilt Packaging (QP) as an interconnect solution in power modules
  - Gate Driver and Auxiliary Components
    - Develop radio frequency (RF) based solutions for ultra compact isolated signal and power transfer

FY19 Milestones and Go/No-Go Decision

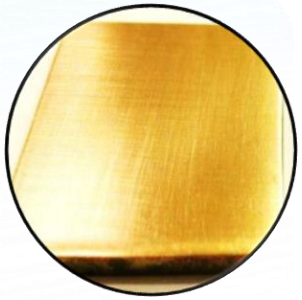
Date	Milestones and Go/No-Go Decision	Status
Q1	Milestone: • Finalize prototyping of insulated metal substrate (IMS) with Thermal Pyrolytic Graphite (TPG) and identify opportunities for Organic Direct Bonded Copper (ODBC)	Completed
Q2	Milestone: • Design and analyse high-density interconnect, and high-performance substrate solutions	Completed
Q3	Go/No-Go Decision: • If the selected design can significantly improve power density and heat extraction capability, then introduce passives, gate driver circuitry and sensor into multi-objective optimization tool	On-track
Q4	Milestone: • Build a baseline power module	On-track

Approach/Strategy

- Increase power density and reliability of power electronics to meet DOE ELT 2025 targets (100kW/L, and 300,000 mile lifetime) by focusing on power electronic module research.

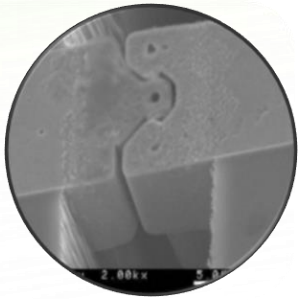
Substrates for Power Electronic Modules

- Identify state-of-the-art (SOA) substrate solutions that allow increased power density and high reliability for WBG device based power modules via
  - Better coefficient of thermal expansion (CTE) matching between WBG devices and power module materials
  - Improved heat extraction
  - Enhanced thermal and power cycling capability



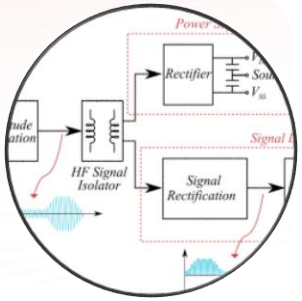
Interconnects with High Power Density

- Evaluate and introduce low profile, high current density reliable chip-to-chip, and chip-to-package interconnects for power modules and auxiliary circuits (e.g. gate drivers) which will enable
  - Reduced parasitic inductance in the system for optimum switching performance
  - Reduced power module size
  - Enhanced reliability by moving to wire bondless solutions



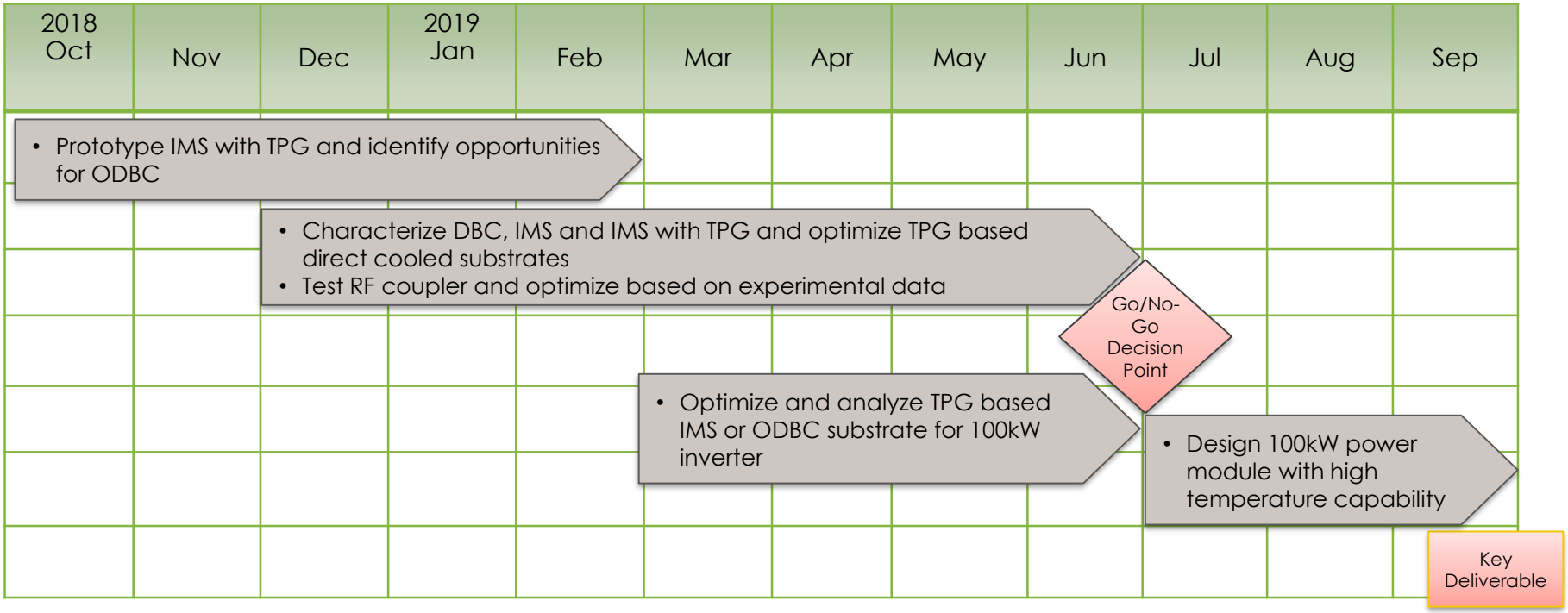
Compact Signal and Power Transfer for Gate Drivers

- Develop novel architectures for combined signal and power transfer with advanced functionalities for gate drivers to achieve
  - High power density by minimizing auxiliary components
  - Integration of gate drive circuitry to WBG modules
  - Advanced gate drive functionality for improved electromagnetic interference (EMI), short circuit protection and loss distribution



Images are courtesy of Momentive and Indiana IC

Approach FY19 Timeline



Go/No-Go Decision Point: If the selected design can significantly improve power density and heat extraction capability, then introduce passives, gate driver circuitry and sensor into multi-objective optimization tool.

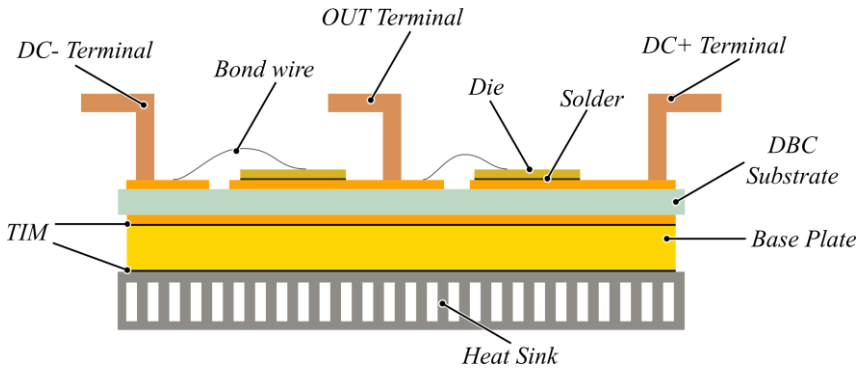
Key Deliverable: 100kW power module design with high temperature capability

Technical Accomplishments – FY19

Compared Substrates for High Power Density – DBC & IMS

- Direct Bonded Copper (DBC) is the conventional solution for isolated, multi-chip power modules
  - DBC provides excellent thermal conductivity and electrical isolation performance
  - CTE mismatch, ceramic and copper (Cu) thickness limitations, multi-layer multi-material structure are the drawbacks of the DBC
- Insulated Metal Substrates (IMS) are formed by stacking copper/aluminum layers with dielectric film
  - IMS provides low cost, flexible structure with variable copper and dielectric thickness
  - Dielectric thermal performance is the major drawback of the IMS

Cross section of conventional power module



Comparison of layer thickness and performance

	DBC	IMS
Top Copper Thickness [µm]	300	300-5000
Dielectric Thickness [µm]	381-1000	25-500
Dielectric Thermal Conductivity [W/(m*K)]	24-170	< 3
Bottom Copper Thickness [µm]	300	300-5000

- The low thermal conductivity of the dielectric film used in insulated metal substrates can be mitigated with optimization top and bottom copper thickness.

Technical Accomplishments – FY19

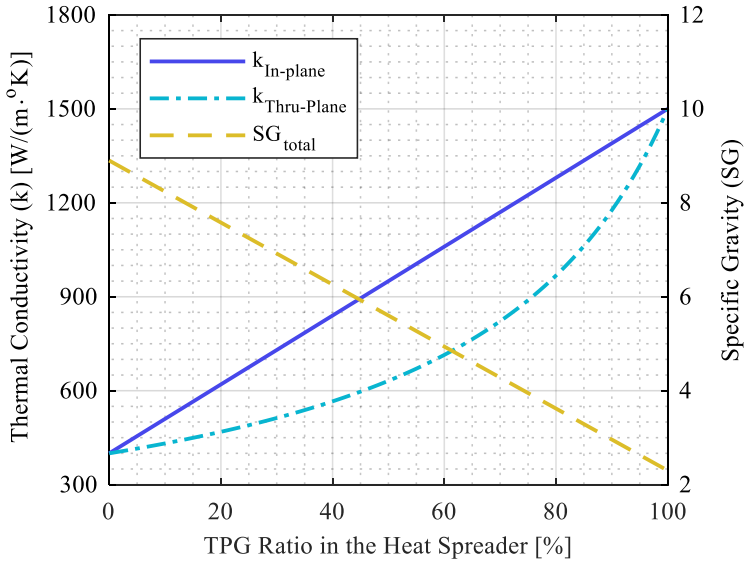
Analyzed Encapsulated Thermally Annealed Pyrolytic Graphite (TPG)

[1]

TABLE I: Typical Property Comparison of Heat Spreader Materials

Material	In-Plane TC $\left[\frac{W}{m\cdot^\circ K}\right]$	Cross-Plane TC $\left[\frac{W}{m\cdot^\circ K}\right]$	In-Plane CTE $\left[\frac{ppm}{^\circ C}\right]$	Specific Gravity	In-Plane TC / Specific Gravity
Aluminum	218	218	23	2.7	81
Copper	400	400	17	8.9	45
AlSiC-12	180	180	11	2.9	62
CuW	185	185	8.3	15.2	12
TPG	> 1500	10	-1	2.3	650

Encapsulated TPG with Cu



With 80% TPG Ratio:

- $k_{In\text{-}plane}$: 3.2 x k_{Cu}
- $k_{Thru\text{-}plane}$: 2.4 x k_{Cu}
- SG_{Total}: 0.4065 x SG_{Cu}

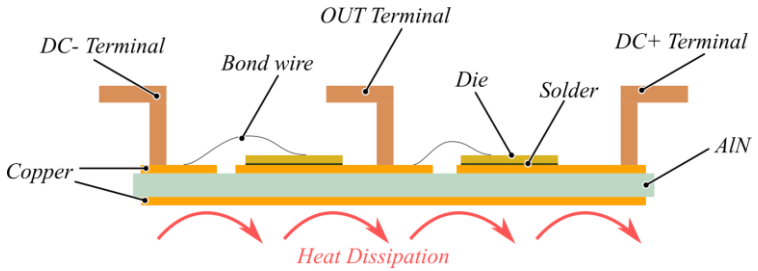
- With 80% TPG ratio in the heat spreader, the thru-plane thermal conductivity can be increased by 2.4 times and total specific gravity can be reduced by 2.46 times in comparison to copper.

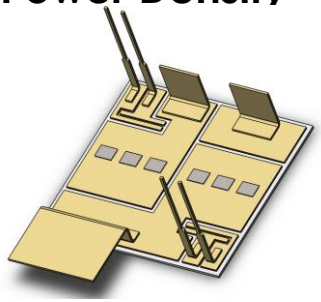
[1] W. Fan and X. Liu, Advancement in High Thermal Conductive Graphite for Microelectronic Packaging, ser. RF and Microwave Microelectronics Packaging II, K. Kuang and R. Sturdivant, Eds. Cham: Springer International Publishing, 2017.

Technical Accomplishments – FY19

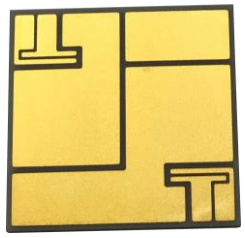
Designed Substrates for High Power Density

DBC

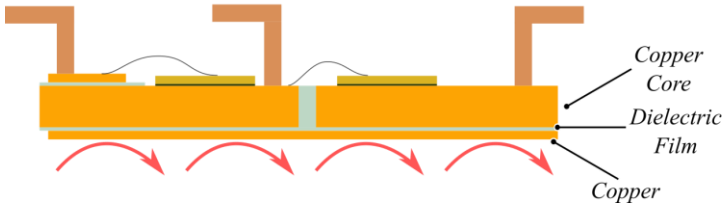


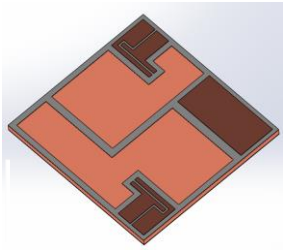


DBC Sample



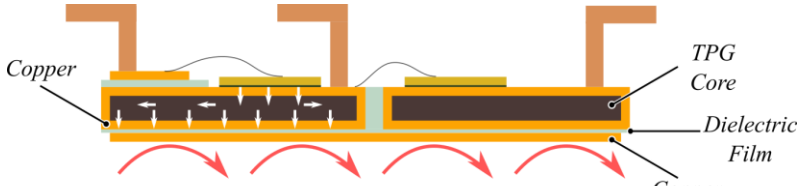
IMS

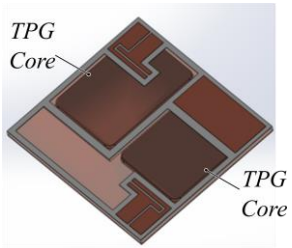


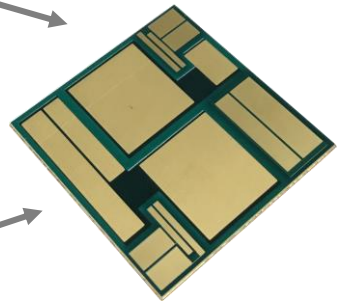


IMS & IMSwTPG Samples

IMS with TPG Core (IMSwTPG)





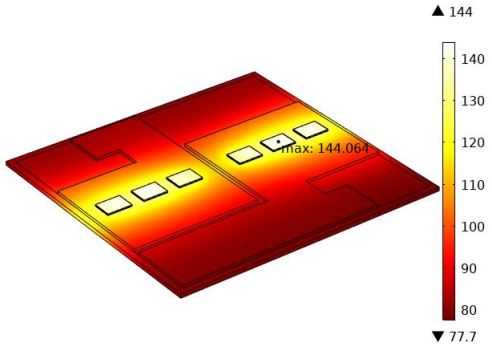


- Three different substrates based on DBC, IMS, and TPG embedded IMS are designed based on identical electrical layout and insulation properties for comparison purposes.

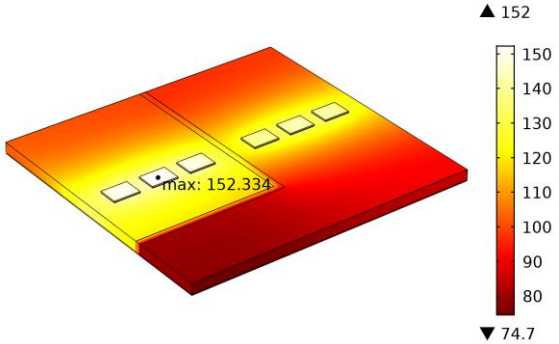
Technical Accomplishments – FY19

Completed Thermal Analysis and Comparison of Substrates

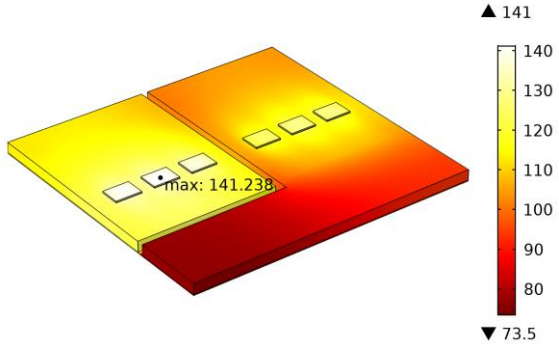
DBC



IMS

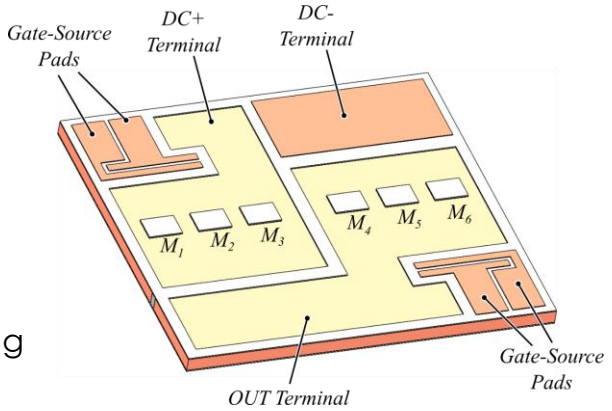


IMSwTPG



- @ 45 W power loss across each die (M_1-M_6), which provides maximum die temperature of 150°C with 65°C base temperature. Maximum junction temperature at each substrate:
  - DBC: 144.1°C
  - IMS: 152.3°C
  - IMSwTPG: 141.2°C
- Heat transfer coefficient at the base of the substrate: 5000W/(m^{2}K)
- Experimental evaluation of the prototype substrates under different loading and ambient conditions will be conducted in the third quarter of FY19.

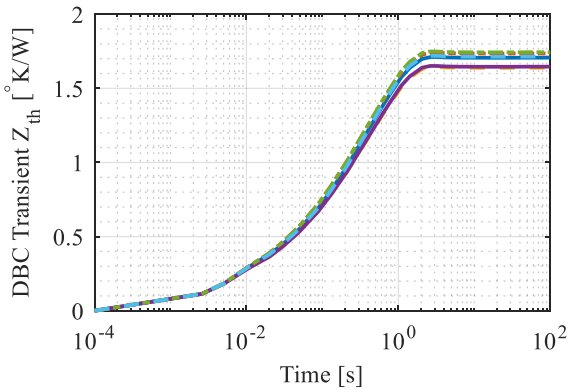
Substrate Layout



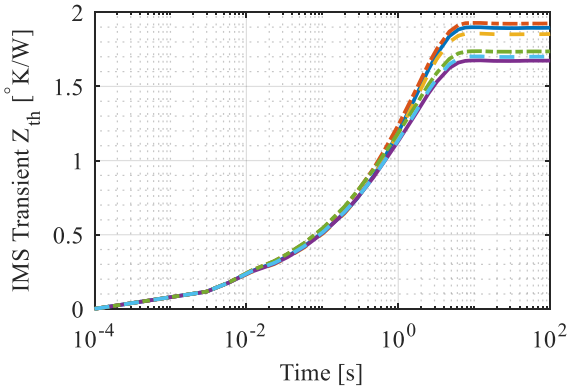
Technical Accomplishments – FY19

Completed Transient Thermal Impedance Comparison

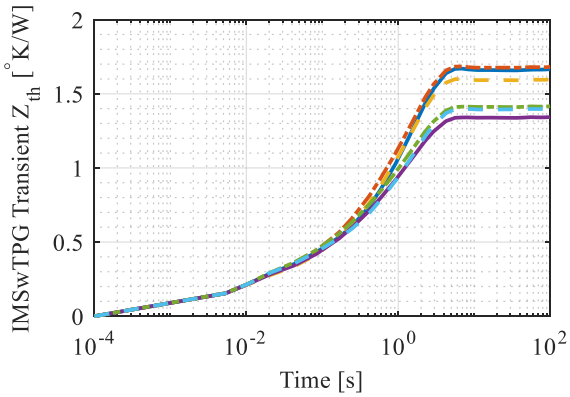
DBC



IMS

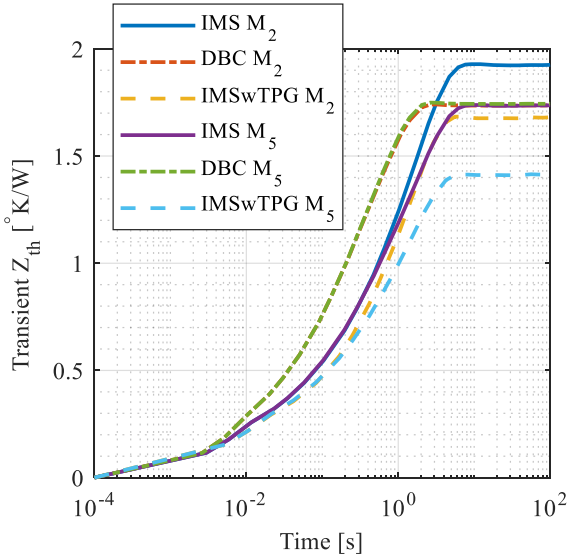


IMSwTPG



- Dies placed on IMSwTPG have either significantly better or equivalent steady-state thermal resistance in comparison to DBC.
- Below 1s transient time, IMS based solutions provide lower thermal impedance due to increased copper underneath the dies.
- If the power cycling frequency of the devices is higher than 1Hz, then the temperature variation across the dies will be less with the TPG based solution. This will lead to lower junction temperature variation.

Comparison

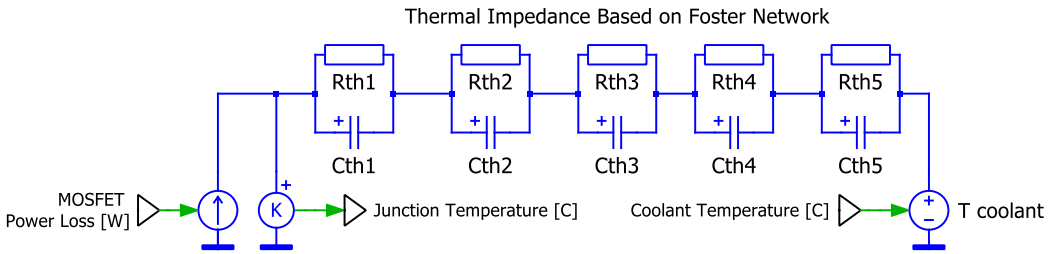


Technical Accomplishments – FY19

Modelled Power Cycling with Different Substrates

- Thermal Foster network for each power semiconductor die on three different substrates have been modelled based on the transient impedance results in COMSOL.

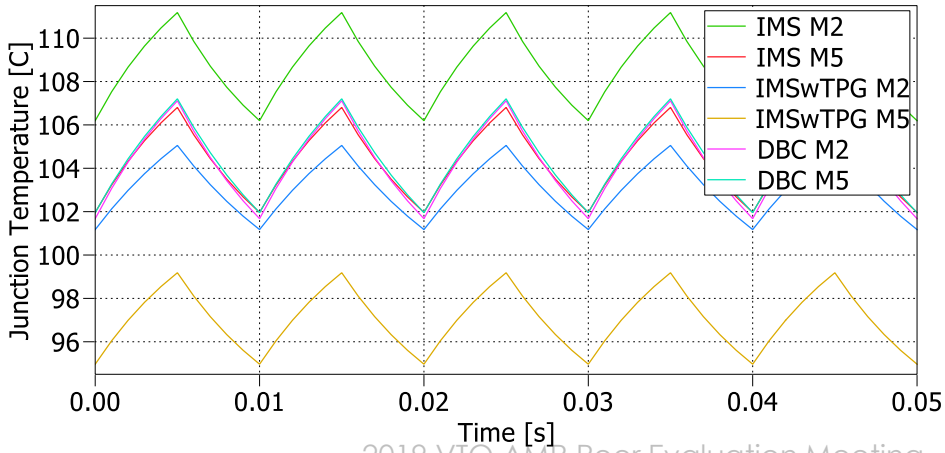
Thermal Modelling in PLECS



Junction Temperature Comparison

	$T_{J\text{-mean}}$ [°C]	ΔT_J [°C]
IMS M_2	108.69	4.99
IMS M_5	104.39	4.84
DBC M_2	104.39	5.44
DBC M_5	104.58	5.25
IMSwTPG M_2	103.1	3.88
IMSwTPG M_5	97.07	4.22

- Power loading for each MOSFET:
  - 45 W (duty cycle=0.5, 100Hz)
- Cooling:
  - 65°C coolant with 5000W/(m^{2}K) heat transfer coefficient
- Thick copper layer under each MOSFET in IMS and IMSwTPG solutions provide lateral heat spreading effect.
- IMSwTPG provides the lowest junction temperature variation ΔT_J and lowest average temperature $T_{J\text{-mean}}$ for each MOSFET.

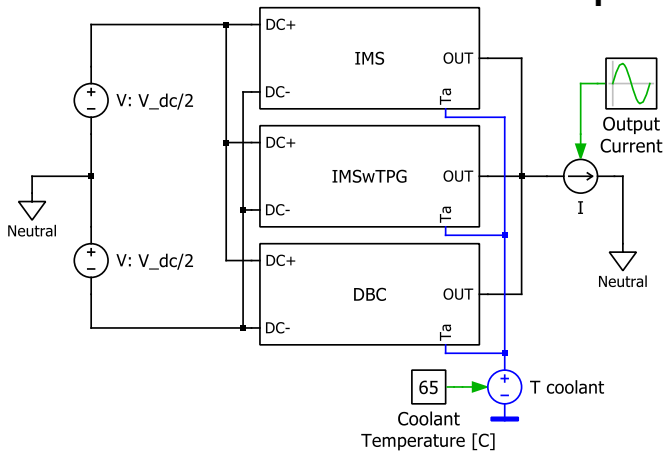


Technical Accomplishments – FY19

Analyzed Power Cycling with Different Substrates in an Inverter Scenario

- The developed thermal Foster network for each substrate is used in a typical inverter scenario for comparison of junction temperature
- IMSwTPG substrate provides lowest $T_{J\text{-mean}}$ and ΔT_J

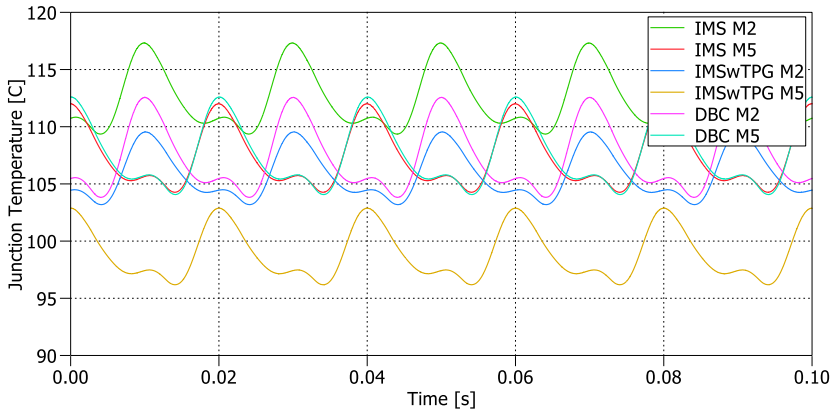
PLECS Model for Substrate Comparison



Junction Temperature Comparison

	$T_{J\text{-mean}}$ [°C]	ΔT_J [°C]
IMS M_2	115.99	8.67
IMS M_5	110.45	8.42
DBC M_2	110.46	9.51
DBC M_5	110.69	9.28
IMSwTPG M_2	108.80	6.91
IMSwTPG M_5	98.86	6.65

- Power loading for each substrate:
  - Output current= 300A_{rms}, 50Hz (100A_{rms} per substrate)
  - Switching frequency= 30kHz
  - DC Link voltage: 600V
  - Power factor = 0.85
  - Modulation Index =0.9
- Cooling:
  - 65°C coolant with 5000kW/(m^2K) heat transfer coefficient
- Symmetrical power loss across different substrates is achieved



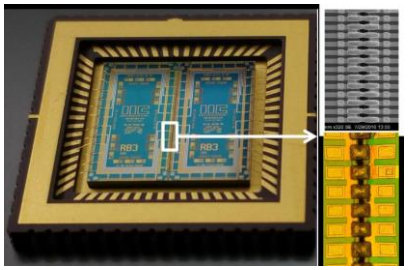
Technical Accomplishments – FY19

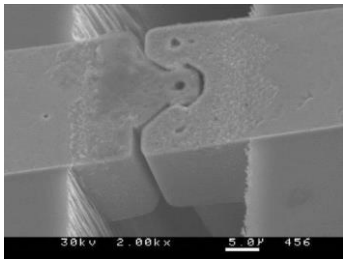
Identified Low Inductance, High Density SOA Interconnects

- QP: chip-to-chip interconnect technology that incorporates conductive metal "nodules" on the sides of the chips

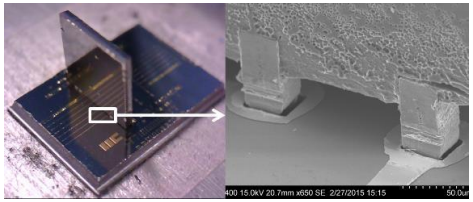
Quilt Packaging Examples in Microelectronics

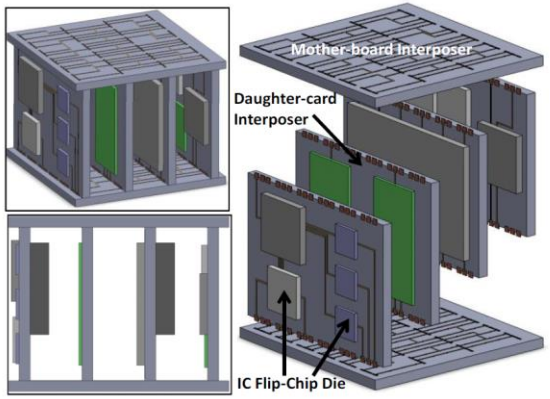
Chip-to-chip Interconnects





Board-to-board Interconnects





Source: Indiana IC

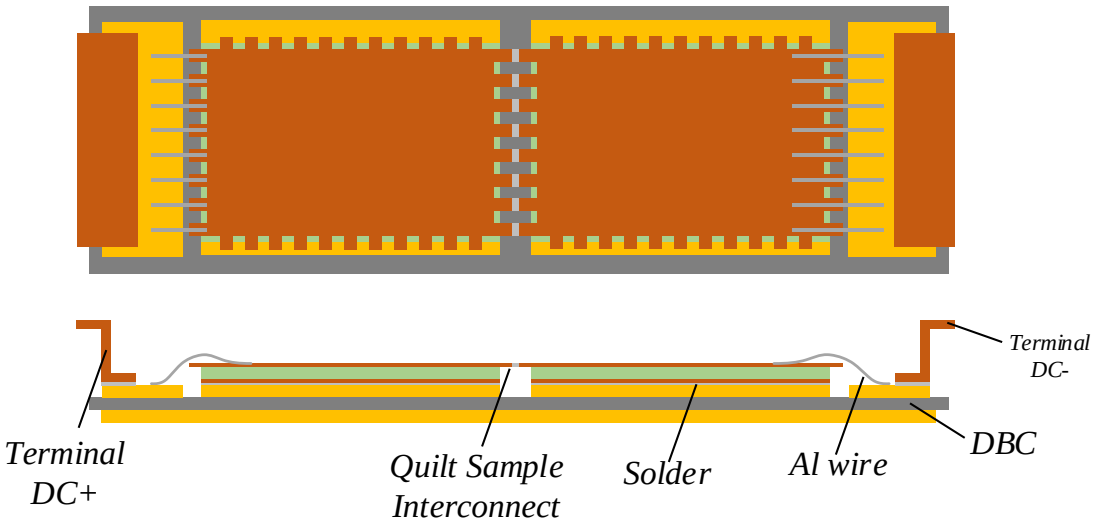
- Solid metal, typically Cu
  - Width: 5 to 500 μm
  - Thickness: 20-50 μm
  - 10 μm nodule pitch possible
- Increased power density
- Robust electrical and mechanical interconnects
- Reduced interconnect parasitic
- High density 3D integration of gate drivers and auxiliary circuits

Technical Accomplishments – FY19

Designed Test Sample for Quilt Interconnect Evaluation

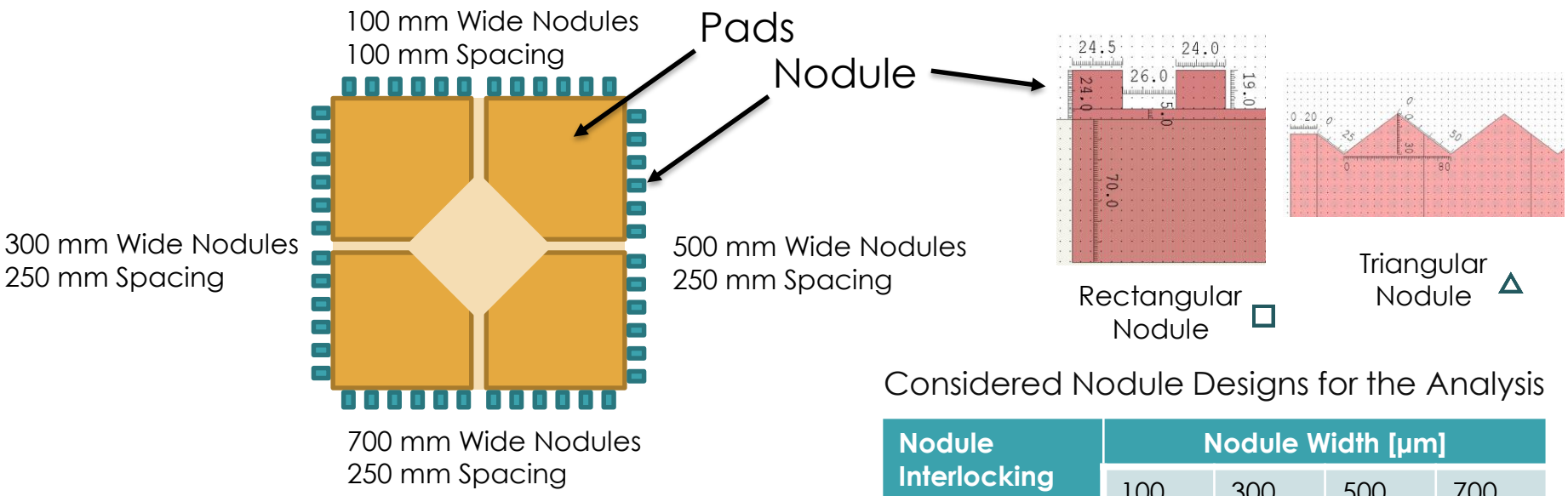
- Electrical characterization of QP for power electronic devices as an interconnect solution will be evaluated in last quarter of FY19.
- A test sample based on QP-on-Silicon will be manufactured by IIC in the third quarter of FY19.
- The test sample will provide direct comparison between conventional wire bond and QP nodules in terms of electrical and thermal performance.

Test Sample Design for Interconnect Evaluation



Technical Accomplishments – FY19

Designed QP-on-Silicon Chips for Current Capability Analysis



Considered Nodule Designs for the Analysis

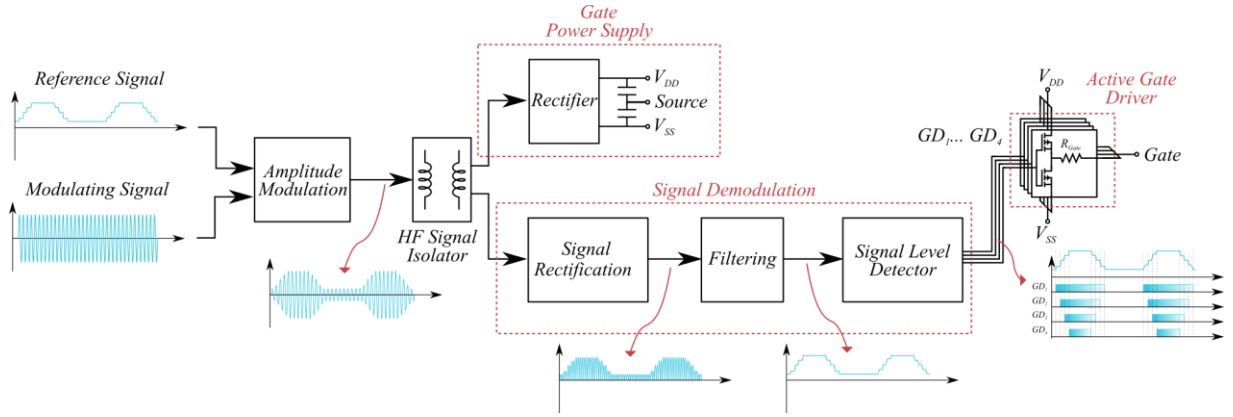
Nodule Interlocking Geometry		Nodule Width [µm]			
		100	300	500	700
Nodule Length [µm] To Chip Interior	30	□ △	□ △	□ △	□ △
		□ △	□ △	□ △	□ △
		□ △	□ △	□ △	□ △
	70	□ △	□ △	□ △	□ △
		□ △	□ △	□ △	□ △
		□ △	□ △	□ △	□ △

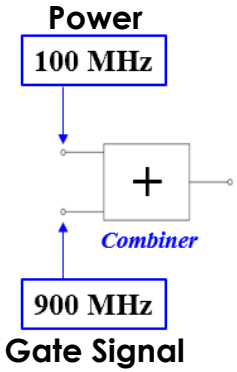
- A single chip will have different nodule width on each side.
- Chips can be rotated 90 degrees to match the sides with the correct nodule size/spacing for quilting.
- The impact of nodule length, width and shape will be evaluated with a single chip design.

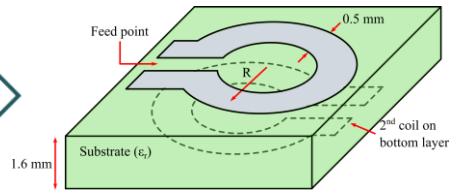
Indiana Integrated Circuits LLC

Technical Accomplishments – FY19

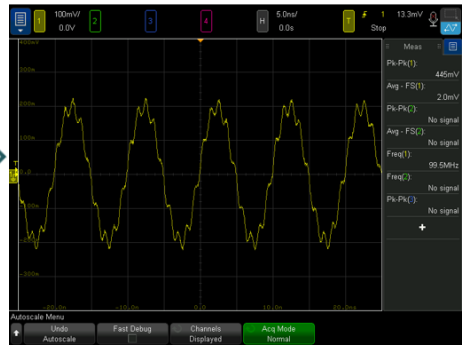
Analyzed Transformers and Rectifiers for RF Coupler Based Gate Driver Concept



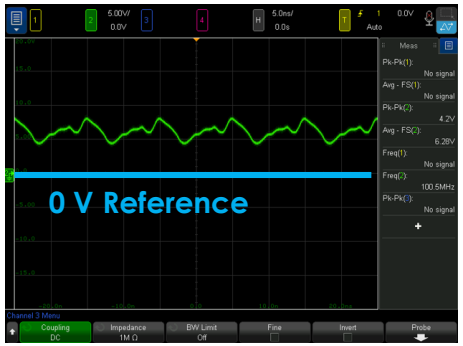




Bespoke wideband transformer



Combined Gate+Power Signal



RF Rectifier @100MHz, 2W

- Commercial and bespoke wideband transformers for effective isolated signal and power transfer have been evaluated.
- Various commercial diodes have been analyzed at different modulation frequencies for selection of signal and power frequency.

Responses to Previous Year Reviewers' Comments

- This project is a new start

Collaboration and Coordination with Other Institutions

Organization	Role
NREL NATIONAL RENEWABLE ENERGY LABORATORY	Thermal Analysis of Substrates
Sandia National Laboratories	WBG device models and samples
IIC Indiana Integrated Circuits LLC	Quilt Packaging Interconnect Design and Manufacturing
MOMENTIVE, BERGQUIST, Henkel	IMS with TPG Insert Design and Manufacturing
DUPONT	Organic DBC Material Provider

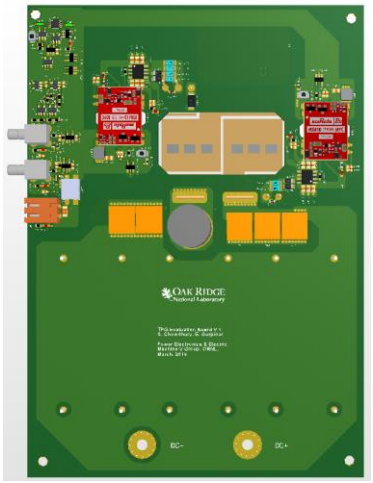
Remaining Challenges and Barriers for FY19

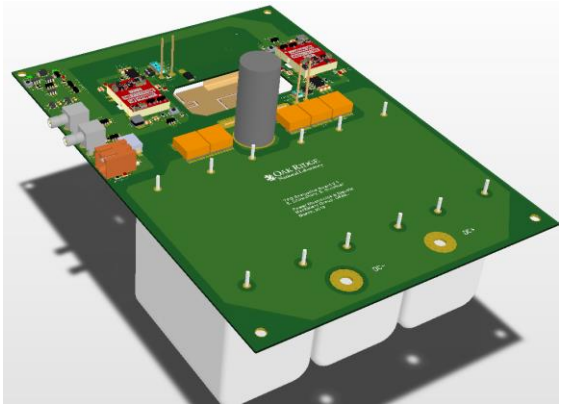
- Application of Quilt interconnects in vertical SiC power MOSFETs
- Impacts of parasitic components to the operation of the RF coupler
- Achieving high efficiency in RF coupler with harmonic content coming from gate driver power supply

Proposed Future Work

- Remainder of FY19
  - Experimental characterization of DBC, IMS and IMSwTPG substrates:
    - Validate thermal performance
    - Characterize dielectric breakdown characterization will be conducted
  - Analyze of ODBC from DuPont and design the substrate for 100kW power module with different WBG devices
  - Compare high power silicon carbide (SiC) MOSFET and gallium nitride (GaN) high electron mobility transistor (HEMT)
  - Analyze electrical performance of quilt nodules for high power applications
- FY20
  - Build and evaluate high power WBG module for DOE ELT 2025 target system
  - Design and test quilt based WBG power devices
  - Experimentally validate RF based gate driver in a high power electronic inverter

Control and Power Board Design for Substrate Evaluation





Any proposed future work is subject to change based on funding levels

Summary

- **Relevance:** DOE ELT 2025 high voltage power electronics targets require revisiting the conventional silicon oriented integration to enable the benefits of WBG devices, and to achieve power density, cost and reliability targets
- **Approach:** Develop substrate, interconnect technologies for power modules, and high power density gate drivers to achieve high power density and reliability in next generation advanced integrated power electronic systems
- **Collaborations:** NREL, SNL, Momentive, Henkel, Indiana IC, and DuPont
- **Technical Accomplishments:**
  - Developed high performance IMS substrates with and without TPG insert, and completed FEA based thermal comparison with SOA DBC
  - Conducted power cycling simulations with various substrates and evaluated performance of each technology under different power cycling conditions
  - Designed various quilt interconnect based silicon chips for electrical evaluation of the technology with different nodule size, thickness and testing conditions
  - Evaluated different transformer and modulation techniques for high performance RF based gate driver solution
- **Future Work:**
  - Characterize different substrates in an experimental setup with SiC MOSFETs
  - Characterize quilt nodules under different current and temperature conditions
  - Build and evaluate RF based gate driver with optimum transformer and modulation scheme
  - Develop substrate for 100kW inverter based on ODBC.

Any proposed future work is subject to change based on funding levels