Wafer Scale Packaging Manufacturing Challenges

DOE SSL Workshop

Raleigh, NC

Shatil Haque
WW Ops Team, Lumileds
04 February, 2016

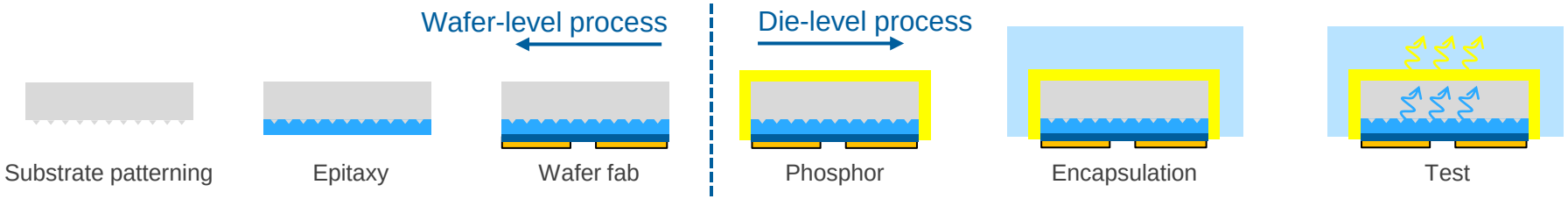
LUMILEDS

Wafer Scale Packaging

CSP LEDs exist today…

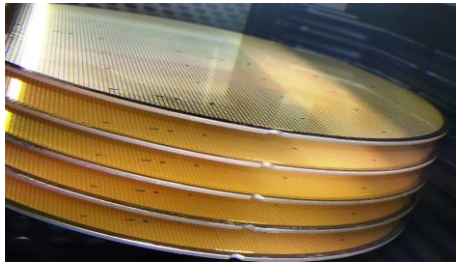
Chip Scale Package
- Reduced cost due to minimal packaging
- Low thermal resistance (no interposer)
- High packing density due to small footprint

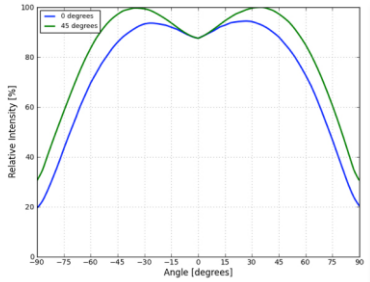
…but involve significant die-level processing



Opportunity for Wafer Scale Packaging

Realize ultimate cost reduction…
- Higher die density in back-end process
- Elimination of pick-and-place steps

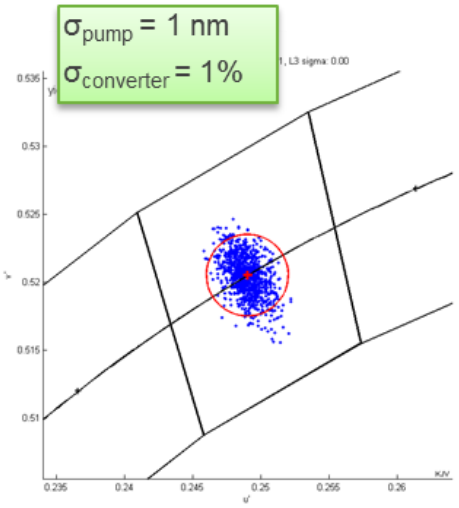




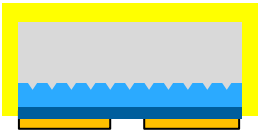
…while maintaining or improving performance in application
- Flux / efficacy
- Radiation profile
- Color over surface/angle
- …

Phosphor Integration Challenges

- **Wafer level integration**
  - Color uniformity larger than industry requirements
  - Requires pump wavelength uniformity within +/-1.25nm across the wafer
  - Requires novel converter (with engineered absorption spectrum) selection in order to be pump wavelength independent if required wafer wavelength uniformity cannot be achieved
  - Requires additional process steps to coat substrate walls upon singulation



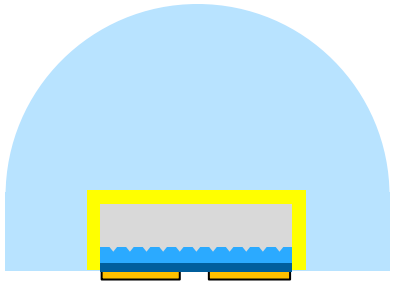
- **Die level integration**
  - Maintaining similar converter optical thickness across all five faces of the die/substrate
  - High aspect ratio of trench limits phosphor integration options



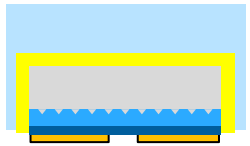
Vertical sidewalls

Optics Integration Challenges - 3D wafer-level processes

Encapsulation: trade-off between lens size and optical performance



"Ideal" lens –
not wafer level



Wafer-level lens –
lower flux and/or changed radiation pattern

➢ Take losses out of LED to reduce need for encapsulation

Novel processes are being developed with high packing density on a wafer

➢ Glass replication (UV casting)
- Thin layer of liquid UV curable polymer replicated on a glass surface, performed at room temperature
- Combination of precision glass molding with the cost benefits of plastic molding

➢ Micro-Optics Foils
- Foil with an optical structure fabricated by soft-lithography
- Desired radiation patterns both from a single or multiple LED sources can be realized

Testing Challenges

- **Full flux measurement**
  - to capture light emitted over a 180deg plane requires singulated testing without blocking side light; significant challenge as LEDs cannot be held mechanically for light blockage reasons
- **Contact issues**
  - vacuum hold needs to counter the upward electrical probe force
  - low force materials to reduce the upward probe force – expensive sockets, higher preventive maintenance due to high wear and tear
  - as package dimensions get smaller, this becomes a bigger challenge
- **Hot testing**
  - providing accurate thermal soak in the optical test environment requires careful setup and thermal characterization
- **UPH constraints**
  - compared to chip-shooter type testers as CSPs have to be mechanically picked and placed onto a delicate socket

Assembly Challenges

- **Electrostatic Discharge (ESD)**
  - Non-CSP LED packages typically carry a TVS on board to protect against ESD; assembly lines will require adequate ESD protection
- **Screen Print accuracy**
  - Due to the smaller size of the component, and especially the smaller distance between the anode and cathode, a tighter control of screen printing is required
- **Die offset and Die rotation**
  - The dimensional tolerances on the side coating process can cause offsets and rotation, where the die does not form the exact center of the package - good design of substrate pad sizes and using the bottom up look camera during placement are required
- **Clamping force at TnR machine**
  - Due to the fragile nature of CSP, the re-centering clamping force could cause crack or damage – require contactless precision mechanism
- **Stacked and Flipped Dies at TnR**
  - With smaller and thinner package, the final process (within TnR process steps) of pick and placement of unit into the carrier tape is vital at high speed of mass volume production

Summary – Critical Success Factors

- **Phosphor Integration**
  - pump wavelength uniformity within +/-1.25nm across the wafer
  - novel converter (with engineered absorption spectrum)
  - materials research on side-coat
  - process for conformal coating on all sides of the die

- **Optics Integration**
  - low cost wafer based processing, tight control on features
  - materials for optics element attach

- **Testing**
  - Testing infrastructure development with contact-less feature, easier calibration, hot testing and high UPH

- **Assembly**
  - Infrastructure development with ESD management, offset for die-rotation, damage and error-free pick and place and/or tape and reel processing


LUMILEDS