Overview

Timeline

• Start – FY15
• End – FY17
• 17% complete

Budget

• Total project funding
  – DOE share – 100%
• Funding received in FY14: $0K
• Funding for FY15: $250K

Barriers

• Achieving $8/kW (peak) integrated traction motor-inverter system
• Mass production and deployment of energy efficient technologies into electric propulsion drives
• Attaining >4kW/L traction drive system power density

Addressed through achievement of higher levels of integration, and increased frequency operation

Partners

• Cree Inc., University of Tennessee-Knoxville
• ORNL team members: Chuck Britton, Laura Marlino, Shane Frank, Dianne Ezell, Leon Tolbert, Jack Wang
Project Objective and Relevance

• Overall Objective
  – Bridge a technology gap presently not addressed by industry.
  – Design, develop, and fabricate a reliable, elevated temperature capable, highly integrated gate drive for use with Wide Bandgap (WBG) devices incorporating slew rate control as an enabler for incorporation of the inverter with the traction motor.

• FY15 Objective
  – Investigate prior and present art in advanced gate drive, slew control and sensing methods.
  – Select/develop an improved topology and associated sensing methods and verify using circuit simulation.
## Milestones

<table>
<thead>
<tr>
<th>Date</th>
<th>Milestones and Go/No-Go Decisions</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dec 2014</td>
<td><strong>Milestone:</strong> Complete research of existing methods for slew rate limiting/control for feasibility and monolithic compatibility.</td>
<td>Complete</td>
</tr>
<tr>
<td>June 2015</td>
<td><strong>Milestone:</strong> Complete initial gate driver architecture design including circuit topology and measurement methods.</td>
<td>In Process</td>
</tr>
<tr>
<td>Aug 2015</td>
<td><strong>Milestone:</strong> Complete the advanced gate driver circuit design and simulation using a WBG load.</td>
<td>In Process</td>
</tr>
<tr>
<td>Aug 2015</td>
<td><strong>Go/No-Go decision:</strong> If simulations do not show the ability to dynamically control the gate drive slew rate, the project will be halted or redirected.</td>
<td></td>
</tr>
</tbody>
</table>
Problem to be Addressed

• Present gate drives are not optimized for use with WBG devices
  - Faster $\frac{di}{dt}$ and $\frac{dv}{dt}$ of WBG devices impose unique system limitations.
  - Fast switching reduces the motor insulation reliability; imposes additional costs in motor, cabling, and EMI filtering.

• Present methods for slew control are lacking:
  - Limited commercial solutions exist – none are dynamic.
  - No methods have been vetted specifically for WBG applications.
  - No methods have been demonstrated for integrated circuit realization or high temperature operation.

• Commercial gate drives are optimized for Si switching speeds— not for the high frequency of WBG devices

**Improved Gate Drive Methods Are Needed for Full Realization of Reliable WBG-Based Systems**
**Strategy:** Create a cost-effective, efficient topology for monitoring and performing dynamic slew control of WBG device gate drive.

**Proposed design will achieve:**
- Higher inverter reliability and efficiency
- Reduction in gate drive electronics volume
- Ultimately, higher temperature capability (>200°C)
- Higher motor reliability
  - Reduced insulation breakdown.
  - Reduced bearing currents.
- Lower cost gate drive systems through parts reduction
  - Gate driver integration.
  - Decreased EMI filtering.
Go No/Go Decision Point: If simulations utilizing the improved gate driver with WBG switches do not show the ability to dynamically control the gate drive slew rate (dynamic range of $\geq 4X$), the project will be halted or redirected.

Key Deliverable: Annual report including design and simulation results of the selected gate driver architecture demonstrating dynamic slew control for $dv/dt$ limiting.
Significant Prior Gate Driver R&D Has Been Performed at ORNL/UT

- **Overcurrent Protection Methods**
  - Solid State Circuit Breaker
  - Fault Current Evaluation
  - Desaturation Detection

- **SOI Gate Driver Chip**
  - Temperature Sensor
  - Under Voltage Lockout (UVLO)
  - Desaturation Detection
  - -55C to 200C Operating Range
  - 10V-30V Operation
### Technical Accomplishments – FY15

Comparison of Conventional Current Measurement Methods

<table>
<thead>
<tr>
<th>Sensor Type</th>
<th>Insertion Loss</th>
<th>External Power</th>
<th>Circuit Isolation</th>
<th>Bandwidth</th>
<th>Size</th>
<th>Accuracy</th>
<th>Relative Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sense Resistor</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
<td>DC to 50MHz</td>
<td>Medium</td>
<td>Medium</td>
<td>Low</td>
</tr>
<tr>
<td>Sense Inductor</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>DC to 50MHz</td>
<td>Small</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Open-Loop Hall Effect</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
<td>DC to &gt;100 kHz</td>
<td>Small</td>
<td>Medium</td>
<td>Medium</td>
</tr>
<tr>
<td>Closed-Loop Hall Effect</td>
<td>Low</td>
<td>Medium</td>
<td>High</td>
<td>DC to 1MHz</td>
<td>Medium/Large</td>
<td>Medium</td>
<td>Medium</td>
</tr>
<tr>
<td>Current Transformers</td>
<td>Medium</td>
<td>None</td>
<td>High</td>
<td>30Hz to 70MHz</td>
<td>Medium/Large</td>
<td>Low-High</td>
<td>High</td>
</tr>
</tbody>
</table>

Sources: Allegro STP98-1-AN, Rev.2, Pearson 2878 Data Sheet

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**The Use of Source-Inserted Passive Devices For Current Measurement Provides the Lowest Cost Solution But Requires Additional Circuitry**
## Technical Accomplishments – FY15

Published Active Gate Drive (AGD) Methods Address Si-based Power Switch Technologies

<table>
<thead>
<tr>
<th>Reference</th>
<th>di/dt</th>
<th>dv/dt</th>
<th>Complexity</th>
<th>i Meas. Method</th>
<th>Chip Compatible</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lobsinger 2012</td>
<td>Y</td>
<td>Y</td>
<td>Moderate</td>
<td>$L_e$</td>
<td>Y</td>
<td>IGBT</td>
</tr>
<tr>
<td>Lobsinger 2015</td>
<td>Y</td>
<td>Y</td>
<td>Moderate</td>
<td>$L_e$</td>
<td>Y</td>
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</tr>
<tr>
<td>Wang 2013</td>
<td>Y</td>
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<td>Low</td>
<td>$L_e$</td>
<td>Y</td>
<td>IGBT</td>
</tr>
<tr>
<td>Park 2003</td>
<td>Y</td>
<td>Y</td>
<td>Low</td>
<td>$L_e$</td>
<td>Y</td>
<td>IGBT / MOSFET</td>
</tr>
<tr>
<td>Gerster 1996</td>
<td>Y</td>
<td>Y</td>
<td>Low</td>
<td>$L_e$</td>
<td>Y</td>
<td>IGBT</td>
</tr>
<tr>
<td>Riazmontazer 2015</td>
<td>N</td>
<td>Y</td>
<td>Moderate</td>
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<td>Y</td>
<td>IGBT / MOSFET</td>
</tr>
<tr>
<td>Chen 2009</td>
<td>Y</td>
<td>Y</td>
<td>Low</td>
<td>$L_e$</td>
<td>Y</td>
<td>IGBT</td>
</tr>
</tbody>
</table>

$L_e = \text{emitter or source inductance measurement}$

These AGD Methods Are Monolithically Compatible, But Have Yet to Address the Specific Drive Needs of SiC Power Devices
Active Gate Drives Can Be Divided Into Two Broad Categories

• Gate “Voltage” Control
  • Gate voltage is fed through a resistor from an amplifier or buffer
  • Implementation Advantages
    • Simple
    • Voltage amplifier can be used.
    • Can be used to control both di/dt and dv/dt loops
  • Implementation Disadvantages
    • Amplifier/resistor combination needs to be able to handle both turn-on and turn-off switching
    • Gate voltage is dropped across a resistor

Technical Accomplishments – FY15

Active Gate Drive Can Be Divided Into Two Broad Categories (cont.)

• Gate “Current” Control
  • Current through a resistor is monitored
  • Implementation Advantages
    • Actual gate voltage is sensed
    • More opportunity for control with greater complexity
    • Can be used to control both di/dt and dv/dt loops
  • Implementation Disadvantages
    • More complex
    • Potentially harder to compensate

Technical Accomplishments – FY15

Active Gate Drive Topology – Initial Design

- Monitor only $dv/dt$ initially.
- Add $di/dt$ capability if simulations indicate a need.
- Incorporate protection circuits including UVLO, desaturation detection, shoot-through protection and short-circuit protection.
- High loop bandwidth ~ 50MHz.
- Provide programming flexibility allowing applicability to varying WBG gate drive needs.
- Maximize compatibility with integrated circuit fabrication for future cost and size reduction.
Technical Accomplishments – FY15

SiC MOSFET – Modeling and Simulation

- Perform a comparison of the vendor-supplied model to measured devices.
- Utilize ORNL WBG power device test and characterization system.
- Perform double pulse testing for observing both turn-on and turn-off characteristics.
- Compare results with vendor provided SPICE simulation models.
- Iteratively modify SPICE models to improve simulation agreement with actual measurements.
- The SiC device ac and dc SPICE model accuracy is key for active gate driver topology optimization.

Accurate Simulation Models Are Essential For AGD Topology Design
Technical Accomplishments – FY15

Summary

• Completed review of closed-loop gate drive techniques.
• Completed review of current and voltage measurement methods.
• Sensing method selected – $\frac{dv}{dt}$ measured from WBG device drain (low cost, miniature, reliable).
• Will investigate performance implications of not monitoring $\frac{di}{dt}$ and will add the $L_e$-based $\frac{di}{dt}$ measurement if determined necessary.
• Initiated Active Gate Driver (AGD) feedback and control topology design.
• Performing testing of SiC MOSFETs to improve SPICE simulation models.
• Initiated AGD circuit simulation using a commercial/custom WBG device model.
Responses to Previous Year Reviewers’ Comments

• This Project is a New Start.
Partners/Collaborators

• Cree, Inc.
  – Consultation regarding commercial WBG device characteristics, modeling and application.

• University of Tennessee, Knoxville
  – Collaboration on integrated circuit design, simulation, layout, and testing.
Remaining Challenges and Barriers

• Refining the AGD architecture and sensing methods for performance and cost-effective implementation.

• Translation of prior circuit designs to SOI.

• Integration of all AGD components onto a single integrated circuit.

• Cost-effective high-temperature packaging for integration into a power module.

• Isolation and shielding packaging requirements in the module for electromagnetic compatibility.

• Variability of parasitics in modules and effect on di/dt and dv/dt controls.

• Availability of high temperature integrated circuit process for highly integrated module.
Proposed Future Work

- **Remainder of FY15**
  - Gate Driver Design & Architecture Selection
  - Gate Driver Design Simulations
  - Annual Report

- **FY16**
  - Board Level Gate Driver Prototyping Using COTS Components
  - Bench Test COTS Gate Driver With WBG Devices
  - Iterate & Finalize Gate Driver Design
  - IC Fabrication Process Evaluation/Selection
  - Annual Report

- **FY17**
  - Gate Driver Integrated Circuit Design and Fabrication
  - Gate Driver Packaging
  - System Test Using the Advanced Gate Driver IC
  - Annual report
Summary

- **Relevance:** Enable size, weight, and cost reduction of electronic drive systems to enable more rapid and reliable deployment of WBG in electric drive systems.
- **Approach:** Develop highly integrated and advanced gate drive methods for WBG drive using integrated circuit technology.
- **Collaborations:** Cree, Inc., The University of Tennessee, Knoxville.
- **Technical Accomplishments:**
  - Completed review of closed-loop gate drive techniques.
  - Completed review of related current and voltage measurement methods.
  - Selected dv/dt as primary sensing method.
  - Initiated AGD feedback and control topology design.
  - Initiated AGD circuit design and simulation activities.
  - Performing WBG power device testing and SPICE modeling.
- **Future Work:**
  - Complete AGD simulation level design.
  - Translate AGD to COTS equivalent and characterize performance with WBG load.
  - Design, layout, simulate, fabricate AGD design in high temperature SOI process (200C).
  - Package for high temperature and characterize AGD integrated circuits with WBG load.
  - Publish research results.
  - Engage OEMs on potential applications for various traction drive platforms.