PACE

ACCELERATING ELECTRIFICATION

MERIT PACE Meeting - PNNL

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MV Converters – Value/Challenges

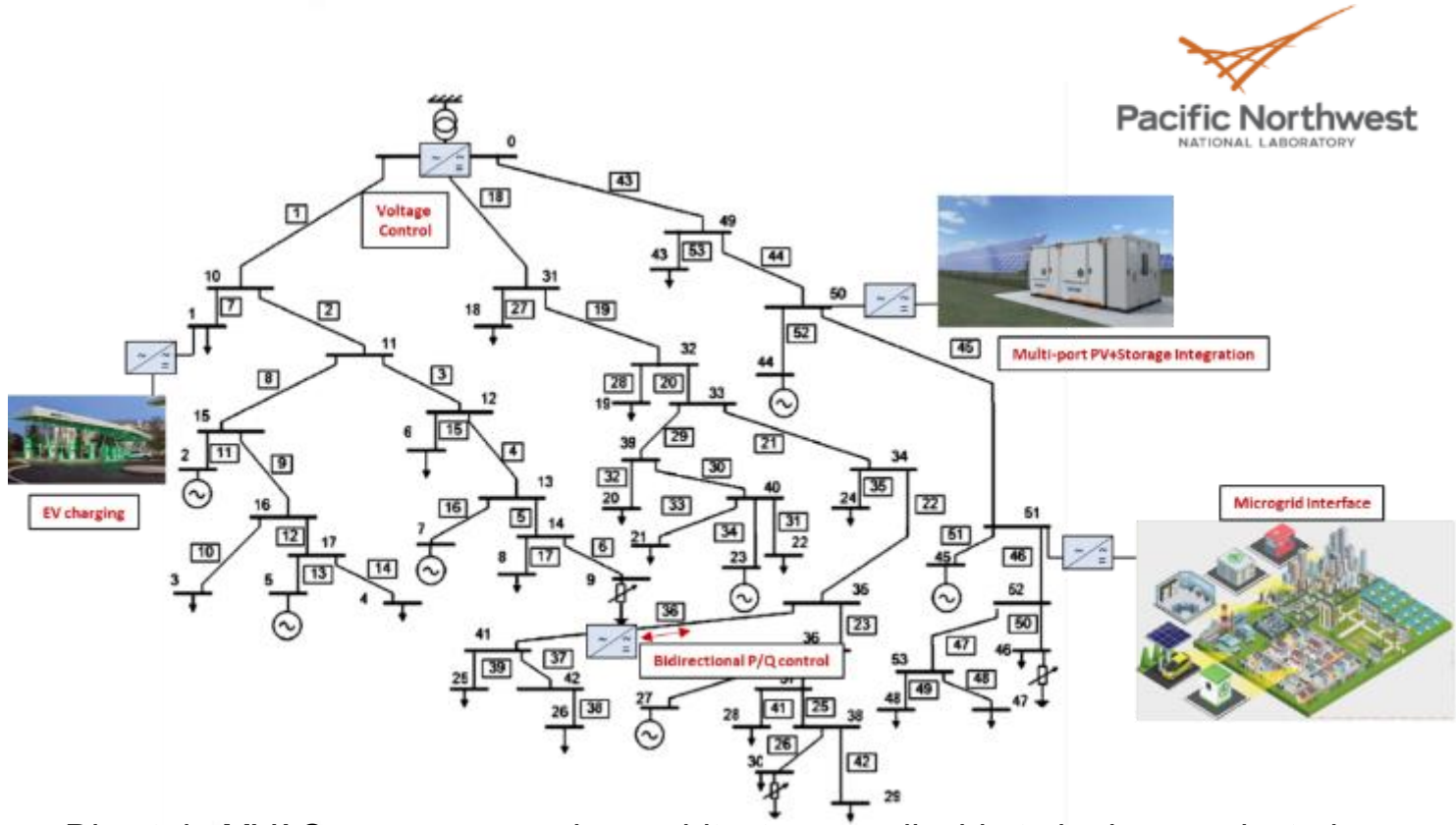
- Tremendous value:
  - Power Density
  - Ease of replacement
  - System Control – P/Q, Voltage, Impedance
  - TriPort applications
  - Resource Integration
- Challenges:
  - Control
  - Coordination
  - Integration
  - Vulnerability

- Emergent and ensemble behaviors under various conditions
- Protections schemes/ controllers and their coordination
- Secondary level control to support system level impact
- Control/sensing and coordination
- Vulnerability and attack graphs

Impact Analysis

PNNL

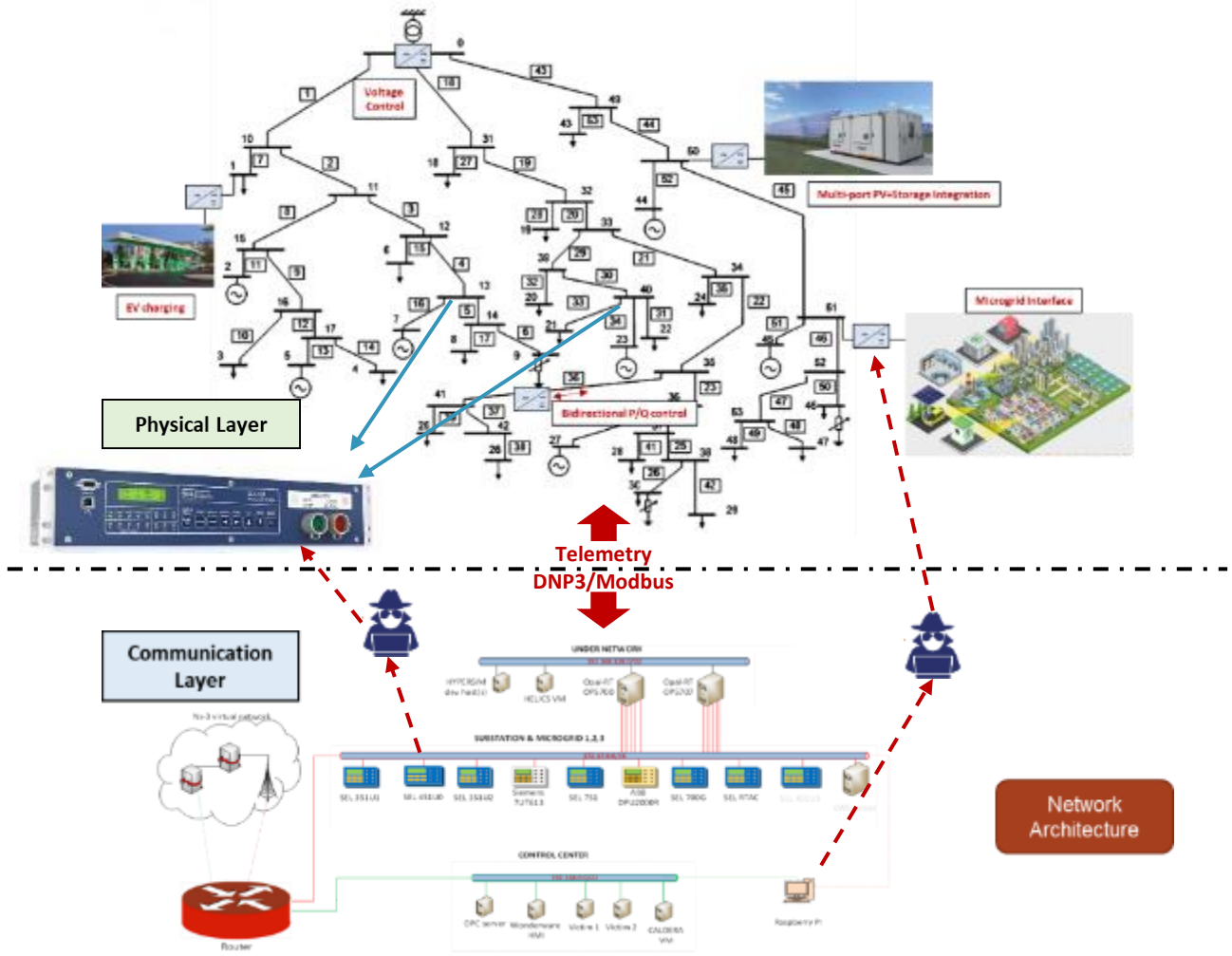
- Conduct studies to determine system level impact in supporting decarbonization, flexibility, stability and added grid services (power flow control, voltage/reactive power support, grid-forming capability, congestion relief).
- Develop secondary control algorithms to support and coordinate intelligent control of multiple MPSSDs on the MV grid operating with various objectives.
- Analyze impacts on system level locational pricing due to added flexibility



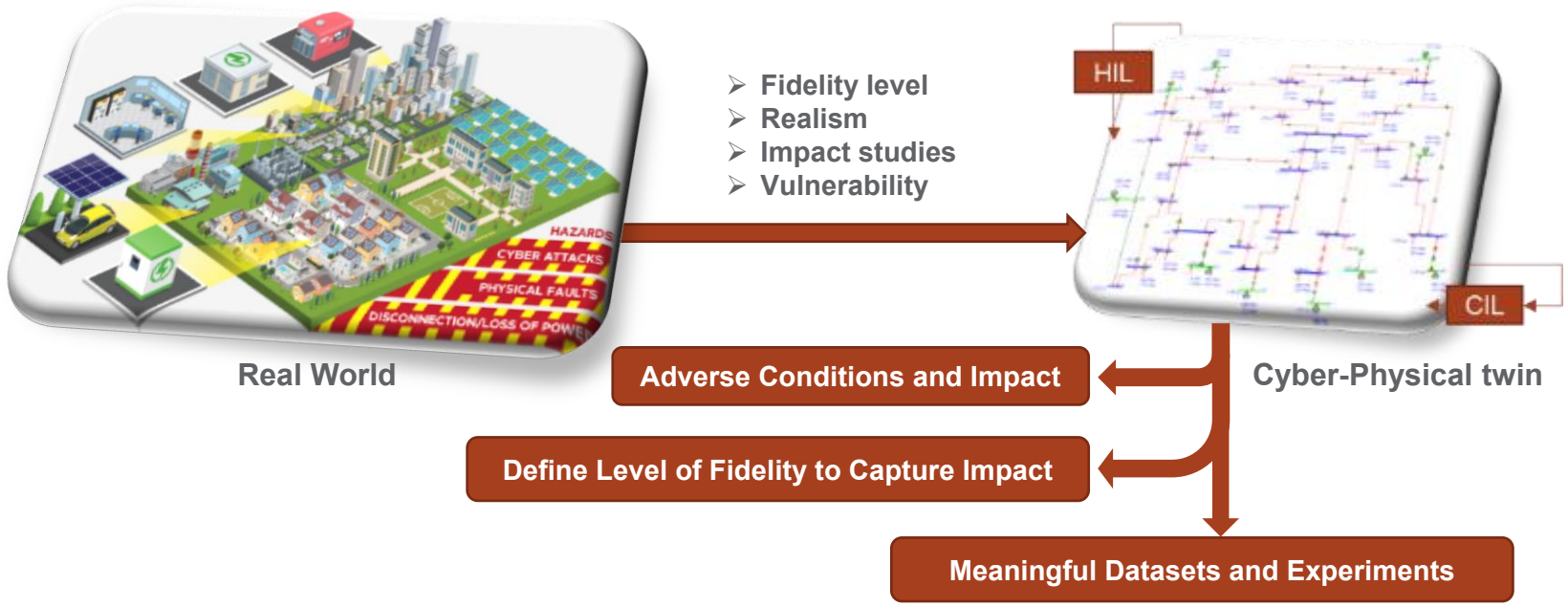
Direct dc-MVAC power conversion architecture, applicable to hydrogen electrolyzer, solar, wind, and storage

Control and Communication

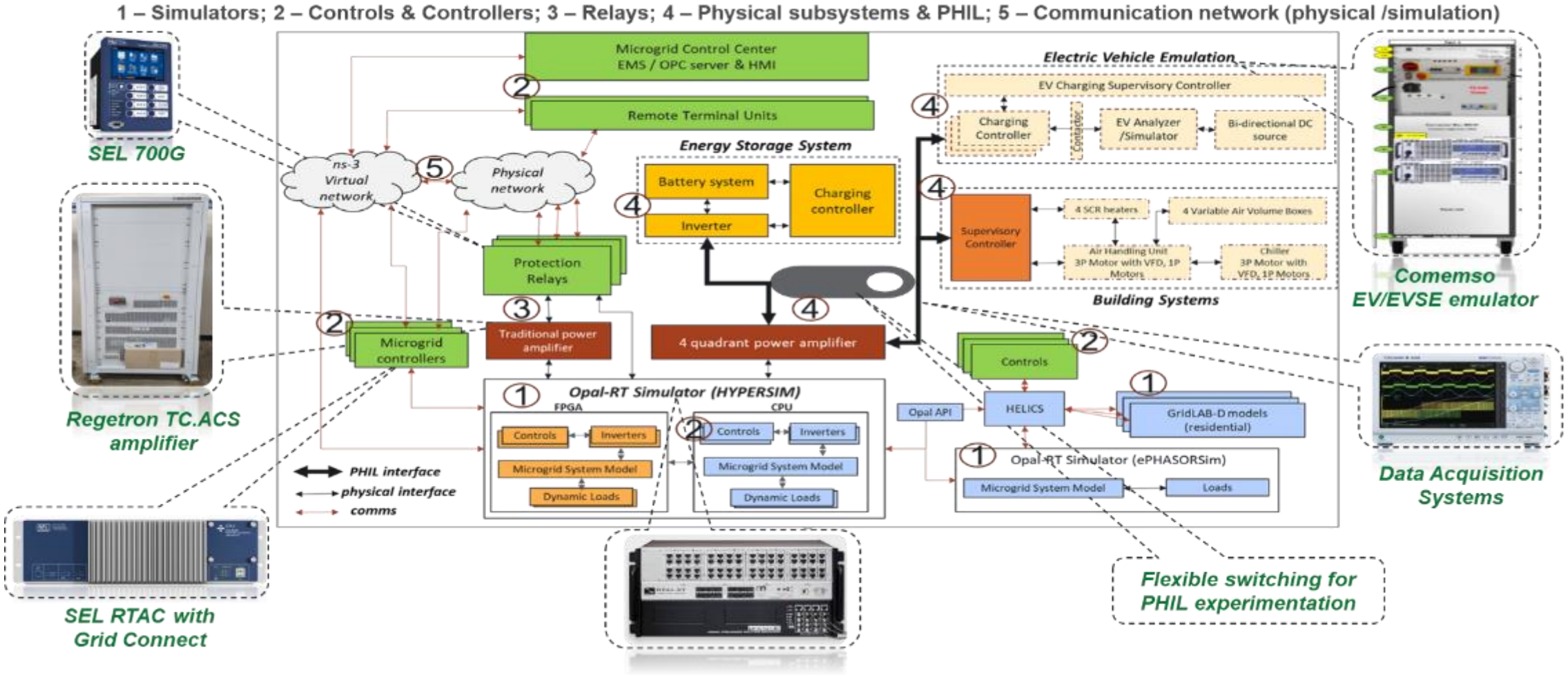
- Correct control and coordination algorithms for
  - Power flow control
  - Voltage Control
  - Microgrid islanding
  - Multiport/ EV charging
  - LMP/DLMP levelling
- Telemetry and communication for control
  - Protocol stack – DNP3/Modbus
- Attack graphs and vulnerability
  - System modes that can be influenced
  - Failure modes
  - Device vulnerability



Approach

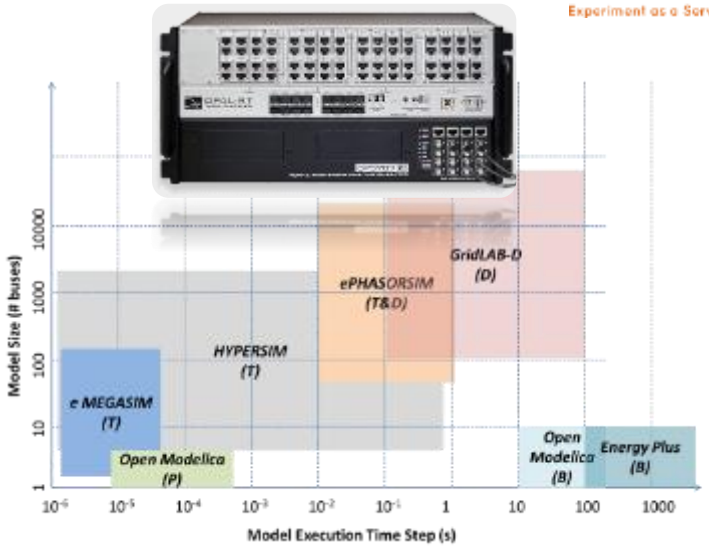

HAZARDS
CYBER ATTACKS
PHYSICAL FAULTS
DISCONNECTION/LOSS OF POWER
Real World
Fidelity level
Realism
Impact studies
Vulnerability
HIL
CIL
Cyber-Physical twin
Adverse Conditions and Impact
Define Level of Fidelity to Capture Impact
Meaningful Datasets and Experiments

High-Fidelity Cyber-Physical Testbed



System Emulation

- **Physical Process Emulation**
  - Hardware-in-the-loop modeling
  - 3 Opal-RT simulators with I/O capabilities (25 + cores)
  - Large scale simulation (systems with over 1000 nodes)
  - HVDC emulators (FPGA based emulations)
- **SCADA Capability and Automation**
  - SEL RTAC
  - OPC Server
  - Support for Modbus, DNP3, and many other protocols
- **Multi-vendor power devices (RTU, relays, meters, microgrid controllers, PMUs)**
  - 11 SEL
  - 7 ABB
  - 5 GE
  - 4 Siemens
  - 3 other
- **5 Building Controllers (ability to connect with Annex)**
- **12 + many software other PLCs**

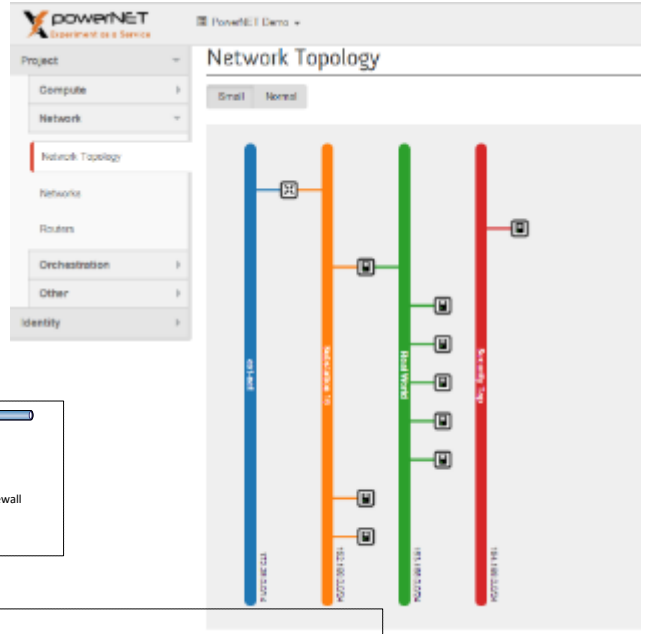


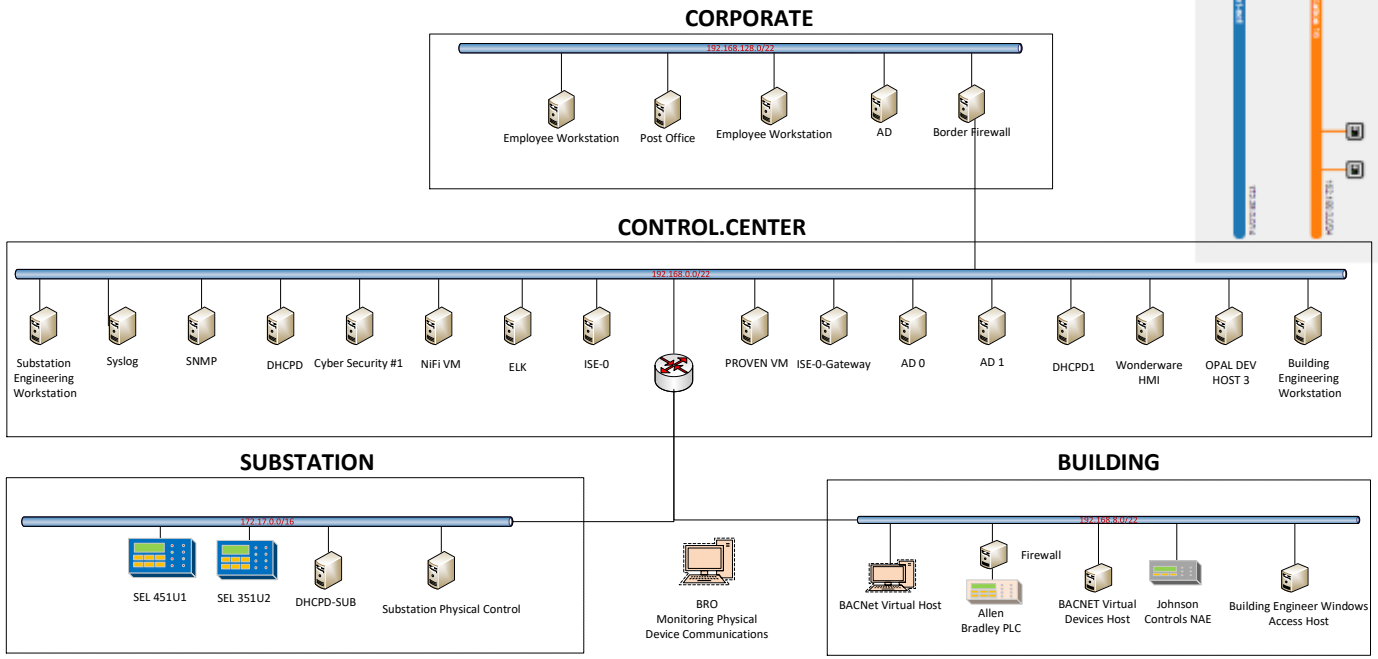
OPAL-RT Emulators

Power Devices and Controllers

Network Emulation

- **Network Virtualization & Emulation**
  - Construct typical network topologies on cloud stack
- **Energy System**
  - SCADA environments
  - Support for legacy communications
  - Synchrophasors
  - Energy Management System
- **Attack Scripting**
  - MITRE Framework
  - Ability to emulate numerous aspects of the kill chain.
  - Man-in-the-middle
  - Command injection

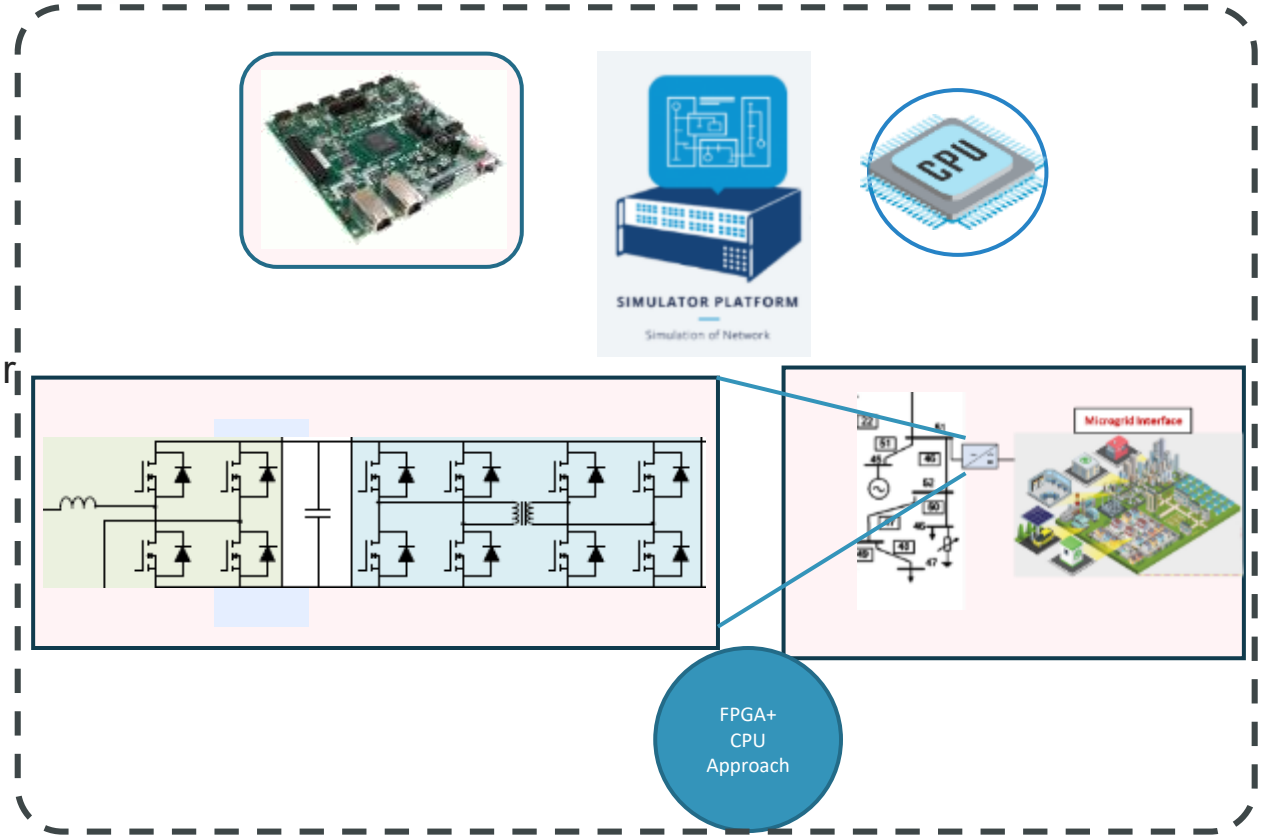




High-Fidelity Adaptation

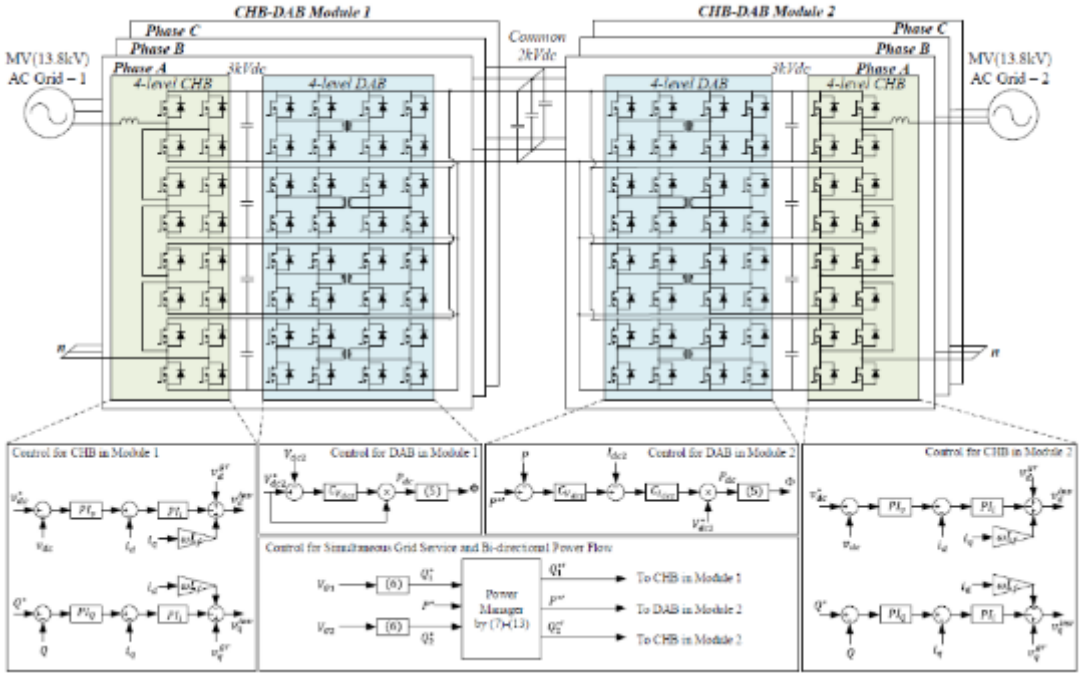
- **Develop high-fidelity models for MV converters on PNNL's testbed using CPU+FPGA based techniques**
  - Emulate detailed converter dynamics at high-fidelity on the FPGA (~10-20 ns)
  - Emulate control, inputs, grid interfaces on the CPU
  - Multi-rate simulation with detailed switching dynamics.
  - Being leveraged to model Solid-state transformers and their system level impact (GMLC).

- **Test novel controls using CHIL approaches**
  - Allows real controller code deployment
  - Inverter behavior can be realistically tested under varying power system conditions



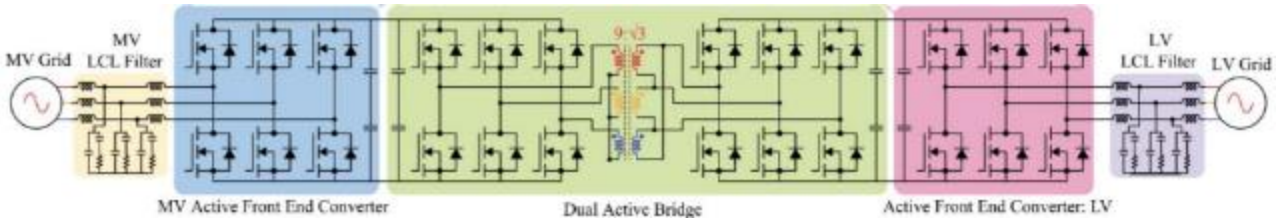
PNNL Task 1: Survey existing MV converter topologies and applications

Topology 1



Source: J. Choi, J. P. Pinto, M. S. Chinthavali and A. Adib, "Medium Voltage Energy Hub Based on Multilevel Cascaded H Bridge-Dual Active Bridge Back-to-Back Converter for Power Distribution Feeders Interconnection and Multiple Simultaneous Grid Services,"

Topology 2

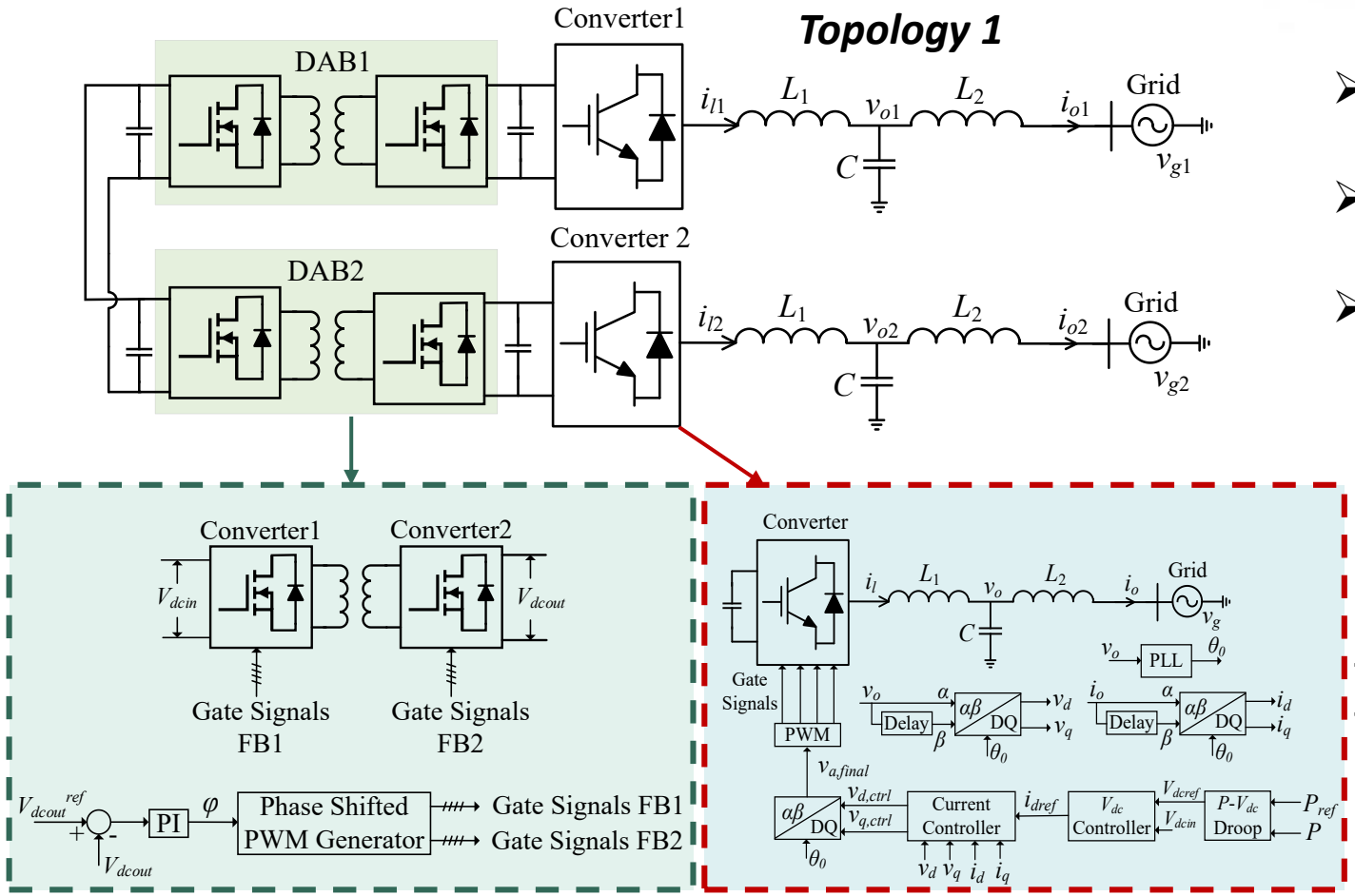


Source: Agarwal, et.al. (2021). Design considerations of 6.5kV enabled three-level and 10kV enabled two-level medium voltage SST

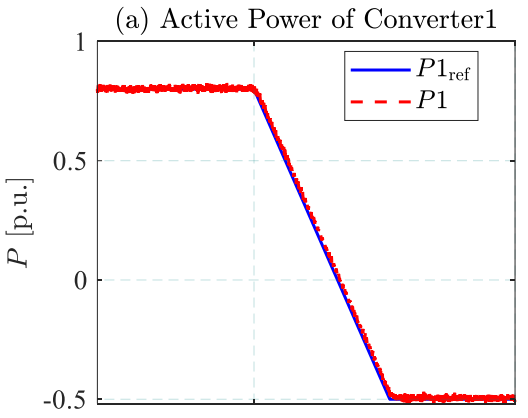
- Modularity – stacked approach
- Scalability – multi-level to realize MV
- Amenable to trip-port applications

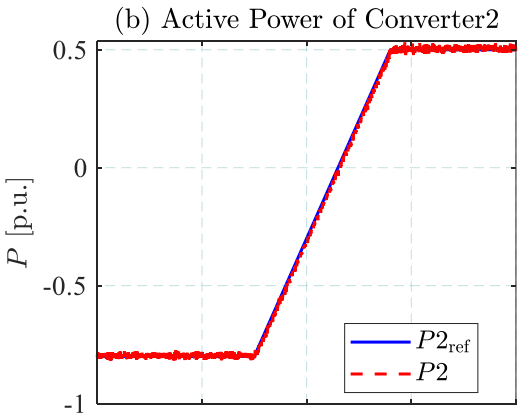
- Lower component count
- Three-phase application specific topology
- Higher device stress

CHB-DAB – Optimized Real-time Models



- Validated the building block at a 2µs timesteps.
- Validated bidirectional power flow application.
- Working with partner (OPAL-RT) to realize stacked MV topology on FPGA





Single-Phase CHB Benchmarking

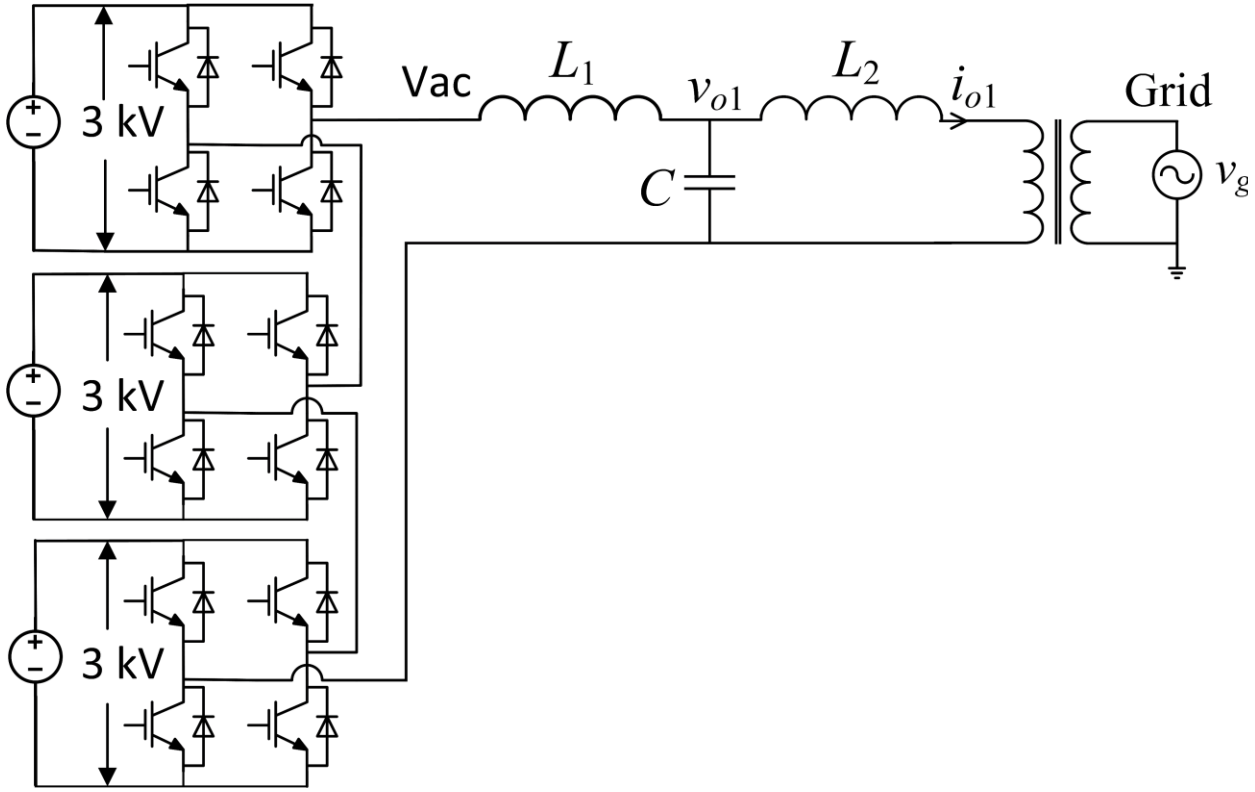
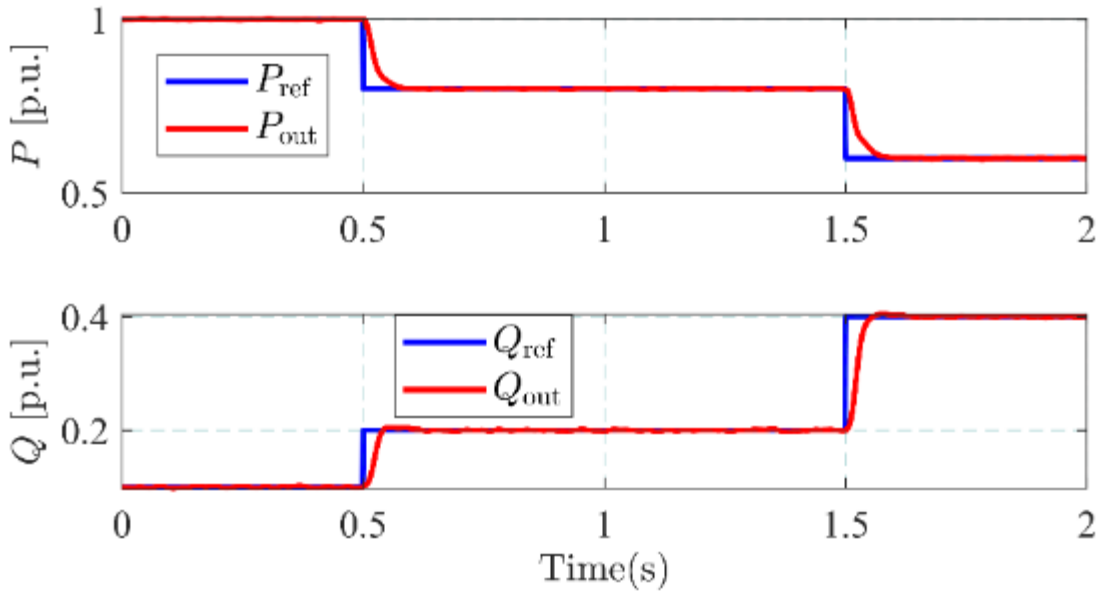


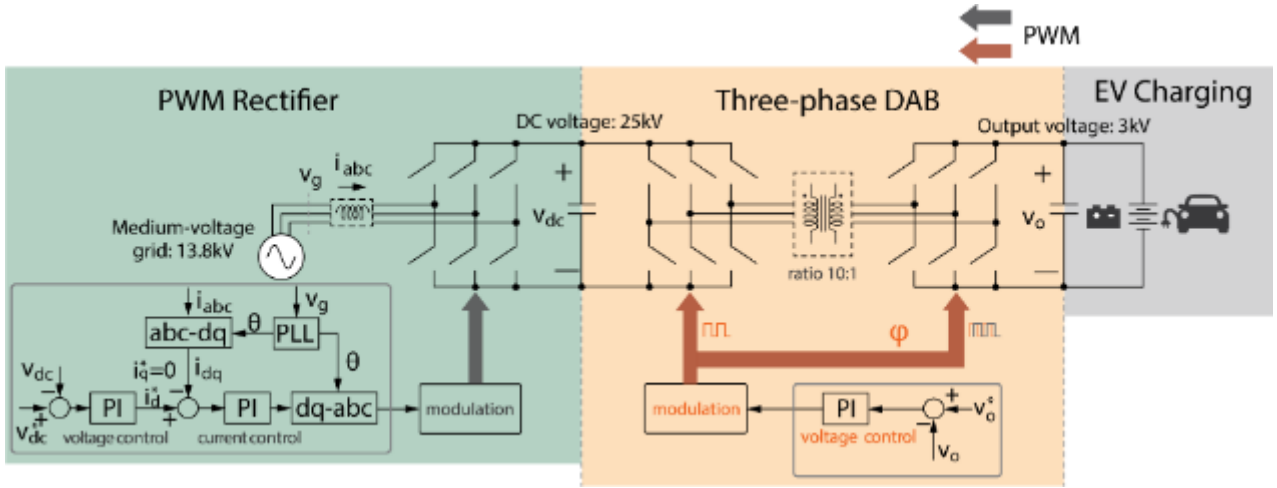
Fig: Topology of the 7-level cascaded converter.

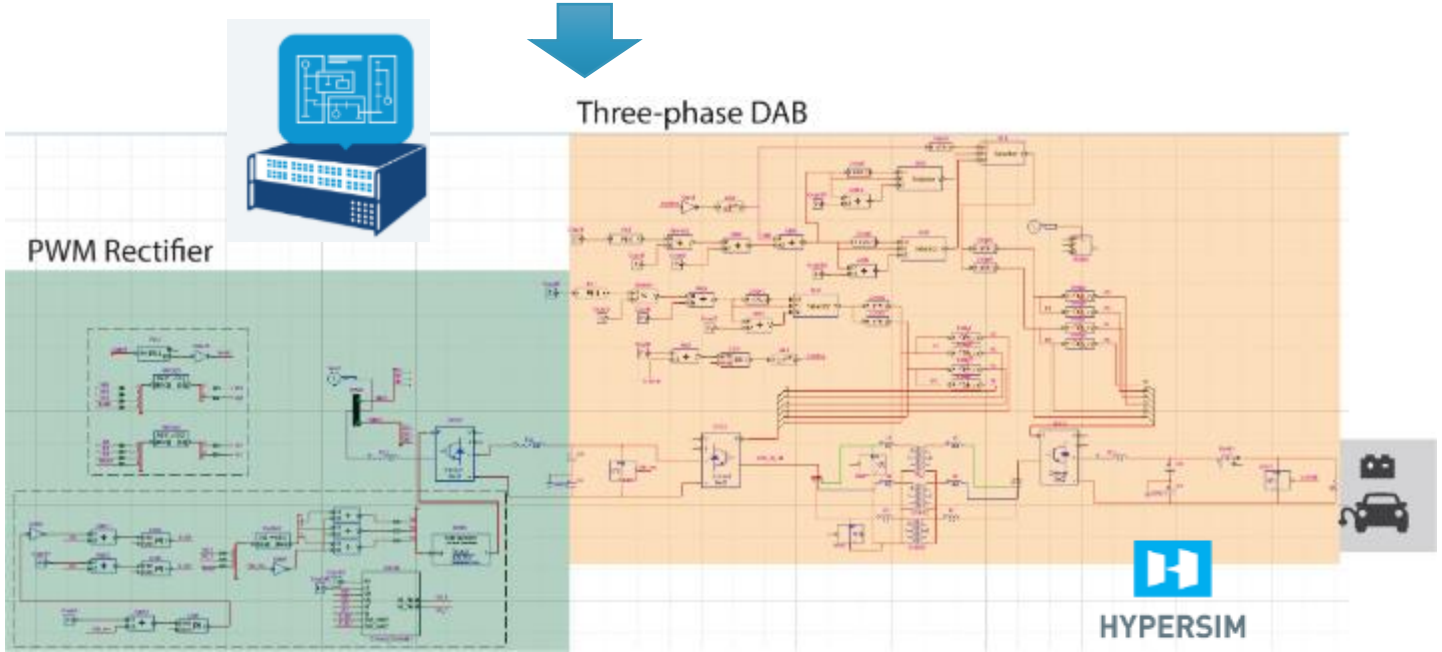
Active-reactive power tracking performances.



The cascaded converter can successfully track the active and reactive power reference injections into the grid.

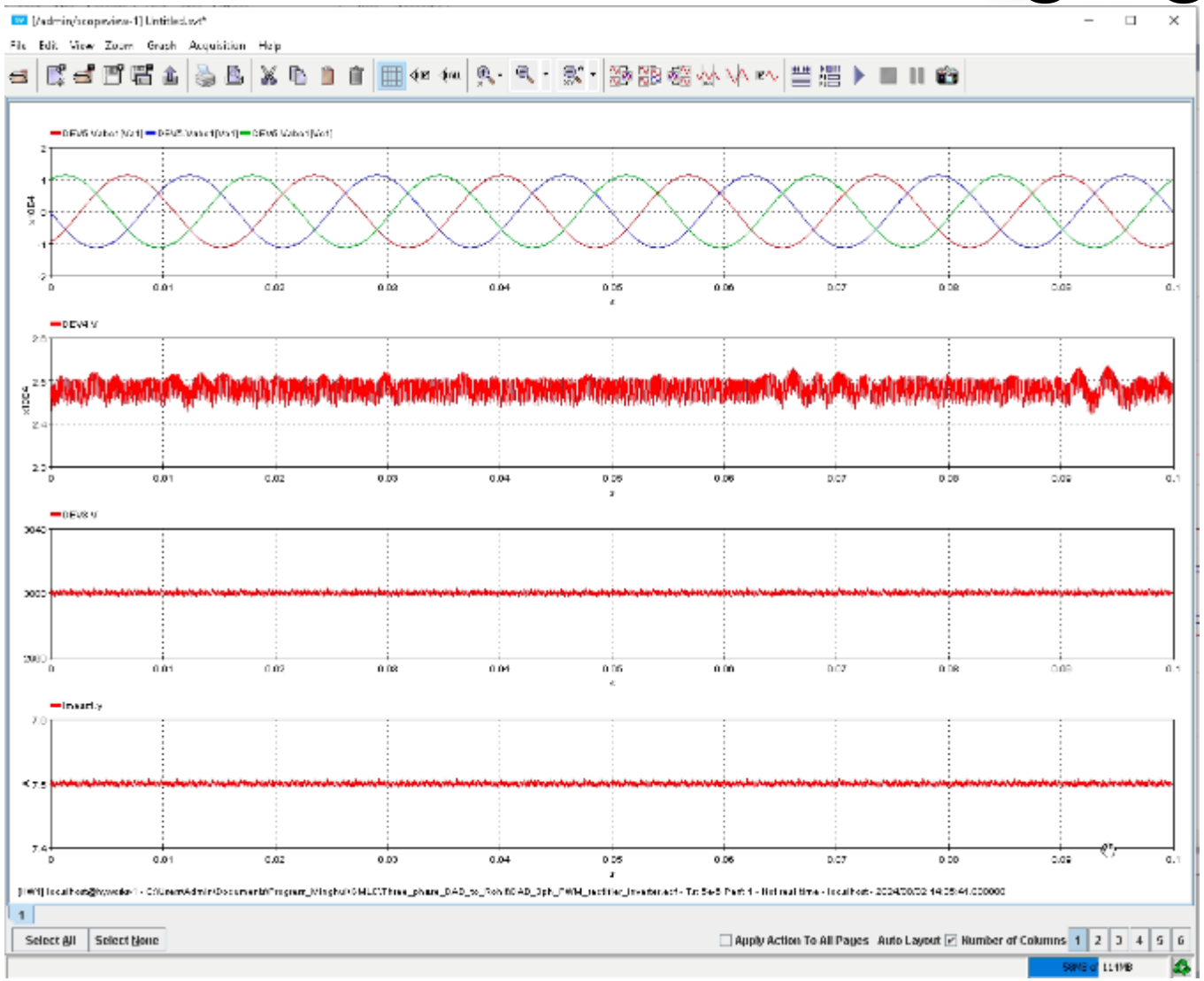
MV Converters – EV Charging Applications





- Validated the building block at a 5µs timesteps.
- Validated bidirectional power flow application.
- Working with partner (OPAL-RT) to realize stacked MV topology on FPGA

MV Converters – EV Charging Applications



- Time step: 5us
- DAB switching freq.: 20kHz
- Rectifier switching freq.: 5kHz
- Transformer ratio 10:1

Medium-voltage grid (LL)
- 13.8 kV

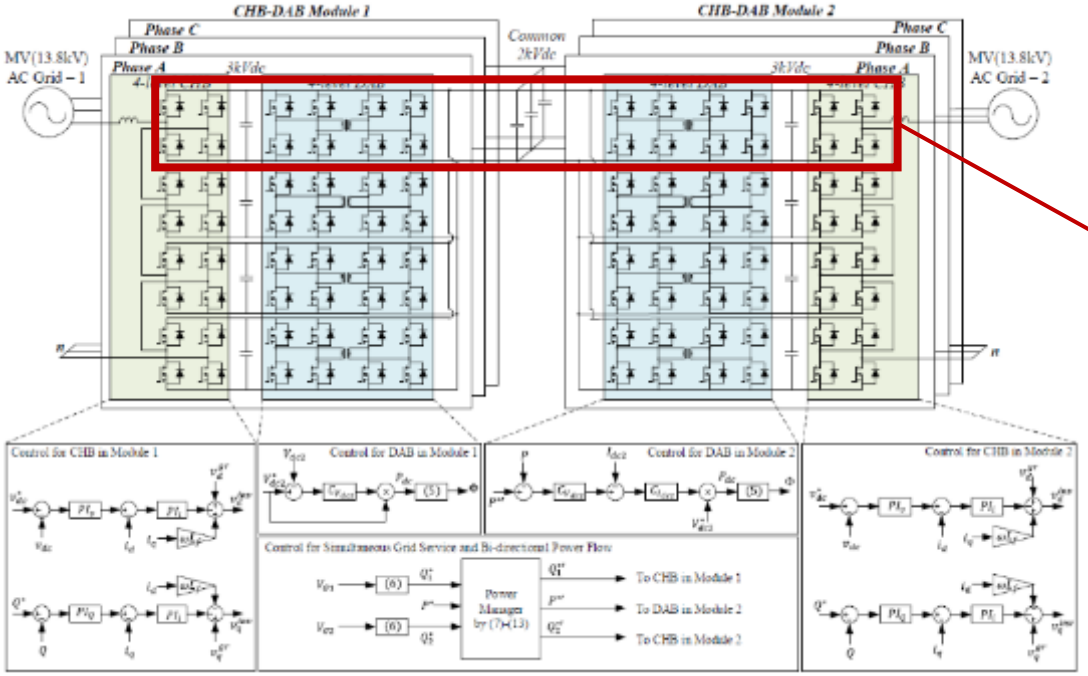
DC voltage after PWM rectifier
- 25 kV

Output voltage
- 3 kV

A resistive load
- 7.5 A

High-Fidelity Implementation Techniques

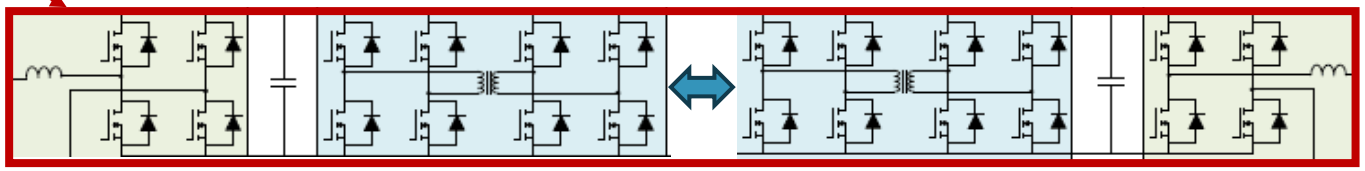
- Focusing on analyzing the computational load to realize building blocks
- Explored CPU + FPGA based modelling capabilities in OPAL-RT platforms.
- Pivoted to eFPGAsim as a platform of choice.



Topology 1

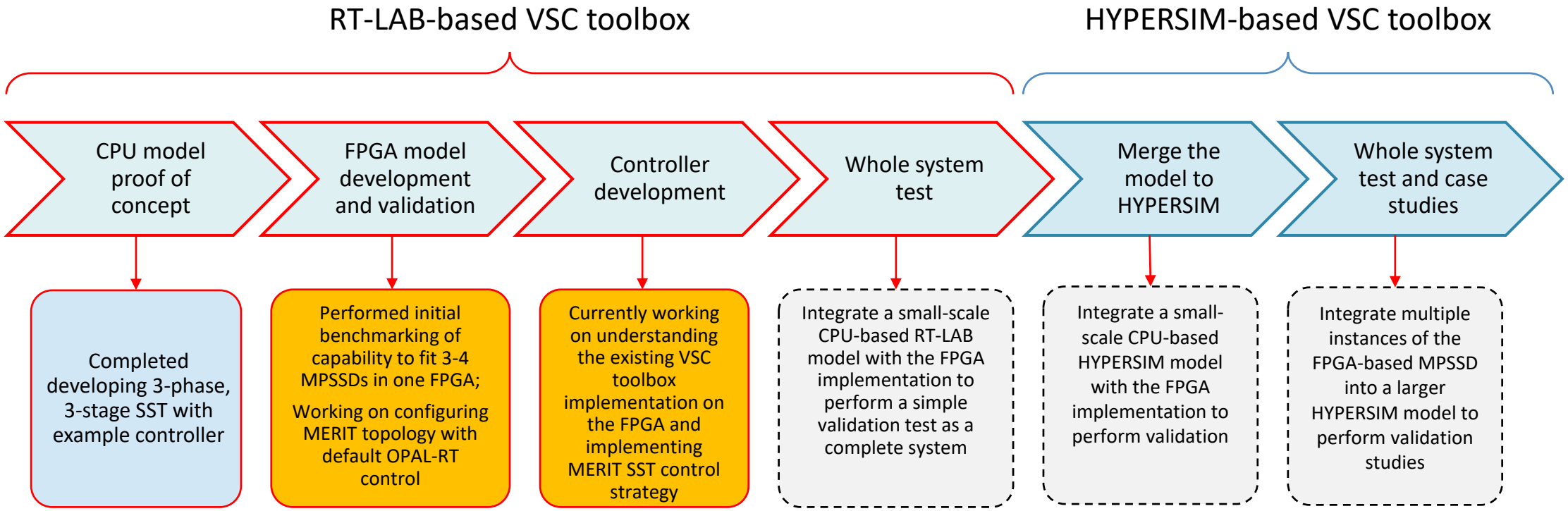
MV Grid - CPU

MV Converter - FPGA



- Explored OPAL-RT's VSC toolbox implementation for rapid FPGA model development
- Building block currently being developed on FPGA

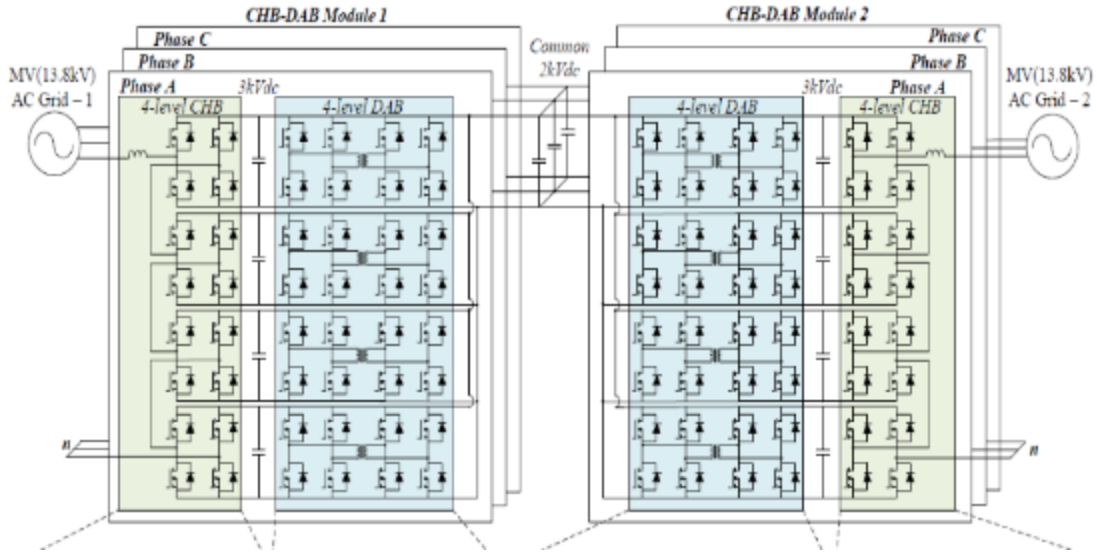
PNNL/OPAL-RT's Development Plan for MERIT SST Topology



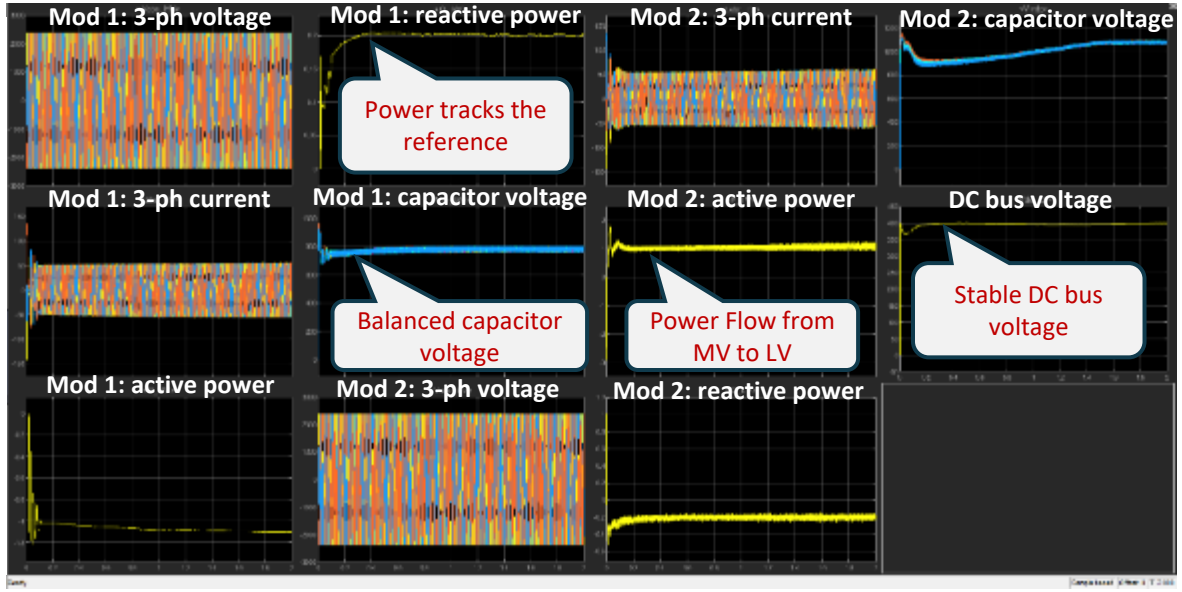
Progress: OPAL-RT

- Developed a CPU-based model in Simulink for demonstrating proof of concept
  - OPAL-RT's VSC toolbox example (CPU-based model) was modified to fit one of the MERIT SST topologies (3-phase, 3-stage)
  - Existing control strategy from the example was used to demonstrate stable results
  - Work is in progress to implement the control approach used for the MERIT SST topology

Diagram of MERIT SST



Preliminary simulation results



Progress Summary

- **Task 1 – Survey MV SST Topologies**
  - Identified two key topologies of interest that could serve a variety of system level applications being explored.
  - Specific aspects of control and implementation were analyzed and discussed with vendor partner OPAL-RT to understand high-fidelity implementation requirements.
  - Task 1 Milestones are on schedule
- **Task 2 – Survey high-fidelity implementation techniques**
  - Developed building block models to understand scalability concerns from a real-time implementation perspective.
  - Explored OPAL-RT's VSC toolbox that can enable building blocks to be directly implemented in FPGA based environments.
  - Currently working on implementing the models using FPGA based techniques and benchmarking them against models developed on CPU based platforms.

Milestone	Description	Scheduled Completion
PNNL.1.1	Survey existing MPSSD topologies and applications	On schedule and completed
PNNL.1.2.	Survey high-fidelity implementation techniques to realize MPSSDs in high-fidelity OPAL-RT platforms.	Initial evaluations completed with vendor partner. Implementation on schedule.
PNNL.1.3.	Create an MV network with MPSSDs modeled at key interfaces like electric vehicle charging stations, PV+ Storage applications and as microgrid interfaces.	BP2Q1
PNNL.1.4.	Implement a secondary control/communication framework to coordinate and control multiple MPSSDs in PNNL's testbed.	BP2Q2