PACE
ACCELERATING ELECTRIFICATION

MERIT: Medium Voltage Resource Integration Technologies

SNL Section

Principal Investigator: Jake Mueller

Affiliation: Sandia National Laboratories

MERIT Overview

Project Objective: Develop modular, cost-effective, and scalable technologies at medium voltage (4.16 kV to 34.5 kV) that will reliably integrate a range of distributed energy resources (solar, wind, fuel cells, etc.) on to the grid.

Target Metrics:
- >97% efficiency
- 40+ year service life
- >90% up-time

Project Pillars

Advanced Components and Power Stages	Advanced Converter Systems	Resource Integration& Management Systems	Grid Integration and Demonstration @scale
Materials & Components, Embedded Controllers	Power Stages & Sub-System Prototypes	Auxiliary Systems, Software Platforms, Algorithms, System Prototypes	Demo Use Case
VALLEY OF CHALLENGES	VALLEY OF CHALLENGES	VALLEY OF CHALLENGES	VALLEY OF CHALLENGES
Sandia National Laboratories; Wolfspeed; SEMIKRON innovation+service; Microchip; HITACHI	Oak Ridge National Laboratory; Virginia Tech; University of Colorado Boulder; University of Arkansas; Sandia National Laboratories	Oak Ridge National Laboratory; Virdi Parente; EATON; NREL Transforming ENERGY	NREL Transforming ENERGY; Pacific Northwest National Laboratory; Southern Company; OPAL-RT Technologies
TRL 2–7	**TRL 3–7**	**TRL 4–7**	**TRL 5–7**
Advanced Components	MV PE Subsystems Inverters converters	Software platforms, Real-time Optimization	**Novel multi-port Medium Voltage PE System: Future pilot**

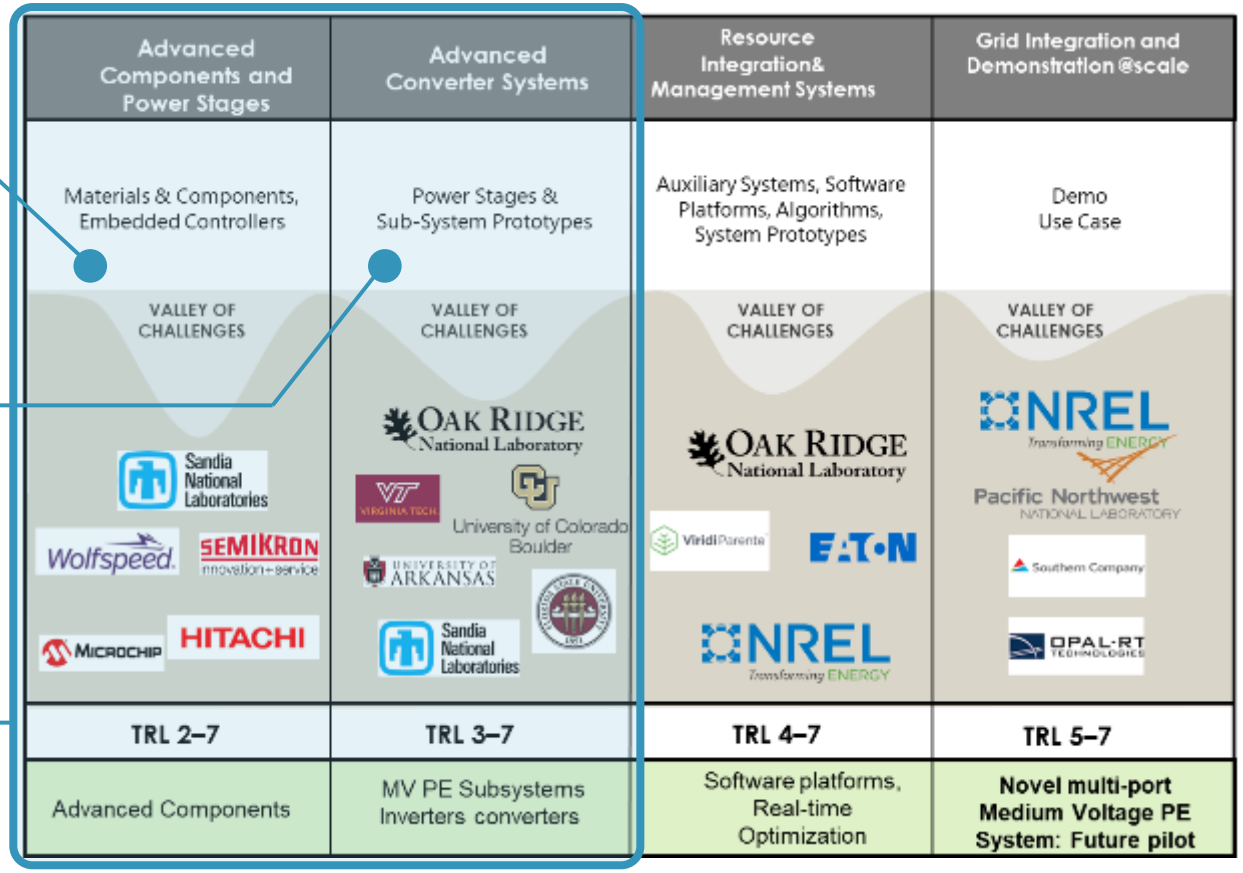
SNL Focus: Devices and Subsystems

Semiconductor Reliability Assessment

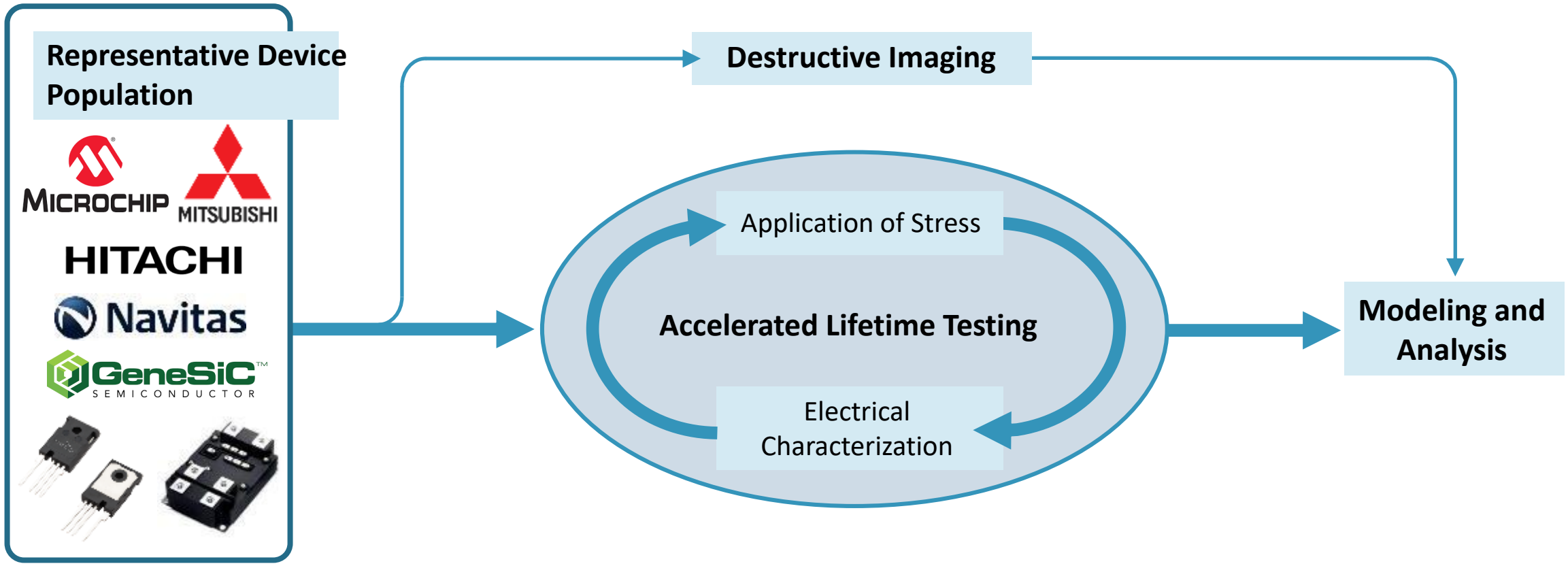
MV DC-DC Subsystem Development

MV Technology Gap Analysis

Project Pillars



Approach: Semiconductor Device Reliability

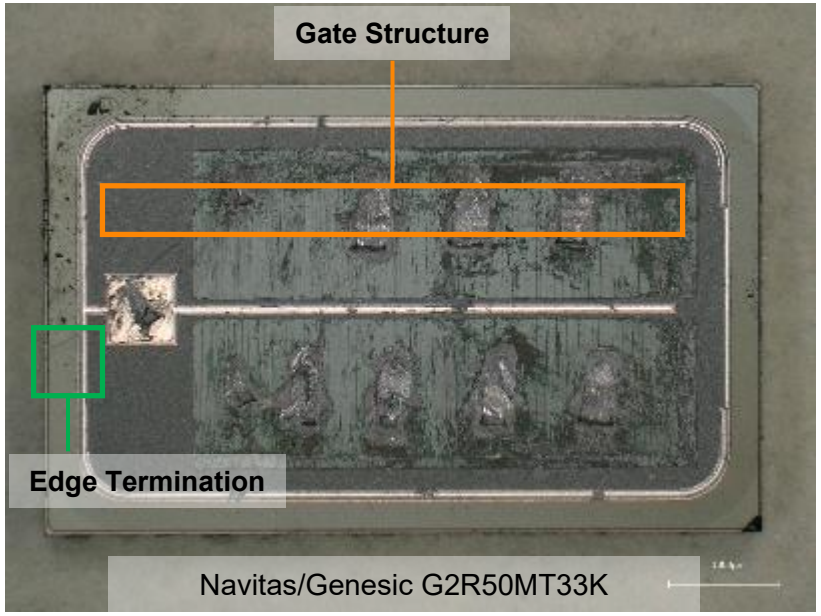


3.3kV+ SiC Device Population

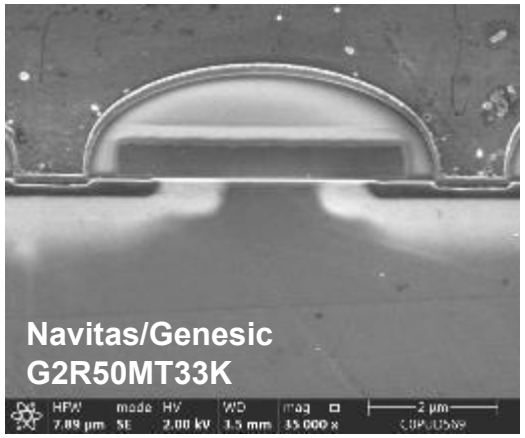
Form Factor	Manufacturer	Part Number	Voltage Rating	Current Rating	Quantity In Hand or On Order	Target Quantity
Bare Die	Microchip	MSC027SMA330D/S	3.3 kV	104 A	44	30
Discrete (TO-247-4)	Microchip	MSC080SMA330B4	3.3 kV	63 A	120	120
Discrete (TO-247-4)	Navitas/Genesic	G2R50MT33K	3.3 kV	41 A	130	120
Power Module	Hitachi	5SFG0500X330100	3.3 kV	500 A	12	12
Power Module	Mitsubishi	FMF200DC-66BE	3.3 kV	200 A	24	24
Power Module	Mitsubishi	FMF25HB-130BE	**6.5 kV**	25 A	24	24
Other Device Candidates						
Bare Die	Wolfspeed	CPM3-3300-R050A	3.3 kV	63 A	0	N/A
Discrete (TO-263-7)	Navitas/Genesic	G2R120MT33J	3.3 kV	35 A	0	N/A
Discrete (TO-263-7)	Navitas/Genesic	G2R1000MT33J	3.3 kV	4 A	0	N/A
Discrete (TO-247-4)	Microchip	MSC400SMA330B4	3.3 kV	11 A	0	N/A
Power Module	Wolfspeed	CAB600M33LM3	3.3 kV	770 A	0	N/A
Power Module	Toshiba	MG800FXF2YMS3	3.3 kV	800 A	0	N/A
Power Module	Mitsubishi	FMF185DC-66A	3.3 kV	185 A	0	N/A
Power Module	Mitsubishi	FMF375DC-66A	3.3 kV	375 A	0	N/A

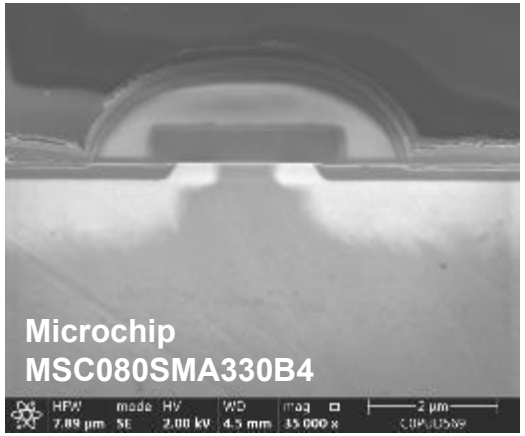
Device Imaging and Characterization

- Device internal structure and composition
  - Gate metal geometries
  - Chemical mapping of the gate structure
  - Channel design and doping strategies
  - Edge termination design and doping strategies
  - Chemical mapping of the passivation stack
- Provides critical context for degradation results

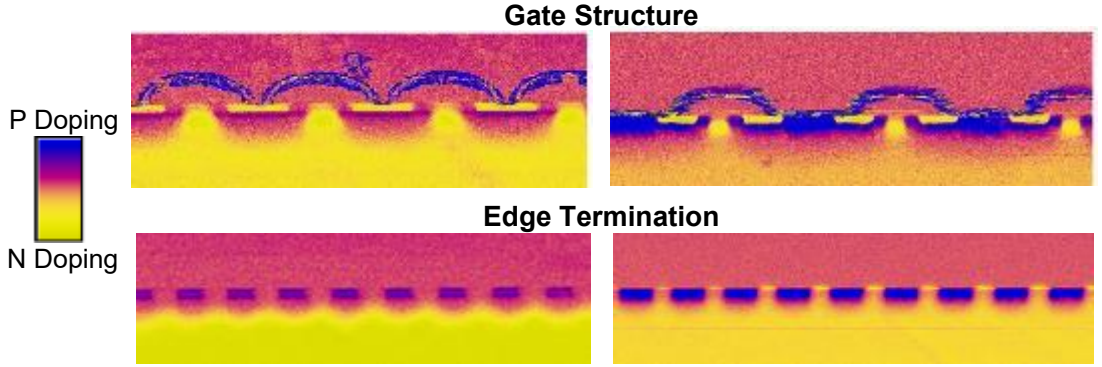


Scanning Electron Microscopy (SEM)





Scanning Capacitance Microscopy (SCM)



Accelerated Lifetime Testing via H3TRB

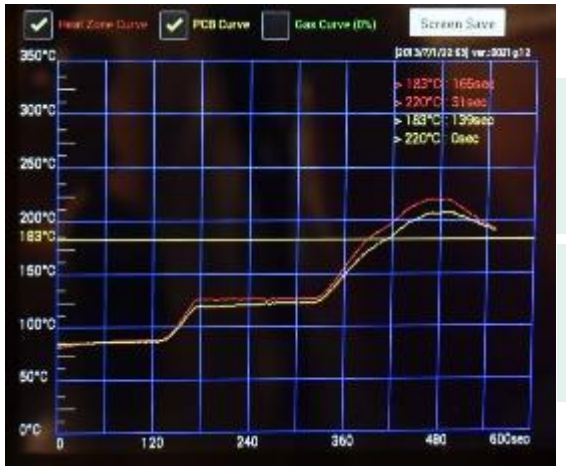
Test Plan

- 85°C, 85% rH, 1100 hours
- 20%/40%/60%/80% of Breakdown Voltage Bias
- Device characterizations at t = [0, 100, 300, 700, 1100] hours
  - Comparing data sheet specs including threshold voltage, transfer characteristics, output characteristics, reverse leakage, and switching capacitances

Current Status

- Device Serialization and Baseline Testing Complete
- Preconditioning Complete
- 'Round 1' H3TRB Chamber Test Initiated
  - ✓ Round 1: 40%/80% Breakdown Bias Condition
  - ○ Round 2: 20%/60% Breakdown Bias Condition

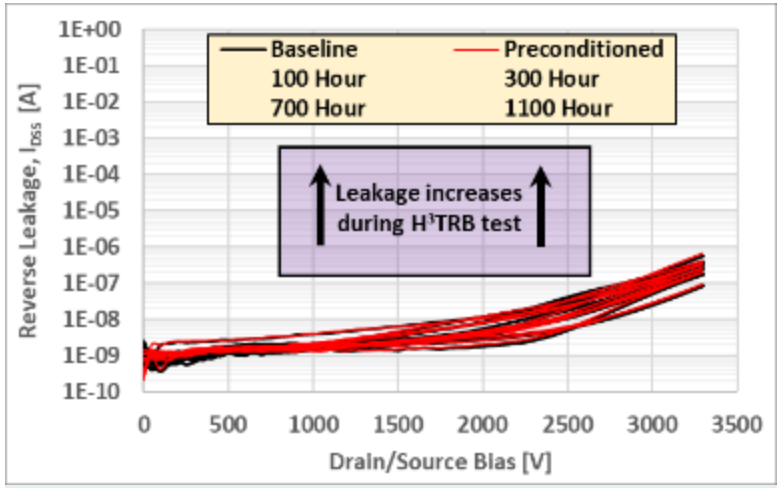
Goal: Conclude 'Round 1' 1100-hr Test by 09/30



Prior to testing, all to-be-tested devices undergo preconditioning steps to emulate a typical industry solder reflow operation

(1) 24-hour bake-out at 125C,
(2) Moisture soak at an rH of 85% at 85C for 168 hours,
(3) Three reflow cycles in accordance with JESD22-A113D.

Reverse Leakage (I_{DSS}) for Microchip MOSFET (MSC080SMA330B4)



Increased reverse leakage is a common failure mode observed in HVDC-H3TRB testing. Additional data sheet specs are monitored

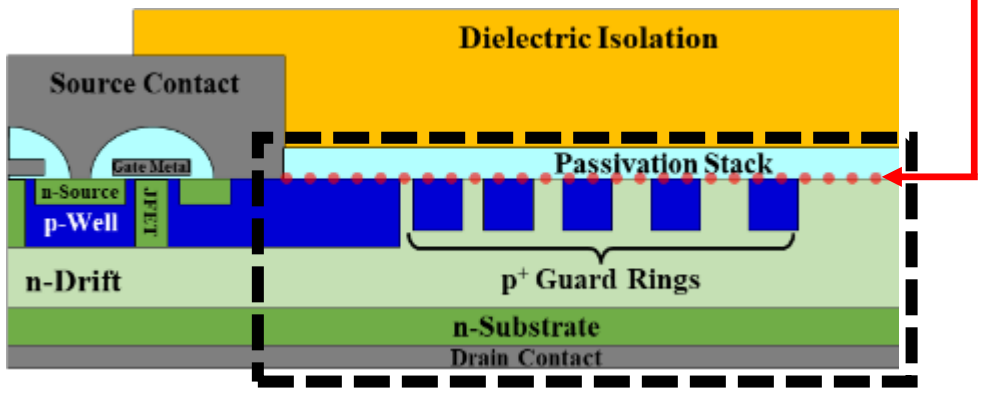
Modeling and Analysis

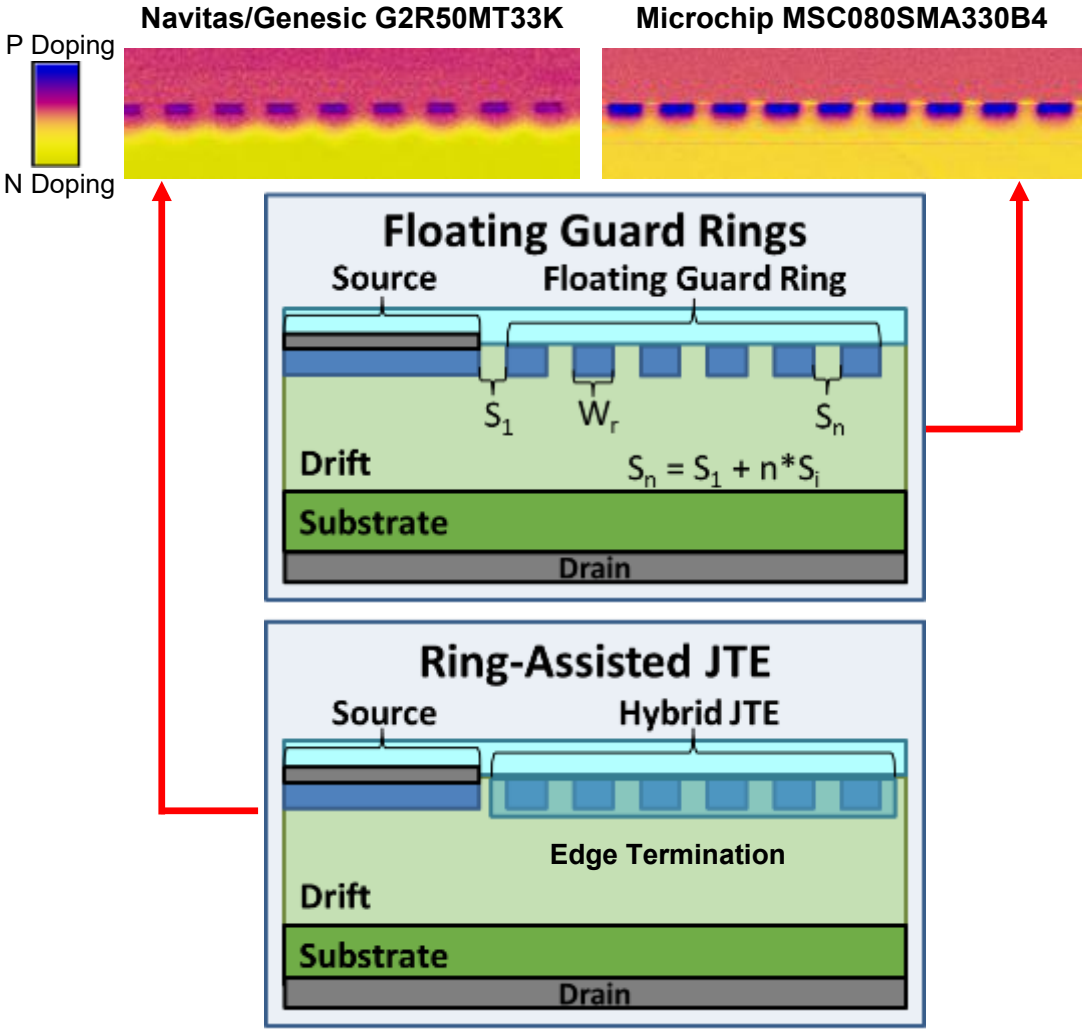
Multiple Edge Termination Styles

- **Floating Guard Rings** utilized by Microchip
- **Ring-assisted JTE** utilized by Navitas/GeneSiC

Deeper investigation of edge termination impacts via TCAD modeling

- Model robustness of JTE to surface charge accumulation (red circles)





Developing Capabilities: Device Reliability

Power Electronics Reliability Lab (PERL)

- Extensive facilities for wide bandgap device characterization and evaluation
- Reliability benchmarking and failure-physics analysis
- Understanding relationships between mission profile and device degradation

Approach: MV Subsystem Development and Integration

- Design, build, and demonstrate two medium voltage DC-DC power stage circuits
  - 4kV DC at high-side port, >50kW rated power
  - Isolated and non-isolated topologies
  - Bidirectional power flow; utility-scale storage as motivating application

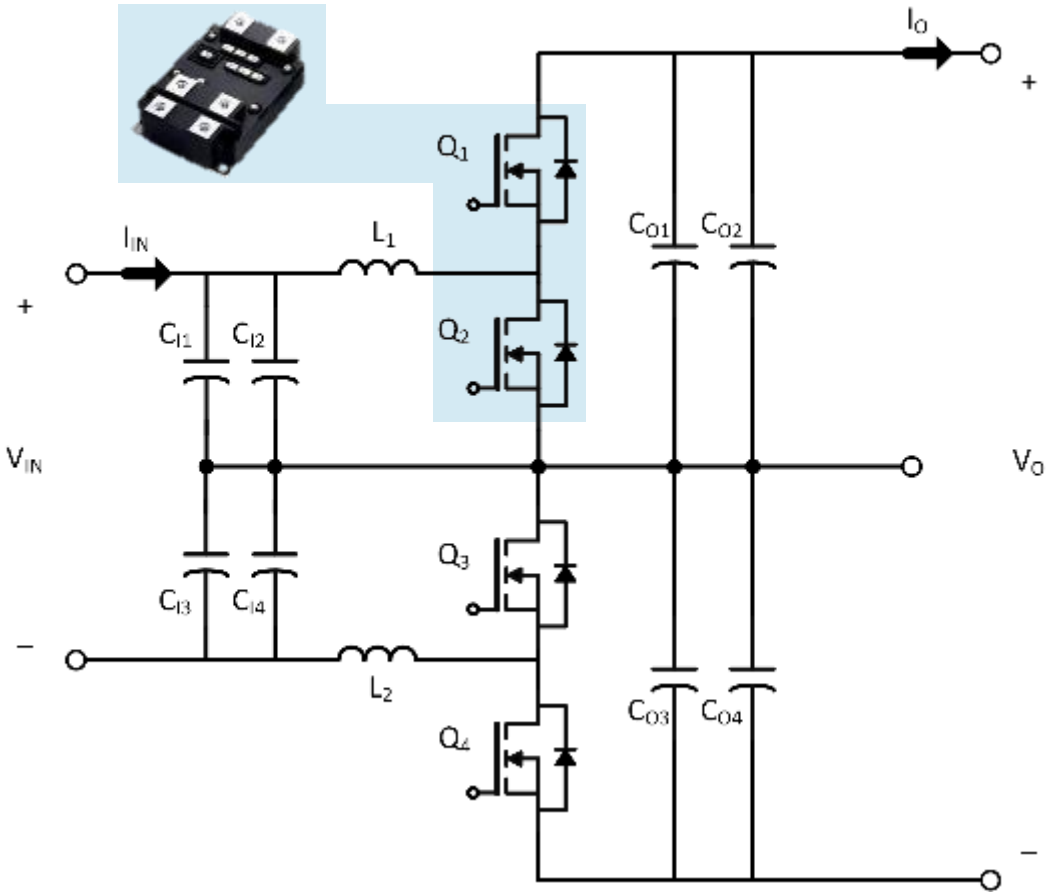
- Adopt perspective of practicing power electronics engineers developing power conversion products for MV systems

- Leverage existing (and opposing) MV design philosophies from power electronics research communities and industry: ***monolithic*** vs. ***modular***

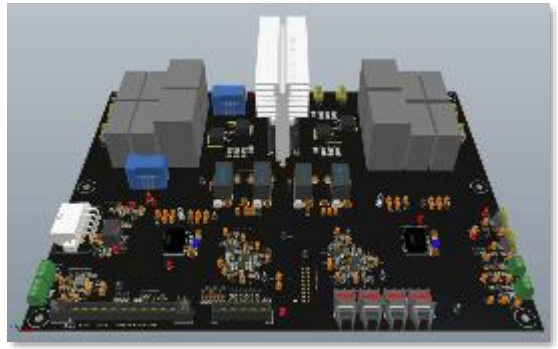
- Design process serves as a practical vehicle for MV power conversion technology **gap analysis**

MV Subsystem Development

Non-Isolated Converter



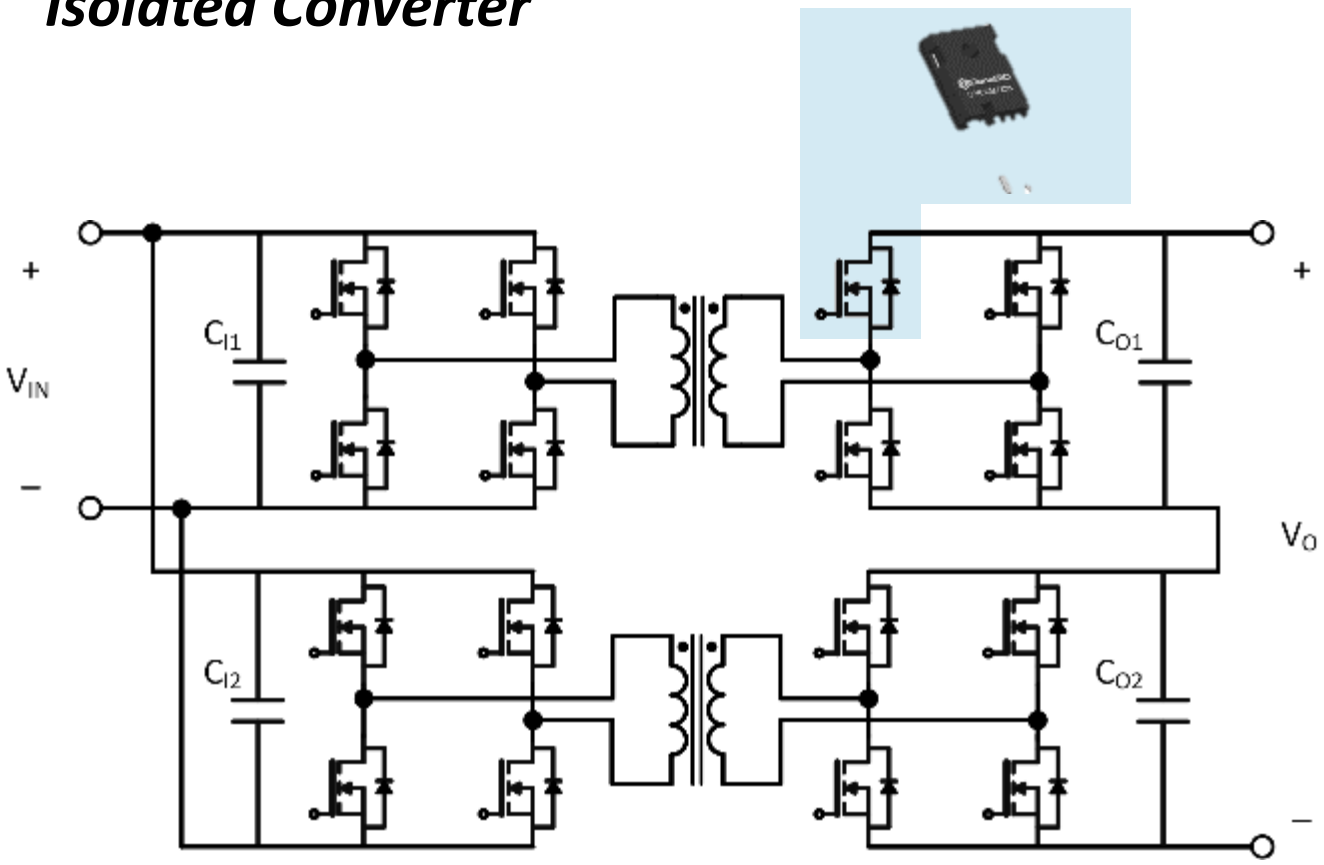
- Design philosophy:
  - Performance and reliability through simplicity
  - Low part count, but high-cost and high-performance components
- Monolithic power handling means custom laminated busbar is required
- Final design will use power module, tentatively Mitsubishi FMF200DC-66BE
- Staged approach to hardware implementation



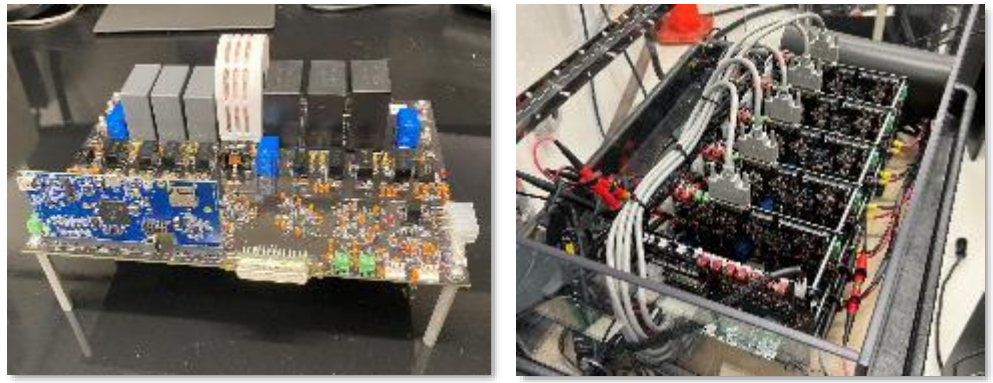
Low voltage non-isolated converter prototypes for lab-scale experiments.

MV Subsystem Development

Isolated Converter



- Design philosophy:
  - Performance and reliability through modularity
  - High part count, but low-cost components and simplified service (module replacement)
- Two dual active bridge modules in an input-parallel-output-series configuration
- Discrete 3.3kV devices at high voltage side, tentatively Navitas/Genesic G2R50MT33K
- PCB-based structure due to low power requirements per module



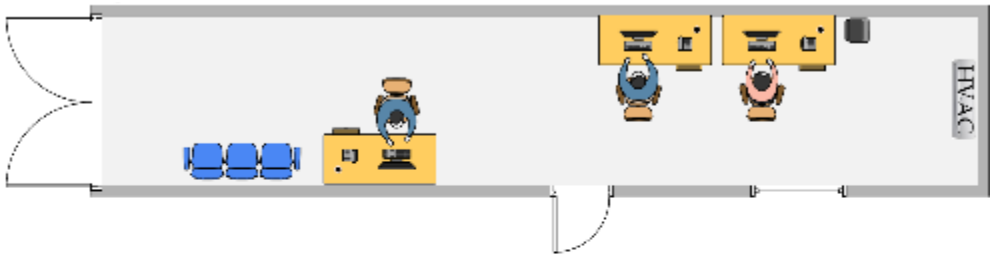
Low voltage isolated converter prototypes for lab-scale experiments.

Developing Capabilities: MV Performance Validation

Medium Voltage Power Electronics Facility

- Dedicated test environment for experimental MV power conversion systems
- Multiple MV sources up to 15kV-class AC and 12kV DC
- Currently in final stages of construction, last outage complete on **8/14** (!)

North Container
Experiment Control



South Container
MV Power Hardware and Experiments

Summary

- **Our Goal:** Comprehensive readiness assessment of MV grid-interactive power electronics
  - What is **working**?
  - What is **missing**?

- **Driving Question**: Can solid state infrastructure meet and exceed the performance and reliability of electromechanical alternatives?

- Strong focus on component-level reliability 3.3kV SiC devices
  - Accelerated lifetime testing via H3TRB
  - Understand physics of degradation and relationship to device structure

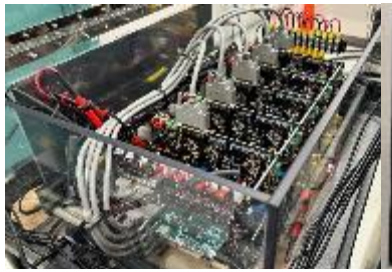
- Construct 4kV DC-DC converter circuits using 3.3kV devices
  - Use design process to identify and understand gaps in supporting technologies
  - **Cast a wide net**: isolated and non-isolated, monolithic vs. modular, power module vs. TO-packaged device

THANK YOU

This project was supported by the Department of Energy (DOE) - Office of Electricity's (OE), Transformer Resilience and Advanced Components (TRAC) program led by the program manager Andre Pereira (OE), Eric Miller (Office of Energy Efficiency & Renewable Energy), and the Grid Modernization Initiative.

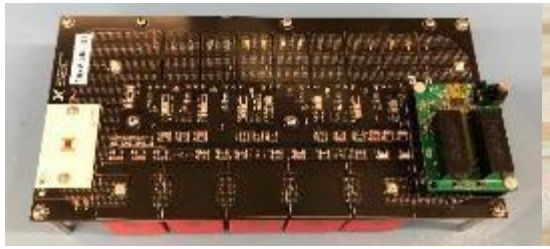
Backup Slides

Developing Power Electronics Capabilities



Application

SST

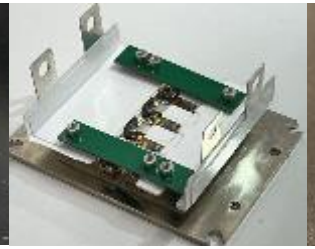
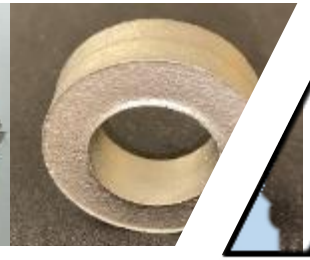



Subsystem

Topologies

Modularization

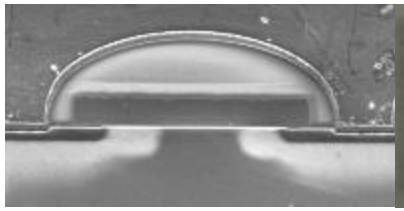
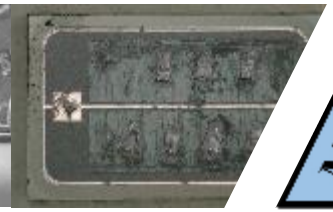
Thermal Management

Packaging Techniques

Semiconductor Devices
(IGBT, MOSFET, IGCT, etc.)

Capacitors, Inductors, Transformers

Material

Advanced Magnetics and Dielectrics

Advanced Conductors and Insulators

Wide Bandgap Semiconductor Materials

Power Electronics Lab Spaces Focused on Grid Modernization

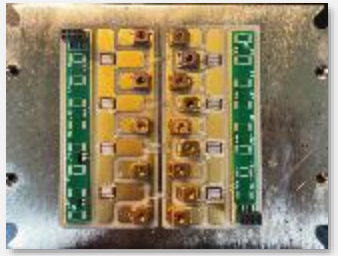
Medium Voltage Power Conversion Facility

DETL: Distributed Energy Technologies Laboratory

APEX: Advanced Power Electronic Conversion Systems Laboratory

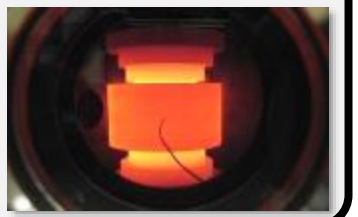
ESCAL: Energy Storage Control and Analytics Lab

PEAK: Power Electronics Advanced Packaging Lab



PERL: Power Electronics Reliability Laboratory

Various Device/Material Characterization Labs



SNL Task Structure

Task ID	Performer	Task Description
WBS T10 SNL Task 1	SNL	This task will define and apply reliability testing protocols to the highest-voltage, commercially available SiC devices (3.3 kV) from multiple vendors. Reliability and performance testing protocols for MV power electronics applications will be proposed.
WBS T11 SNL Task 2	SNL	This task will develop and demonstrate multiple DC/DC converter module types with common DC link voltage of 4kV. These designs include both isolated and non-isolated topologies for energy storage resources. The Year 1 sub-task will focus on detail electrical and thermal design, culminating in a complete design package.
WBS T12 SNL Task 3	SNL	This task will focus on assembly of hardware prototypes, validation of design objectives, and performance analysis with converters demonstrated in operation both individually and in a cohesive modular system with multi-chemistry storage assets.
WBS T13 SNL Task 4	SNL	A supervisory control algorithm for ensuring optimal utilization of heterogenous storage and power conversion resources (e.g. different battery chemistries, different DC/DC topologies) will be developed, demonstrated, and packaged as an API for integration with higher-level energy management platforms.
WBS T14 SNL Task 5	SNL	The storage resource control algorithm developed in T13 (SNL Task 4) will be demonstrated using the 4kV converter prototypes constructed in T11 (SNL Task 3).
WBS T15 SNL Task 6	SNL	Meetings and workshops with stakeholders
WBS T16 SNL Task 7	SNL	Identification of barriers for adoption of the MV sub-system

MV Semiconductor Reliability

MV Subsystem Design and Demonstration

Utility-Scale Storage Resource Integration

Stakeholder Engagement and Gap Analysis

Progress Summary

- **All SNL tasks**: Most significant project risk (inability to source sufficient number/diversity of 3.3kV devices) eliminated through early manufacturer engagement and proactive procurements
- **Task 1 – Semiconductor Reliability**
  - Finalized H3TRB test plan
  - H3TRB in progress, analysis of imaging data in progress
  - Task 1 Milestones (M.SNL.1.1 and M.SNL.1.2) are on schedule
- **Task 2 – MV Subsystem Design/Demonstration**
  - Circuit topologies selected and design timeline solidified
  - Simulation models of power stage circuits and closed loop control system developed
  - Initial hardware designs in progress, long-lead components ordered
  - Task 2 Milestone (M.SNL.2.1 Go/No-Go) is well ahead of schedule

Milestone	Description	Scheduled Completion
M.SNL.1.1	Finalize specification of test protocols for reliability characterization of semiconductor devices	BP1Q2
M.SNL.1.2	Completion of reliability data collection, characterization and analysis	BP1Q4
M.SNL.2.1 Go/No-Go	Completed 4kV converter design package	BP1Q4
M.SNL.2.2	Final demonstration of 4kV converter hardware prototypes	BP2Q4
M.SNL.3.1 Go/No-Go	Storage resource control/management algorithms developed	BP2Q4
M.SNL.3.2	Storage resource control/management algorithms demonstrated in hardware	BP3Q4