PACE
ACCELERATING ELECTRIFICATION

High dv/dt and high voltage insulation derisking technology for medium-voltage power electronics

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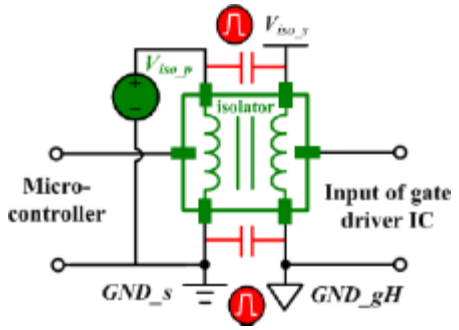
Team Member: Jianzhi Xu (PhD student)

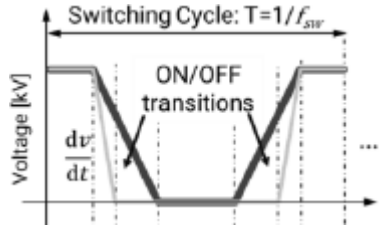
Project Background

1. EMI Challenge

high dv/dt cause false triggering and feedback



MV WBG Power Electronics



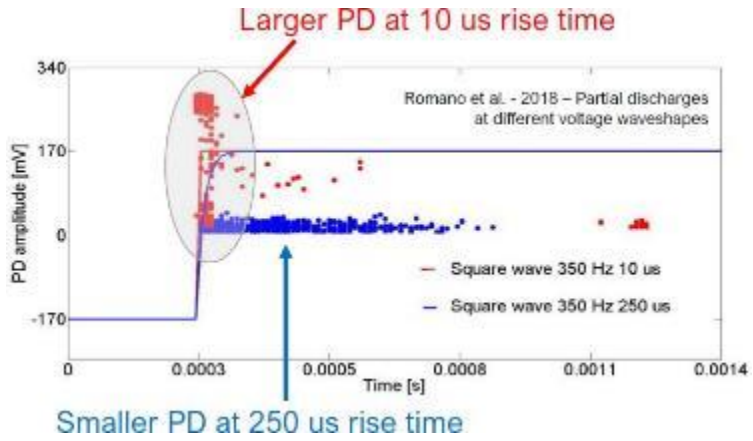
High dv/dt

Switching loss ↓ *fs* ↑ Power density ↑

Faster control

2. HV Insulation Challenge

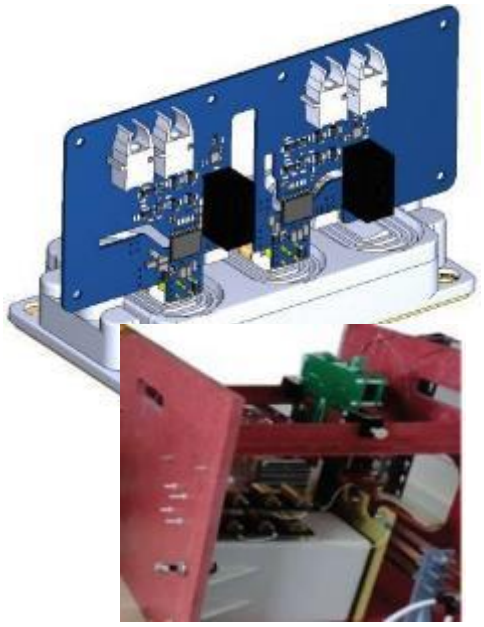
PWM (high dv/dt, high fs) increase PD magnitude and PD events



Objective: develop advanced technologies to address the above-mentioned challenges for MV power electronics.

Impact of Work

Noise-immune Power Cells



Fast and Robust MMC

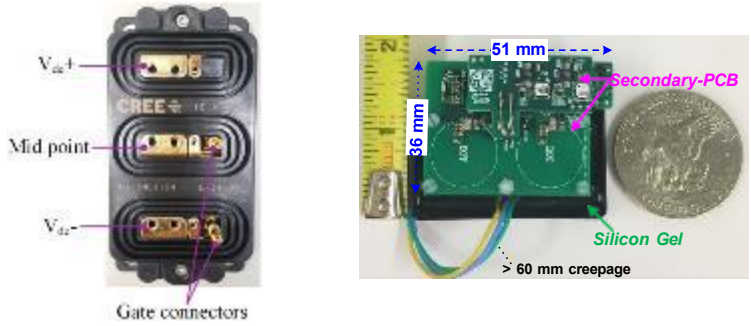
Unbreakable MV/HV Grid System

Source: SiC MMC developed by FSU team using 10 kV SiC device

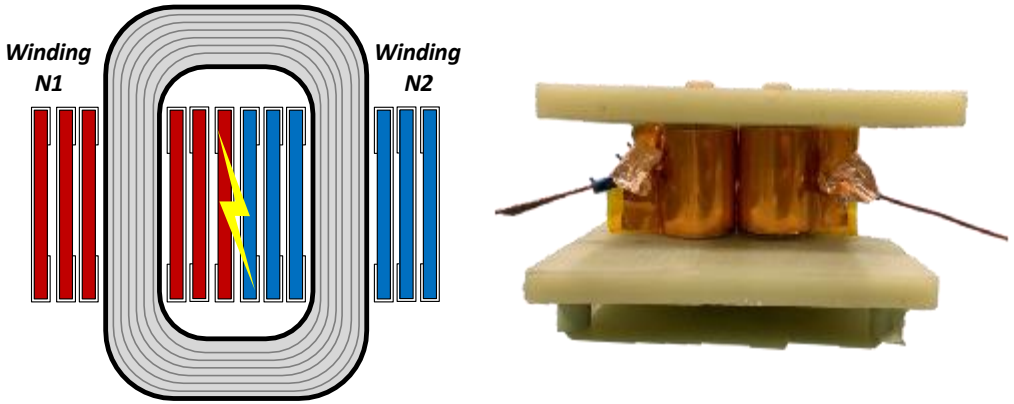
Source: Andrea Pereira “Transforming the Grid: Innovations in Next-Generation Hardware

Technical Approach

Gate driver for MV SiC Device



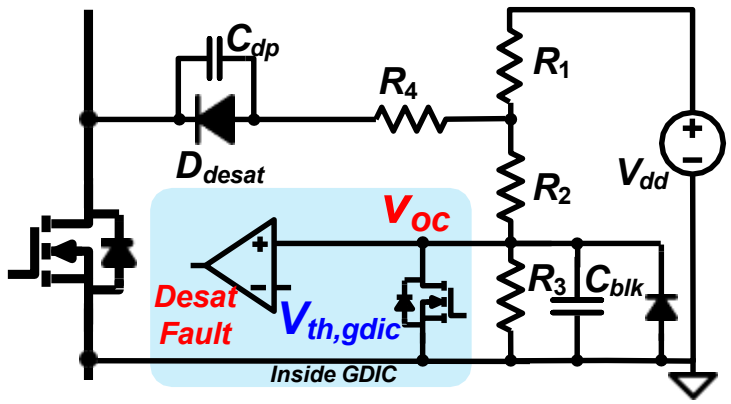
PD Characterization of Magnetics



Enhanced Noise-immune Fault Protection

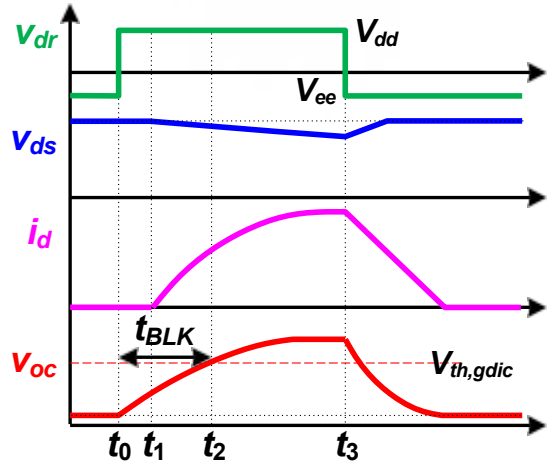
- Develop enhanced noise-immune fault protection for MV SiC GD;
- Characterize MV gate driver under high frequency and high dv/dt PWM voltage;
- Partial discharge (PD) characterization of magnetics.

Task 1: GD Enhanced Noise-immune Fault Protection

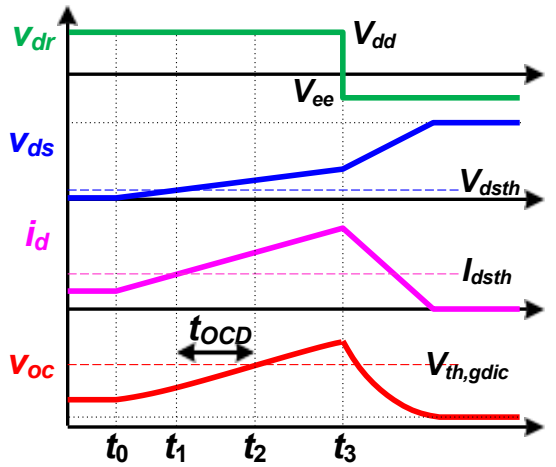


Conventional DESAT Circuit

- Simple, low cost.
- DESAT integrated into commercial GDICs.
- Prone to high dv/dt induced noise.



SC fault waveform
(t_{BLK}: Blanking time for SC fault)

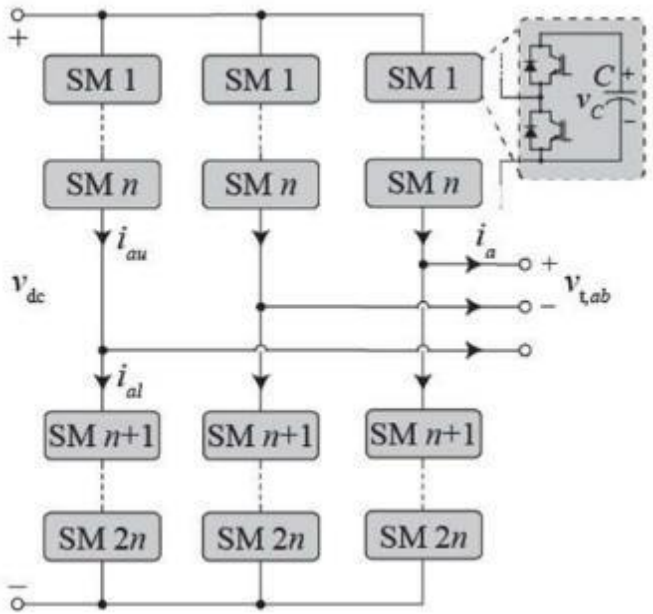


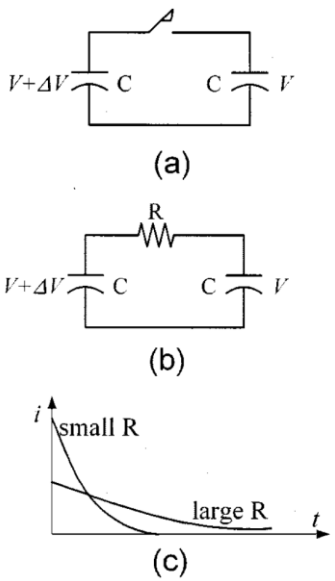
OC fault waveform
(t_{OCD}: OC fault detection time,
V_{dsth}: OC fault threshold of v_{ds})

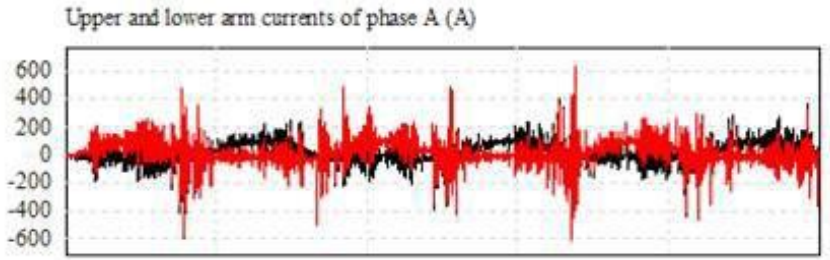
Z. Guo, H. Li and X. Dong, "A Self-Voltage Balanced Hybrid Three-Level MV Inverter Using 3.3-kV SiC MOSFET Module With **False-Trigger-Proof Design**," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Dec. 2022.

❑ Optimized DESAT Circuit Design can achieve: a) high dv/dt induced false-trigger-free SC protection;
b) fast OC fault response time.

Inrush Current Noise Induced False-triggering Issue



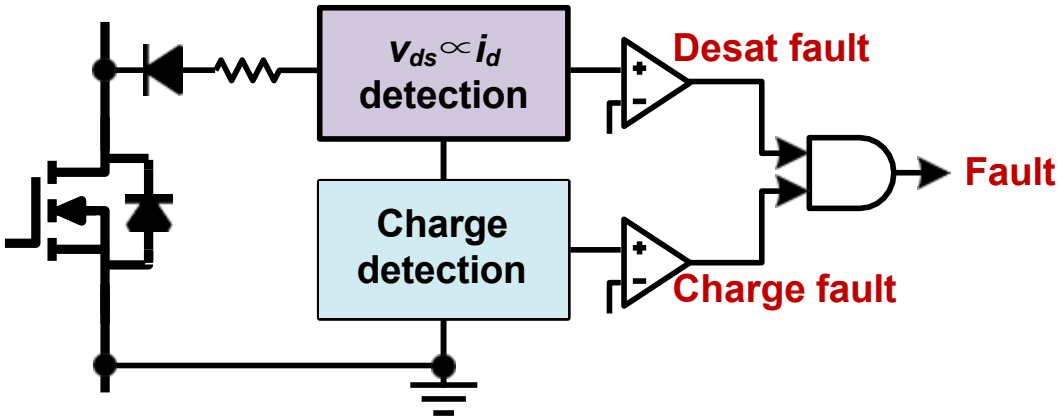




Simulated arm current waveform
@ 1 MVA, 13.8 kVac, 40 Arms output
Carrier frequency: 5 kHz, switching frequency: ~3 kHz

- ❑ Inrush current occurs during the capacitor voltage equalization.
- ❑ Inrush current has a high magnitude but lasts for a short time.
- ❑ The blanking time of conventional DESAT protection cannot screen the inrush current noise.

Proposed Charge-based DESAT Protection

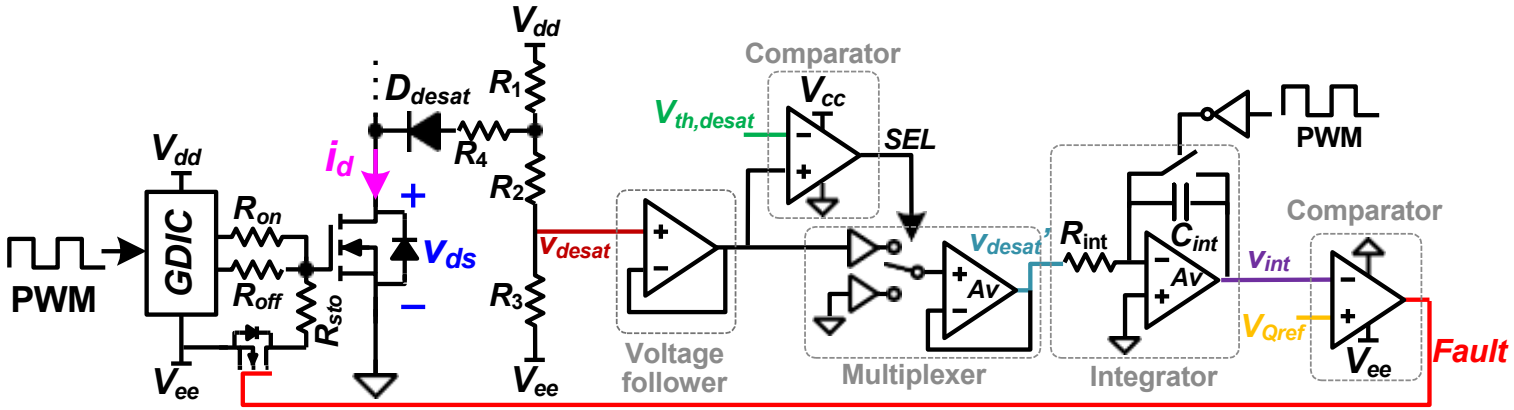


Proposed Charge-based DESAT Protection

$$\begin{cases} v_{desat} = \min\left(\lambda V_{dd} + \alpha\left(v_{ds} + V_f\right) + \frac{R_2+\alpha R_4}{R_2+R_3} V_{ee} \quad , V_{\text{sat}}\right) \\ V_{sat} = \delta V_{dd} + (1-\delta) V_{ee} \\ \delta = \frac{R_3}{R_1+R_2+R_3} \\ \lambda = \frac{R_3 R_4}{R_1R_2+R_1R_3+R_1R_4+R_2R_4+R_3R_4} \\ \alpha = \frac{R_1 R_3}{R_1R_2+R_1R_3+R_1R_4+R_2R_4+R_3R_4} \end{cases}$$

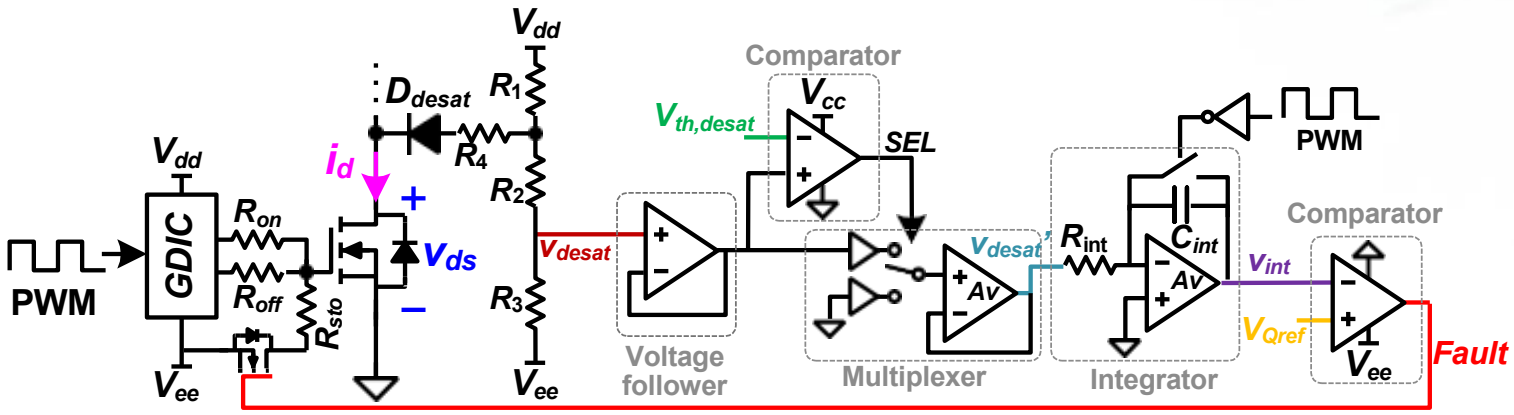
- "fault charge" (**the integral of fault current**) rather than the "fault current" is detected to enhance the noise immunity to inrush current noise.

PATENT PENDING



Circuit schematic

Key Waveforms

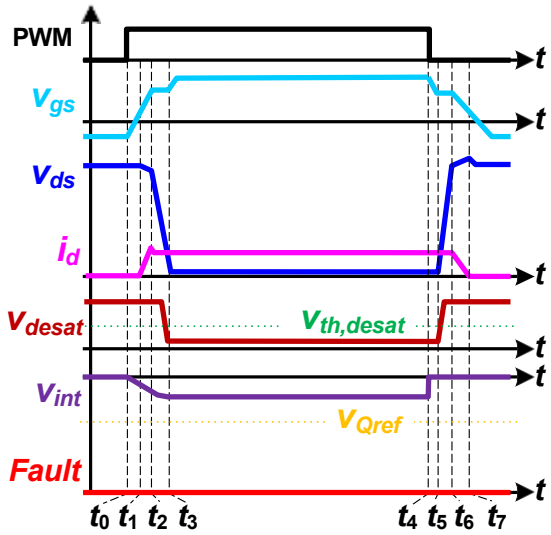


$$v_{desat}' = \begin{cases} 0, & v_{desat} < V_{th,desat} \\ A_v \times v_{desat}, & v_{desat} \geq V_{th,desat} \end{cases}$$

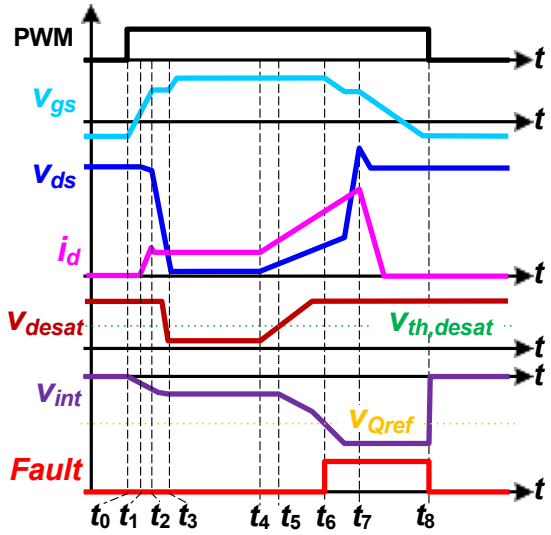
$$v_{int} = -\frac{1}{R_{int}C_{int}} \int (v_{desat}')\, dt$$

$$t_{sc} = \frac{|V_{Qref}|\, R_{int}C_{int}}{A_v V_{sat}}$$

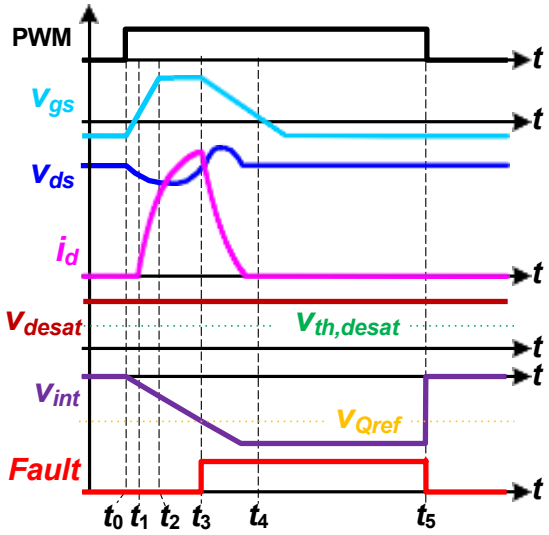
t_{oc} is determined by the di/dt of fault current.



Waveforms @ normal switching condition

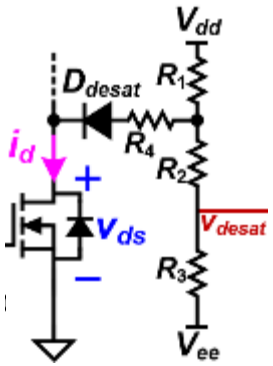


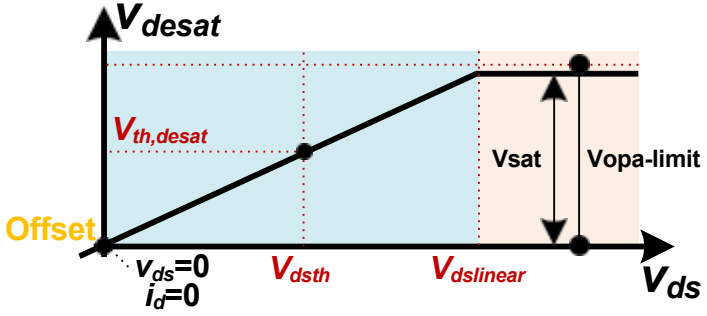
Waveforms @ OC fault



Waveforms @ SC fault

Circuit Design





$$\begin{cases} v_{desat} = \min\left(\lambda V_{dd} + \alpha\left(v_{ds} + V_f\right) + \frac{R_2+\alpha R_4}{R_2+R_3} V_{ee} \quad , V_{\text{sat}}\right) \\ V_{sat} = \delta V_{dd} + (1-\delta) V_{ee} \\ \delta = \frac{R_3}{R_1+R_2+R_3} \\ \lambda = \frac{R_3 R_1}{R_1R_2+R_1R_3-R_1R_4+R_2R_4-R_3R_4} \\ \alpha = \frac{R_1 R_3}{R_1R_2+R_1R_3+R_1R_4+R_2R_4+R_3R_4} \end{cases}$$

- Design constraint (1): $V_{offset} = v_{desat}(v_{ds}=0) = 0$.

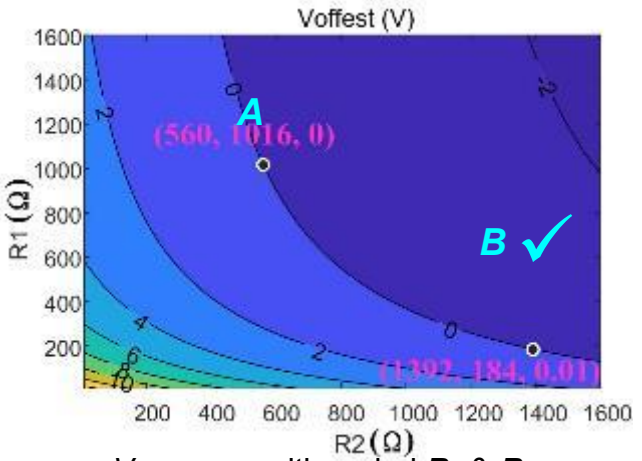
$$V_{offset} = \lambda V_{dd} + \alpha V_f + \frac{R_2 + \alpha R_4}{R_2 + R_3} V_{ee} = 0$$

- Design constraint (2): Multiplexer/OPA non-saturated.

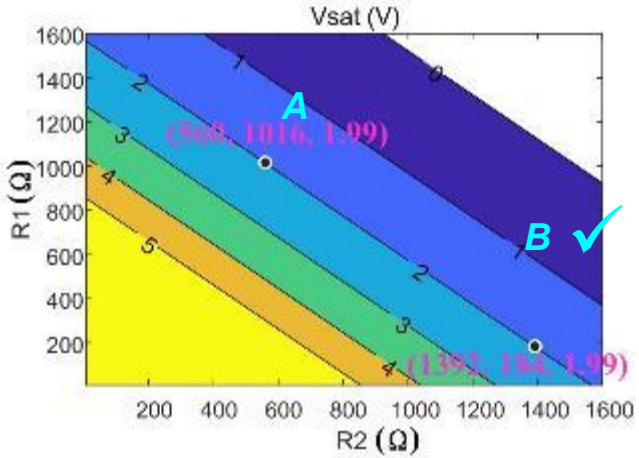
$$V_{sat} = \delta V_{dd} + (1-\delta) V_{ee} < V_{opa-limit}$$

- Design constraint (3): large $V_{dslinear}$ is preferred.

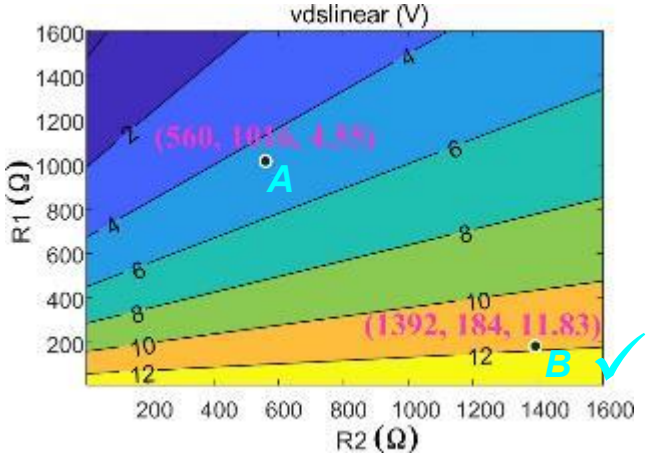
$\{R_1, R_2, R_3, R_4\}$ selection



V_{offset} map with varied R_1 & R_2



V_{sat} map with varied R_1 & R_2

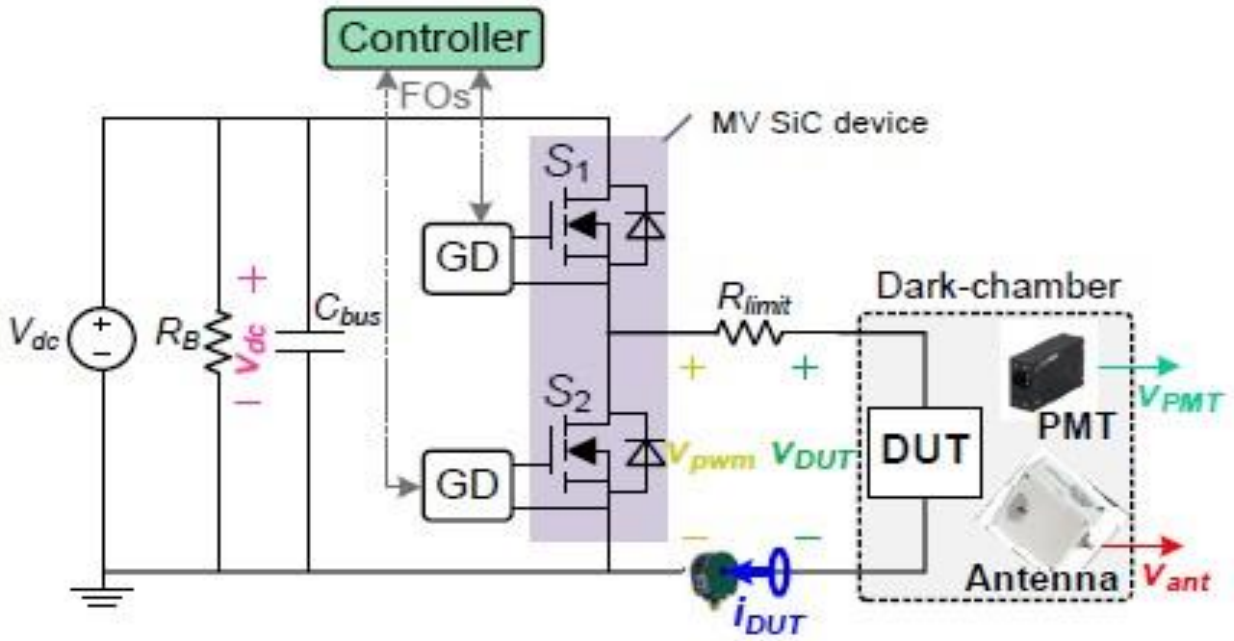


$V_{dslinear}$ map with varied R_1 & R_2

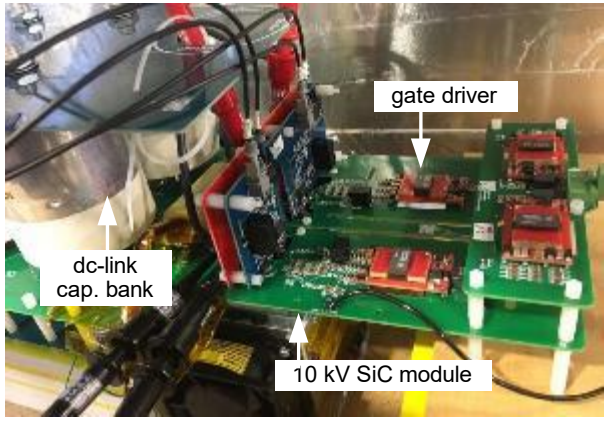
Given V_{offset} = 0 V, V_{sat} = 2 V,
$V_{th,desat}$ = 1.25 V, R_3 = 800 Ω, R_4 =200 Ω

Slect R_1 = 184 Ω, R_2 = 1392 Ω
V_{dsth} = 7.4 V, $V_{dslinear}$ = 11.83 V
R_{int} = 301 Ω, C_{int} = 122 *nF*, t_{sc} = 344 *ns*

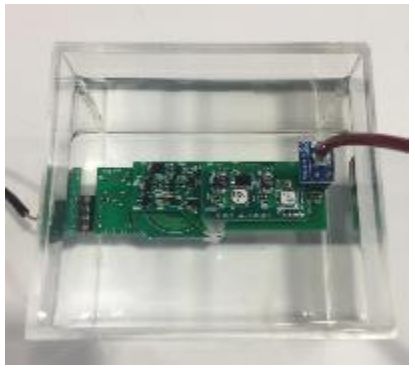
Task 2: PD Characterization @ high *dv/dt* PWM Voltage



PD test setup @ high dv/dt PWM



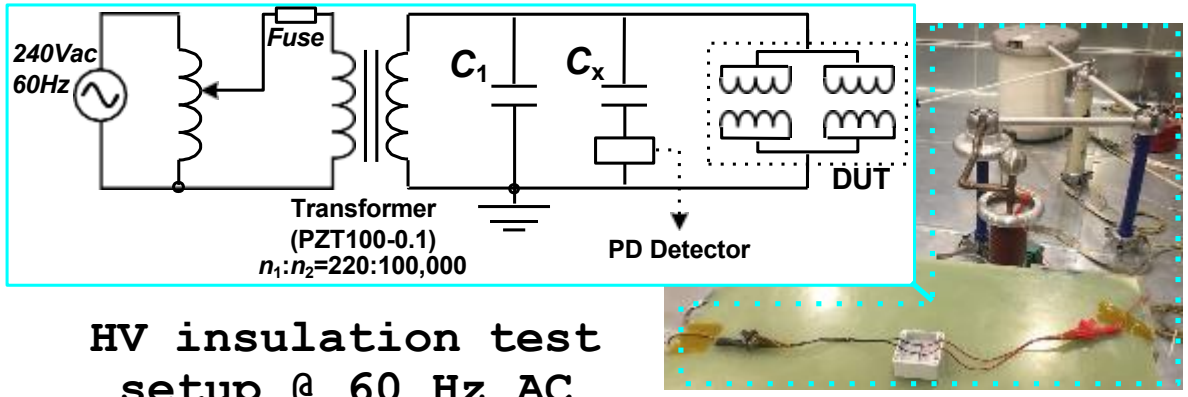
PWM voltage generator



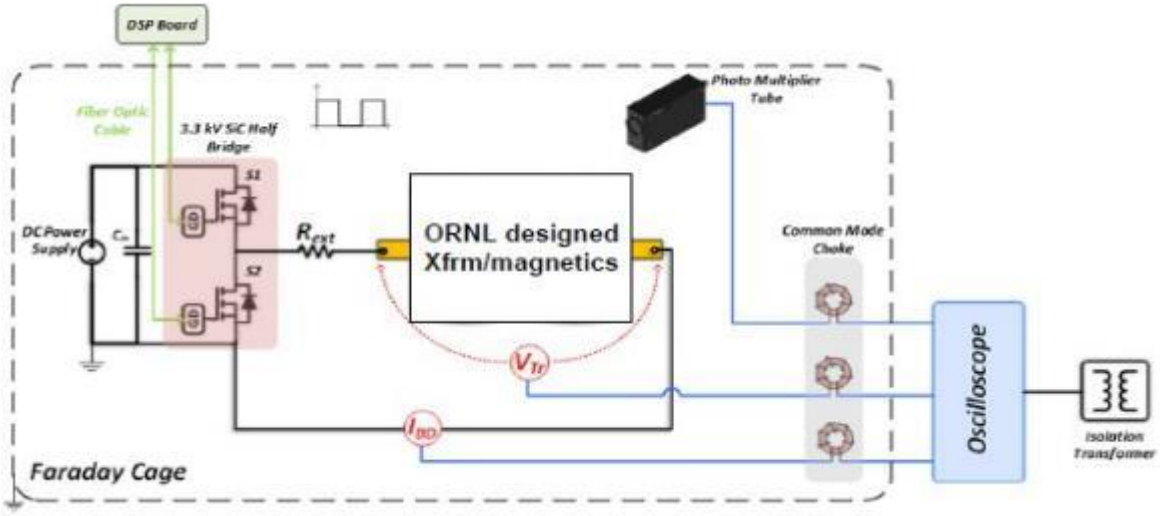
Device under test

✓ Coordinated PD detection is implemented by: Photomultiplier tube (PMT) + UHF antenna + HFCT

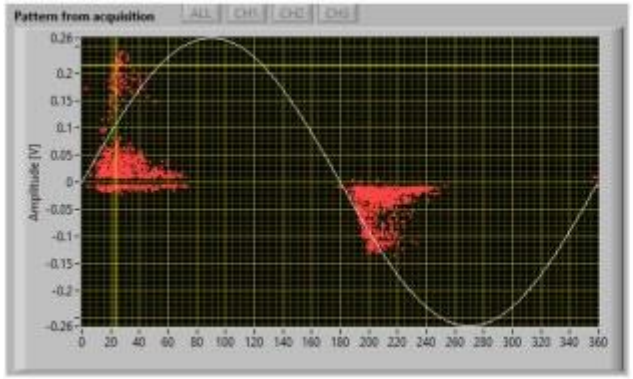
Task 3: PD Characterization of Magnetics

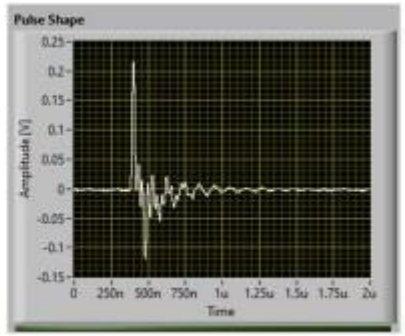


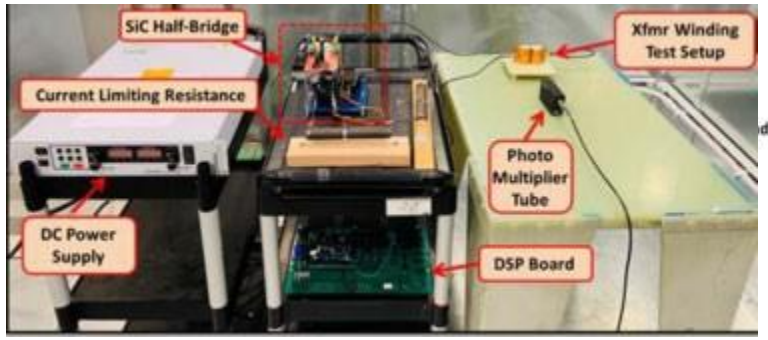
HV insulation test setup @ 60 Hz AC

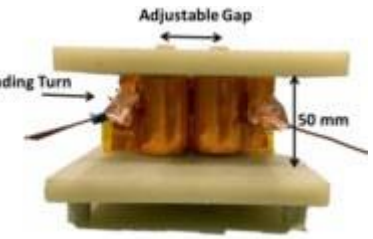


PD test setup @ PWM Voltage

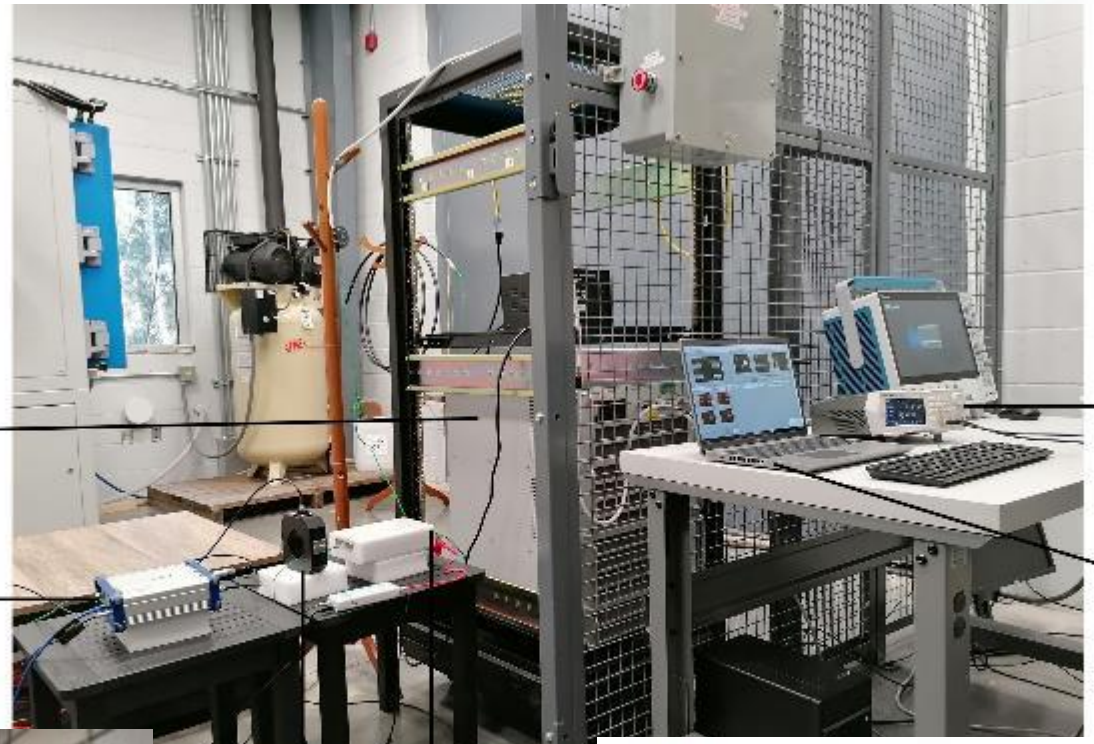


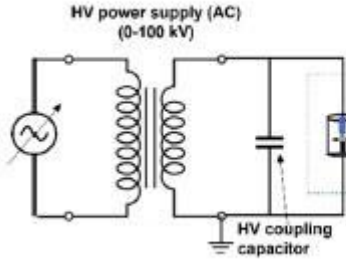


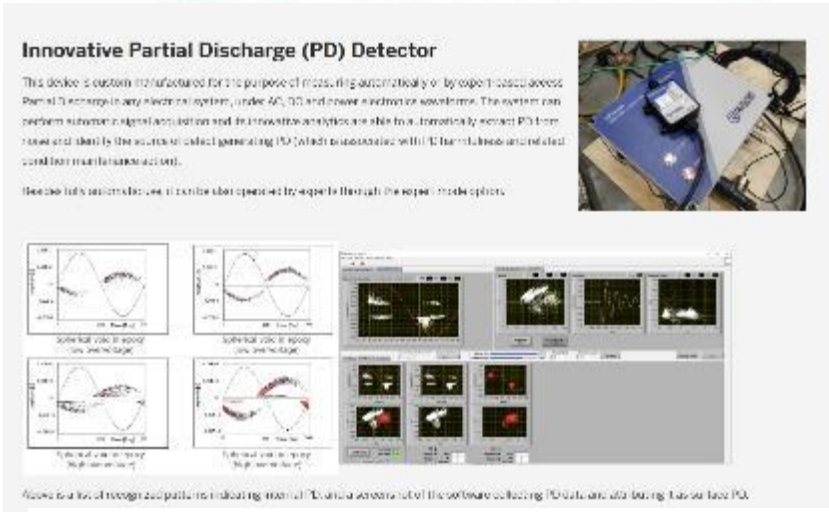


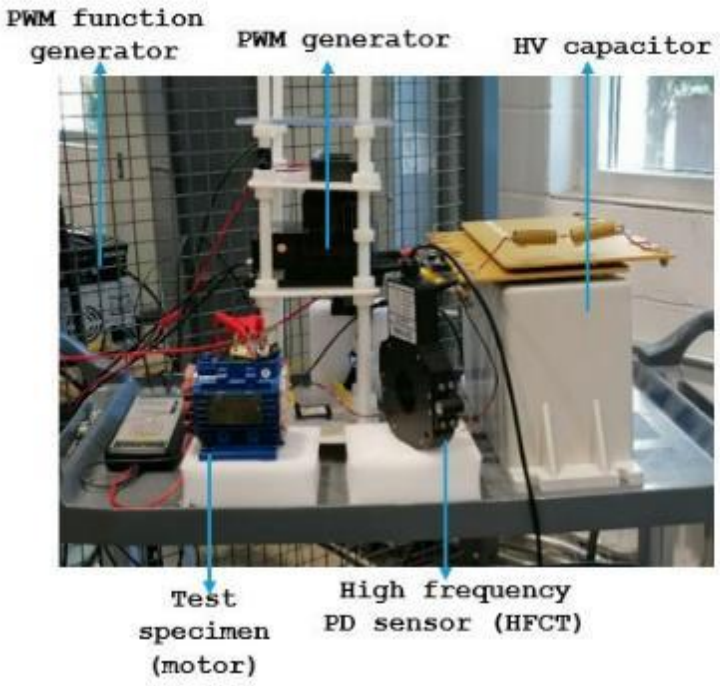


CAPS HEFL Lab PD Test Facility









Accomplishments

- Developed the charge-based fault protection method to solve the false-triggering induced by the inrush current noise;
- A testbed is under construction that can characterize the PD performance under high switching frequency and high dv/dt;
- Leverage CAPS existing PD facilities to perform PD characteristics of magnetics.

Future Work

- To design charge-based fault protection circuit;
- To build hardware of charge-based fault protection and conduct experiments on MV SiC device;
- To modify the existing testbed to test PD of MV inductors and transformers developed by ORNL team under 60Hz AC and PWM voltage;

THANK YOU

This project was supported by the Department of Energy (DOE) - Office of Electricity's (OE), Transformer Resilience and Advanced Components (TRAC) program led by the program manager Andre Pereira (OE), Eric Miller (Office of Energy Efficiency & Renewable Energy), and the Grid Modernization Initiative.

Backup Slides

Acronyms

WBG:	Wide bandgap
PD:	Partial discharge
MMC:	Modular Multilevel Converter
GD:	Gate driver
DESAT:	Desaturation protection
OC:	Over current
SC:	Short circuit
PMT:	Photomultiplier tube
HFCT:	High frequency current transformer
DUT:	Device under test