SSPS 1.0 Hardware Prototype Development

Smart Universal Power Electronics Regulators (SUPERs) & Intelligent Power Stages (IPSs) for SSPS 1.0

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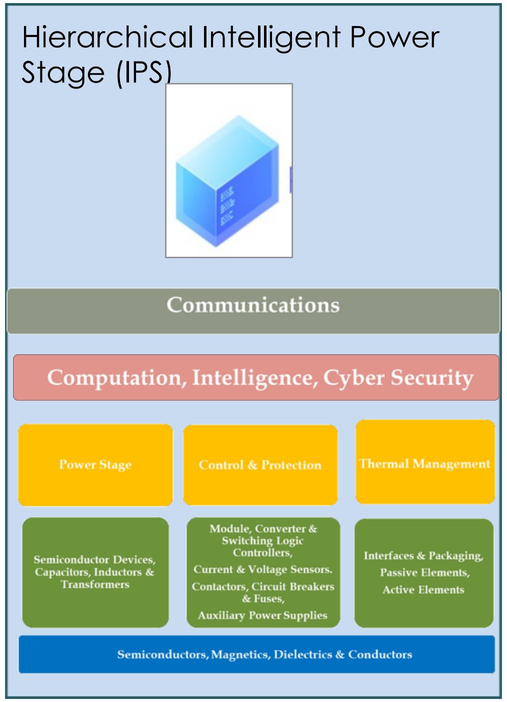
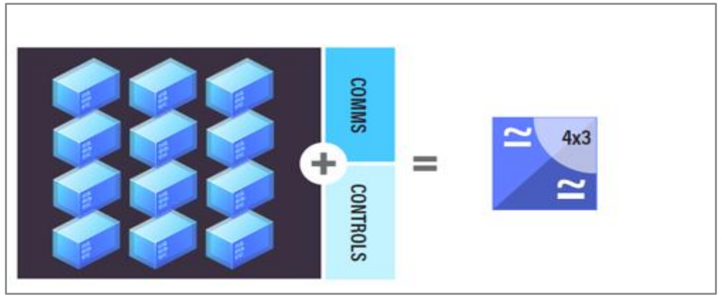
Solid State Power Substation

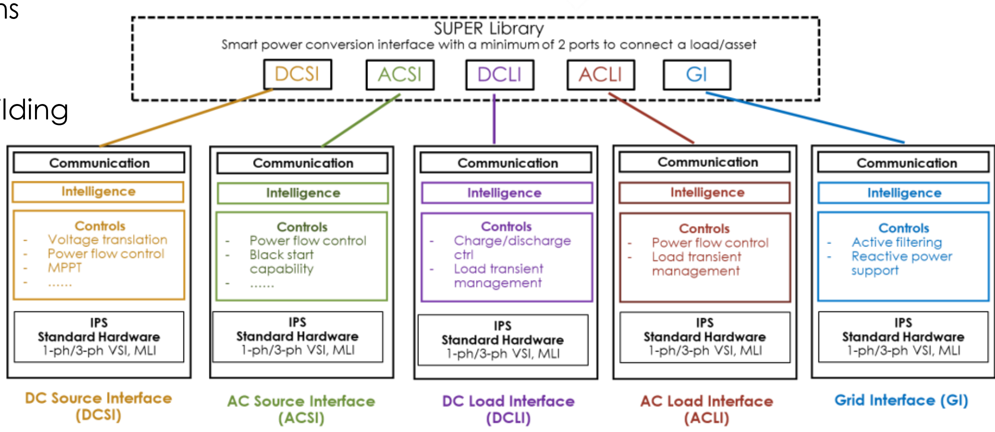


Strategic integration of modular, scalable, flexible, intelligent and adaptable power blocks and their auxiliary systems

Smart Universal Power Electronics Regulator (SUPER)

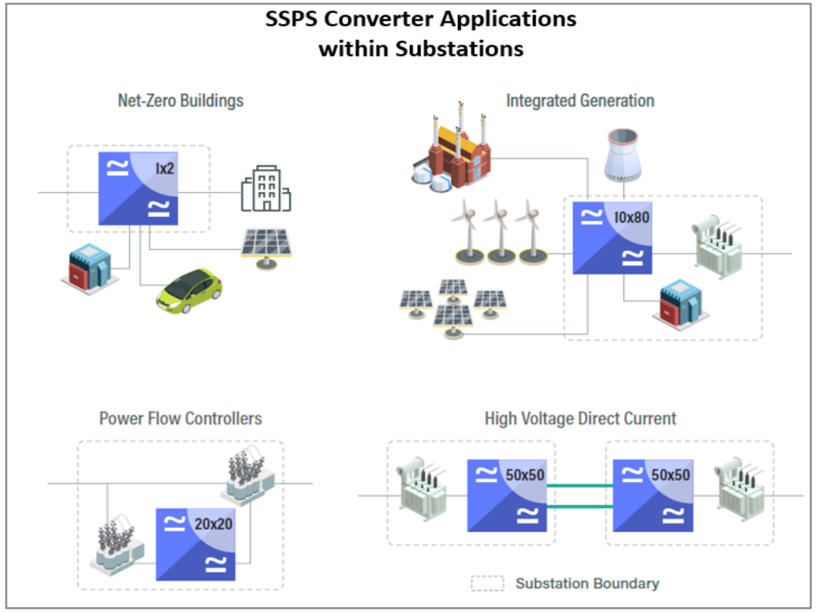


Library of SUPERs for DC or AC systems



Multiple Applications with Power Electronics Systems Building Blocks

Hubs/Nodes



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https://www.energy.gov/sites/prod/files/2020/06/f75/2020%20Solid%20State%20Power%20Substation%20Technology%20Roadmap.pdf

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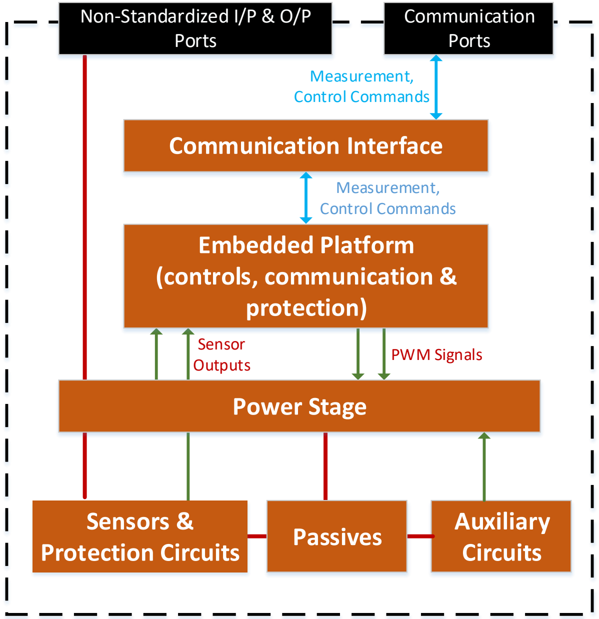
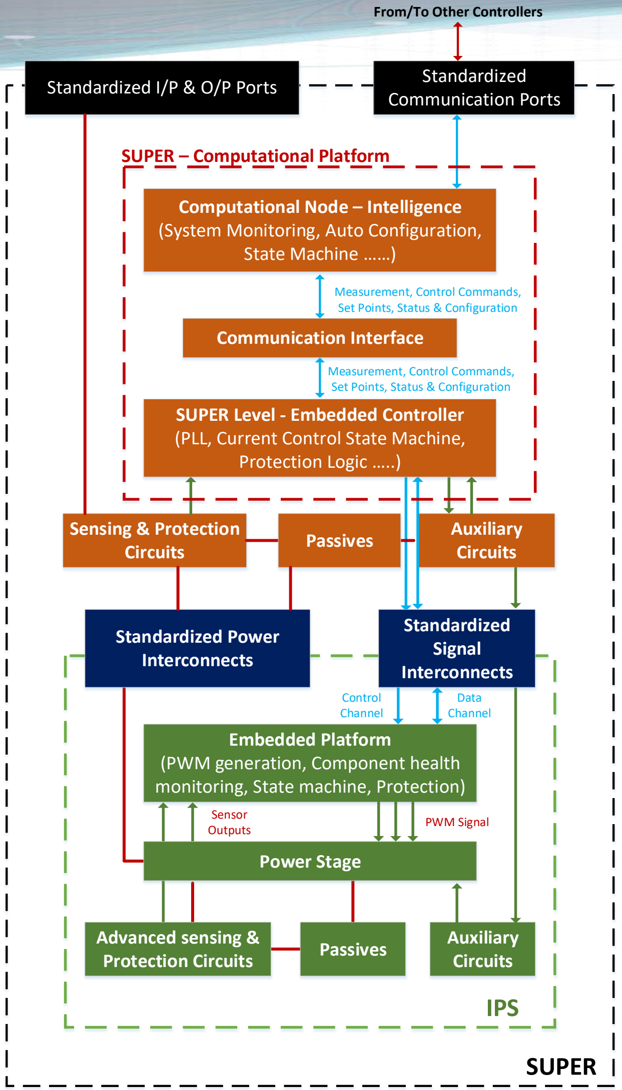
SUPER & IPS



State of the Art



SUPER

SUPER Features	Metrics/Requirements
1. Interoperability ☑	• Coordination between the building blocks under normal and transient conditions • Synchronized operation • Minimum latencies • Standardization of hardware and software
2. Embedded intelligence & decision-making capability with a flexible scalable platform ☑	• Provisions for advanced controls • Plug and play capability • Should enable system automation
3. Embedded online health monitoring system – Diagnostics/Prognostics ☑	• Sensors for more data procurement from the system • Crucial for reliability enhancement
4. Cyber-physical security	• Technology to prevent attacks at all levels of the system
5. Modularity / Scalability ☑	• Self contained systems with auxiliary power gate drivers etc. • Design to parallel or intertie multiple systems

Objectives

Partners

Overall Objective:

- Demonstrate the fundamental building blocks for solid state power substation (SSPS) with advanced features & standardized interconnects
- Building block specification: 480 V, 500 ~ 1 kV, 75 kVA power conversion units

Objectives - ORNL:

- Demonstrate the architecture of the fundamental building blocks i.e., Smart Universal Power Electronics Regulators (SUPERs) & Intelligent Power Stages (IPSs) with controls, communication, protection and synchronization.

Objectives – Partners:

- IPSs with advanced sensing techniques, algorithms capable of estimating the health of at least 2 components

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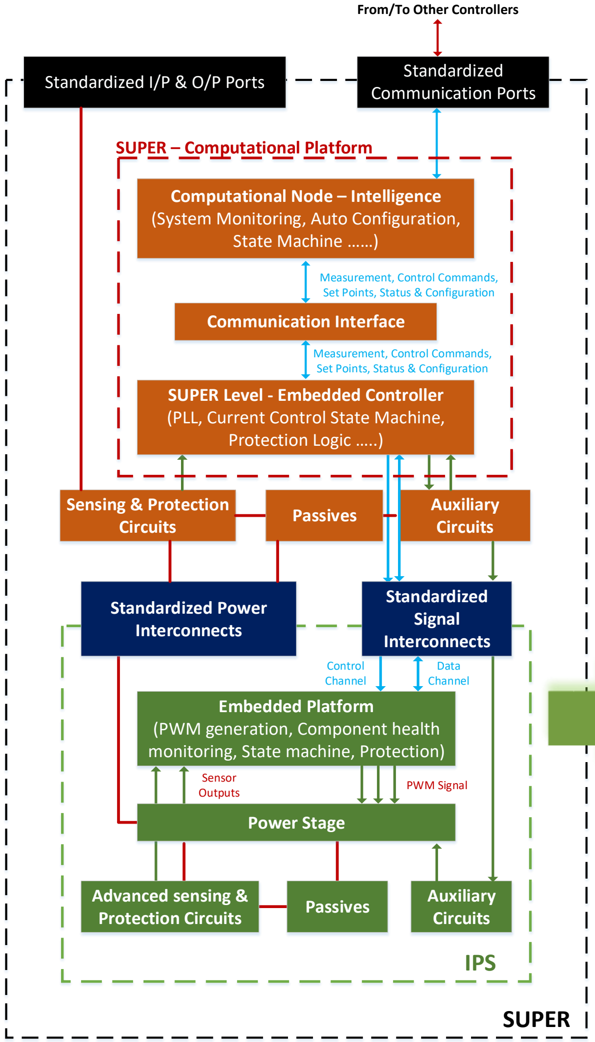
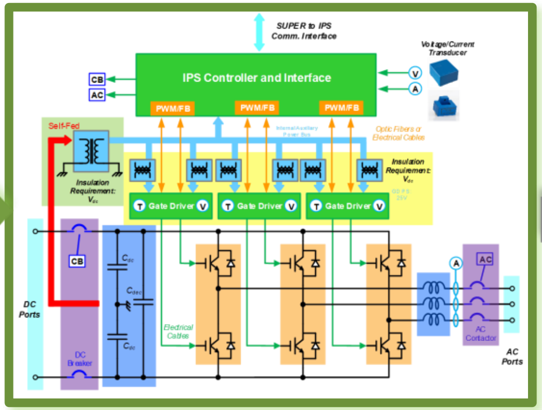
The Numbers

- DOE PROGRAM OFFICE:
  OE – Transformer Resilience and Advanced Components (TRAC)
- FUNDING OPPORTUNITY:
  Annual Operating Plan (AOP)
- LOCATION:
  Knoxville, TN
- PROJECT TERM:
  07/01/2020 to 12/30/2022
- PROJECT STATUS:
  Completed
- AWARD AMOUNT (DOE CONTRIBUTION):
  $9,000,000
- AWARDEE CONTRIBUTION (COST SHARE):
  $0
- PARTNERS:
  Consortium of University Partners

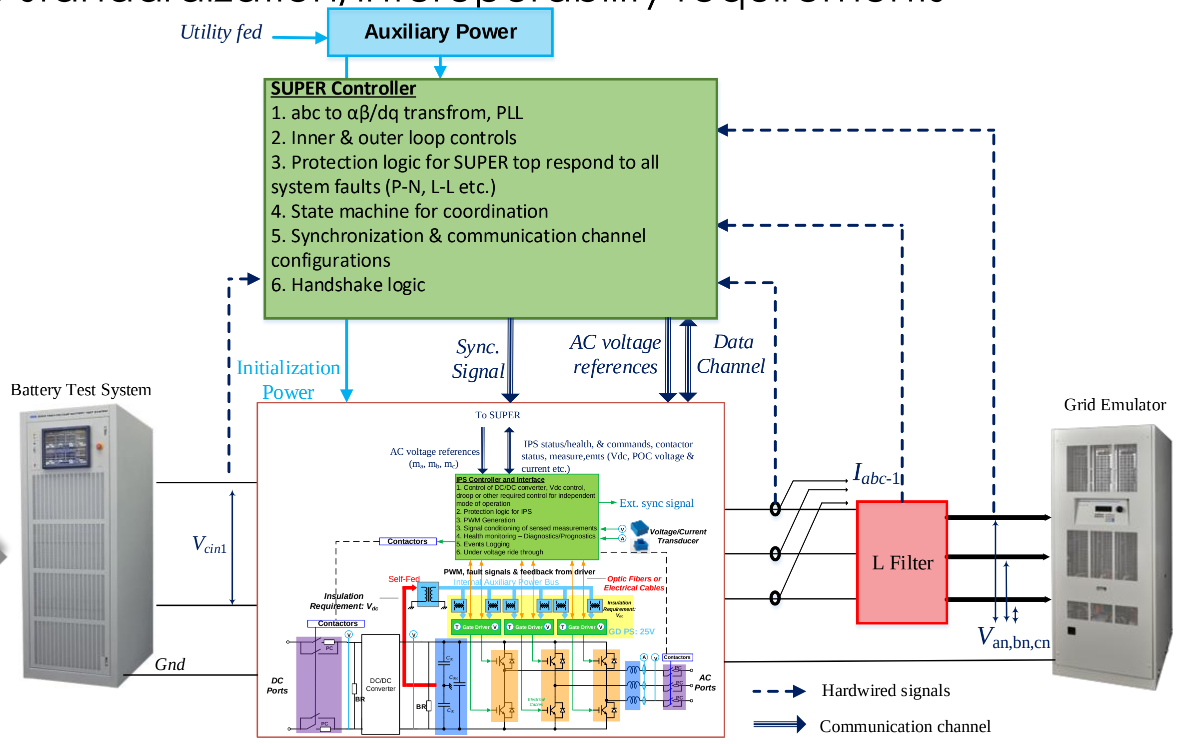
Technical Approach



- **ORNL** formulated the framework for building blocks i.e., SUPER & IPS framework & validates in hardware it using a baseline.
- Communicated the standardization/interoperability requirements to partners



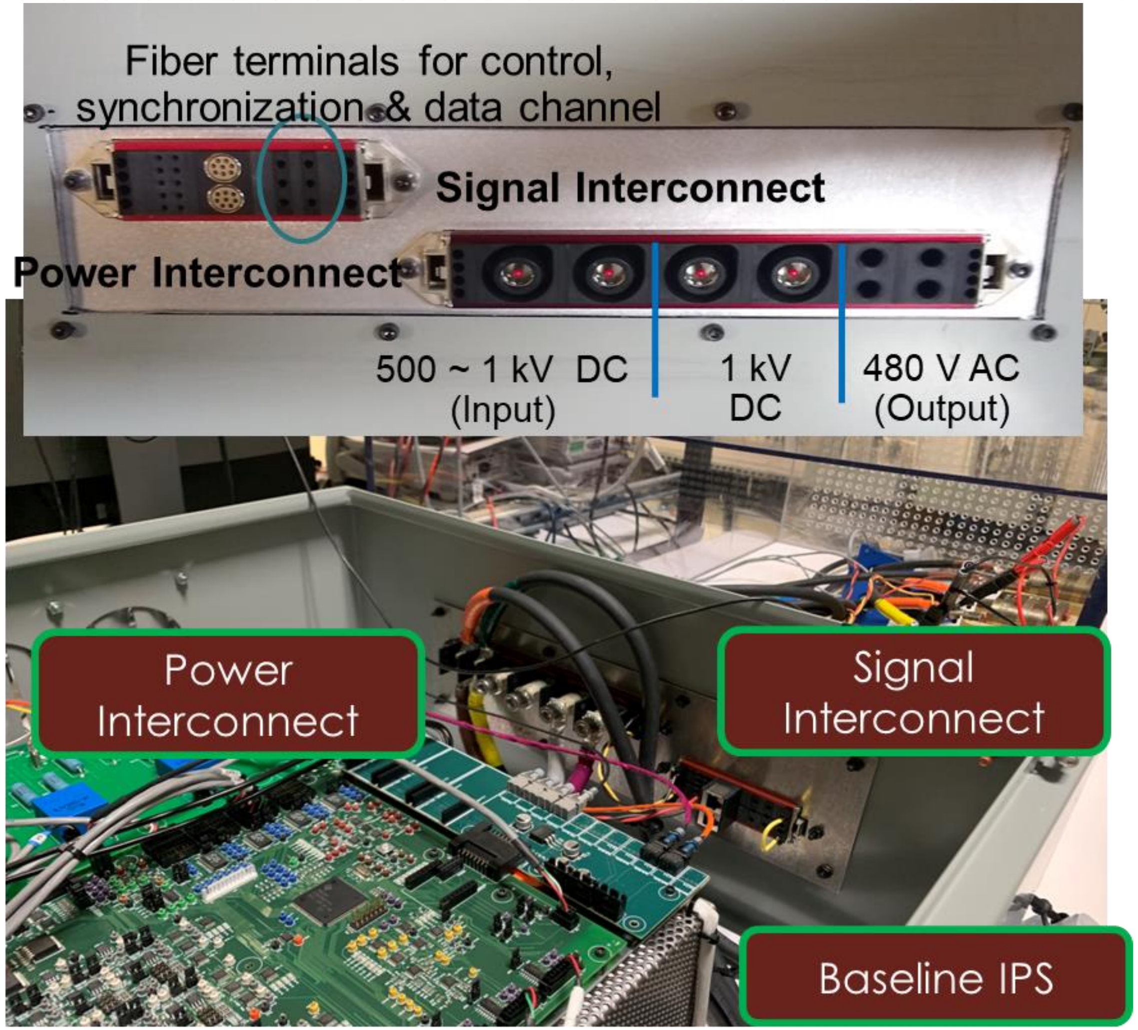
Partners developed standardized/vendor agnostic IPSs with advanced sensing components

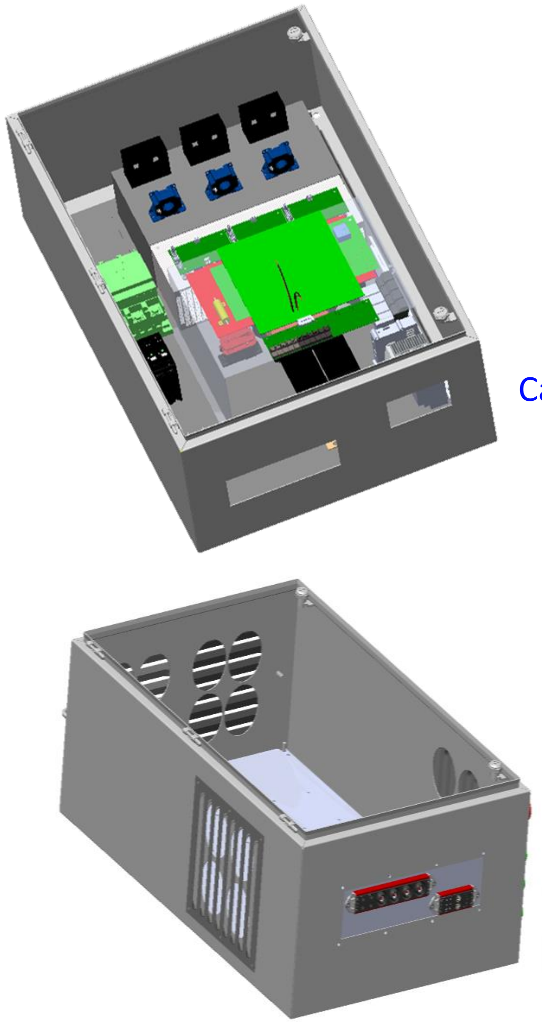


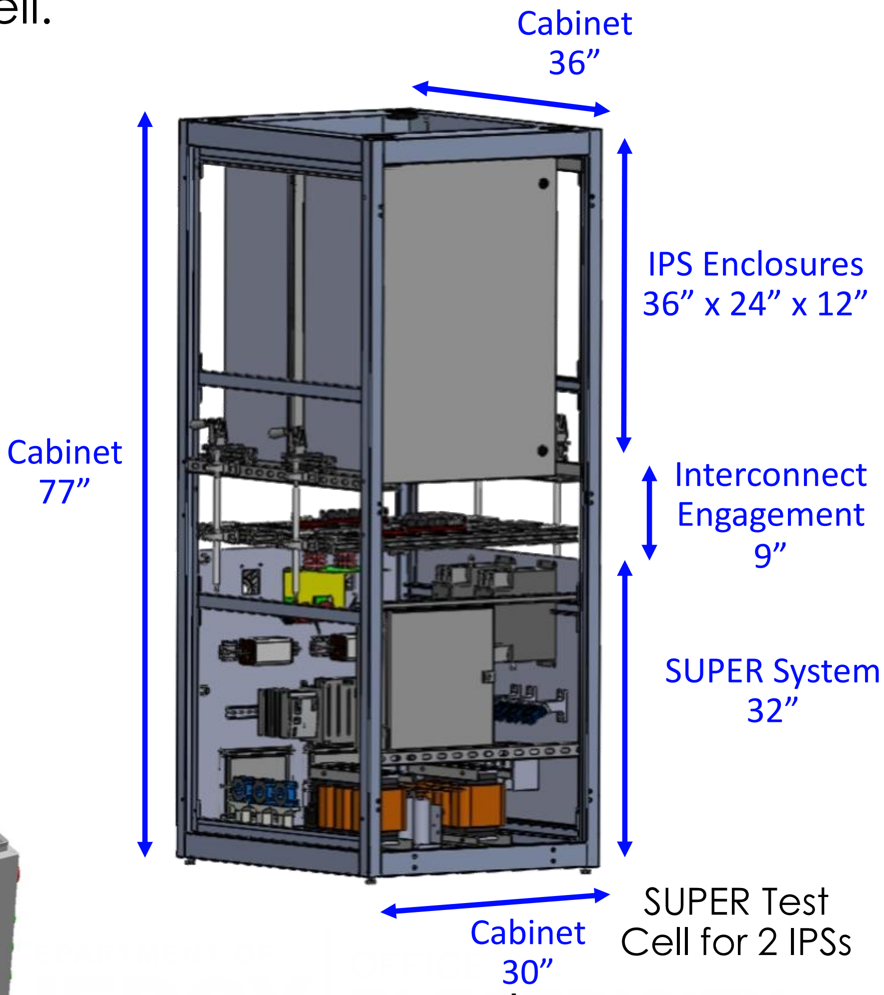
IPS from partners were tested at ORNL in the SUPER test platform

#1- Hardware Standardization for Interoperability of Blocks

Accomplishment: IPS enclosure, power & signal connections were standardized to interoperate the blocks in SUPER test cell.



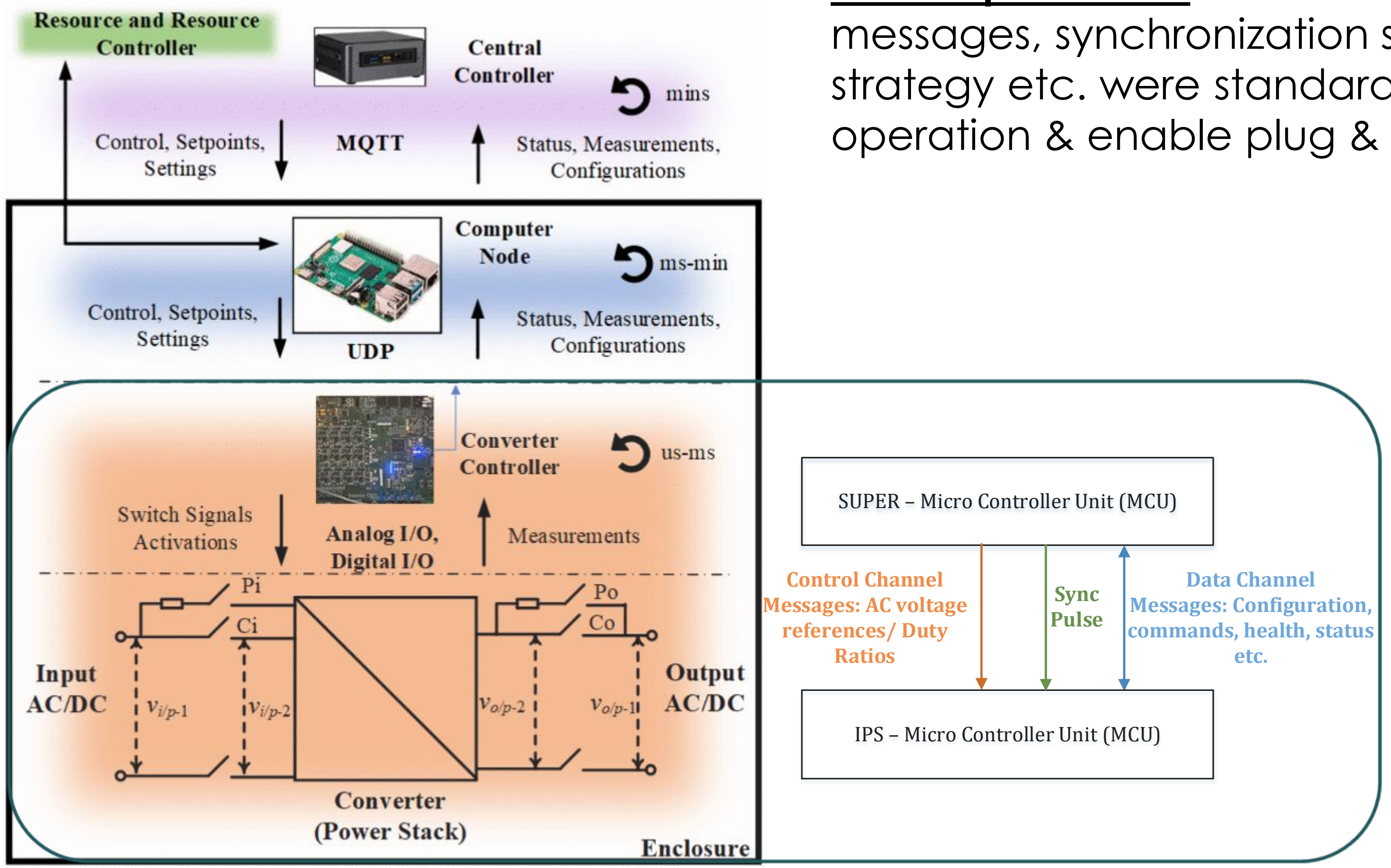




SUPER Test Cell for 2 IPSs

#2 – Software & Communication Standardization

Accomplishment: The communication protocol, messages, synchronization strategy, coordination strategy etc. were standardized for vendor agnostic operation & enable plug & plug.



Data Flow between SUPER & Hierarchical Controller

Channel /Link	Information Flow Direction	Messages
Data (100 kbps)	IPS to SUPER	Configuration, Status, General Faults, Gate Driver Faults, **Health**, Warnings
	SUPER to IPS	Commands, Setpoints
Control (6.25 Mbps)	SUPER to IPS	Control values at every sampling instance
Sync (30 kHz)	SUPER to IPS	Short pulse at switching instances to synchronize systems

Data Flow between SUPER & IPS

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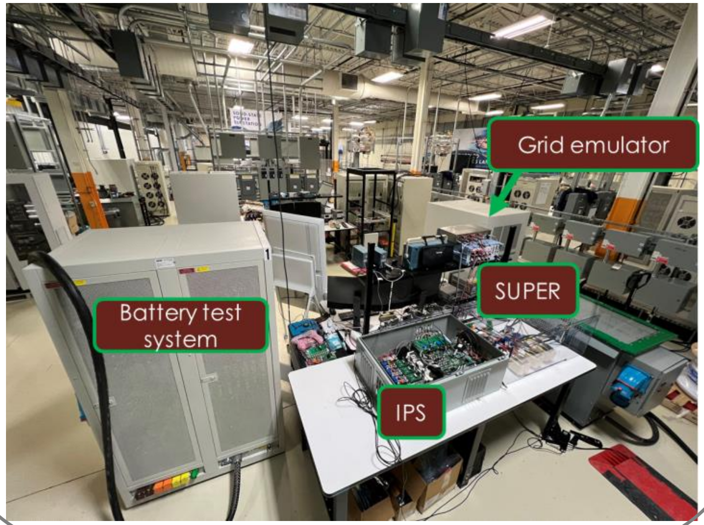
#3 – SUPER Architecture Validation

Testbed

The testbed was used to validate the power stage & the standardized interconnects at 1kV, 480 V, 30 kW.

Using the testbed SUPER architecture was validated for controls, communication, protection & coordination.

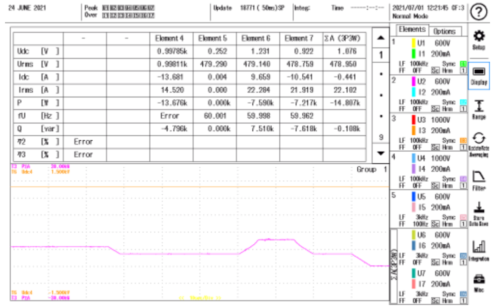


Control Modes

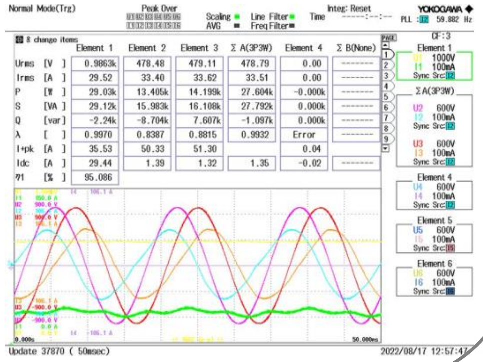
The control loops for various grid following modes the control channel was verified

The data channel used for coordinating the SUPER & IPS for operation was also verified.

Mode -1: Vdc regulation

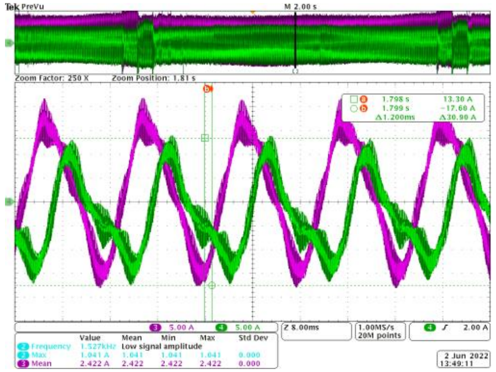


Mode -2: P/Q compensation

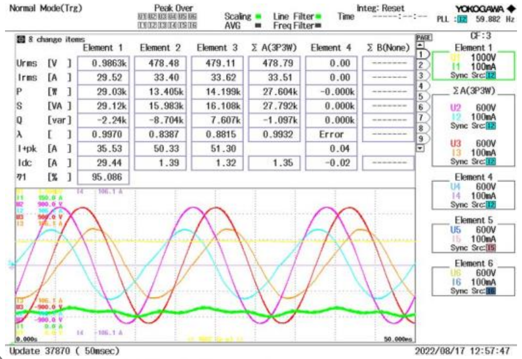


Issues Resolved

Synchronization was crucial even with 1 IPS to structure the communication packages received and enable them accurately.



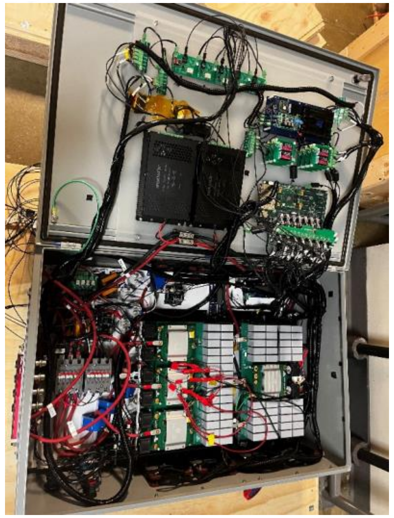
Current distortions w/o synchronization

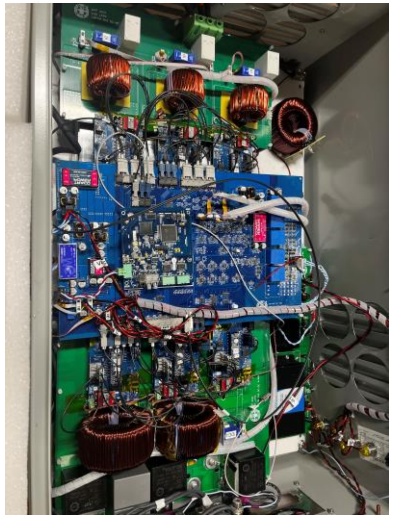


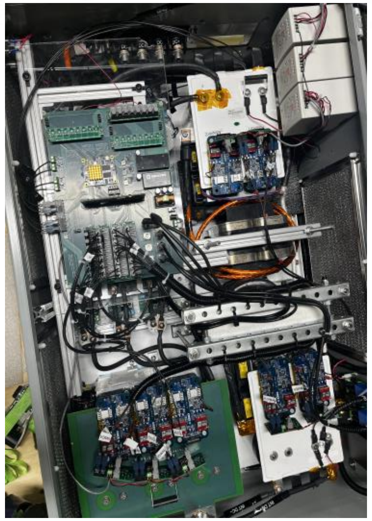
Cleaner currents with synchronization

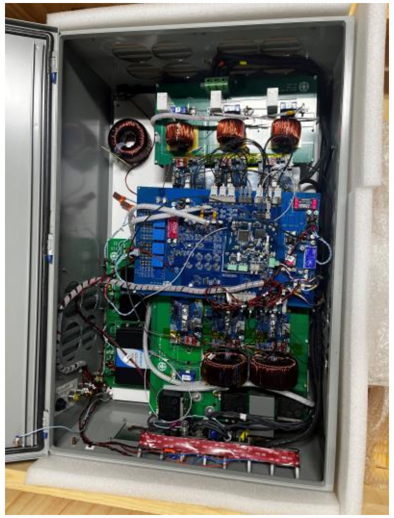
#4 – Library of IPSs from Partners with In-situ Estimates


UNCC


VTECH


FSU


UARK


NY-SB


UT-Austin


OSU

In-situ parameters

V_{dson}, $V_{ds,off}$, I_{ds}, R_{dson}, T_b, C_{dc}

#4 – Library of IPSs from Partners with In-situ Estimates

IPS from University Partners	Topologies		Features	In-situ Parameters
	DC/DC	DC/AC		
Florida state university (FSU)	Interleaved buck boost converter with coupled inductor	3-ph 2-level voltage source inverter (VSI)	Interleaved configuration reduces the Input current ripple. Ideal for BES applications	Gate leakage current
Ohio State University (OSU)	Traditional boost converter	3-ph 2-level VSI with carrier frequency modulation	Capability to integrate the inductor with the liquid metal cooling	Health & stress index based on on-state resistance
University of Arkansas (UARK)	Soft-switching CLLC Bidirectional dc/dc converter	3-ph 2-level VSI	Resonant configurations for power transfer at higher frequencies and with soft switching	Junction temperature & passives estimation
University of New York, Stony Brook (NY-SB)	Interleaved boost converter	3-ph 2-level VSI with redundant half bridge legs & coupled ac inductors	Capitalizes on P & N cell layout to optimize switching speeds	Digital twin for passives estimation
University of North Carolina, Charlotte (UNCC)		4-leg 3-ph 2-level VSI	4-leg configuration is suitable for harmonic filtering applications	DC-link capacitance, on-state resistance & base plate temperature
University of Texas, Austin (UT-Austin)	DC/DC stage with parallel devices	3-ph 2-level VSI with parallel devices	Parallel devices for current handling capability	On-state resistance
Virginia Polytechnic University (Vtech)	3-level dc/dc converter	3-ph 2-level VSI	3-level configuration reduces the EMI	On-state resistance

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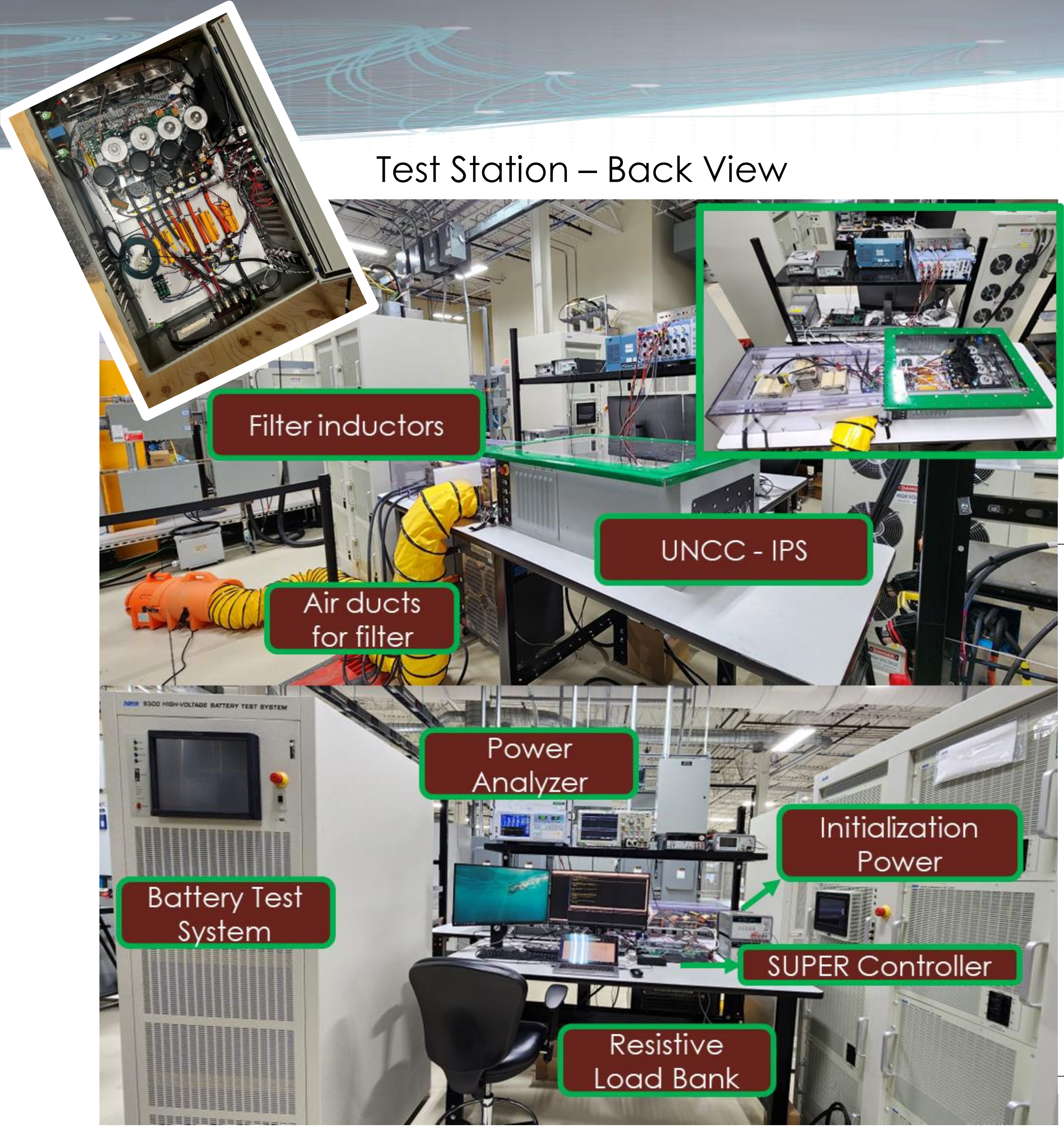
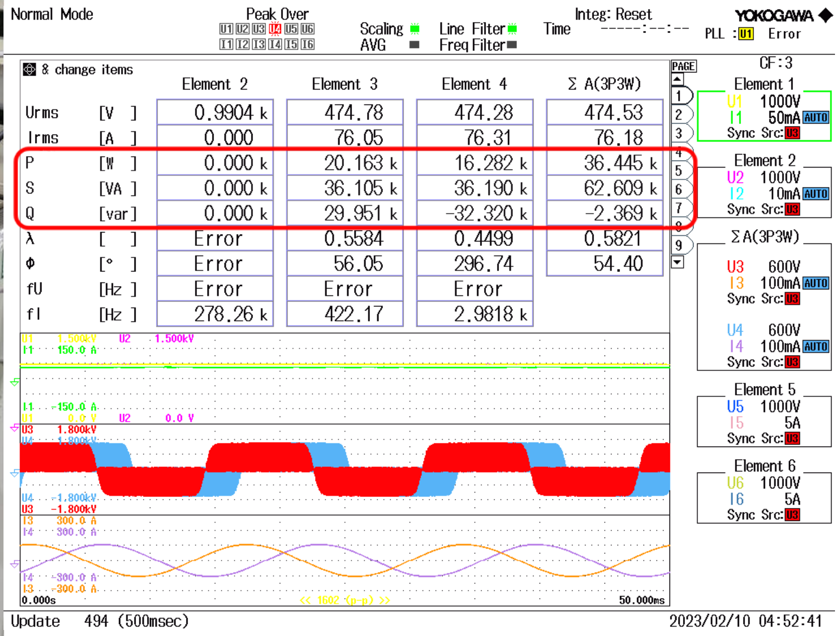
#5 – IPS Validation at ORNL

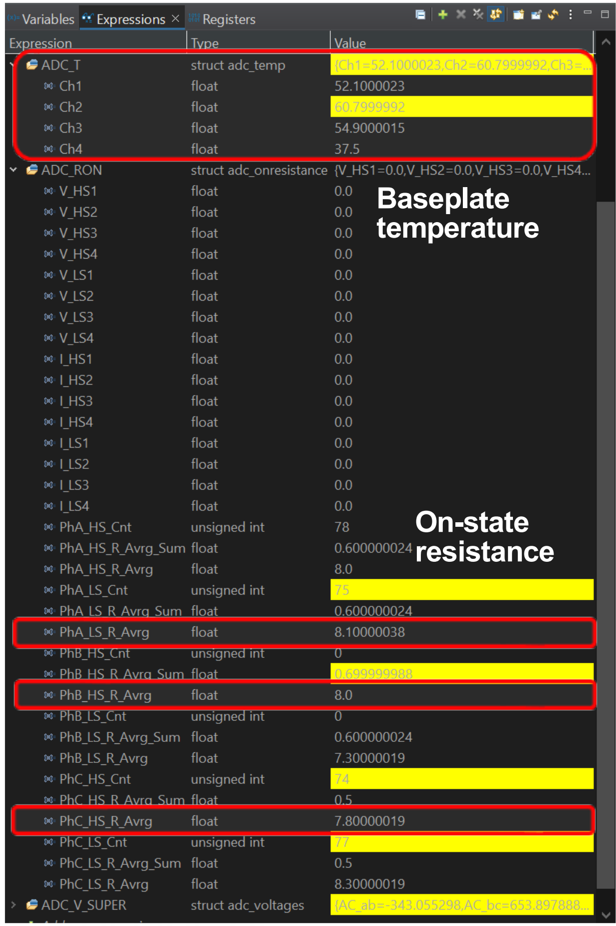
Test Station – Back View



Test Station – Front View

- IPS from UNCC was tested up to 36 kVA (Inverter only) in SUPER configuration in standalone mode with resistive load.
- Insitu measurements - **on-state resistance, base plate temperature and dc-link capacitance** estimates were verified.





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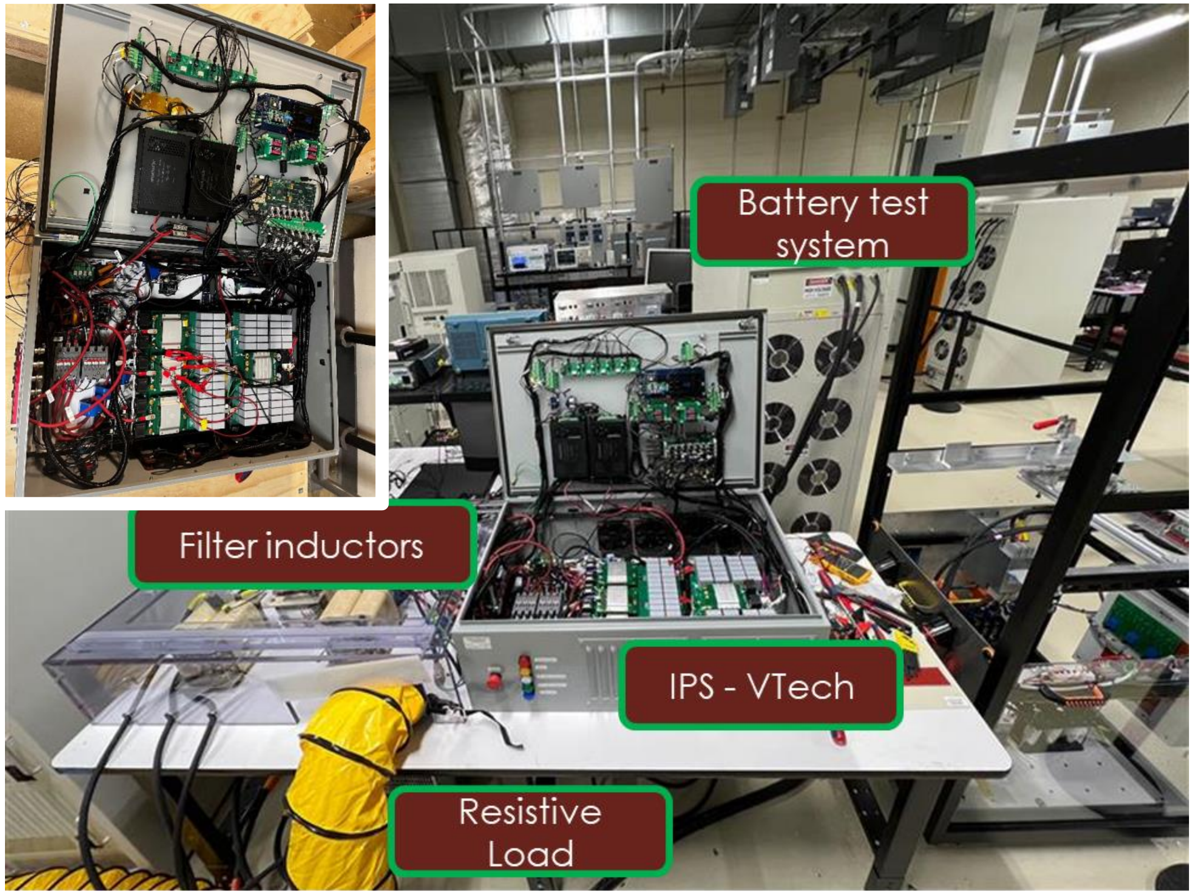
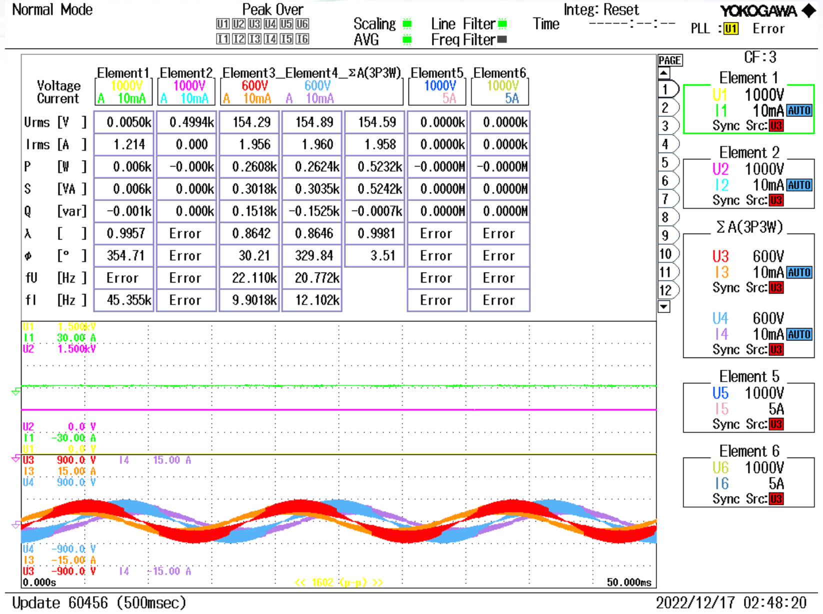
#6 – IPS Validation at ORNL

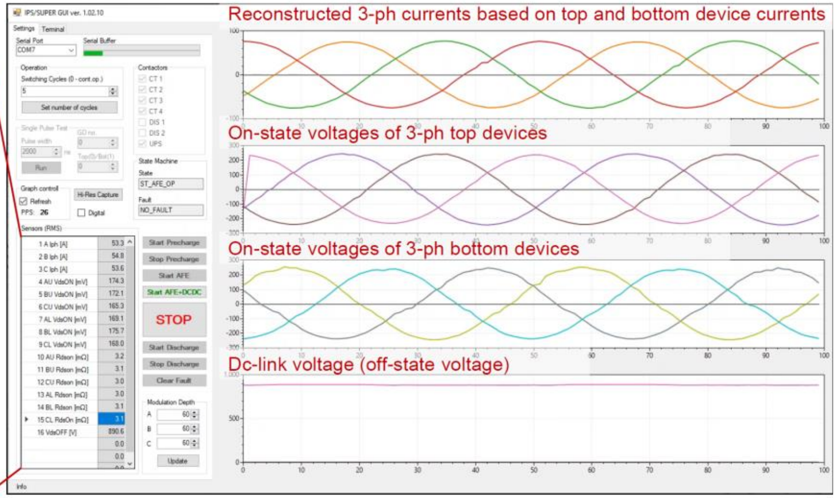
- **Vdson, Vdsoff and Ids measurements** were verified at at 900 V, 30 kW, 30 kHz for the inverter at Virginia Tech
- Power Stage operation verified at ORNL in standalone mode



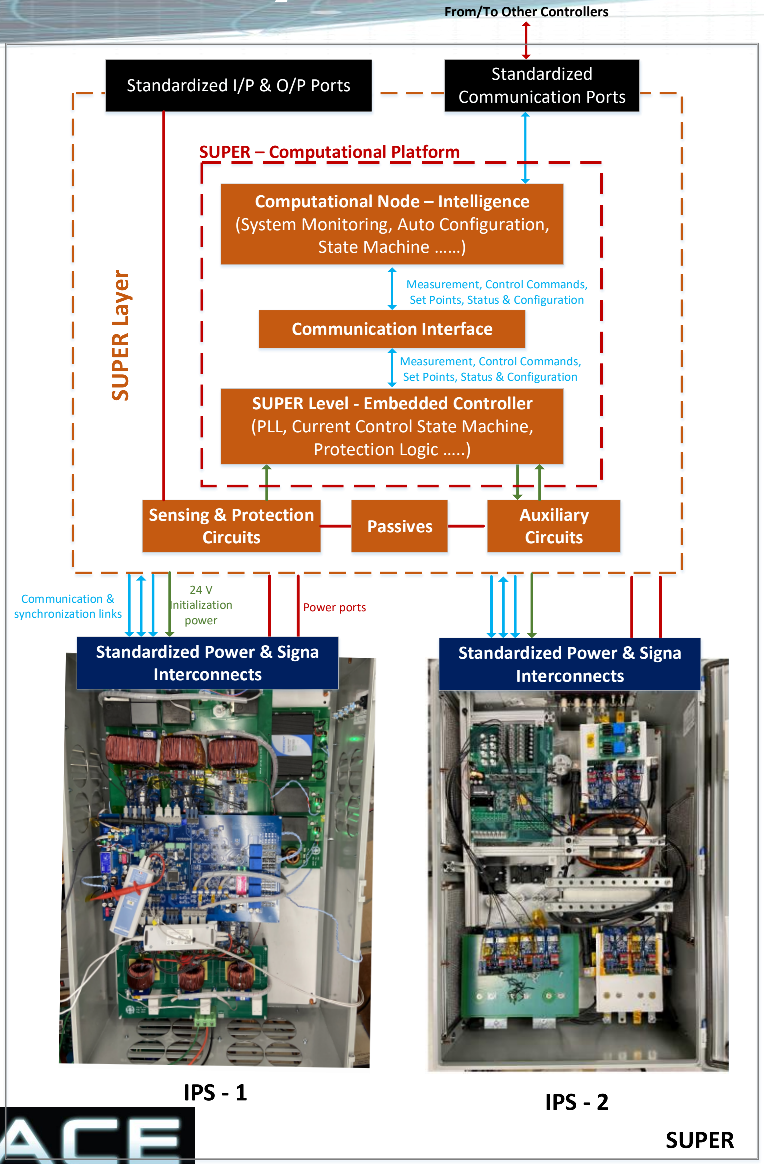


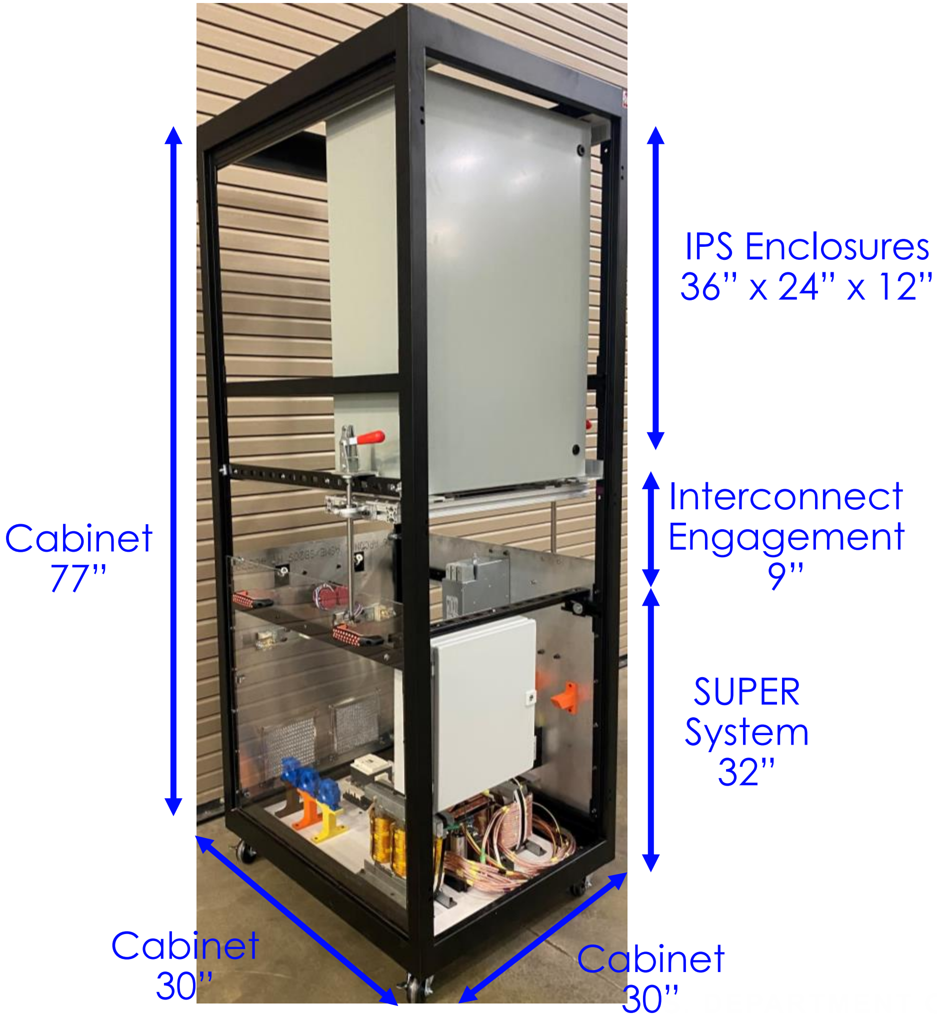
RMS value

Phase current	1 A Iph [A]	53.3
	2 B Iph [A]	54.8
	3 C Iph [A]	53.6
Six device on-state voltage	4 AU VdsON [mV]	174.3
	5 BU VdsON [mV]	172.1
	6 CU VdsON [mV]	165.3
	7 AL VdsON [mV]	169.1
	8 BL VdsON [mV]	175.7
	9 CL VdsON [mV]	168.0
Six device on-state resistance	10 AU Rdson [mΩ]	3.2
	11 BU Rdson [mΩ]	3.1
	12 CU Rdson [mΩ]	3.0
	13 AL Rdson [mΩ]	3.0
	14 BL Rdson [mΩ]	3.1
	15 CL RdsOn [mΩ]	3.1
Dc-link volt.	16 VdsOFF [V]	890.6



Outcome – Design for Interoperability, Scalability & Modularity





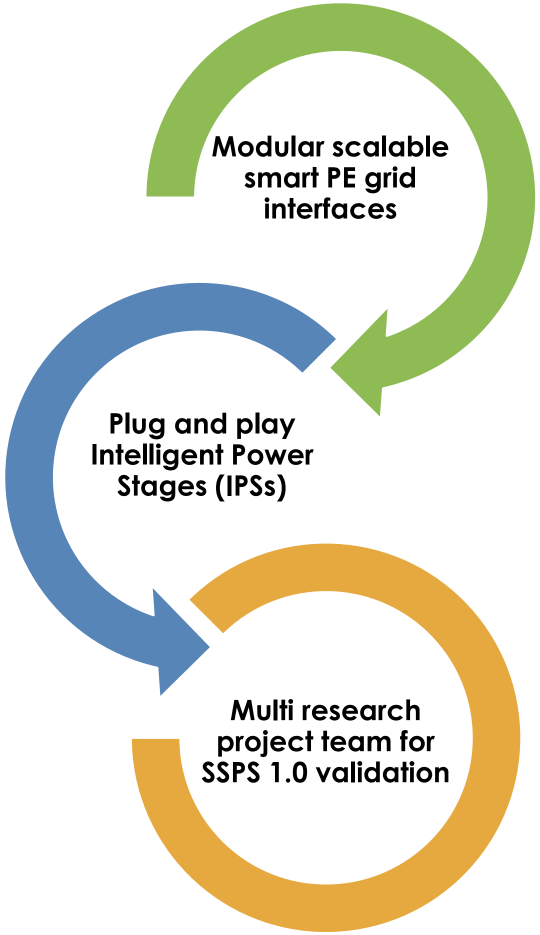
Requirements:

1. Synchronization Standardization (Hardware & Software) ☑
2. Dedicated communication link for control & data ☑
3. Dedicated computational nodes & auxiliary circuitry ☑
4. Advanced sensing circuits for health parameters☑

Timeline: Milestone Update

Milestone Description (or Go/No-Go Decision Criteria)	Period	Status
1. Validation of SUPER architecture through simulation	BP1-Q1	Completed
2. CHIL validation of the SUPER architecture for different control modes	BP1-Q2	Completed
3. Open loop testing of SUPER 1.0	BP1-Q3	Completed
4. Autonomous operation of SUPER with baseline IPS	BP1-Q4	Completed
5. Testbed development for validation IPS from partners	BP2-Q1	Completed
6. Performance evaluation of IPS from partners	BP2-Q2	Completed
7. Evaluation of IPS from partners for grid functions and advanced features	BP2-Q3	Completed
8. Demonstration of SUPER with IPS from partners	BP2-Q4	Completed

Impact/Commercialization



- Provides a pathway to develop power electronics interfaces with well defined hierarchy in controls, communication, protection, intelligence and optimization for scalability & modularity
- Provides a pathway to develop a library of power converters for SSPS 1.0
- Provides a pathway for interface, communication, protection standardization
- Provided a pathway to develop holistic systems with embed intelligence & advanced features systematically and strategically in fundamental blocks
- Helps emulate the different vendor scenario to access interoperability & standardization

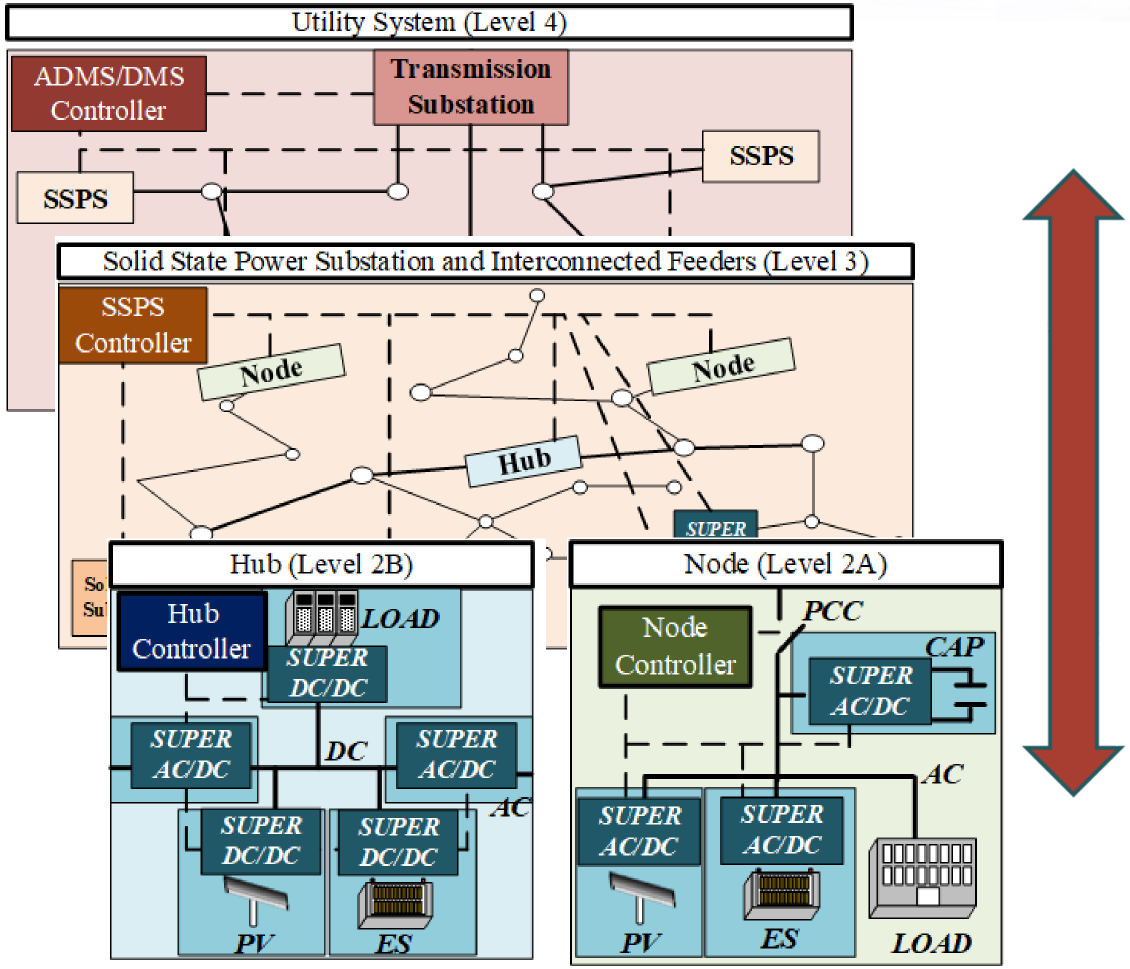
14 Professors/PIs, 6 Postdocs, 26 Students

Total. no. of publications ~ 20

Total. No. of. Patents – 6

Future Work

- Integrate fundamental building blocks i.e., SUPER & IPS in SSPS & highlight the benefits of the architecture
- Integrate the health data from IPS & SUPER for system optimization & control.



ORNL - TEAM

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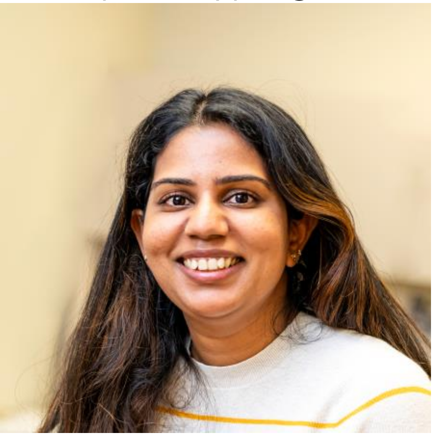
Power Electronics System Architecture

Brian Rowden
Hardware design and prototyping

Steven Campbell
System Integration & Testing

Rafal Wojda
Magnetics Design

Jonathan Harter
Hardware development



Radha Krishna Moorthy
Software framework development

Aswad Adib
SUPER and IPS simulation

Namwon Kim
IPS software validation

THANK YOU

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