DOE Office of Electricity TRAC

Peer Review



Intelligent Power Stages (IPSs)

PRINCIPAL INVESTIGATORS

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PROJECT SUMMARY

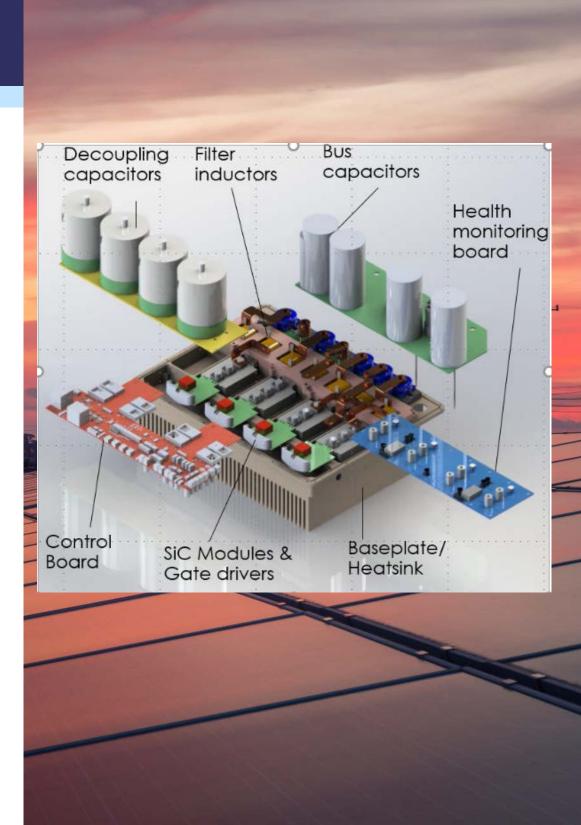
Smart Universal Power Electronic Regulators (SUPERs) & Intelligent Power Stages (IPSs)

The project focuses on developing and validating an intelligent power stage (IPS) incorporating system interoperability, diagnostics, and prognostics features.



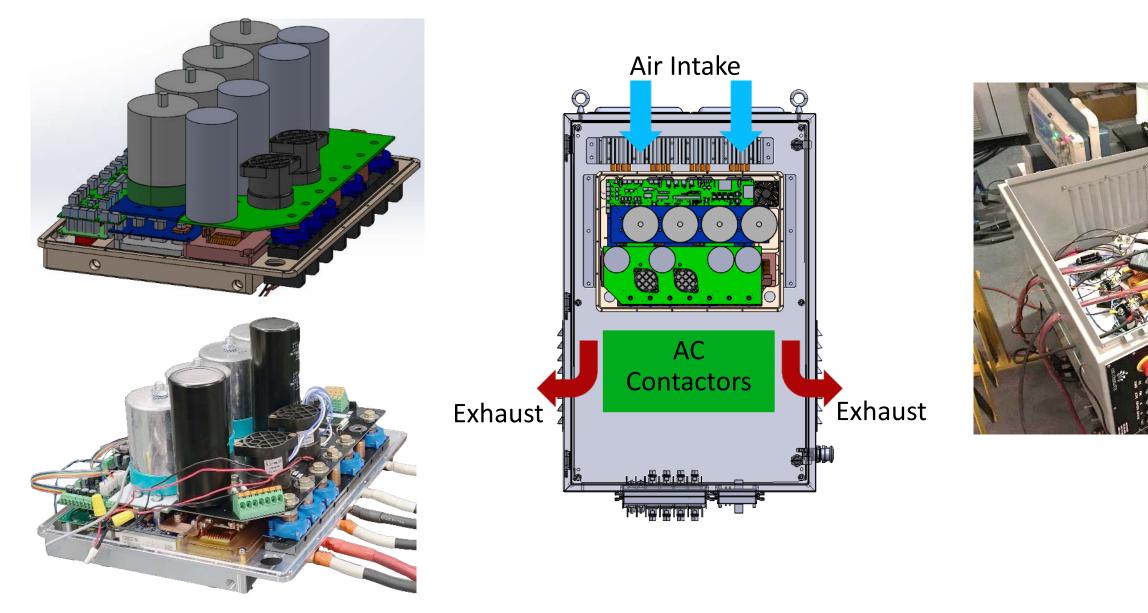
Innovations

- Development of an interoperable inverter with a secondary controller (IPS-SUPER)
 - Operation of the IPS with an emulated SUPER with less than 1 switching cycle delay
- Development of key elements/sensors/modules to monitor and report on status of the IPS (Diagnostics and Prognostics)
 - Key feature for diagnostics: Shoot-through detection of SiC power modules
 - Key feature for prognostics: resistance change and characterization of SiC semiconductor power modules



Innovation Update: IPS-SUPER Hardware

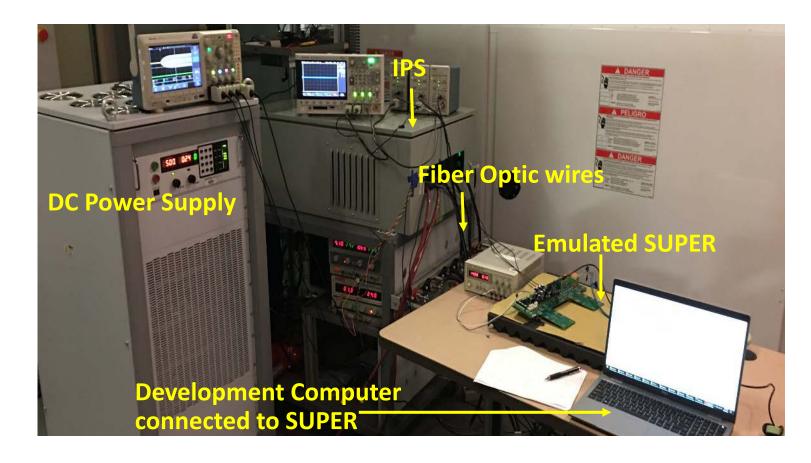
• Interoperable Intelligent Power Stage (IPS)

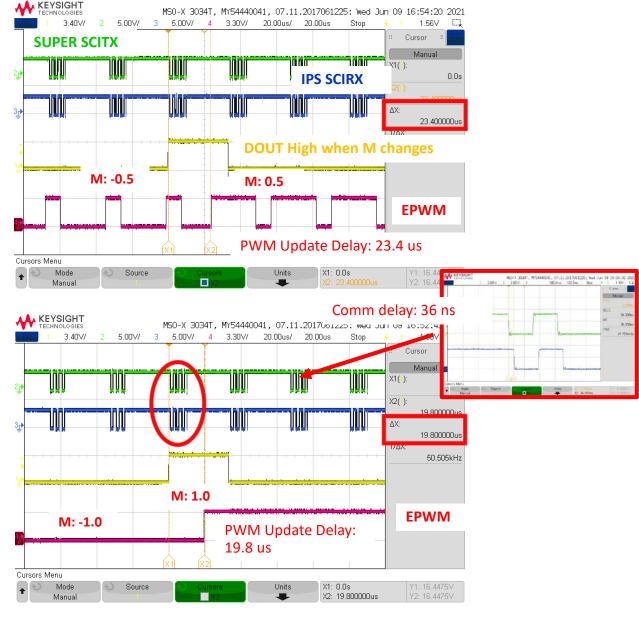




Innovation Update: Control Concept -1

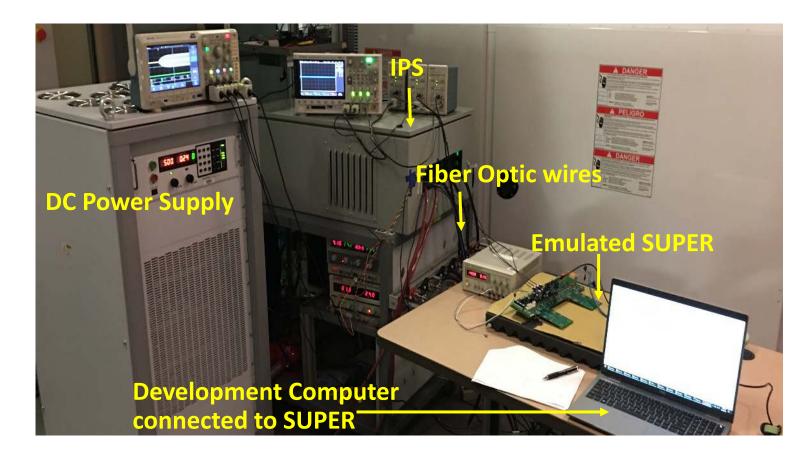
- Interoperable Intelligent Power Stage (IPS)
 - **Control Channel Communication Characterization**
 - Verified the delay is within one switching cycle

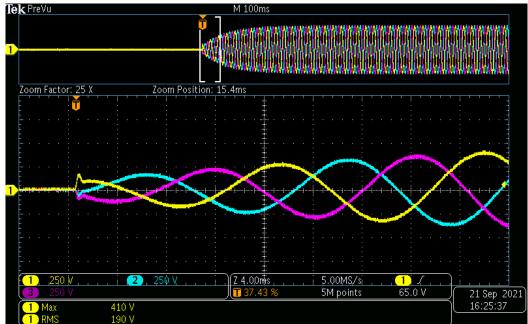


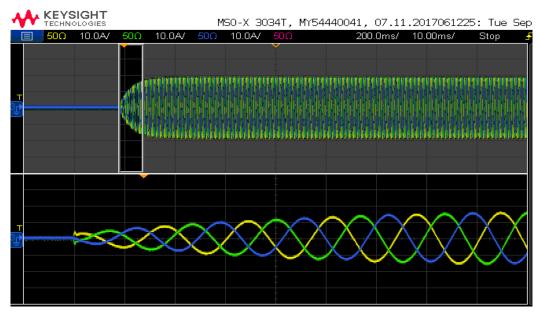


Innovation Update: Control Concept-2

- Interoperable Intelligent Power Stage (IPS)
 - Closed-loop (voltage-mode) at 10kW, 480VAC, 800VDC







3φ L-L voltages

3ф phase currents

Innovation Update: Robustness

- Interoperable Intelligent Power Stage (IPS)
 - Open-loop Control through Emulated SUPER at 75kW, 480VAC, 900VDC

Normal Mode		Peak Ove	er 110 Scalir 112 AVG	ng 📫 Line Fil 💻 Freq Fil	ter Time	nteg: Reset ::	YOKOGAWA ♦ PLL : 01 59.987 Hz
Voltage Current	Element 1 A 600V A 100mA	Element 2 A 600V A 100mA	Element 3 A 600V A 100mA	_ΣA(3V3A)_	Element 4 A 1000V A 100mA	Element 5 A 1.5V 5A	AGE CF:3 Δ Σ A(3V3A) 1 11 600V ΜΠΠ
	480.11 91.47 37.98k 43.92k -22.05k 0.8648 D30.14 59.987 4.3683k	A 100mA 480.19 91.49 37.89k 43.93k 22.24k 0.8624 G30.41 59.987 10.570k 	A 100mA 480.08 91.67 -0.00k 44.01k -44.01k -0.0000 D90.00 \$9.987 7.0647k	480.13 91.54 75.87k 76.13k 0.19k 0.9966 4.74	A 100mA 0.9059k 91.62 77.13k 83.00k -30.64k 0.9293 D21.67 Error 97.835k	0.6455 0.000 -0.000 0.000 Error Error 204.41k Error	1 U1 600V 1 100mA 100mA 2 Sync Src: 11 11 3 U2 600V 11 4 Sync Src: 11 12 5 U3 600V 11 6 Element 4 100mA 7 U4 1000V 10 8 Element 5 9 15 5A 9 U5 1.5V 10 Element 6 10 Element 6 11 U6 1.5V 111 10 Sync Src: 11 11 16 5A Sync Src: 11 12 U6 1.5V 111 16 5A
Update 342	(500msec)						2021/10/28 03:16:42

> 98.36% efficiency was obtained

P _{IN}	P _{OUT}	η	P _{LOSS}
77.13 kW	75.87 kW	98.36 %	1.26 kW

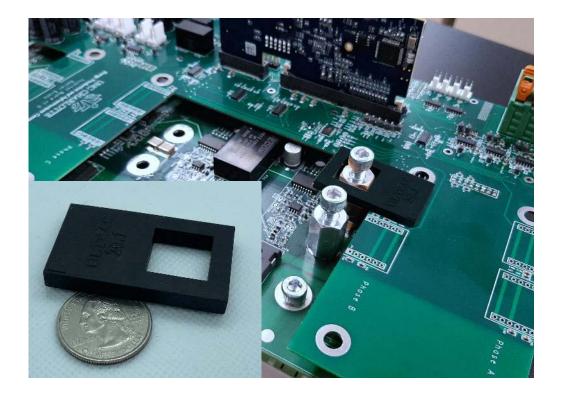
Waited until the equilibrium temperature point

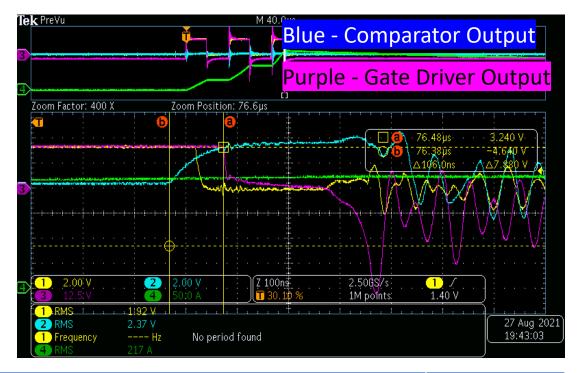
(saturation point)

Module-	Module-	Module-	Module-	Ambient
PhA	PhB	PhC	PhN	
49.7 °C	52.9 °C	46.8 °C	32.0 °C	25 °C

Innovation Update: Shoot-Through Sensor

- Diagnostics: Shoot-Through Protection
 - Typical de-saturation technique delay is greater than 2 microseconds and highly depends on temperature.
 - Shoot-through alarm & protection in less than 400 nsec.
 - Inverter tripped at 220 Apeak.

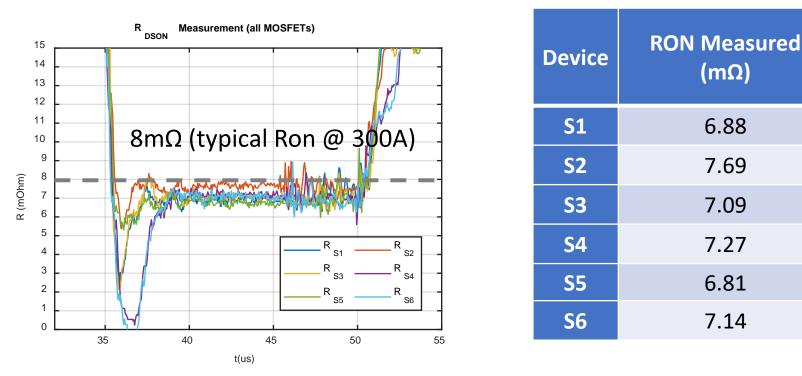


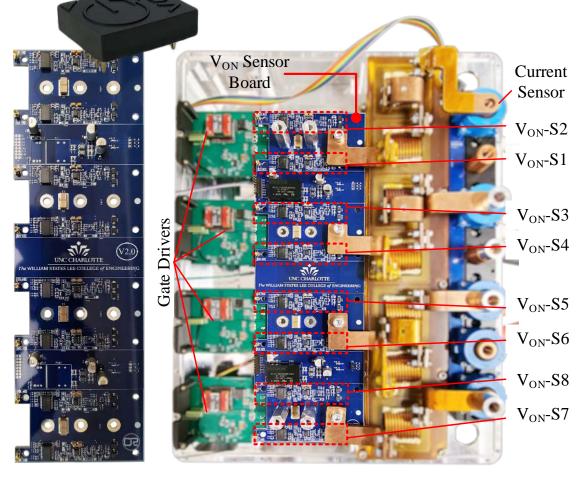


Symbol	Description	Time
T _{comp}	Comparator Propagation Delay	76 ns
T _{GPIO}	GPIO Input – RC Pullup Time	32 ns
T _{MCU}	ePWM Trip Latency	20 ns
T _{GD}	Gate Driver Delay	53 ns
T _{SiC}	SiC Module Turn Off time (datasheet)	219 ns
T _{total}	Shoot-through protection delay	400 ns
		9

Innovation Update: R_{ON} Sensor

- Prognostics: In-situ real-time R_{ON} Estimation
 - Developed isolated sensors and an algorithm to monitor the on-state resistance of SiC power modules,
 - Average reporting, one value/second to SUPER: two-four samples per switching cycles, > 30 A.
 - Relative parameter (value) to each device baseline value will be reported to SUPER or IPS-edge processor



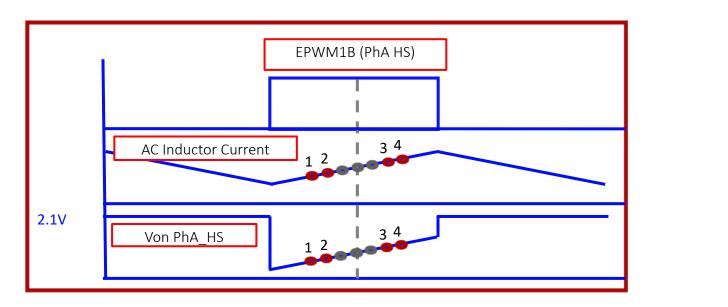


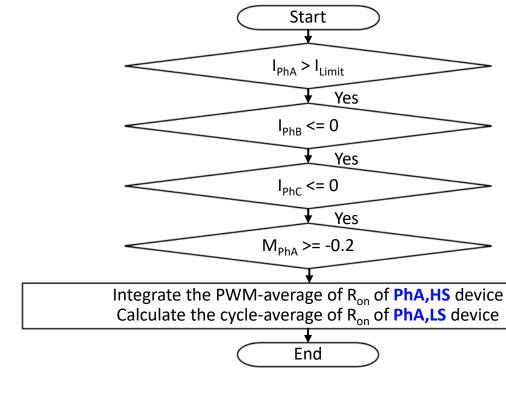
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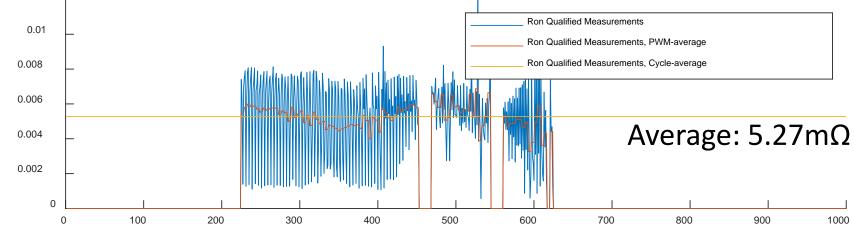
Conditions: 1kVDC, 140Amax, DPT (Second pulse)

Innovation Update: R_{ON} Algorithm

- Prognostics: In-situ real-time R_{ON} Estimation 2
 - Multi-sample averaging approach



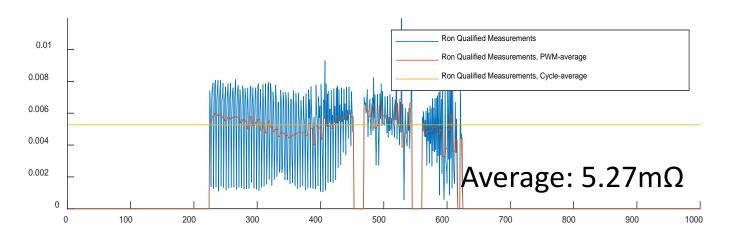




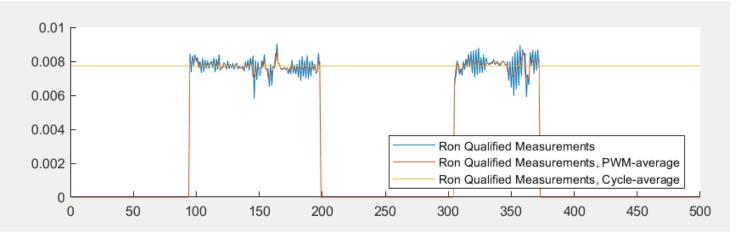
rt	>
Limit	
Yes	
= 0	
Yes	
= 0	
Yes	
= -0.2	
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Innovation Update: R_{ON} Consistency

- Prognostics: In-situ real-time R_{ON} Estimation 3
 - To improve the consistency: hardened the sensing hardware and developed a data qualification algorithm



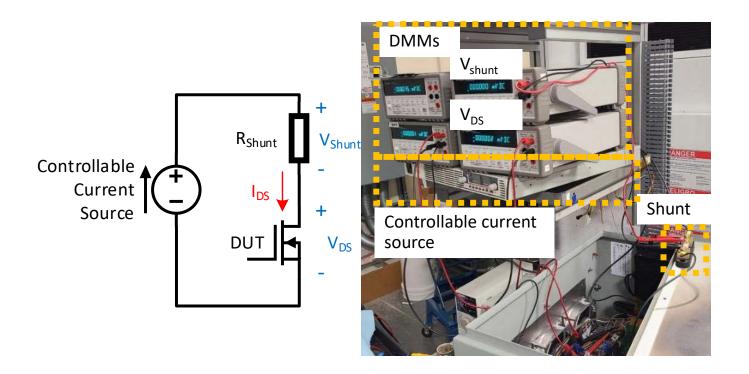


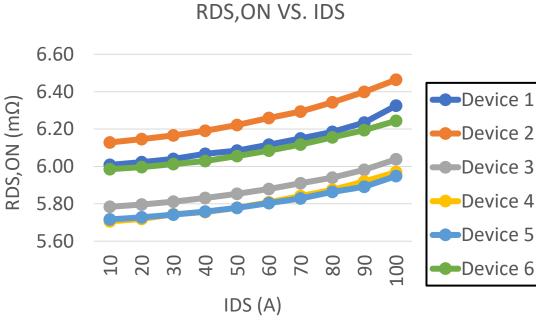


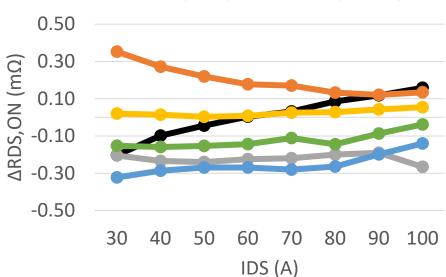
Cycle-Avrg	PhA,H S	PhA,L S	PhB,H S	PhB,L S	PhC,H S	PhC,L S
MATLAB	7.72	7.67	6.01	6.83	7.03	6.59
IPS DSP	7.71	7.67	6.02	6.82	7.02	6.58

Innovation Update: R_{ON} Accuracy

- Prognostics: In-situ real-time R_{ON} Estimation 4
 - A true (offline) on-resistance set up developed to measure the reference values for six devices
 - Observed differences from $-0.32m\Omega$ to $+0.35m\Omega$ which is equivalent to 5%-7%







Error: RDS,ON (DSP) - RDS,ON (DMM)

Innovation Update : Future

- Calibration of the relative R_{ON} based on the current value and temperature
- Health monitoring of electrolytic DC link capacitors in IPS.
- Development of algorithm identifying the health status of the DC link capacitors.

Impact/Commercialization

Include the impact/commercialization status here: With our industrial partners, an LOI is submitted to DOE SBIR program under DE-FOA-0002555 to commercialize and demonstrate the developed sensors and features in a commercial inverter

IP STATUS

Provisional patent application: Title: On-State Voltage Measurement of High-Side Power Transistors in Three-Phase Four-Leg Inverter for In-Situ Prognostics **No.**: 63/203,405 **Inventor(s)**: Chondon Roy, Namwon Kim, James Gafford, and Babak Parkhideh Status: Filed new provisional patent application.

THANK YOU

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