DOE Office of Electricity TRAC

Peer Review

U.S. DEPARTMENT OF ENERGY | OFFICE OF ELECTRICITY

IPS Hardware Prototype Development

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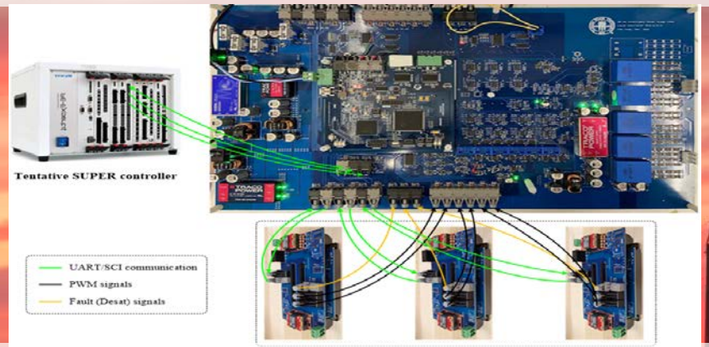
PROJECT SUMMARY

The objective of this project is to develop and validate an intelligent power stage (IPS) with advanced features to improve the robustness and reliability of grid-tired converters interfacing renewable energy source and energy storage elements. The prototype will be a 3-phase interleaved DC/DC stage with a 500V-1kV DC input and a 3-phase DC/AC stage rated at 50 kW and 480 Vac. The proposed advanced features will be verified on the developed IPS hardware.

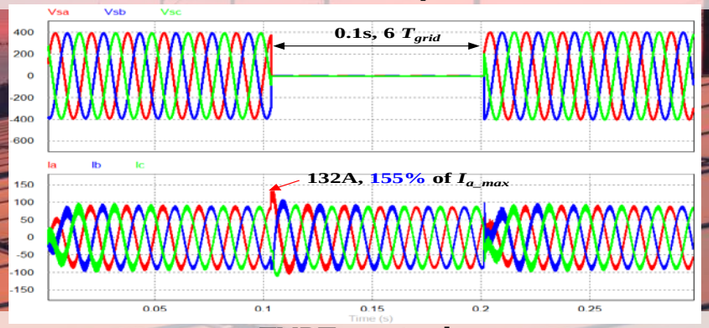
Innovations

- ✓ Active Gate Driver (AGD)
  - Control dv/dt and switching loss based on load current & device temperatures.
  - Integrate fault/protection with active gate driver functions.
- ✓ Prognosis & Diagnosis (P&D)
  - Integrate device aging prognosis and diagnosis of gate driver status based on gate current sensing.
  - Low-cost and anti-noise implementation.
- ✓ Control and Communication
  - Enhanced EMI-immune IPS control with high A/D sampling CM noise rejection ratio.
  - up to 50Mbps bidirectional all fiber optic-based communication among SUPER, IPS control and gate drivers.
- ✓ LVRT/ZVRT functions
  - Low-latency hardware-based approach to suppress inrush current.
  - Mitigate transient inrush current from 312% → 155%.
- ✓ Self-sustained Auxiliary Power Supply (APS)
  - Dual inputs from DC or AC bus.
  - Enhanced common-mode noise immunity.

Integrated and intelligent gate driver: AGD + P&D



EMI-immune Control and fiber optic communication

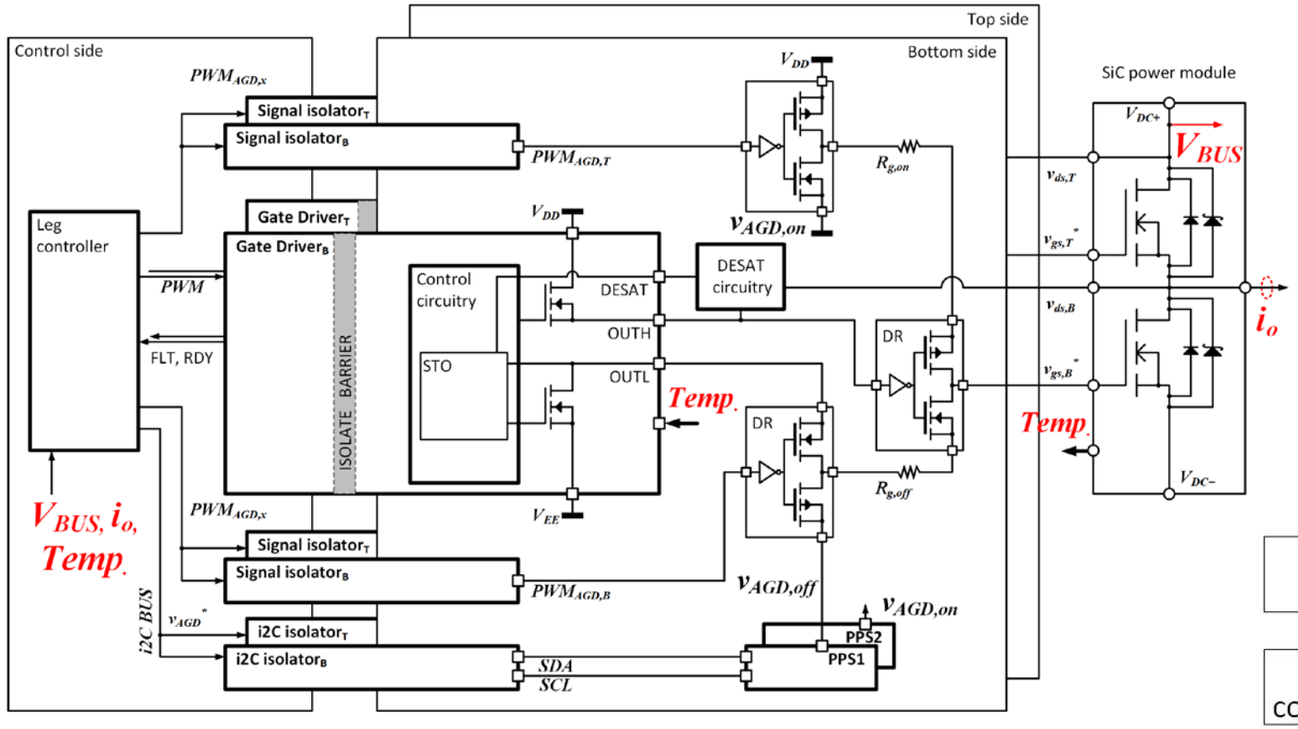


ZVRT control

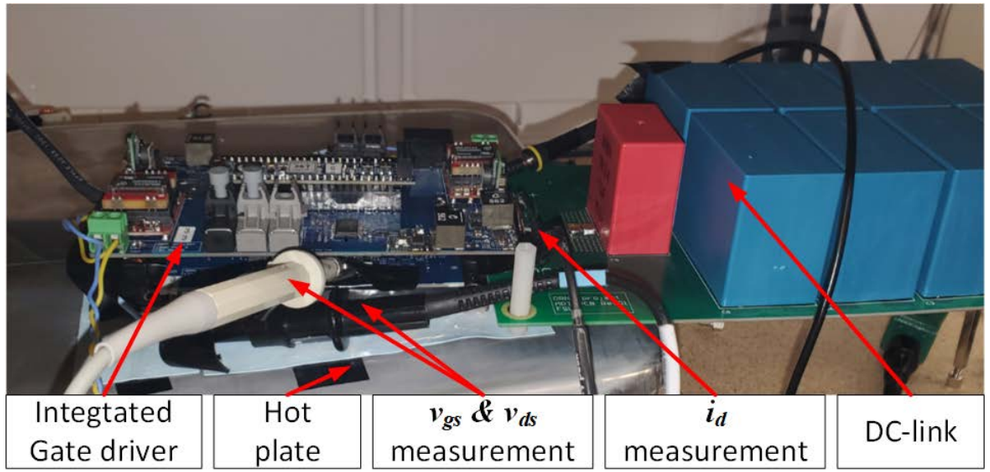
Self-sustained APS

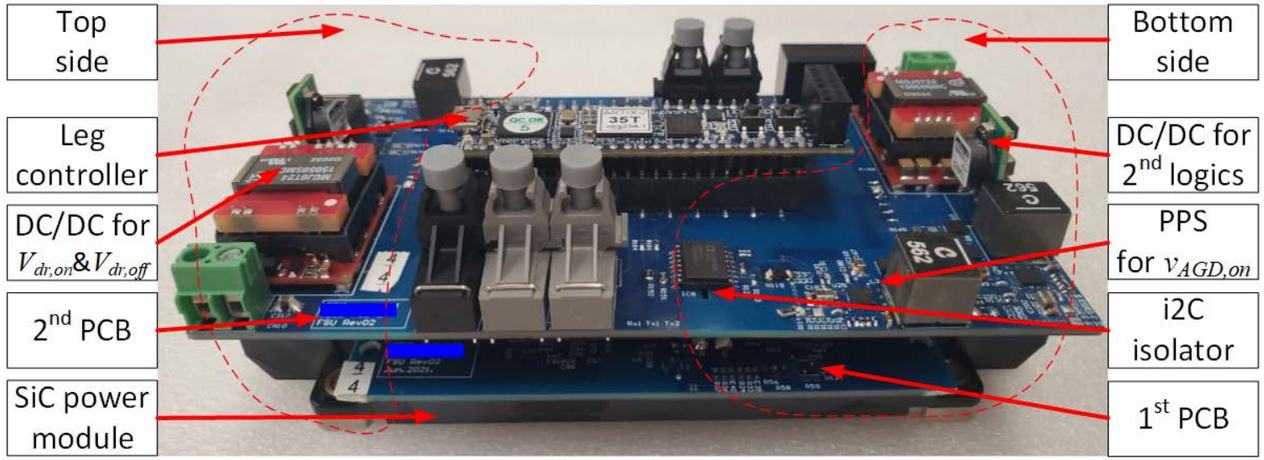
AGD Function and Experimental Verification (1/2)

- Proposed AGD circuit



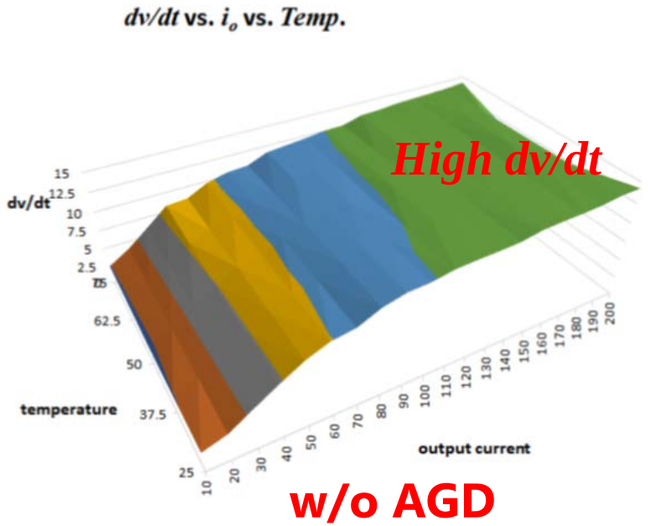
- Hardware prototype



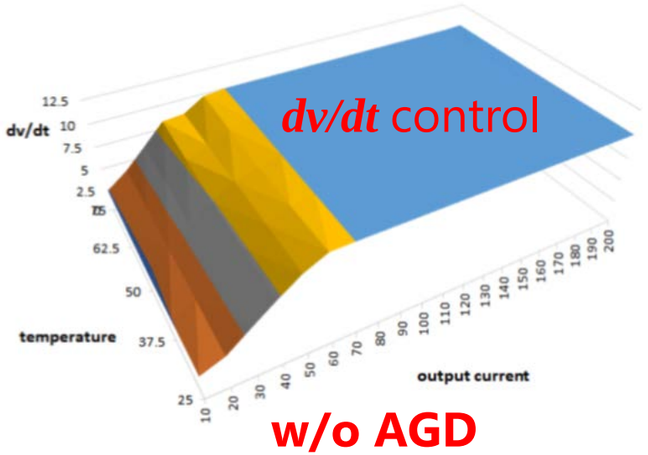


- Control dv/dt and switching loss.
- Integrated AGD circuit with fault/protection functions.
- Optimized circuit design for precise AGD control.
- AGD control based on load current and device temperature.

AGD Function and Experimental Verification (2/2)

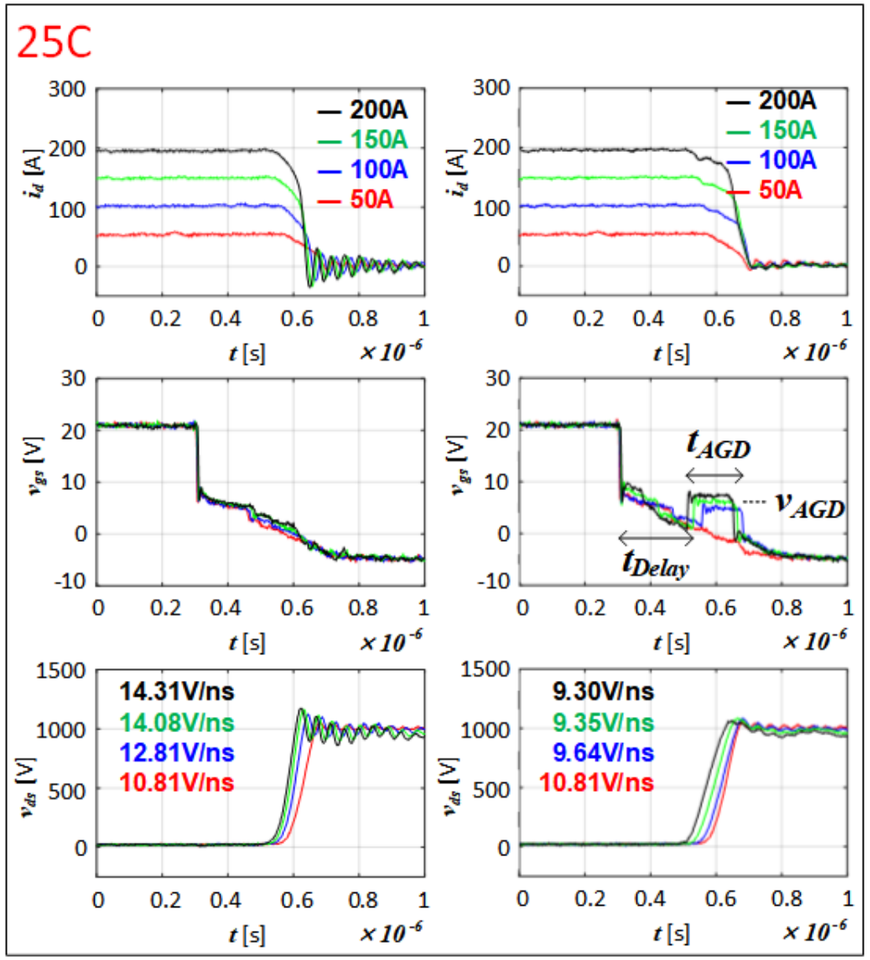


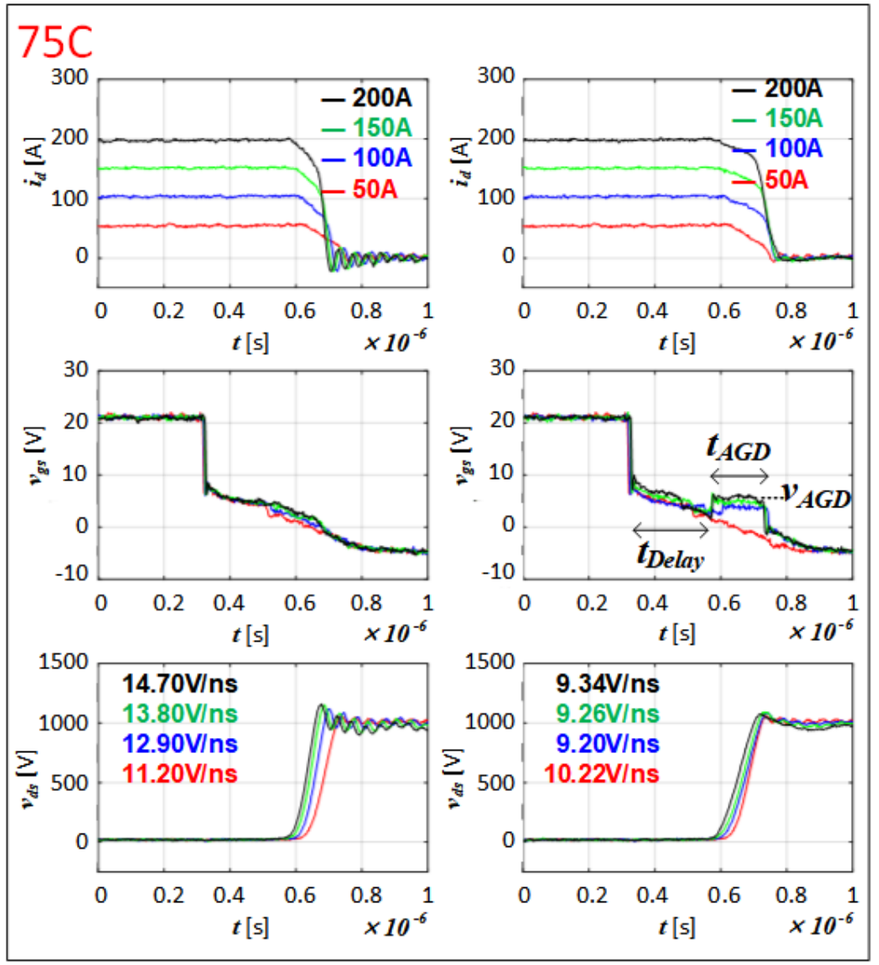
w/o AGD



w/o AGD

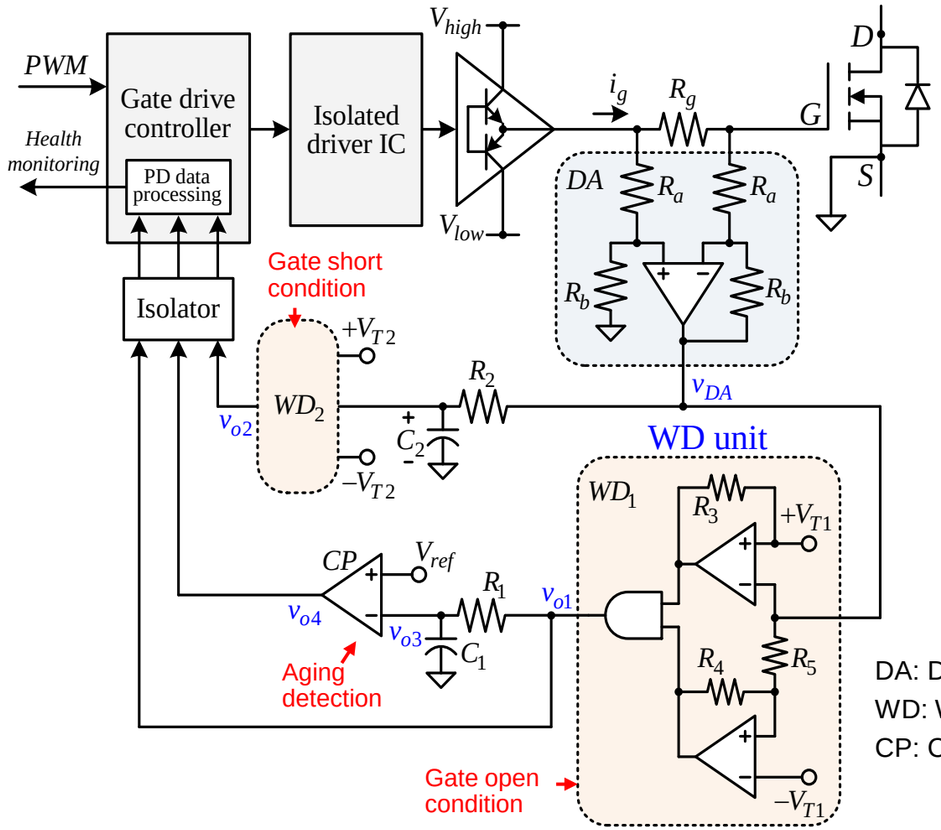
dv/dt controlled under different load current and device temperatures





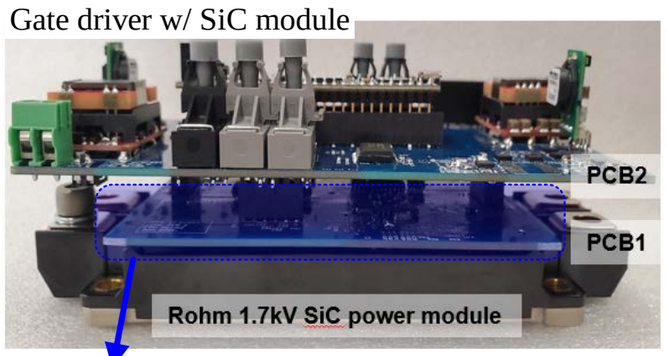
P&D Function and Experimental Verifications(1/2)

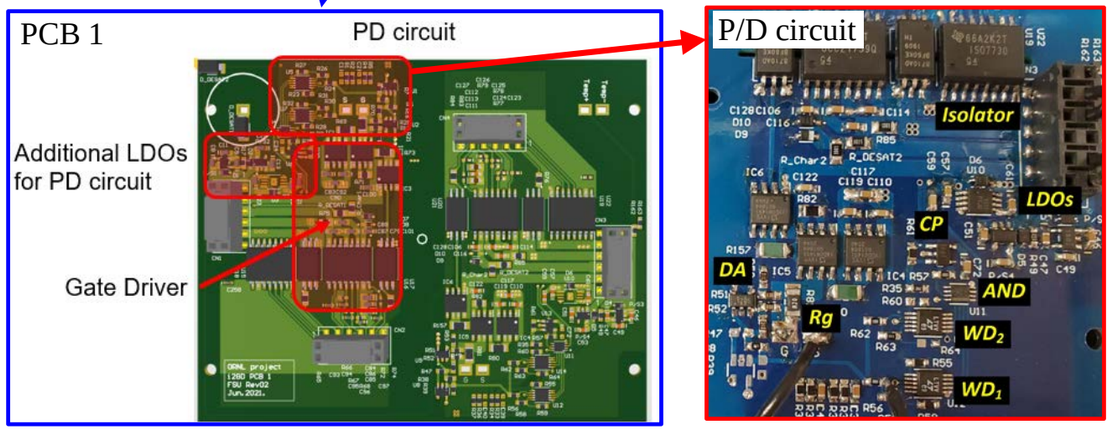
- Proposed P&D circuit



DA: Difference amplifier
WD: Window detector
CP: Comparator

- Hardware prototype

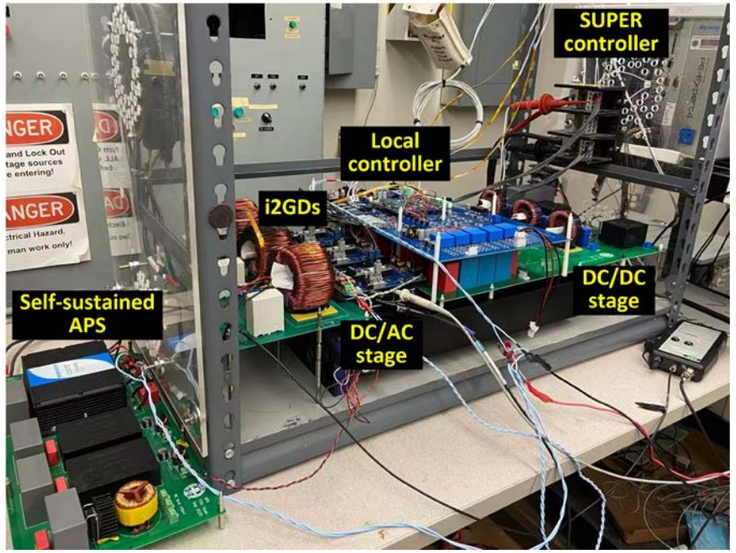




- Diagnose status of both power device and gate driver (GD) based on monitoring gate current
- Diagnosis of gate open/short circuit conditions, connection verification, and GD board fault
- Prognosis of device aging → generating early warning signal

P&D Function and Experimental Verifications (2/2)

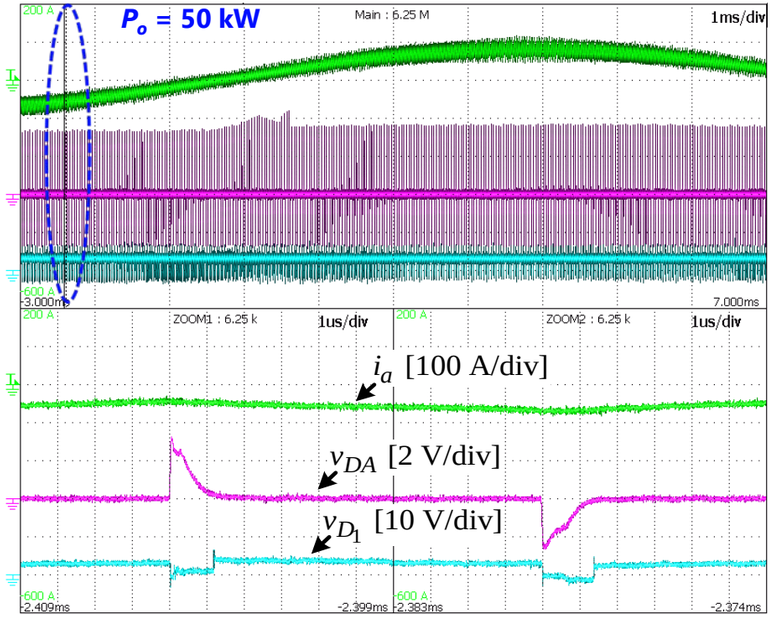
➢ Inverter based verification



Specification:

- V_{dc} = 1 kV
- $V_{ac_LL_rms}$ = 480 Vrms
- P_o = 50 kW
- f_{sw} = 30 kHz
- L_{DM} = 300 uH

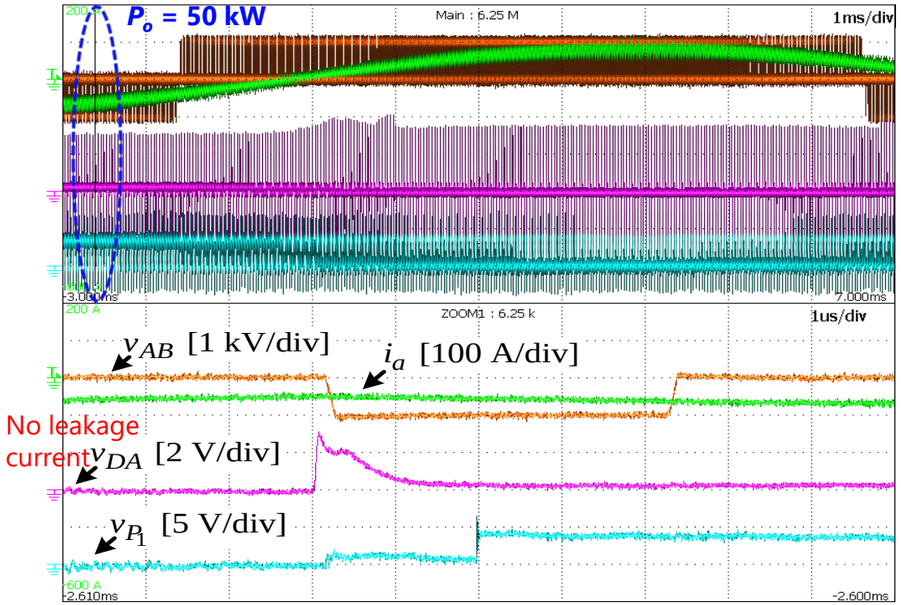
✓Diagnosis verification



phase current (i_a): Green v_{DA}: pink v_{D1} : Blue

- When gate open: no gate current → VD1 becomes logic"1"
- When gate short circuit: continuous gate short current → VD2 becomes logic"0"

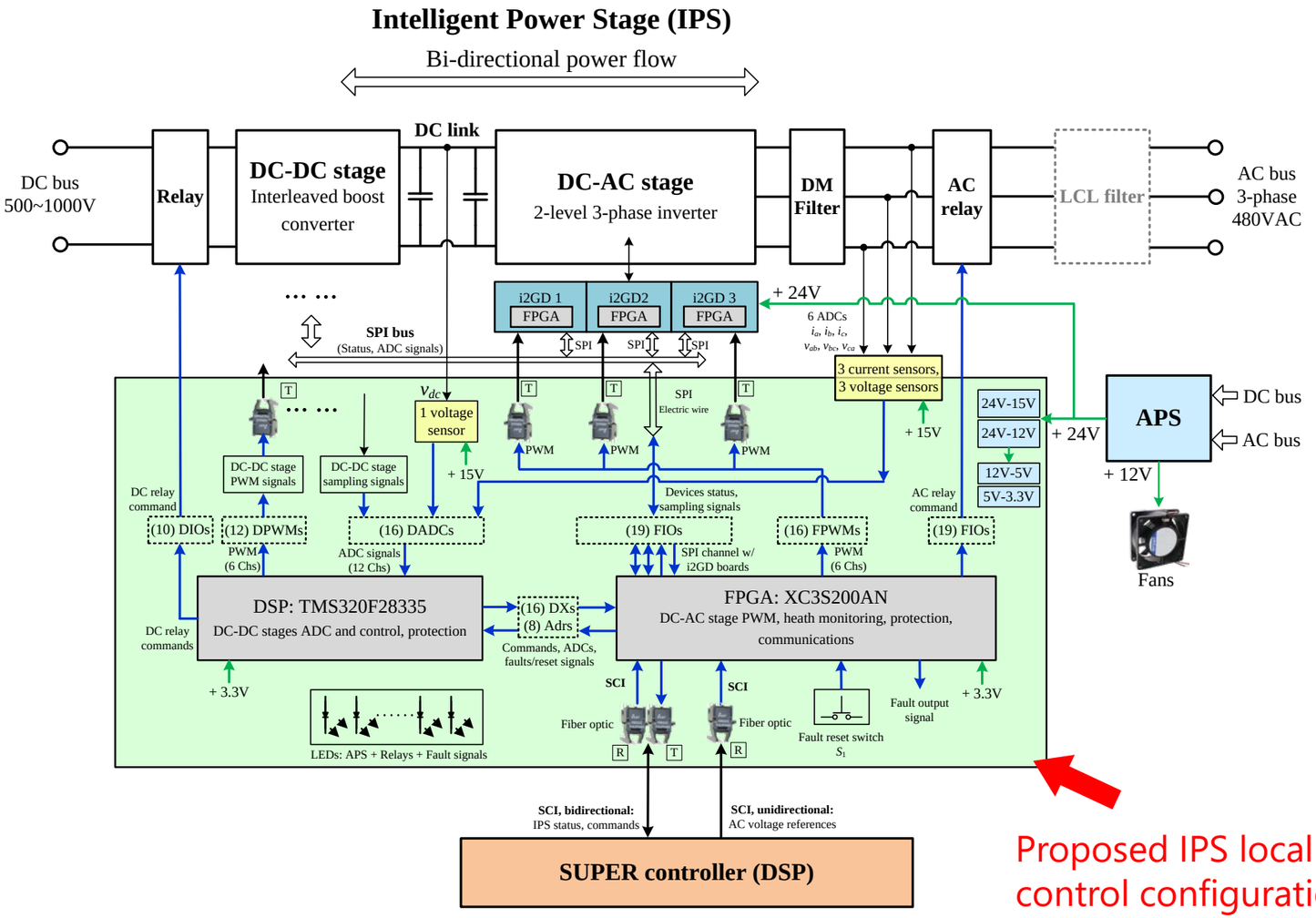
✓Prognosis verification



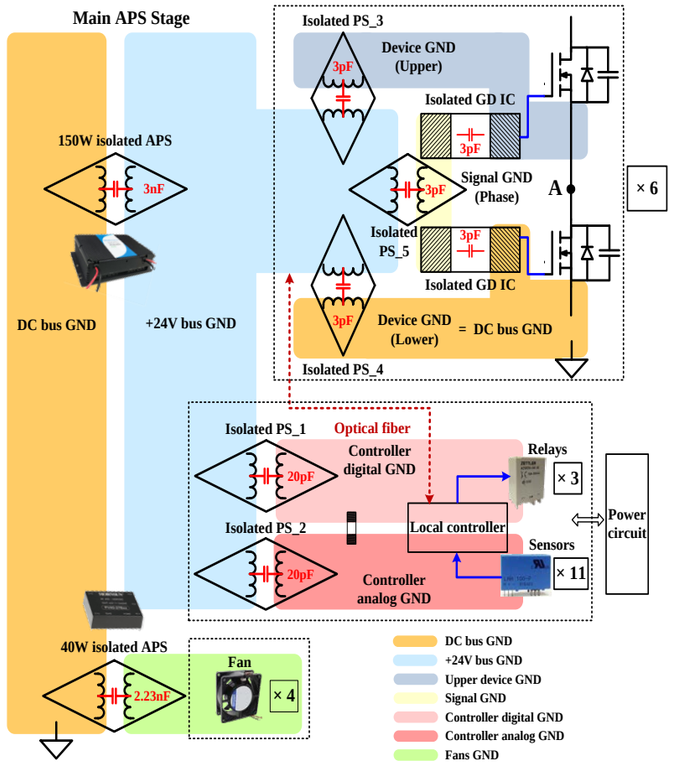
phase current (i_a): Green v_{DA}: pink, v_{P1} : Blue

- When gate leakage current is zero → Vp1 is logic"0", device not aged;
- When gate leakage current › 200 mA → Vp1 becomes logic"1", device aged;

IPS Control with Enhanced EMI-immunity



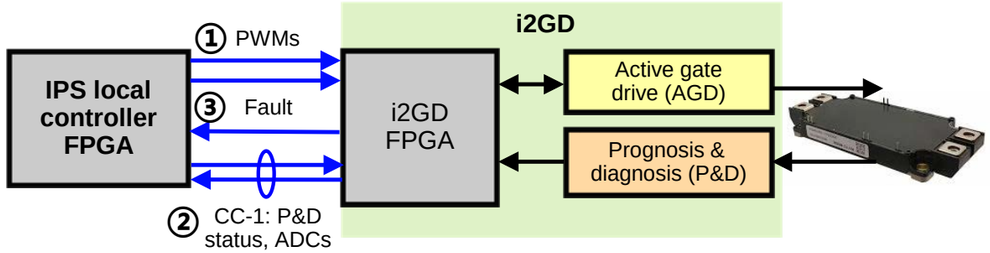
Proposed IPS local control configuration



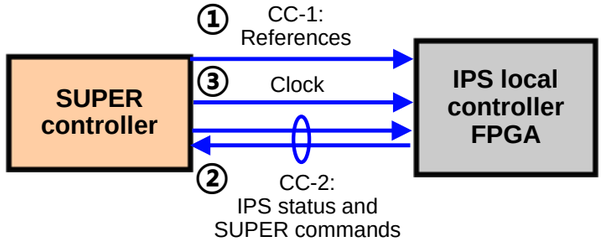
Enhanced EMI-immunity design to reduce parasitic capacitors

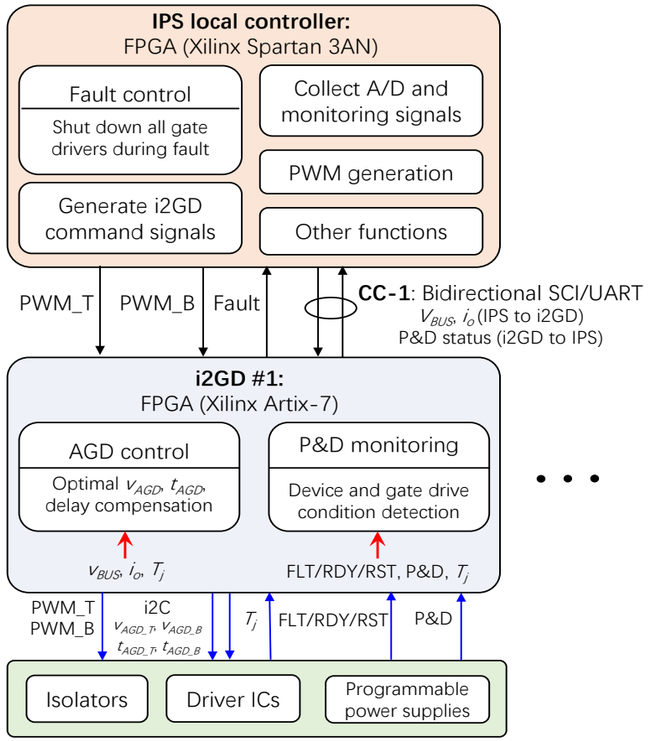
IPS Communication with SUPER and Gate Drive

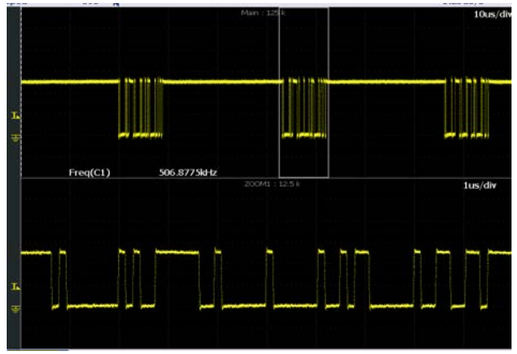
Communication between IPS control and GD



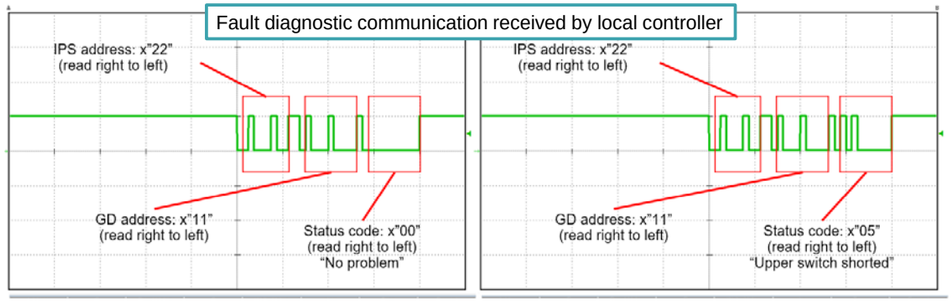
Communication between SUPER and IPS control



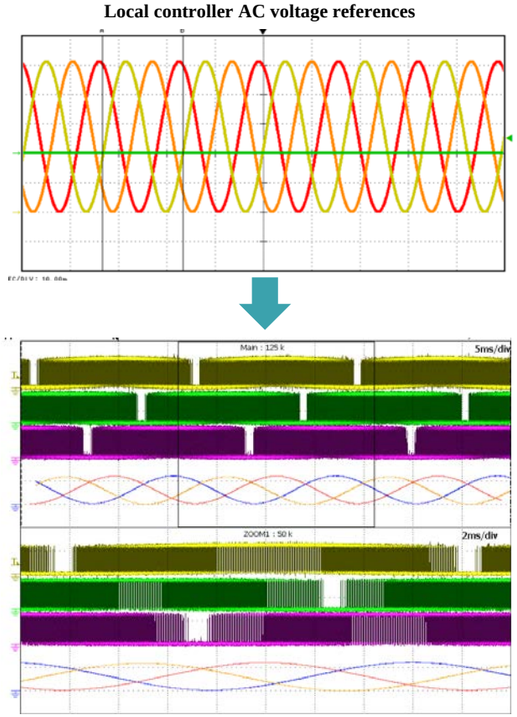




Communication validation of AGD function



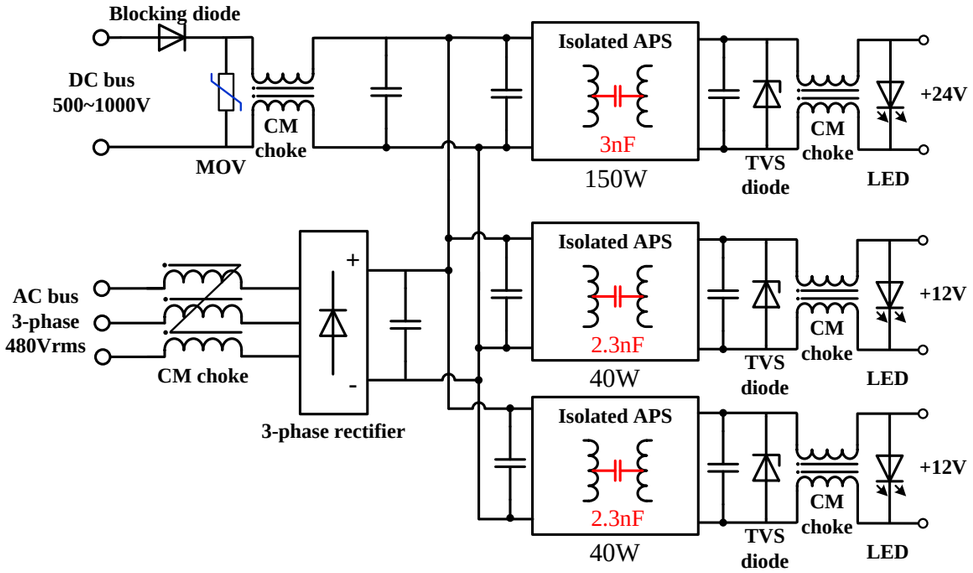
Communication validation of P&D status



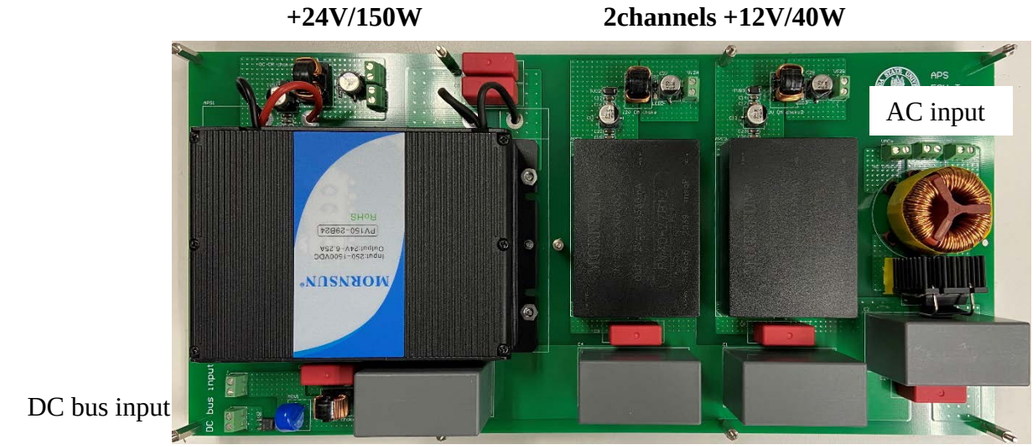
Communication validation of PWM signals

Self-sustained Auxiliary Power Supply (APS)

- Proposed APS circuit

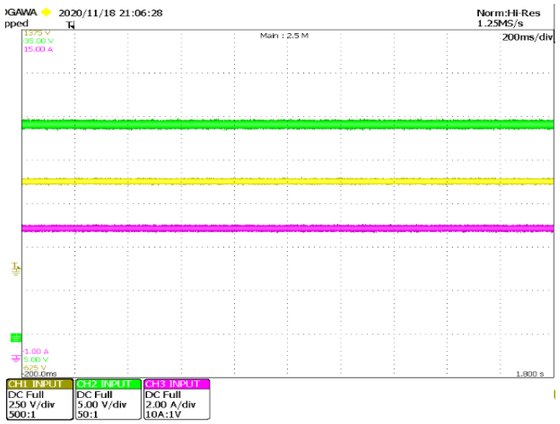


- Prototype



- Dual input from DC or AC buses
- Input dc voltage range: 250V~1200V
- +24V bus: 150W, +12V bus: 40W×2
- Efficiency: ~90%

- Experimental results

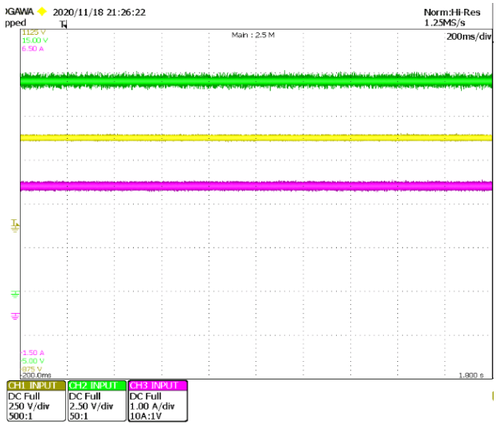


V_{+24}: 24V

V_{in}: 500V

I_{+24}: 6A

+24V bus waveforms@150W



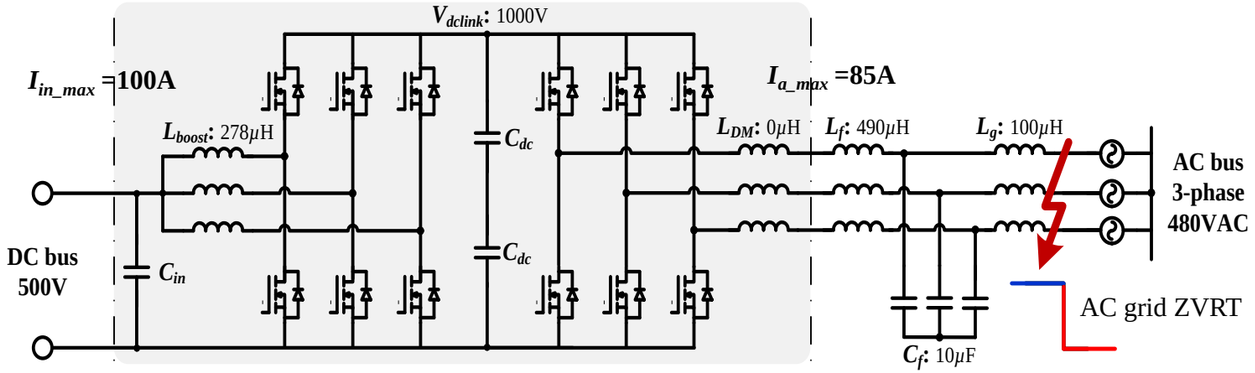
V_{+12} : 12V

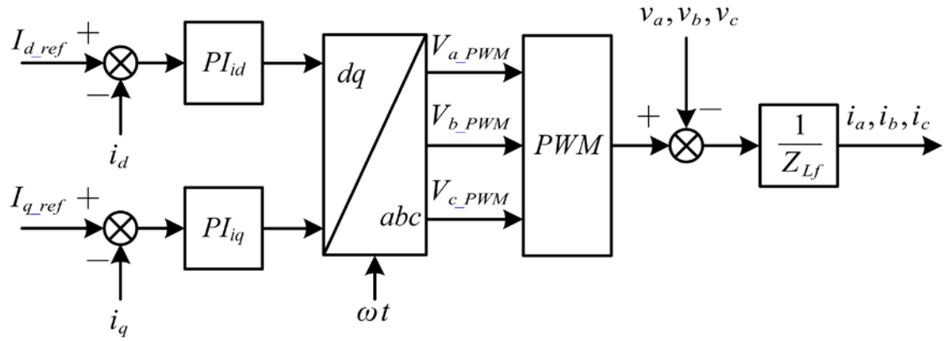
V_{in} : 500V

I_{+12} : 3A

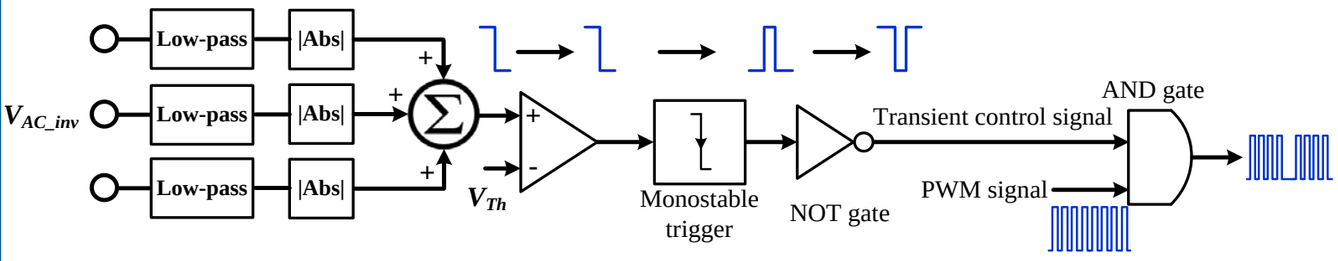
+12V channel waveforms@40W

Zero-voltage Ride Through (ZVRT) Control



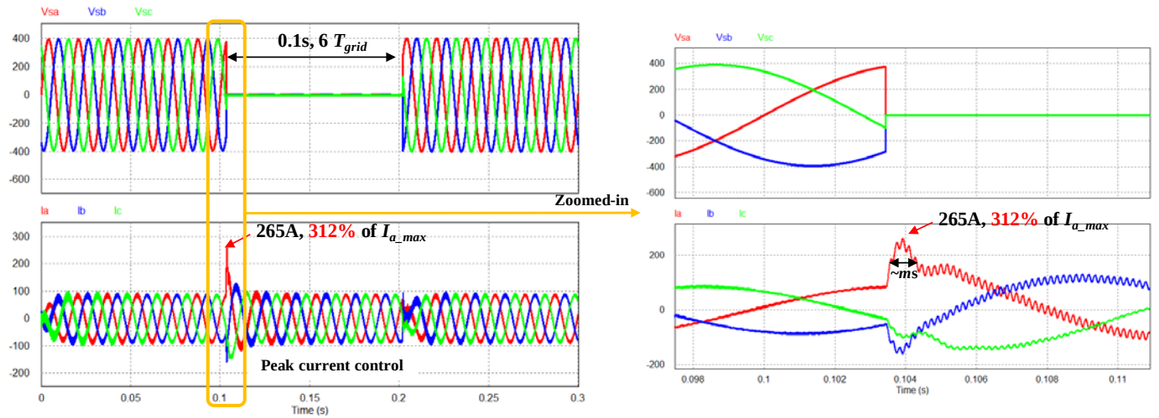


Tradition ZVRT control

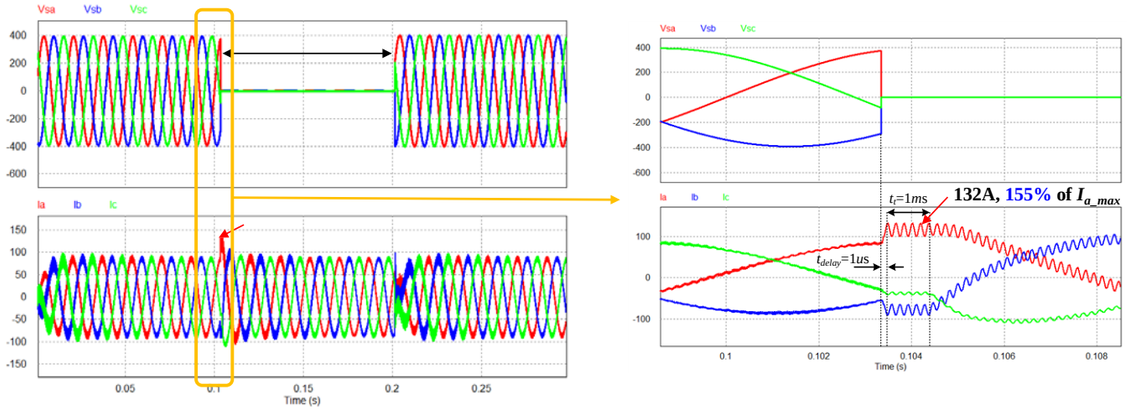


Proposed hardware-based control to mitigate inrush current

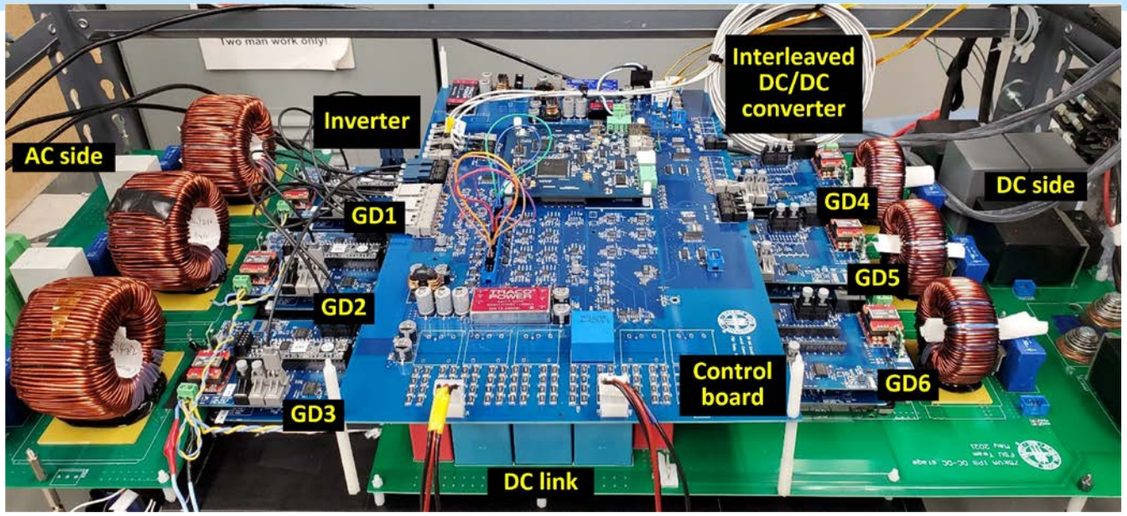
with tradition ZVRT control



with proposed ZVRT control

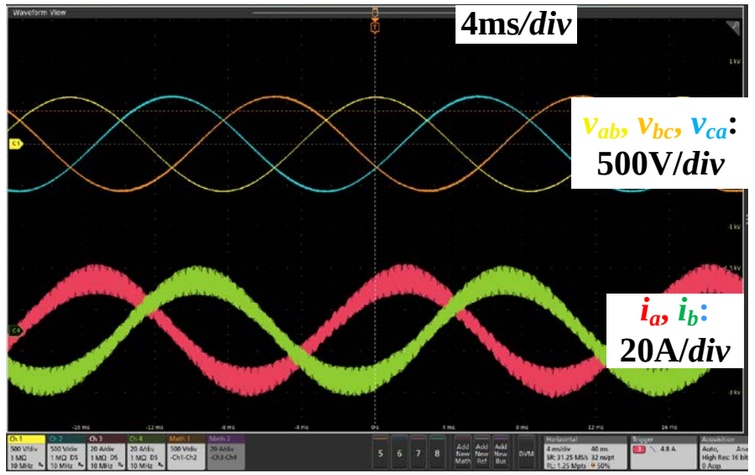


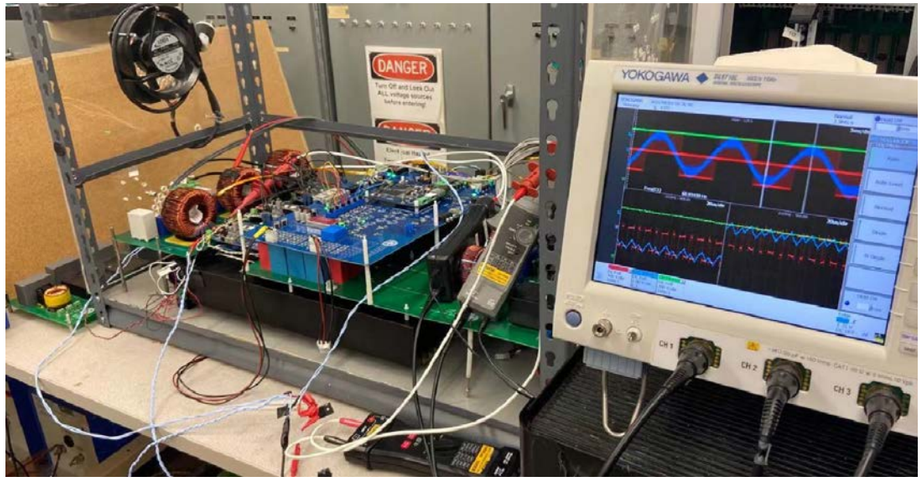
Grid-tied Closed-loop Experimental Results



Hardware prototype

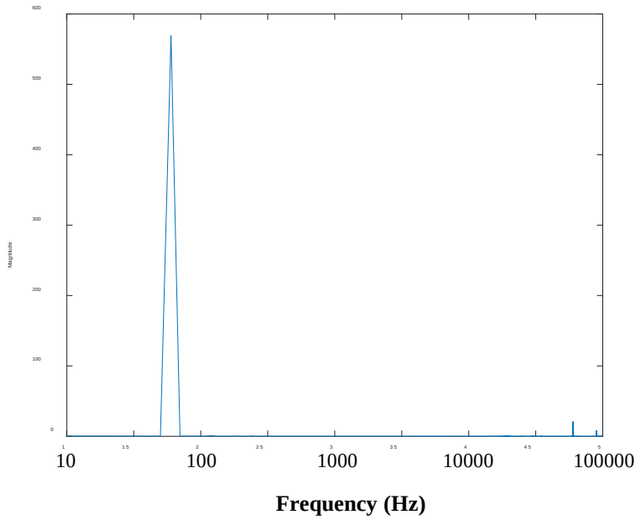
Measured voltage and current waveforms



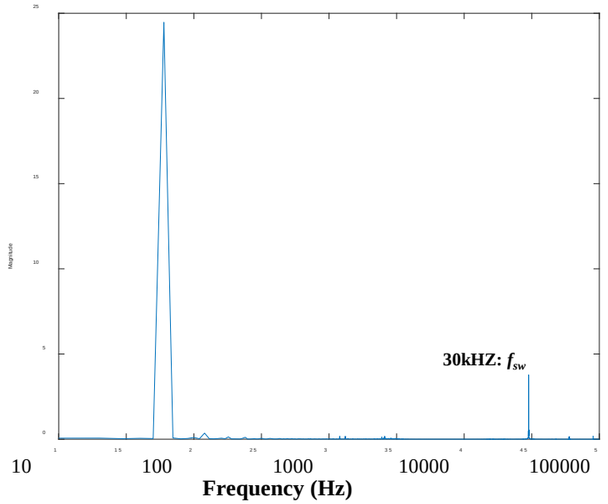


Experimental testbed

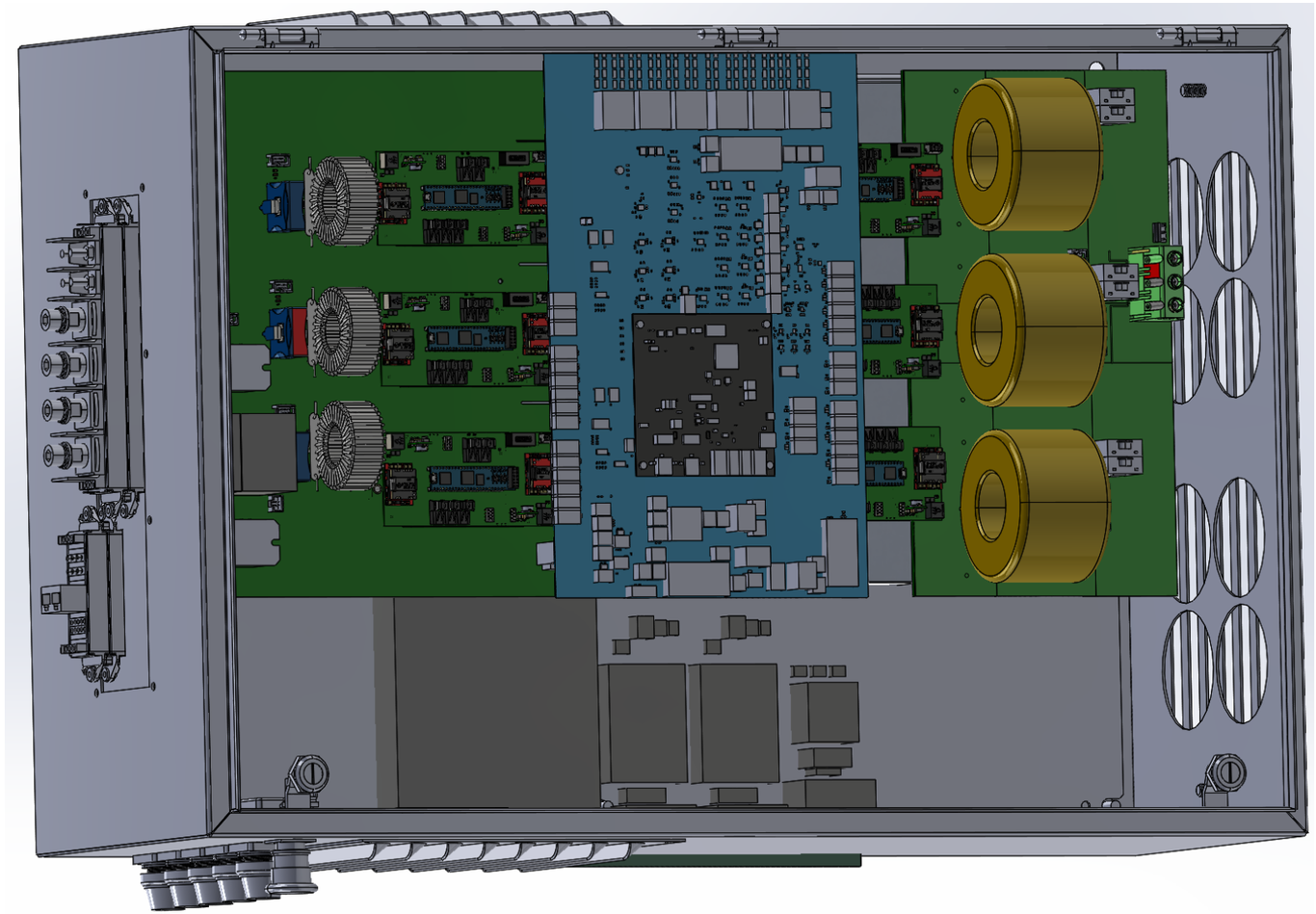
Grid voltage FFT



Grid current FFT (iTHD =1.65%)



IPS with the Standardized Enclosure



3D CAD/picture of the IPS with the standardized enclosure: 36” x 24”x 12”

Milestone Update

BP1 Milestones

Milestones	% Progress toward Completion
M 1.1 Intelligent gate drive, APS, DC/DC stage and DC/AC stage design	100%
M 1.2 Simulation verification of design	100%
M 1.3 Local controller, APS and gate drive hardware fabrication	100%
M 1.4 DC/DC and DC/AC power stage hardware fabrication and subcomponent demonstration	100%

BP2 Milestones

Milestones & Subtasks Description	Schedule	% Progress toward Completion
M 2.1 Closed-loop experimental validation of IPS DC/AC stage	2021.9.16-2021.12.15	100%
M 2.2 IPS system-level advanced features validation	2021.12.16-2022.3.15	30%

Accomplishment Summary and Future Work

- 50kW IPS hardware built and tested at 50kW in open-loop mode.
- Advanced features of AGD and P&D functions has been verified experimentally
- Grid-tied closed-loop experiments have been tested successfully
- The communication between SUPER and IPS local controller has been implemented and tested.

- The LVRT experiments, the communication between IPS controller and gate driver, the integration of DC/DC stage and DC/AC stage will be tested in 2022.

Impact/Commercialization

- Provide a general solution to improve reliability and resilient grid integration of renewable energy with storage.
- Apply not only to next generation WBG device based grid-tied power electronics but to traditional grid-tied power electronics as well.
- Enable the revolutionary approach to integrate renewable energy based on SUPER+IPS.

IP STATUS

NA.

Publications

- "An Intelligent Gate Driver With Self-diagnosis and Prognosis for SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE),2021.*
- "An Integrated Active Gate Driver for SiC MOSFETs," in *Proc. IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2021.*
- "SiC-Based Intelligent Power Stage with Device Prognostics/Diagnostics and ZVRT Capability for Smart Universal Power Electronic Regulators (SUPER) Application," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC), 2022.*
- "An Integrated Active Gate Driver for Half-bridge SiC MOSFET Power Modules", in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC), 2022.*

Risks and Mitigation Strategy

- Supply chain shortage will delay the 2nd hardware unit development.
- Redesign the IPS to use available components but will be time-consuming.

THANK YOU

This project was supported by the Department of Energy (DOE) - Office of Electricity's (OE), Transformer Resilience and Advanced Components (TRAC) program led by the program manager Andre Pereira & Oak Ridge National Laboratory (ORNL)

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Acronyms

SUPER: Smart Universal Power Electronic Regulator

IPS: Intelligent Power Stage

GD: Gate Drive

AGD: Active Gate Drive

P&D: Prognosis and Diagnosis

LVRT/ZVRT: Low-voltage ride through/zero-voltage ride through

APS: Auxiliary Power Supply

EMI: Electromagnetic Interference

CM: Common-mode