DOE Office of Electricity TRAC

Peer Review

U.S. DEPARTMENT OF ENERGY | OFFICE OF ELECTRICITY

Intelligent Power Stage (IPS)

PRINCIPAL INVESTIGATORS

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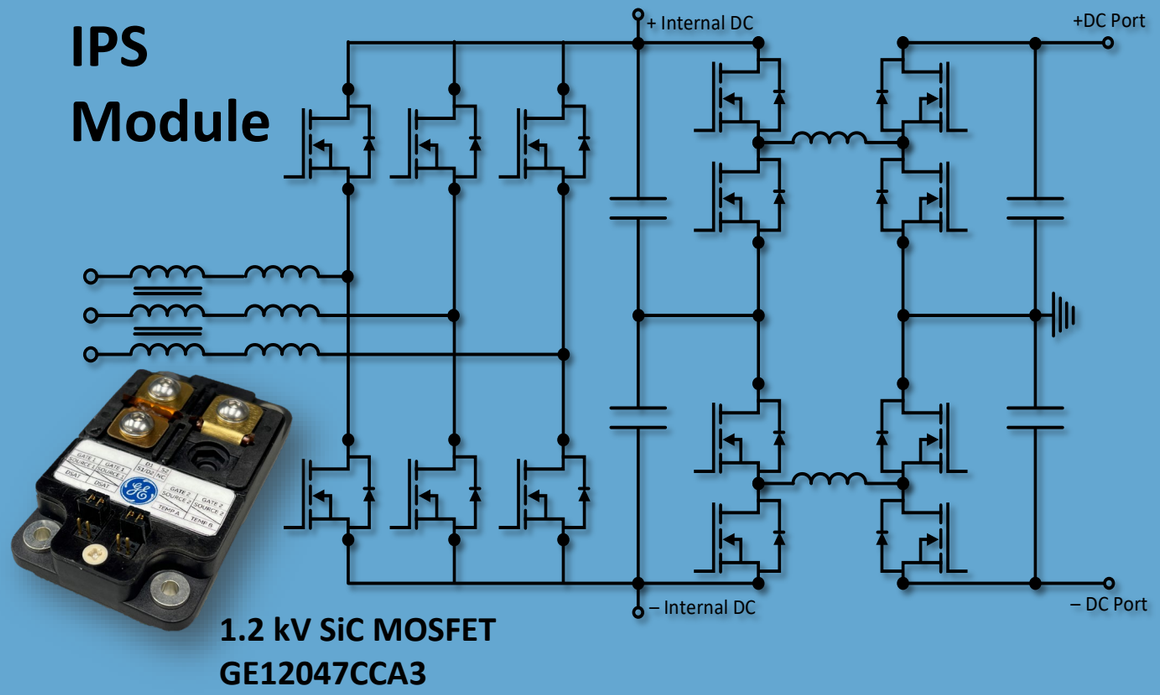
PROJECT SUMMARY



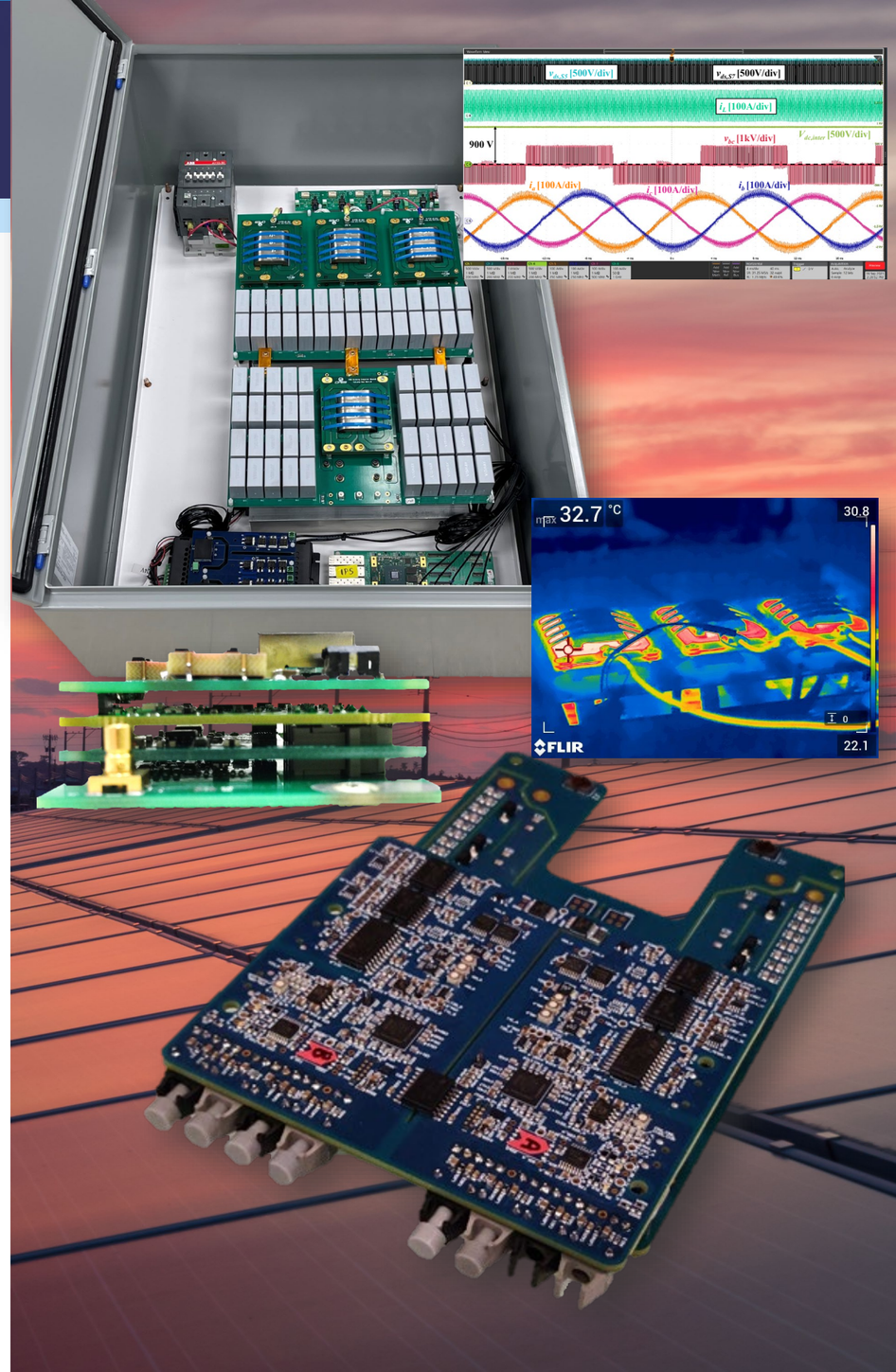
Goal: Development of intelligent power stage (IPS) three-phase ac-to-dc power converter module with advanced power processing, monitoring, and diagnostic capabilities based on high efficiency Silicon-Carbide power semiconductor devices.

Background:

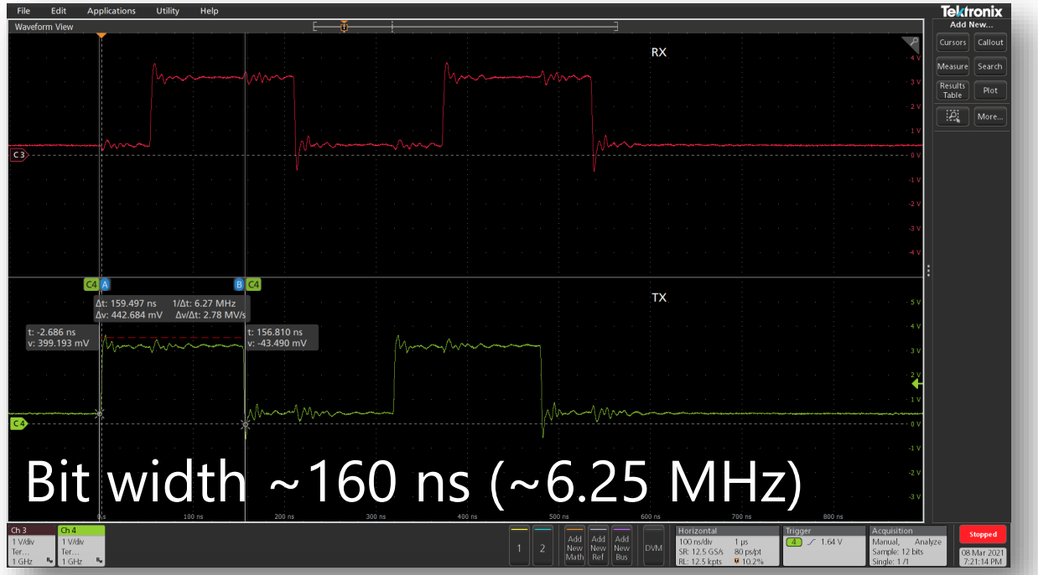
- Future grid-specific power electronics remains hindered by the strong industrial reliance on custom-design power converters
- Modular, IPS-based solutions seek to unleash the development of grid power electronics enabling their flexible, scalable integration featuring advanced power processing, monitoring and diagnostics capabilities

Innovations

- Topology: 2-level ac-dc converter with split dc-bus and cascaded 3-level buck-boost dc-dc converter
- Ancillary Circuitry: fiberoptic communication network (25 Mbps) between controller, gate-drivers (GD) and sensors; auxiliary power network with high dv/dt immunity (>100 V/ns); minimized EMI susceptibility
- Monitoring and diagnostics: GD-integrated SiC MOSFET Rdson, Tj measurement and dc-bus voltage; dc-bus capacitance measurement based on I_d and off-state V_{ds} measurements

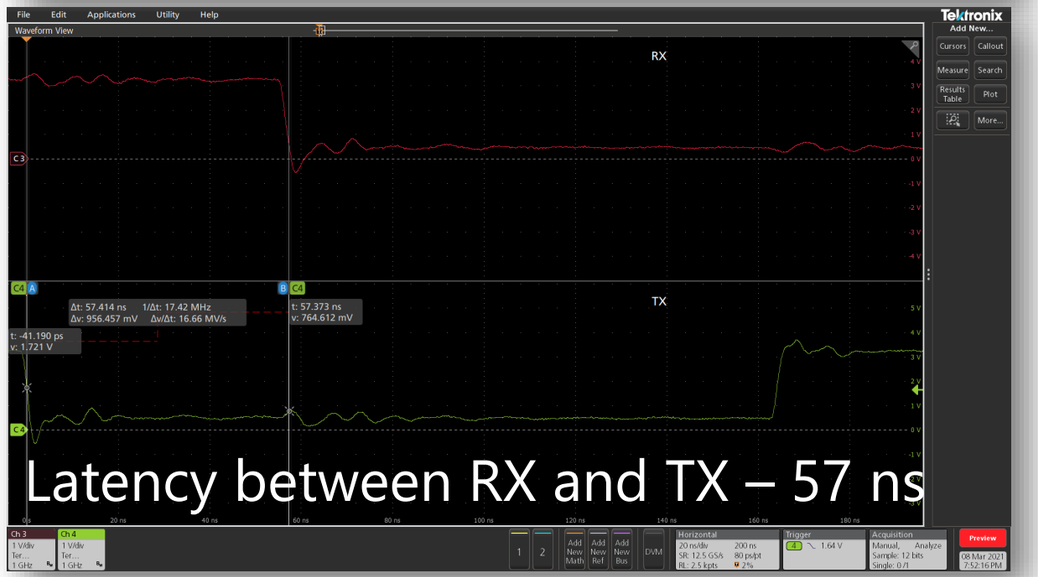


SUPER to IPS Communication Tests (UART 6.25 Mbps)

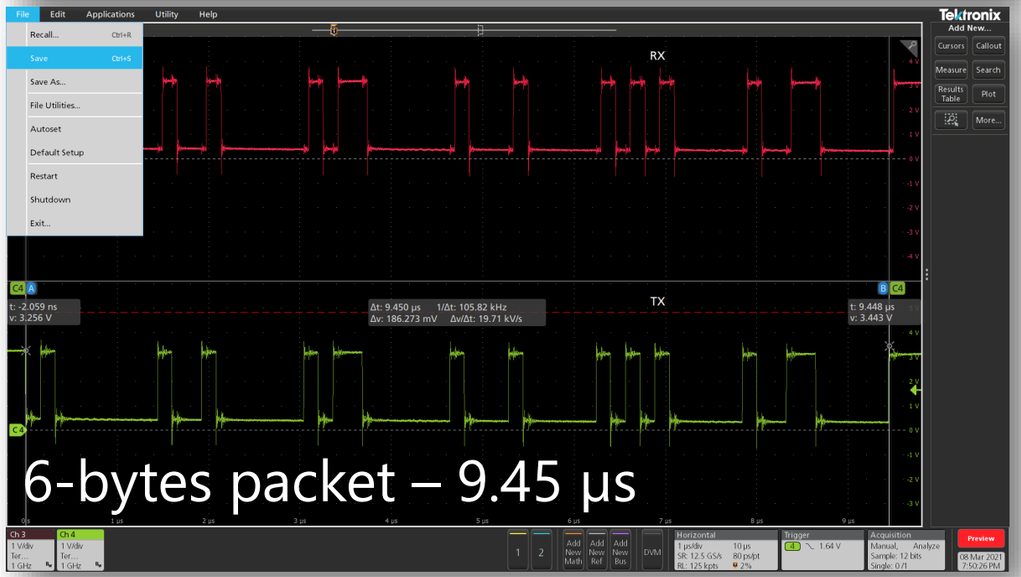


Bit width ~160 ns (~6.25 MHz)

5-byte packet – 7.84 µs



Latency between RX and TX – 57 ns



6-bytes packet – 9.45 µs

IPS Internal Communication Protocol

- Based on 10BASE-T ethernet standard
- Physical layer: Plastic Optical Fiber
- Data rate: 25 Mbps
- Packet structure: inspired by MODBUS

Data Packet Structure

Part	Length - Subpacket
Preamble	4 bytes
Payload	4 bytes – SYNC
	4 bytes - CTRL
CRC32	4 bytes

Difference between Custom protocol and 10BASE-T

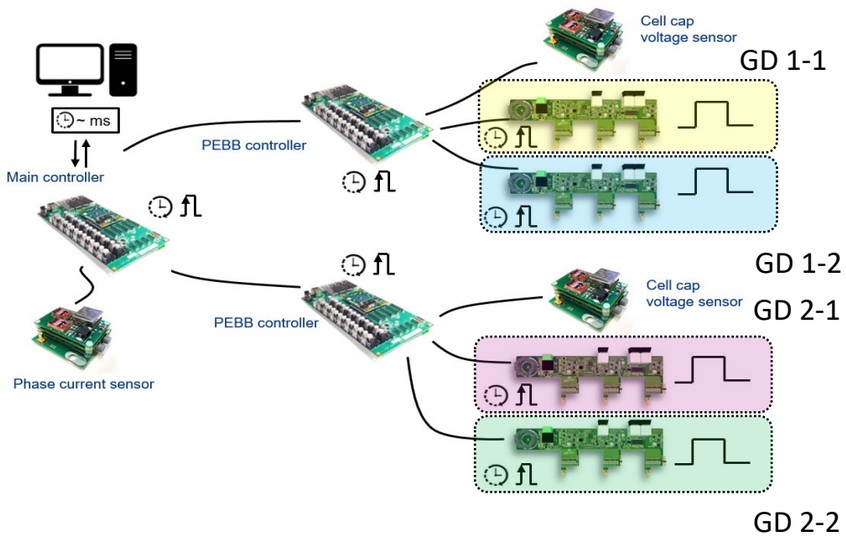
	10BASE-T	Custom protocol
Speed	10 Mbps	25 Mbps
Preamble + SOF	7+1 octets (64 bit)	3+1 octets (32 bit)
Payload/Packet	**64–1,552 octets (variable size)**	**12 octets (96 bit, fixed size)**
Frame check sequence	32-bit CRC	32-bit CRC
Encoding/Decoding	Manchester	Manchester

SYNC/CTRL related block

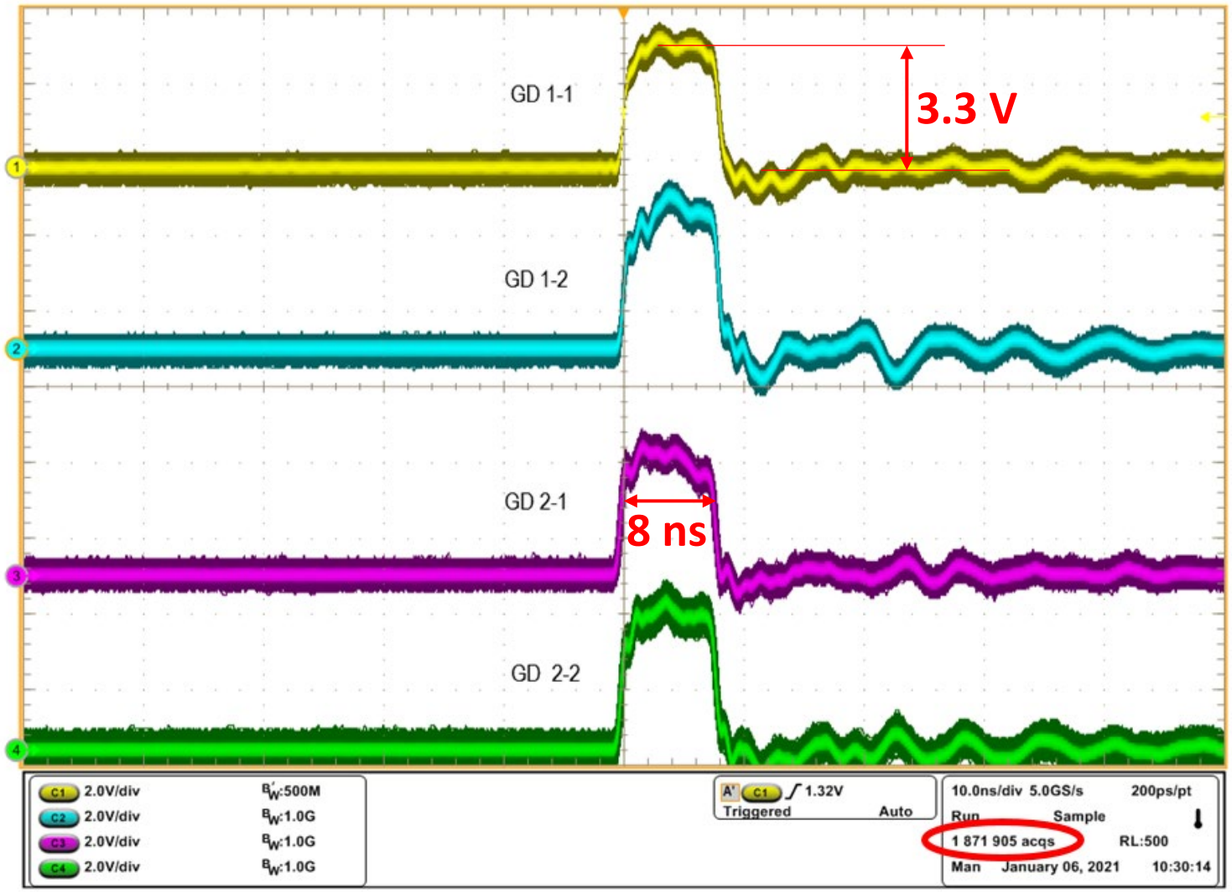
Value	Length
Function	8 bits
Data	24 bits

Sub-Nanosecond Synchronization Capability

- < 1 ns synchronization jitter achieved with physically distributed clock
- Timers in GD and Controller are synchronized using PTP (IEEE 1588)



Benchmark System



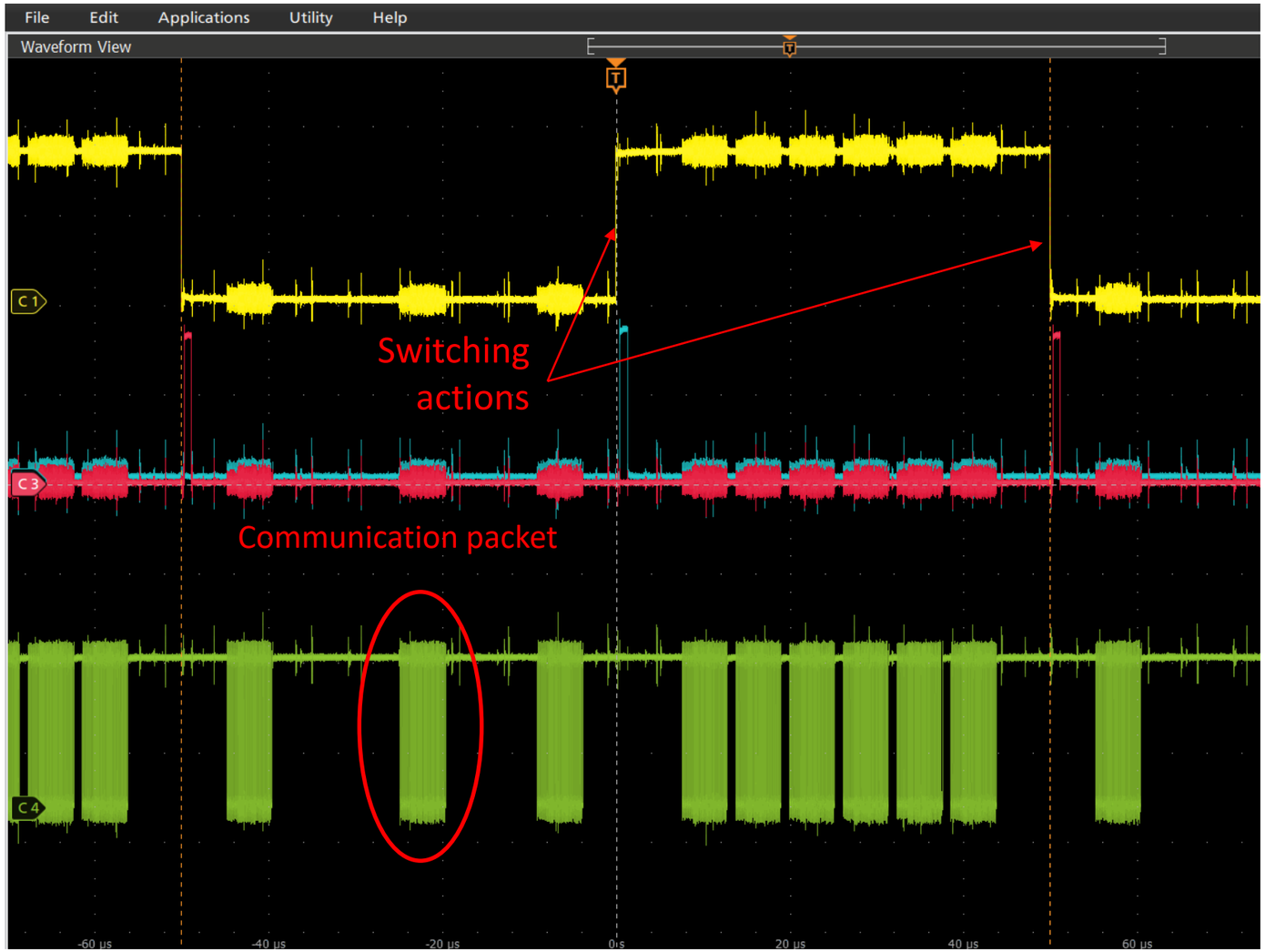
Enhanced Immunity to SiC-Generated EMI

Challenge

- Fast switching frequency and dv/dt rates of SiC devices heighten EMI emissions disrupting communications

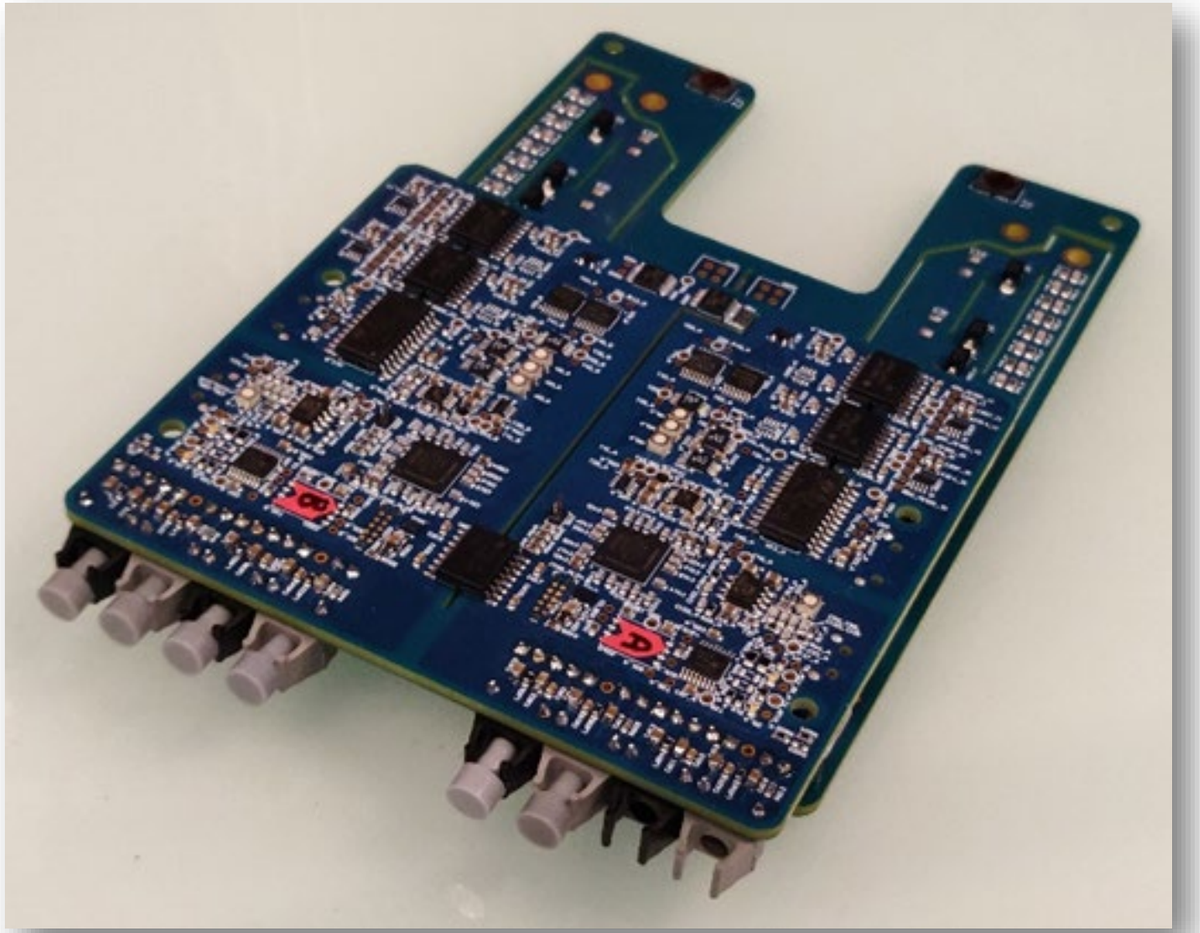
Solution

- Switching-proof communication protocol
- Data packets are synchronized and not transmitted during turn-on and turn-off SiC MOSFET switching events



Enhanced Gate-Driver for SiC MOSFET Module

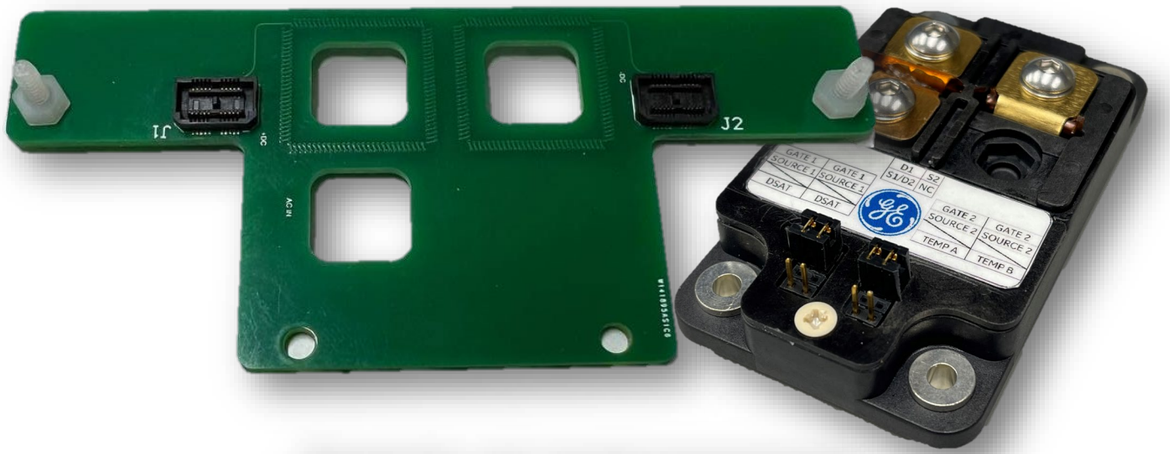
- Drives half-bridge 1.2 kV SiC MOSFET module
- Modular, triple board design:
  - Digital, analog, and interface boards
- Double MAX10 FPGA controllers
- Integrated sensors
  - Top and bottom I_d, V_{dson}, V_{dsoff}, substrate temperature
- Communication protocol used for PWM, control, status, and transmission of measured data back to controller
- Dv/Dt immunity: 100 V/ns

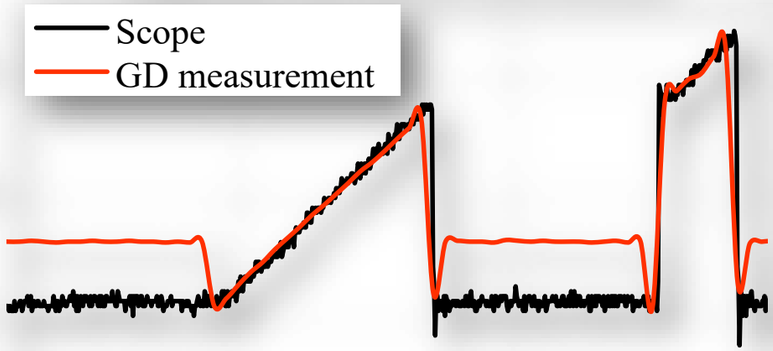


Gate-Driver-Integrated I_d and V_{dson} Sensors

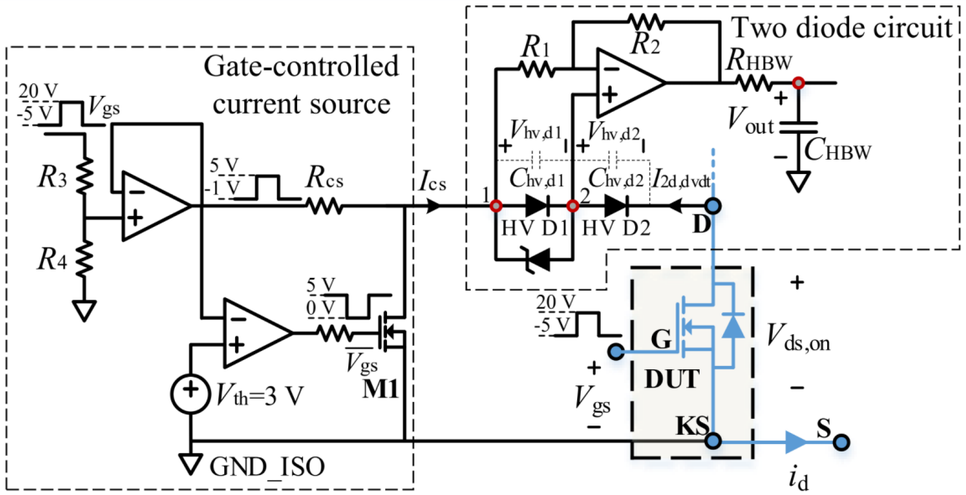
I_d Sensor, Top and bottom Current (15 MHz Bandwdith)

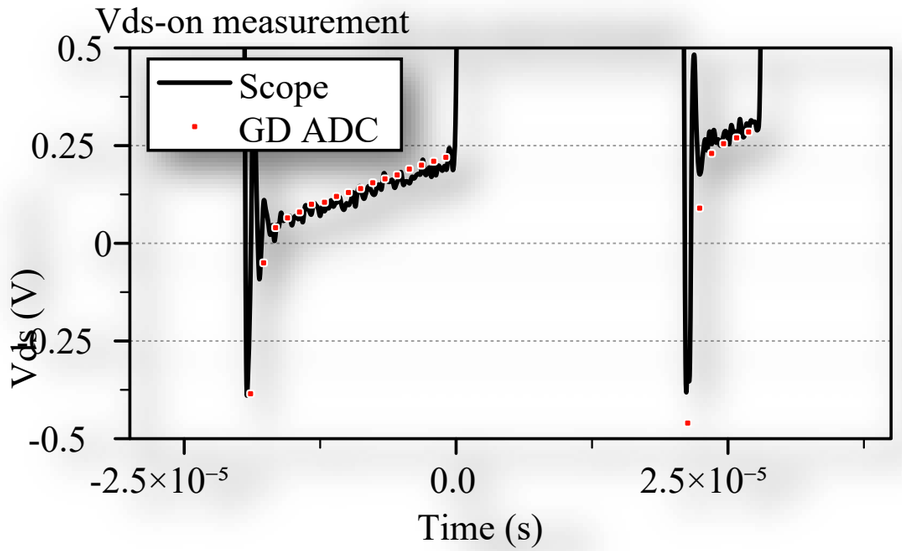
Double Rogowski Coil PCB





V_{dson} Sensor with 5 mV Resolution

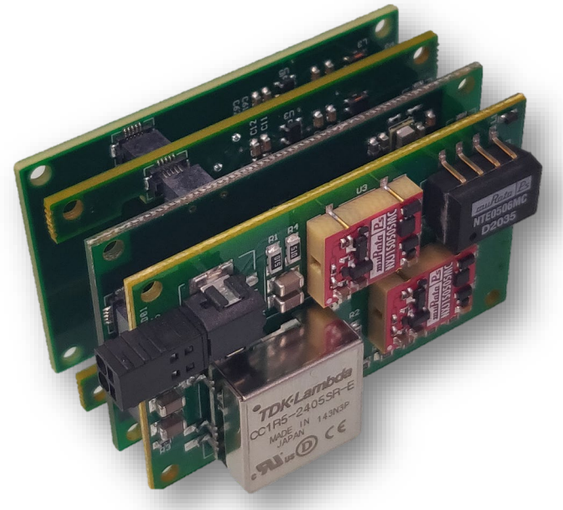


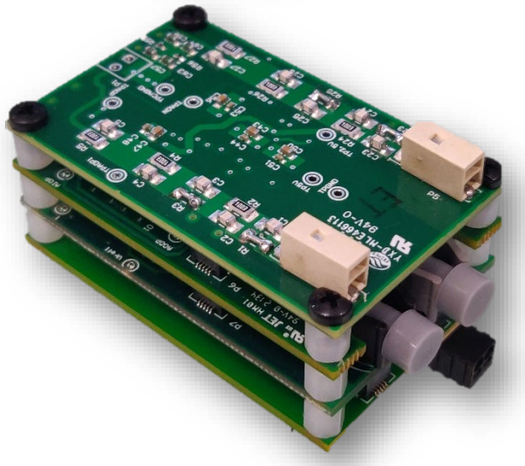


- I_d sensors enable phase-current reconstruction
- V_{dson} and I_d sensors enable T_j estimation

Digitally-Interfaced Sensing Network

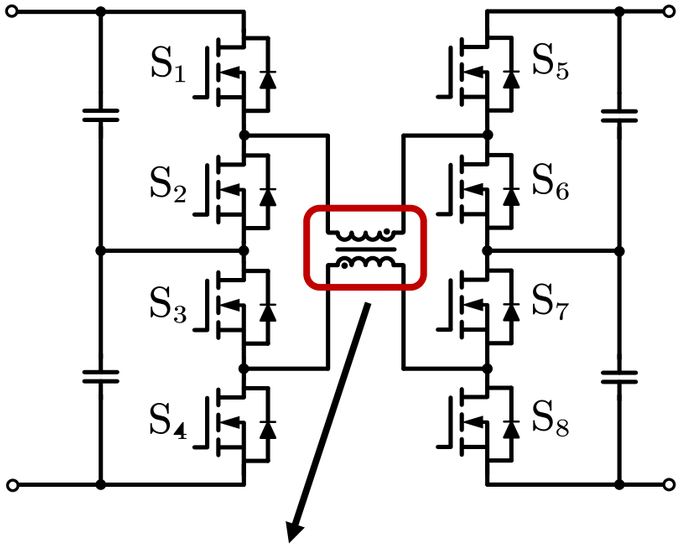
- Four-board, modular sensor design
  - Digital board, signal conditioning, power supply, and sensor interface boards
- MAX10 FPGA controller
- Sensor interface boards:
  - Voltage, current and temperature
- Communication protocol: IPS internal protocol based on 10Base-T
- Sampling rate: 2 Msps
- Transmission rate: 200 ksps



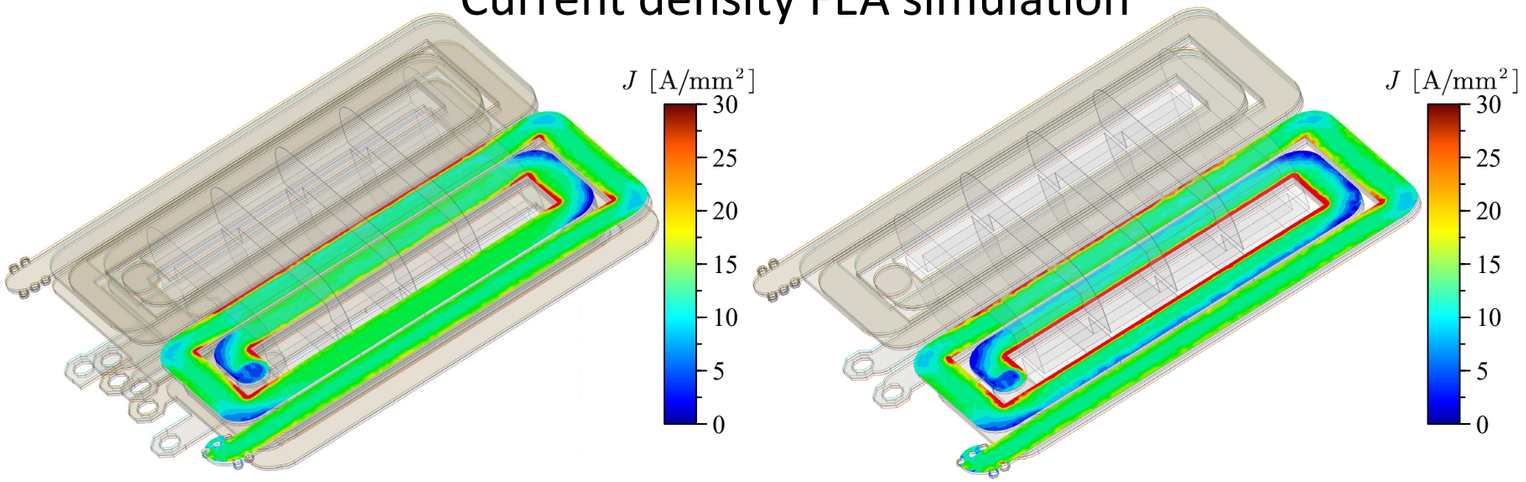


PCB-Winding Coupled Buck-Boost DC Inductor

- Low-profile design (3.5 kVA/in^3)
- Simple assembly with commercial AMCC core
- Heavy copper PCB (15 oz Cu, 50 kW, 90 A dc)
- Double PCB winding design to educe fringing effect
- ➢ Continuous and discontinuous current modes

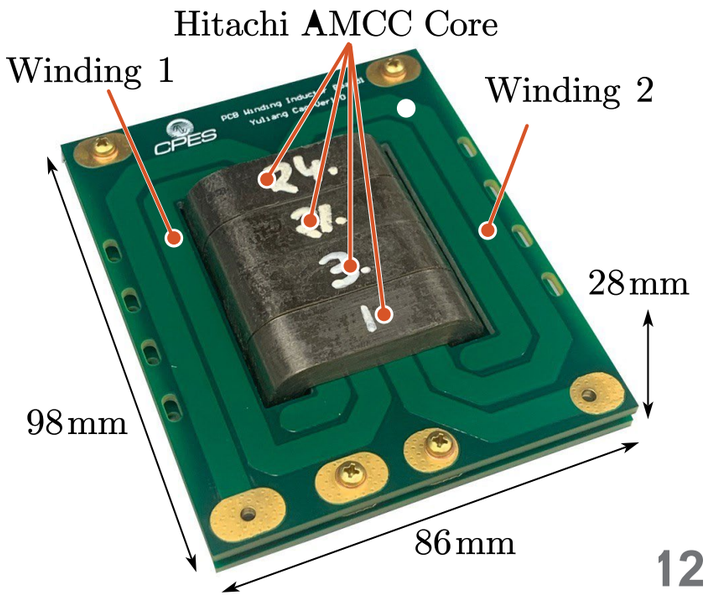


Current density FEA simulation



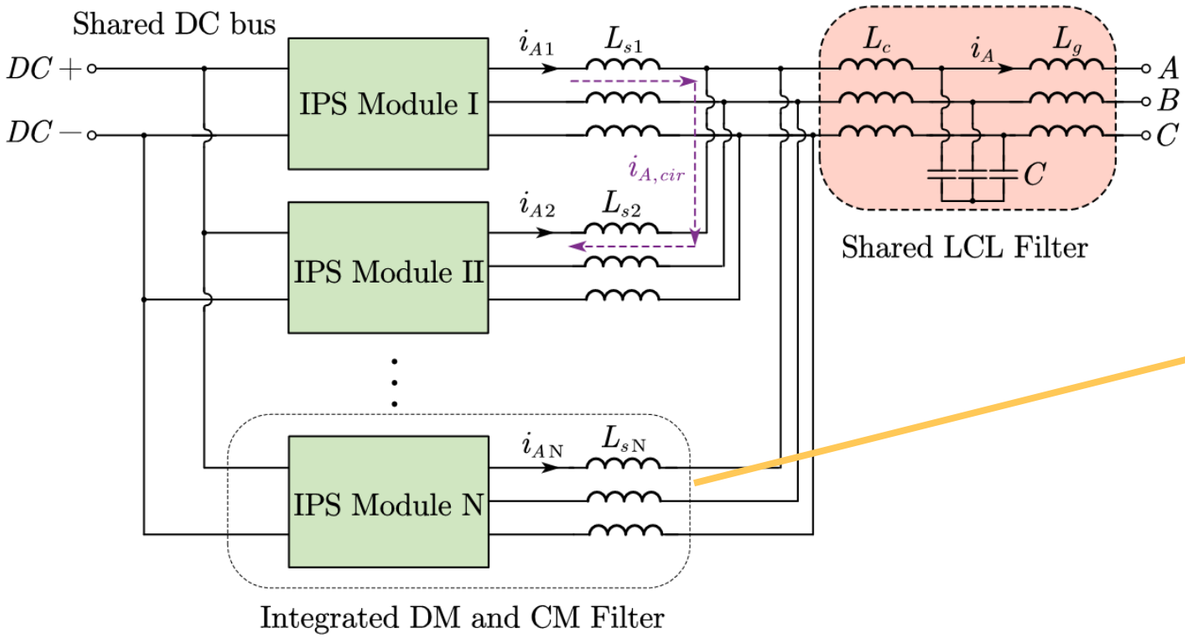
Two-board design (even distribution)

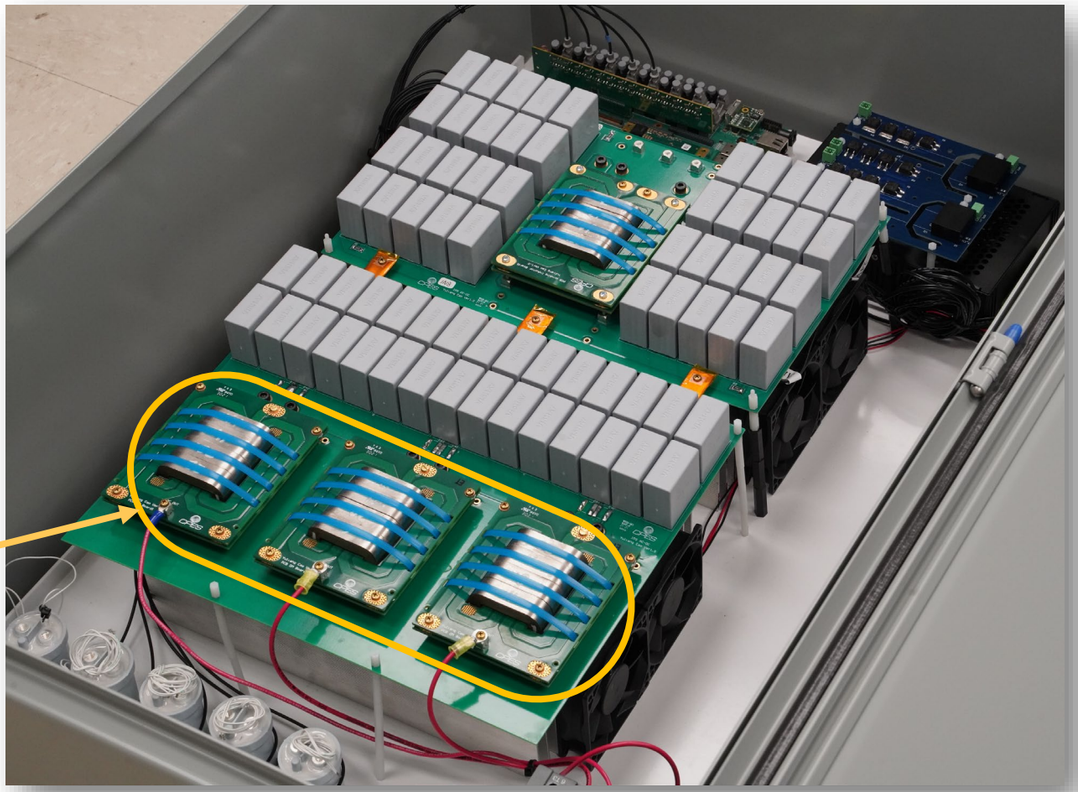
One-board design



PCB-Winding Three-Phase Boost Inductors

- Low-profile design (2 kVA/in^3)
- Simple assembly with commercial AMCC core
- Heavy copper PCB (12 oz Cu, 75 kVA, 90 Arms)
- Integrated in IPS to mitigate circulating current

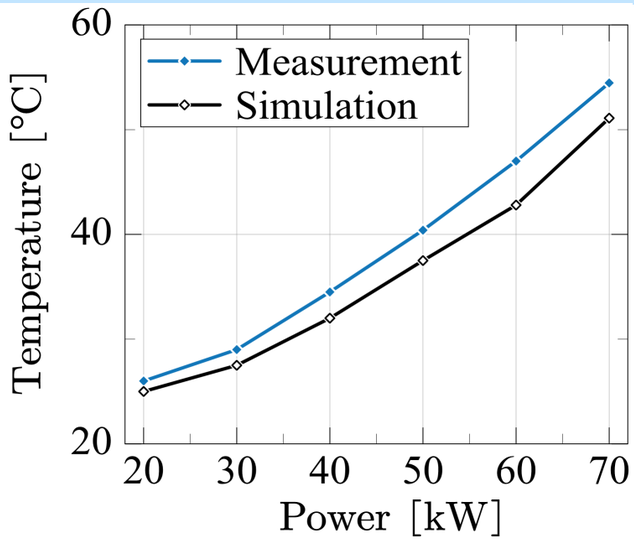




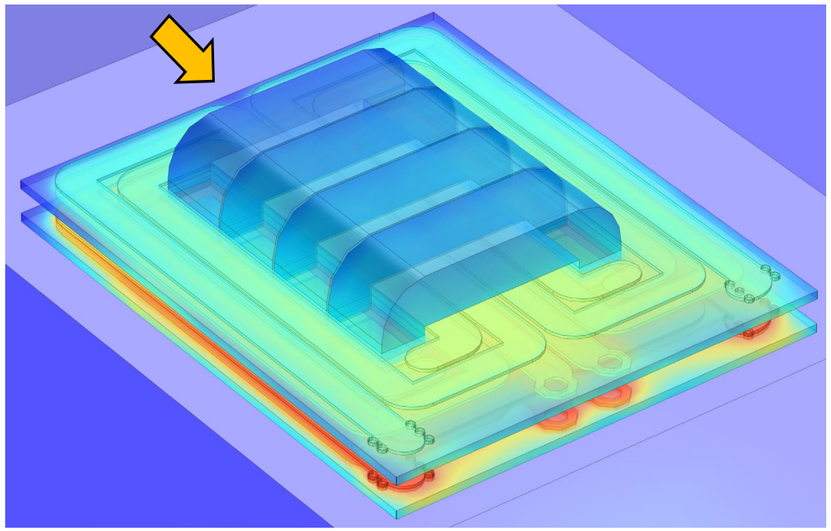
Three-Phase Boost Inductors

Thermal Performance of PCB-Winding Magnetics

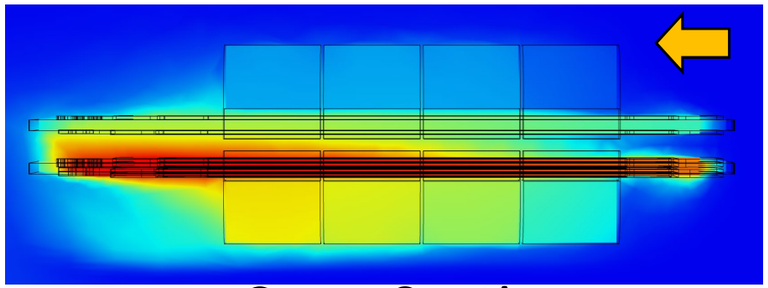
- Dc coupled inductor and ac three-phase boost inductor
- Analytic and FEA simulations validated experimentally
- Maximum temperature limited to 60 °C



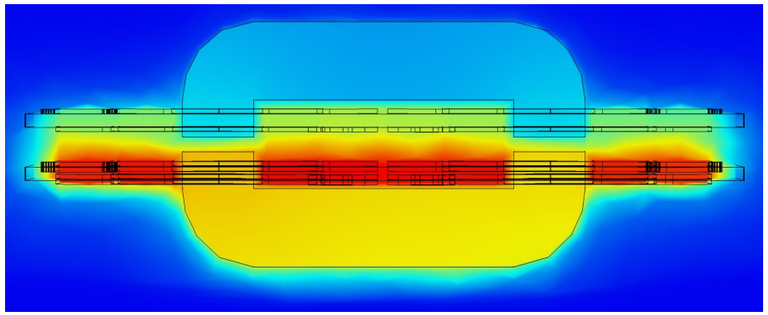
FEA simulation

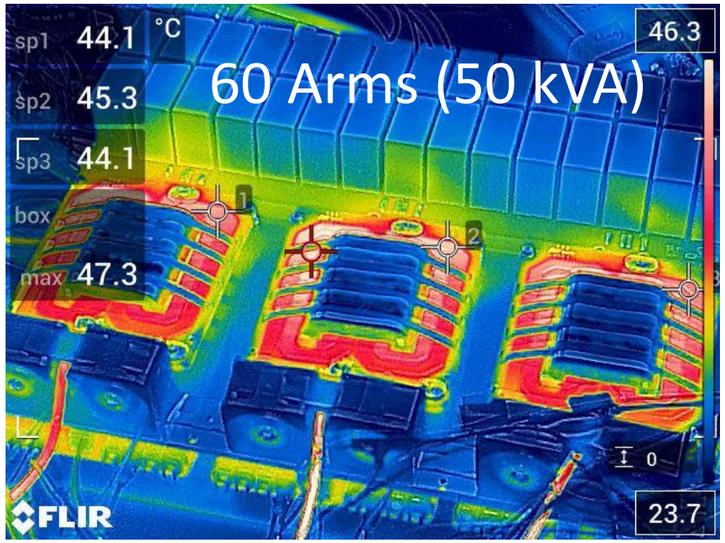


Side view



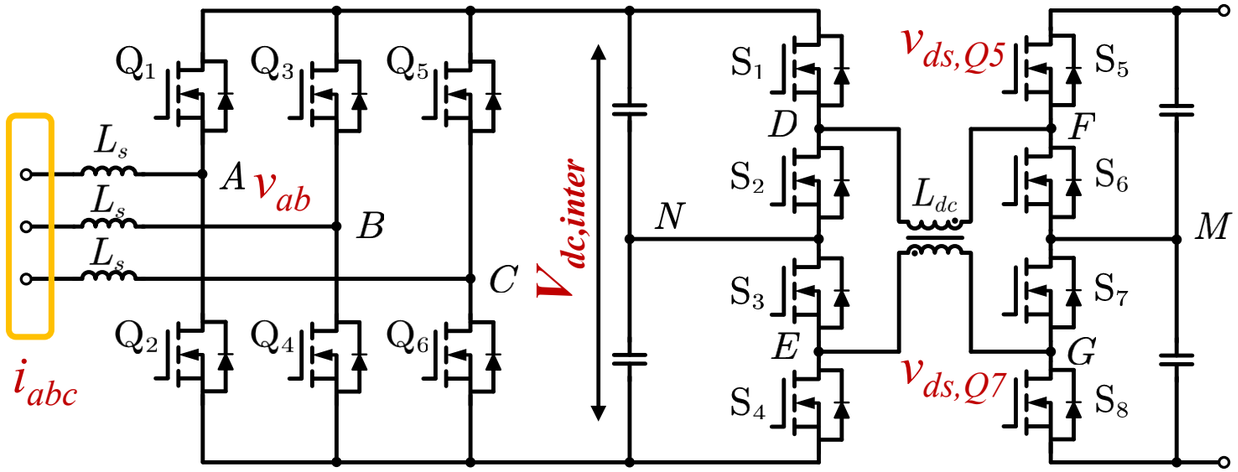
Cross Section

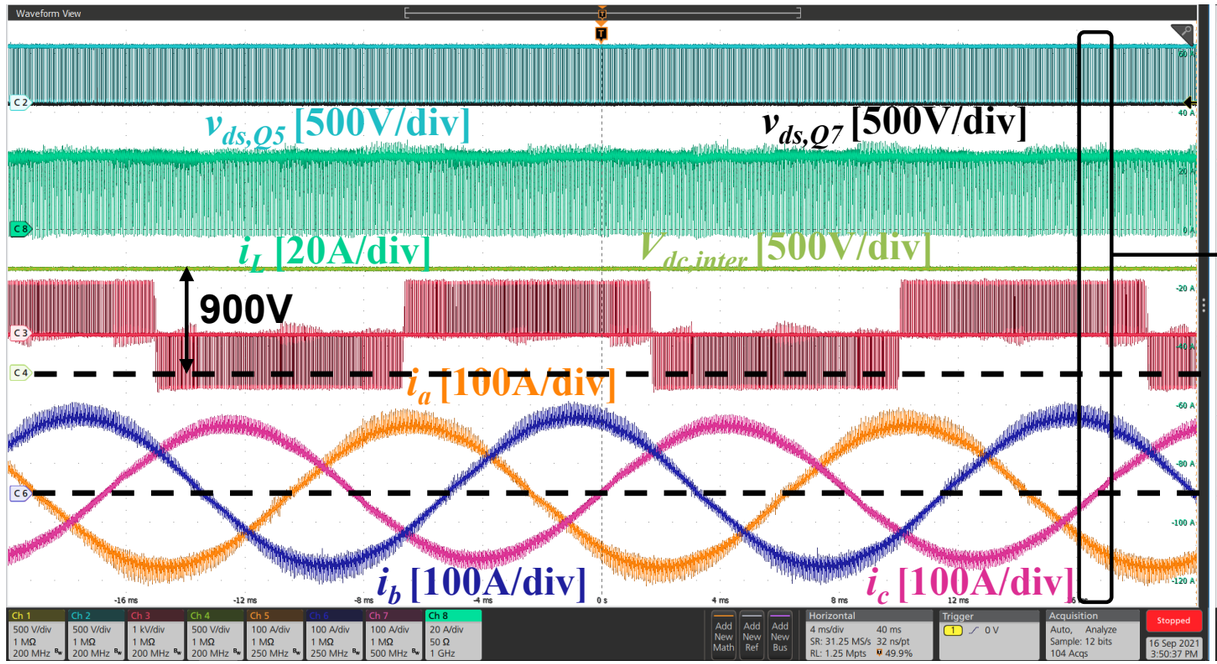


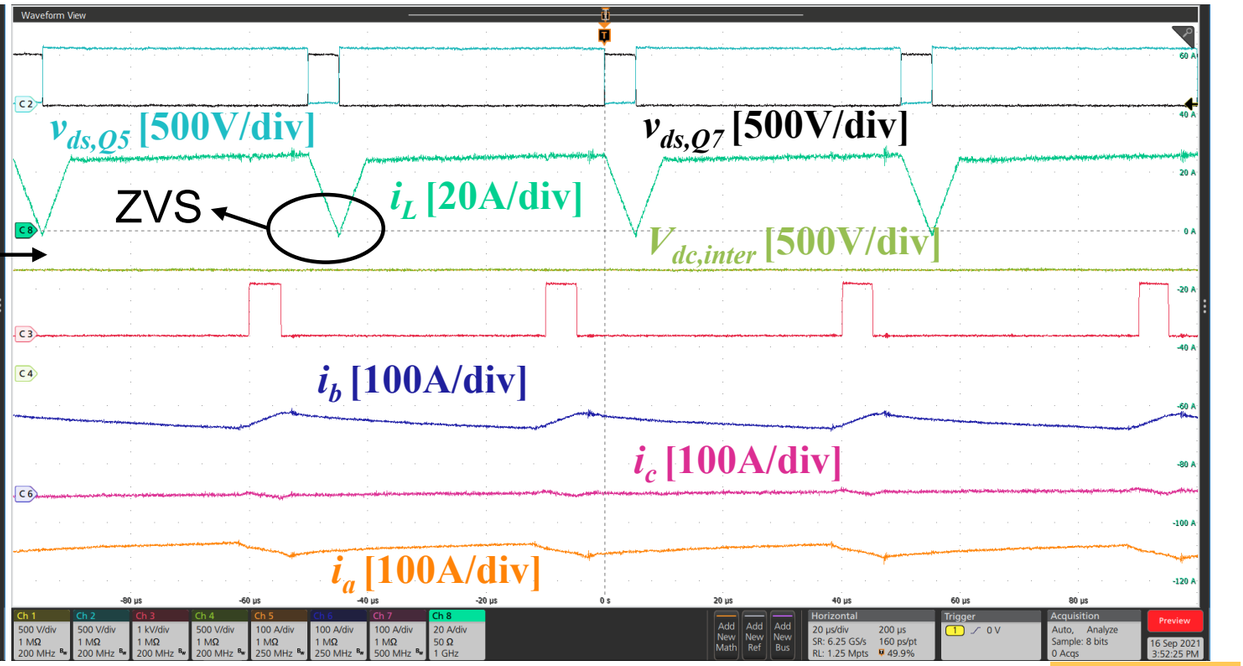


IPS Nominal Power Testing

- Nominal power rating test (75 kVA)
- Zero-voltage-switching for all dc-dc stage semiconductors
- Quadrangular current control scheme







Milestones Update

- *BP1 Milestones*

✓ M1.1 "IPS electrothermal design meets target specifications"

✓ M1.2 "Gate-driver unit is built and functionally tested"

✓ M1.3 "Auxiliary power supply are built meeting their specifications, and PCB-based dc-bus planar structures are built"

✓ Go/No-Go "IPS power stage subcomponents are demonstrated"

- *BP2 Milestones*

- M2.1 "Full power testing of IPS validated. Prototype P1 ready for testing at ORNL" [completion: 85 %]
- M2.2 "Filters are built and ready for testing. Digital sensors (V, I, T) are built and ready for testing, and digital control system communication is tested" [completion: 95 %]

➢ M2.3 and Go/No-Go due in July and September 2022

Risks Mitigation Strategy

- Supply chain challenges has led to widespread shortage of electronic components and longer component manufacturing timeframes leading to IPS development and construction delay
  - All circuit designs were revised to replace key parts that were not available, and had lead times of months up to a year
  - Scavenged components with suppliers around the world

- Acquisition of SiC MOSFETs was delayed 4 months due to contractual barriers between GE and Virginia Tech, which is bound by VA state law

Future Work

- Task 2.1 Integration and thermal testing of IPS-1
  - Hardware integration and testing of IPS-1 unit and EMC verification
- Task 2.2 Advanced functionality
  - Program Iphase, Rdson and Tj temperature estimation
  - Program dc-bus capacitance Cdc value estimation
- Task 2.3 Integration, thermal testing and qualification of IPS-2
  - Hardware integration of IPS-2 unit using enhanced gate-drivers
  - Testing and demonstration of Iphase, Rdson, Tj, and Cdc estimation
- Task 2.4 Advanced functionality update
  - Program Iphase, Rdson and Tj temperature estimation in IPS-1
  - Program dc-bus capacitance Cdc value estimation in IPS-1
  - Testing and demonstration of Iphase, Rdson, Tj, and Cdc estimation

Impact & Commercialization

IMPACT

- Modularity of IPS concept combined with automated-manufacturing-oriented design of proposed IPS will expectedly favor multi-supplier IPS market development attaining economy of scales benefits

- IPS internal digital control and communication network will demonstrate a viable alternative to operating in the harsh EMI environment generated by SiC power semiconductors (main collateral effect of this technology)
  - This is critical for modular systems as the EMI generated is directly proportional to the number of modules used, in this case IPS units

Impact & Commercialization

PUBLICATIONS

- "A 50kW Planar PCB-based Heavy Copper Coupled Inductor for FSBB," submitted to ECCE 2022.
- "Real-Time Network Protocols for GD Communication and Control," submitted to ECCE 2022.

IP STATUS — *Invention disclosures in preparation*

1. "Buck-boost dc-dc converter high-efficiency and low EMI emissions current control scheme"
2. "IPS control and sensing communication network with sub-nanosecond synchronization"

THANK YOU

This project was supported by the Department of Energy (DOE) - Office of Electricity's (OE), Transformer Resilience and Advanced Components (TRAC) program led by the program manager Andre Pereira & Oak Ridge National Laboratory (ORNL)

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Acronyms

SiC: Silicon-Carbide, semiconductor material

MOSFET: metal-oxide field-effect transistor

GD: Gate-driver, i.e., electronic circuit that controls the turn-on and turn-off of SiC power transistors

PTP: Precision time protocol

Mbps: mega bits per second

Msps: mega samples per second

PCB: printed circuit board

EMI: electromagnetic interference