IPS Hardware Prototype Development

PRINCIPAL INVESTIGATORS
Dr. Yue Zhao, Associate Professor
Dr. Juan Carlos Balda, University Professor
University of Arkansas
The Objective of this project is to develop and demonstrate the intelligent power stage (IPS), i.e., an interoperable plug-and-play power stage with embedded intelligence and online health monitoring capability. Through the standardized communication interface, IPS can provide sufficient component level status information to interact with the Smart Universal Power Electronics Regulator (SUPER). The IPS developed in this project consists of an isolated DC/DC converter stage, a three-phase inverter stage, self-maintained auxiliary power supplies, sensors and a powerful control platform with communication channels.
Innovations – Overview

- **IPS**: Intelligent Power Stages
- **SUPER**: Smart Universal Power Electronic Regulators

**External Parameter Identifications**
Interoperability, Situation Awareness
- External LCL parameter estimation.

**Onboard Health Monitoring and Prognosis**
Reliability, Resiliency (Internal)
- Junction temperature estimation for the SiC power modules used in IPS;
- DC link capacitance identification.
- Capacitor end-of-life (EOL) indication using estimated DC link capacitance.

**Advanced Gate Driving (AGD)**
Reliability, Efficiency, Performance
- AGD with optimized multi-stage turn-off;
- Capability to manipulate voltage overshoot, switching loss and dv/dt.

**IPS Controller Platform**
Interoperability, Performance
- Standardized communication interface;
- Optimized layout w. enhanced noise immunity.

**Diagrams**
- UA IPS
- Isolated DC/DC
- DC Link
- Inverter
- Controller w/ Std. Comm.
- AC voltage references \(m_a, m_b, m_c\)
- IPS status/health, & commands, contactor status, measurements

---

4
Innovations – Overview

- In addition to the **validation & demonstration** of the advanced features ...
LCL Parameter Identification

- LCL filter is critical to the performance of the IPS;
- LCL filter, which is part of SUPER, is external to the IPS;
- The knowledge of LCL parameters can be used to enhance the control performance and for the purpose of state estimation.
Innovation Update

- LCL Parameter Identification – Experimental Studies


Innovation Update

- DC Link Capacitance Estimation

- The control gains of the DC/DC stage are designed based on the capacitance in the HV DC link;
- SUPER may add additional capacitance to the HV DC link to enhance the system stability;
- If DC link capacitance (IPS internal + SUPER external) can be estimated, the control gains can be updated online to improve the DC bus voltage regulation;
- The estimated capacitance can be used as an indicator for the end-of-life (EOL) of the capacitors.
• DC Link Capacitance Estimation – Experimental Studies

DC/DC Converter Testing Setup

Typical Results for Capacitance Estimation

\[ C_{est,ss} = 382 \, \mu F \]
Innovation Update

- Module Junction Temperature Estimation

Power Stage Thermal Characterization Setup

Block diagram for $T_j$ estimation

Voltage drop across external gate resistance

- Volt./Temp. (°C) sensitivity analysis

Voltage drop across external gate resistance

- Averaged Voltage Drop Peaks
- Linear Trendline

Linear: $y = -0.003973x + 15.33$

$R^2 = 0.9912$
Innovation Update

- Digital Gate Driver Demonstration for 1.7kV SiC Modules

DGD Core with Custom Adaptor Board

Typical Results without 2-level turn-off

CIL Setup for 1.7kV CREE Module

Typical Results with 2-level turn-off

Impact to Voltage Overshoot

Impact to Turn-off loss
Innovation Update

- IPS Controller Platform
Innovation Update

- IPS Control and Data Architecture Validation with Emulated SUPER controller

![SUPER TX](image1)

![IPS RX](image2)

Controller Test Setup

Tx/Rx Modulation Index Profile

Inductive Load Test Setup for UA IPS

60 Hz line voltage under 1 kV DC bus
Innovation Update

- Status of the IPS Hardware Development & Testing

Test Setup for DC/DC Converter

1 MW
1.5kV Supply

Test Setup for Inverter Stage

750 kW
Load Bank
Innovation Update

- Close-loop control for DC/DC Converter

![Graph showing output voltage and reference voltage with a step change from 800 V to 1000 V.](image-url)
Innovation Update

• Continuous Power Testing for Inverter Stage @ 50kW (1kV DC bus, 480V AC)
Innovation Update

• Continuous Power Testing for Inverter Stage @ 75kW (1kV DC bus, 480V AC)
Innovation Update

- Thermal Validation

![Graph and Images related to thermal validation](image-url)
Innovation Update

• Milestone update
  • Completed the design and validation of hardware subcomponents in IPS, including DC/DC, Inverter, Gate Drivers, and Controller.
  • Implemented and validated various advanced features using the IPS hardware, including LCL parameter identifications, DC link capacitance estimation, module junction temperature estimation, communications, etc.
• Summarize the risks and mitigation strategy
  • COVID
  • Components long lead time
Innovation Update

BP2 Tasks

• Task 2.1 – IPS System Integration
  • Cabinet level integration
• Task 2.2 – IPS System Demonstration at University of Arkansas
  • Basic and advanced inverter functionalities
• Task 2.3 – Testing and Demonstration with ORNL
  • Grid functions
  • Integration and demonstration with SUPER
Impact/Commercialization

• The **advanced features** developed for IPS will enable its situational awareness, enhance the interoperability and system reliability.
• Further with the **standardized architecture**, the IPS can be easily connected to the generic testing environment or standardized SUPER to demonstrate advanced grid functionalities.
THANK YOU

This project was supported by the Department of Energy (DOE) - Office of Electricity's (OE), Transformer Resilience and Advanced Components (TRAC) program led by the program manager Andre Pereira & Oak Ridge National Laboratory (ORNL)
IPS: Intelligent Power Stages
SUPER: Smart Universal Power Electronic Regulators