SSPS 1.0: Hardware Development

Smart Universal Power Electronics Regulators (SUPERs) & Intelligent Power Stages (IPSs) for SSPS 1.0

PRINCIPAL INVESTIGATOR
Dr. Madhu Chinthavali,
Leader – Power Electronics Systems Integration (PESI) Group,
Distinguished R&D Staff Professional,
ORNL
Demonstration of advanced and standardized power electronics interfaces (SUPER & IPS) for the grid

- Universal design for grid interfaces – Interfaces that can be tied to assets or loads with changes only to the software layer
- Grid interfaces with advanced & intelligent features – Autonomous operation, online health monitoring & decision-making capability
- Scalable and interoperable design with standardized interfaces
- IPSs with advanced sensing techniques, algorithms capable of estimating the health of at least 2 components
DOE PROGRAM OFFICE:
OE – Transformer Resilience and Advanced Components (TRAC)

FUNDING OPPORTUNITY:
AOP

LOCATION:
Knoxville, Tennessee

PROJECT TERM:
07/01/2020 to 09/30/2022

PROJECT STATUS:
Ongoing

AWARD AMOUNT (DOE CONTRIBUTION):
$9,000,000

AWARDEE CONTRIBUTION (COST SHARE):
$0

PARTNERS:
Consortium of University Partners
ORNL - SUPER architecture, functionalities & advanced algorithms, IPS (developed by ORNL), integration of IPSs from partners

Madhu Chinthavali
Power Electronics System Architecture

Brian Rowden
Hardware design and prototyping

Steven Campbell
System Integration & Testing

Rafal Wojda
Magnetics Design

Jonathan Harter
Hardware development

Radha Sree Krishna Moorthy
Project Lead & Software framework development

Aswad Adib
SUPER and IPS simulation

Jang Euk
Fiber Optic Interface Development
University Partners – Library of IPSs

- The Ohio State University, Columbus, Ohio: Dr. Jin Wang
- Virginia Polytechnic Institute and State University (Vtech), Blacksburg, Virginia: Dr. Rolando Burgos
- Florida State University (FSU), Tallahassee, Florida: Dr. Helen Li
- The University of Texas at Austin, Texas: Dr. Alex Huang
- The University of Arkansas (UARK), Fayetteville, Arkansas: Dr. Yue Zhao
- The State University of New York (SUNY) at Stony Brook, New York: Dr. Fang Luo
- The University of North Carolina at Charlotte (UNCC), North Carolina: Dr. Babak Parkhideh

14 Professors/PIs, 6 Postdocs, 26 Students
SSPS Hubs & Nodes – An autonomous grid entity capable of power and information exchange serving as an interface between the grid and end user.

SSPS concept will enable hierarchical control, communication, optimization, protection and intelligence

Architecture realized by fundamental building blocks – modular, interoperable, scalable, autonomous & intelligent grid tied systems

**“Solid state power substation Technology Roadmap”, U. S DOE Office of Electricity, Transformer Resilience and Advanced Components (TRAC) Program, Jun. 2020.**
Innovation: SUPER

SUPER Features

1. Interoperability
   - Easy integration & reduction in BOS costs

2. Embedded intelligence & decision-making capability with a flexible scalable platform
   - Improved voltage profile at the point of connection (POC)
   - De-rated/continuous operation during failure events

3. Embedded online health monitoring system – Diagnostics/Prognostics
   - Allows maintenances to be pre-planned
   - Can prevent the loss of the inverter from affecting the overall system
   - Increases lifetime
   - Data for offline learning algorithms

4. Cyber-physical security
   - Improved protection against cyber threats

5. Self contained intelligent power stages
   - Decouples parasitics and noise loops
   - Additional sensing & processor can be utilized for internal health monitoring of IPS
Innovation: Fundamental Building Blocks - SUPER

Smart Universal Power Electronics Regulators (SUPERs) – Modular, interoperable entities that are for fundamental blocks of SSPS

- Continuous monitors the POC and acts immediately on nodal abnormalities
- Self contained power stages with passives, aux power, sensing etc. to decouple parasitic loops, noise loops etc.
- Increases system reliability, reduces downtime by continuously monitoring the health of the components
- Enables transactive function for P & Q
- Embedded intelligence for fault tolerant operation etc.
- Enables autonomous operation & maximizes grid support. Enables dynamic voltage & frequency regulation etc.
Innovation – Fundamental Building Blocks – IPS

**Controller:** More powerful computation and communication capability to handle data processing to enable diagnostics and prognostics

**Auxiliary power supply:** Self-maintained power supply provides safe shut-down during system crash and minimize the Interconnection between SUPER and IPS

**Integrated passives:** Ensure safe and reliable performance with the minimum required parameters, so the

**Device:** Advantage packaging to shrink overall SUPER and IPS form factor

**IPS Critical Features Desired by SUPER:**
- Interoperable plug-and-play power stage
- Provide sufficient component-level status information to enable accurate SUPER-level diagnostics and prognostics

**Sensors:** Several sensors can be integrated into gate drivers to improve the overall form factor and mitigate noise interference

**Interconnectors between components within IPS:** More optical interconnections involved to improve the noise immunity capability, especially at higher switching frequency of utilized WBG devices

**Gate driver:** Integrated and intelligent gate driver (i2GD) enables integrated sensing (e.g., dc link voltage, device or phase current), active gate driving, and initially enable diagnostics and prognostics features for SUPER
Innovation Update #1: Communication Validation

- Validation of SUPER & IPS control architecture with a high-speed communication link (6.25 Mbps)
- The communication architecture was validated by all partners

**SUPER – Micro Controller Unit (MCU)**

- CC-1 Messages: AC voltage references
- CC-2 Messages: Configuration, commands, health, status etc.

**IPS – Micro Controller Unit (MCU)**

- Received data is decoded in IPS to generate the PWM
- Encoded AC voltage references send at 30 kHz interval from SUPER

**CHIL Setup for SUPER validation in Grid-C**
Components of the baseline IPS including contactors, gate drivers, IPS controller, communication expansion board were tested extensively during integration.

IPS tests at 800 V, 3.8 kW, 30 kHz in open loop configuration.
Validation of SUPER & IPS architecture with high-speed communication links, controls, protection and standardized interfaces for grid functions
Innovation Update #2: Overall Architecture Validation

- Vdc regulation (GI): The SUPER maintained the dc-link at 1-kV & real power P (up to 15 kW), was injected/absorbed using battery test system

- P/Q Compensation (DCSI): SUPER injected/absorbed P/Q from/to the grid (Tested up to 10 kW & -5 kVAR)

Mode -1: Vdc regulation

Mode -2: P/Q Compensation
Innovation Update #3: Standardized Interconnects & Enclosure

- Modular test cell configuration to show interoperability between IPSs from university partners
- Test cell designed to operate at 1kV, 480 V & 150 kVA and be agnostic to IPS design and non-idealities & support parallel operation.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Fiber Optic</th>
</tr>
</thead>
<tbody>
<tr>
<td>POF Diameter (core)</td>
<td>980/1000 um</td>
</tr>
<tr>
<td>Protective Covering Diameter</td>
<td>2200 um</td>
</tr>
<tr>
<td>Insertion Loss</td>
<td>&lt; 3dB @ 650nm (socket/pin depends on assembly)</td>
</tr>
<tr>
<td></td>
<td>&lt; 6 dB@ 650nm (common lens)</td>
</tr>
<tr>
<td>Mating cycles</td>
<td>500 (socket/pin) / 100,000 (lens)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameters</th>
<th>AC Terminals</th>
<th>Intermediate DC-Link Access / DC Terminals</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated voltage</td>
<td>600 V ac</td>
<td>5 kV dc (line – line) 2.9 kV (phase – neutral)</td>
</tr>
<tr>
<td>Rated current/contact</td>
<td>150 A</td>
<td>20 A (2 poles) / 32 A (1 pole)</td>
</tr>
<tr>
<td>No. of poles</td>
<td>2</td>
<td>1 or 2</td>
</tr>
<tr>
<td>Contact diameter</td>
<td>8 mm</td>
<td>3 mm</td>
</tr>
<tr>
<td>Contact resistance</td>
<td>&lt; 150 µΩ</td>
<td>&lt; 1.1 mΩ</td>
</tr>
<tr>
<td>Mating cycles</td>
<td>100,000</td>
<td>100,000</td>
</tr>
<tr>
<td>Type of termination</td>
<td>Screw</td>
<td>Crimp</td>
</tr>
</tbody>
</table>
Modular test cell configuration to show interoperability between IPSs from university partners

Power Routing
- DC Bus, Intermediate DC Bus, Precharge circuits
- DC Fusing, and DC Main Interconnects
- AC Routing, Filters, to LCL Interface

SUPER Auxiliary Supply Routing
- 480Vac to 24V Supply and Battery backup
- SUPER 15V and 5V Supply
- Wide range DC input to 24V supply
- Interconnect Switch

LCL Interface
- LCL (configurable for 1 or 2 IPS test positions) and Sensors
- AC Bus, Fusing and Grid Interconnect

Shielded Control Cabinet
- Houses the controller & the communication interfaces
- Receives the signals through the standardized signal interfaces from IPS

Engaging & Disengaging Mechanism for the Interconnects
Library of IPSs from university partners to validate **vendor agnostic design** of SUPER

<table>
<thead>
<tr>
<th>IPS from University Partners</th>
<th>Topologies</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Florida state university (FSU)</td>
<td>Interleaved buck boost converter with coupled inductor</td>
<td>3-ph 2-level voltage source inverter (VSI)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Interleaved configuration reduces the Input current ripple. Ideal for BES applications</td>
</tr>
<tr>
<td>Ohio State University (OSU)</td>
<td>Traditional boost converter</td>
<td>3-ph 2-level VSI with carrier frequency modulation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Capability to integrate the inductor with the liquid metal cooling</td>
</tr>
<tr>
<td>University of Arkansas (UARK)</td>
<td>Soft-switching CLLC Bidirectional dc/dc converter</td>
<td>3-ph 2-level VSI</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Resonant configurations for power transfer at higher frequencies and with soft switching</td>
</tr>
<tr>
<td>University of New York, Stony Brook (NY-SB)</td>
<td>Interleaved boost converter</td>
<td>3-ph 2-level VSI with redundant half bridge legs &amp; coupled ac inductors</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Capitalizes on P &amp; N cell layout to optimize switching speeds</td>
</tr>
<tr>
<td>University of North Carolina, Charlotte (UNCC)</td>
<td>-</td>
<td>4-leg 3-ph 2-level VSI</td>
</tr>
<tr>
<td>University of Texas, Austin (UT-Austin)</td>
<td>DC/DC stage with parallel devices</td>
<td>3-ph 2-level VSI with parallel devices</td>
</tr>
<tr>
<td>Virginia Polytechnic University (Vtech)</td>
<td>3-level dc/dc converter</td>
<td>3-ph 2-level VSI</td>
</tr>
</tbody>
</table>

*green color text highlights IPS with discrete devices*
### Innovation Update #5: IPS Library & Features

<table>
<thead>
<tr>
<th>IPS Features</th>
<th>University Partners</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1. Interoperability</strong></td>
<td>• Execution by ORNL with all university partners</td>
</tr>
<tr>
<td>- Standardized electrical ports and communication interface</td>
<td></td>
</tr>
<tr>
<td>- Enclosure scalability and standardization</td>
<td></td>
</tr>
<tr>
<td>- Compliance to standards &amp; protocols</td>
<td></td>
</tr>
<tr>
<td><strong>2. Embedded intelligence &amp; decision-making capability with a flexible platform</strong></td>
<td>• Framework is developed by ORNL and will be communicated with all university partners</td>
</tr>
<tr>
<td>- Interoperable/scalable with different embedded controllers</td>
<td></td>
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<tr>
<td>- Monitors the point of connection continuously</td>
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<tr>
<td>- Easy transition between control mode required by SUPER</td>
<td></td>
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<tr>
<td>- Immediate response to IPS internal faults with least impact to the SUPER</td>
<td></td>
</tr>
<tr>
<td><strong>3. Embedded online health monitoring system – Diagnostics/Prognostics</strong></td>
<td>• In-situ on-state resistance measurement (Vtech, UT-Austin &amp; UNCC)</td>
</tr>
<tr>
<td>- Embeds temperature sensors in IPS to enhance thermal monitoring for</td>
<td>• In-situ junction temperature measurement (UARK &amp; UT-Austin)</td>
</tr>
<tr>
<td>prognostics</td>
<td>• In-situ gate leakage current measurement (FSU)</td>
</tr>
<tr>
<td>- Monitors the health and degradation status of critical components in IPS</td>
<td>• Estimation of passive components (UARK)</td>
</tr>
<tr>
<td>- Captures/maps faults to their corresponding signatures</td>
<td>• DC-link capacitance health estimation (NY-SB, UNCC, Vtech &amp; UARK)</td>
</tr>
<tr>
<td>- Robust/retrievable events recording and reporting system</td>
<td></td>
</tr>
<tr>
<td><strong>4. Integrated minimum passive, intelligent gate driving, sensing and protection</strong></td>
<td>• Intelligent gate driver (Vtech &amp; FSU)</td>
</tr>
<tr>
<td>- Standardized minimum integrated passives</td>
<td>• Advanced current sensors (UNCC)</td>
</tr>
<tr>
<td>- Intelligent and robust gate driving scheme</td>
<td>• Fusion algorithms for sensed signals (OSU)</td>
</tr>
<tr>
<td>- Integrated sensing and protective device</td>
<td>• Digital twin for prognostics/diagnostics (NY-SB)</td>
</tr>
<tr>
<td><strong>5. Cyber-physical security</strong></td>
<td></td>
</tr>
<tr>
<td>- Hardware and software mechanisms to secure power electronics systems</td>
<td></td>
</tr>
<tr>
<td><strong>6. Self-contained auxiliary power supply</strong></td>
<td>• All universities</td>
</tr>
<tr>
<td>- Draws the required power from IPS itself and power all the contained components</td>
<td></td>
</tr>
</tbody>
</table>
## Milestone Update

<table>
<thead>
<tr>
<th>Milestone Description (or Go/No-Go Decision Criteria)</th>
<th>Period</th>
<th>Status</th>
<th>Accomplishments/Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1.1 - Validation of SUPER design, operation and controls through simulation and establishing the major IPS design requirements.</td>
<td>BP1 – Q1</td>
<td>Completed</td>
<td>❑ Identified the hardware, controls, communications, interface requirements for SUPER &amp; IPS considering the project objectives.</td>
</tr>
</tbody>
</table>
| 1.2.1 - CHIL validation of the agent framework, the control modes & protection logic and strategy. 1.2.2 - 3D layout of the SUPER 1.0 with all its subcomponents. | BP1 – Q2| Completed | ❑ The entire agent framework with the control, protection & communication were validated in CHIL.  
❑ The passives for SUPER have been designed and validated through simulations.  
❑ The 3D layout of the SUPER with all its subcomponents has been developed.                                           |
| 1.3.1 - Preliminary results from open loop testing of SUPER 1.0                                                                                     | BP1 – Q3| Completed | ❑ Magnetics prototyping and testing has been completed.  
❑ Standardization details for IPS including constraints were articulated to the university partners.  
❑ Open loop testing of SUPER has been completed.                                                                                         |
<p>| 1.4.1 – Experimental results of autonomous operation of SUPER functioning as G with IPS 1.0.                                                              | BP1 – Q4| Completed | ❑ Closed loop operation of SUPER has been validated experimentally with the agent.                                                                                     |</p>
<table>
<thead>
<tr>
<th>Milestone Description (or Go/No-Go Decision Criteria)</th>
<th>Due</th>
<th>Status</th>
<th>Accomplishments/Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1.1 - Complete the development of testbed for experimentally validating IPS 2.0 and its subcomponents.</td>
<td>BP2 – Q1</td>
<td>Completed</td>
<td>❑ The SUPER test cell development has been completed</td>
</tr>
<tr>
<td>2.2.1 - Complete the performance evaluation and validation of IPS 2.0 power stage from university partners.</td>
<td>BP2 – Q2</td>
<td>In Progress</td>
<td></td>
</tr>
<tr>
<td>2.3.1 - Experimental results validating the response of IPS 2.0 for a grid function. 2.3.2 – Demonstration of advanced</td>
<td>BP2 – Q3</td>
<td>Not Started</td>
<td></td>
</tr>
<tr>
<td>featured of IPS 2.0.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.4.1 - Demonstration of autonomous operation of SUPER 2.0 functioning as G with IPS 2.0s</td>
<td>BP2 – Q4</td>
<td>Not Started</td>
<td></td>
</tr>
<tr>
<td>2.4.2 - Demonstration of SUPER 2.0 operating as L</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.4.3 - Demonstration of scalability of SUPER 2.0 with two non-identical IPS 2.0s</td>
<td></td>
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<tr>
<td>Complete the final report with the summary of the results.</td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>
Innovation Update

Risks

- Anticipated delays in validation of IPS in the SUPER test cell owing to the pandemic
- Anticipated delays in the integration of IPS from university partners in the SUPER test cell
Innovation Update

Future Work

- Validate advanced features like online health monitoring in SUPER with IPSs from partners
- Validate advanced algorithms in SUPER for grid support
- Demonstrate the grid support capabilities of SUPER
Impact:

- Provides a pathway to develop power electronics interfaces with well defined hierarchy in controls, communication, protection, intelligence and optimization for scalability & modularity

- Provides a pathway to develop a library of power converters for SSPS 1.0

- Provides a pathway for interface, communication, protection standardization

- Provided a pathway to develop holistic systems with embed intelligence & advanced features systematically and strategically in fundamental blocks

- Helps emulate the different vendor scenario to access interoperability & standardization
Impact/Commercialization

Invention Disclosures Filed:


Publications:

THANK YOU