Intelligent Power Stage (IPS)

PRINCIPAL INVESTIGATORS
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**Goal:** Development of intelligent power stage (IPS) three-phase ac-to-dc power converter module with advanced power processing, monitoring, and diagnostic capabilities based on high efficiency Silicon-Carbide power semiconductor devices.

**Background:**
- Future grid-specific power electronics remains hindered by the strong industrial reliance on custom-design power converters
- Modular, IPS-based solutions seek to unleash the development of grid power electronics enabling their flexible, scalable integration featuring advanced power processing, monitoring and diagnostics capabilities.
Innovations

- **Topology:** 2-level ac-dc converter with split dc-bus and cascaded 3-level buck-boost dc-dc converter
- **Ancillary Circuitry:** fiberoptic communication network (25 Mbps) between controller, gate-drivers (GD) and sensors; auxiliary power network with high dv/dt immunity (>100 V/ns); minimized EMI susceptibility
- **Monitoring and diagnostics:** GD-integrated SiC MOSFET Rdson, Tj measurement and dc-bus voltage; dc-bus capacitance measurement based on $I_d$ and off-state $V_{ds}$ measurements
SUPER to IPS Communication Tests (UART 6.25 Mbps)

Bit width ~160 ns (~6.25 MHz)

Latency between RX and TX – 57 ns

5-byte packet – 7.84 µs

6-bytes packet – 9.45 µs
IPS Internal Communication Protocol

- Based on 10BASE-T ethernet standard
- Physical layer: Plastic Optical Fiber
- Data rate: 25 Mbps
- Packet structure: inspired by MODBUS

Data Packet Structure

<table>
<thead>
<tr>
<th>Part</th>
<th>Length - Subpacket</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preamble</td>
<td>4 bytes</td>
</tr>
<tr>
<td>Payload</td>
<td>4 bytes – SYNC</td>
</tr>
<tr>
<td></td>
<td>4 bytes - CTRL</td>
</tr>
<tr>
<td>CRC32</td>
<td>4 bytes</td>
</tr>
</tbody>
</table>

**Difference between Custom protocol and 10BASE-T**

<table>
<thead>
<tr>
<th></th>
<th>10BASE-T</th>
<th>Custom protocol</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed</td>
<td>10 Mbps</td>
<td>25 Mbps</td>
</tr>
<tr>
<td>Preamble + SOF</td>
<td>7+1 octets (64 bit)</td>
<td>3+1 octets (32 bit)</td>
</tr>
<tr>
<td>Payload/Packet</td>
<td>64–1,552 octets (variable size)</td>
<td>12 octets (96 bit, fixed size)</td>
</tr>
<tr>
<td>Frame check sequence</td>
<td>32-bit CRC</td>
<td>32-bit CRC</td>
</tr>
<tr>
<td>Encoding/Decoding</td>
<td>Manchester</td>
<td>Manchester</td>
</tr>
</tbody>
</table>

**SYNC/CTRL related block**

<table>
<thead>
<tr>
<th>Value</th>
<th>Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>8 bits</td>
</tr>
<tr>
<td>Data</td>
<td>24 bits</td>
</tr>
</tbody>
</table>
Sub-Nanosecond Synchronization Capability

- < 1 ns synchronization jitter achieved with physically distributed clock
- Timers in GD and Controller are synchronized using PTP (IEEE 1588)

Benchmark System
Enhanced Immunity to SiC-Generated EMI

**Challenge**
- Fast switching frequency and \(dv/dt\) rates of SiC devices heighten EMI emissions disrupting communications

**Solution**
- Switching-proof communication protocol
- Data packets are synchronized and not transmitted during turn-on and turn-off SiC MOSFET switching events
Enhanced Gate-Driver for SiC MOSFET Module

- Drives half-bridge 1.2 kV SiC MOSFET module
- Modular, triple board design:
  - Digital, analog, and interface boards
- Double MAX10 FPGA controllers
- Integrated sensors
  - Top and bottom $I_d$, $V_{dson}$, $V_{dsoff}$, substrate temperature
- Communication protocol used for PWM, control, status, and transmission of measured data back to controller
- $Dv/Dt$ immunity: 100 V/ns
Gate-Driven-Integrated $I_d$ and $V_{ds\text{on}}$ Sensors

- $I_d$ sensors enable phase-current reconstruction
- $V_{ds\text{on}}$ and $I_d$ sensors enable $T_j$ estimation
Digitally-Interfaced Sensing Network

• Four-board, modular sensor design
  ➢ Digital board, signal conditioning, power supply, and sensor interface boards
• MAX10 FPGA controller
• Sensor interface boards:
  ➢ Voltage, current and temperature
• Communication protocol: IPS internal protocol based on 10Base-T
• Sampling rate: 2 Msps
• Transmission rate: 200 ksp
PCB-Winding Coupled Buck-Boost DC Inductor

- Low-profile design (3.5 kVA/in³)
- Simple assembly with commercial AMCC core
- Heavy copper PCB (15 oz Cu, 50 kW, 90 A dc)
- Double PCB winding design to reduce fringing effect
  - Continuous and discontinuous current modes

Current density FEA simulation

Two-board design (even distribution)  One-board design

Hitachi AMCC Core

Winding 1  Winding 2

28 mm

98 mm

86 mm
PCB-Winding Three-Phase Boost Inductors

- Low-profile design (2 kVA/in³)
- Simple assembly with commercial AMCC core
- Heavy copper PCB (12 oz Cu, 75 kVA, 90 Arms)
- Integrated in IPS to mitigate circulating current
Thermal Performance of PCB-Winding Magnetics

- Dc coupled inductor and ac three-phase boost inductor
  - Analytic and FEA simulations validated experimentally
  - Maximum temperature limited to 60 °C

![Graph showing temperature vs. power with a maximum of 60°C at 60 Arms (50 kVA)]

![FEA simulation, side view, and cross section images with a color scale indicating temperature from 30 to 70 °C]
IPS Nominal Power Testing

- Nominal power rating test (75 kVA)
- Zero-voltage-switching for all dc-dc stage semiconductors
- Quadrangular current control scheme
Milestones Update

- **BP1 Milestones**
  - M1.1 “IPS electrothermal design meets target specifications”
  - M1.2 “Gate-driver unit is built and functionally tested”
  - M1.3 “Auxiliary power supply are built meeting their specifications, and PCB-based dc-bus planar structures are built”
  - Go/No-Go “IPS power stage subcomponents are demonstrated”

- **BP2 Milestones**
  - M2.1 “Full power testing of IPS validated. Prototype P1 ready for testing at ORNL” [completion: 85 %]
  - M2.2 “Filters are built and ready for testing. Digital sensors (V, I, T) are built and ready for testing, and digital control system communication is tested” [completion: 95 %]
  - M2.3 and Go/No-Go due in July and September 2022
Risks Mitigation Strategy

• Supply chain challenges have led to widespread shortage of electronic components and longer component manufacturing timeframes leading to IPS development and construction delay
  ▪ All circuit designs were revised to replace key parts that were not available, and had lead times of months up to a year
  ▪ Scavenged components with suppliers around the world

• Acquisition of SiC MOSFETs was delayed 4 months due to contractual barriers between GE and Virginia Tech, which is bound by VA state law
Future Work

- Task 2.1 Integration and thermal testing of IPS-1
  - Hardware integration and testing of IPS-1 unit and EMC verification
- Task 2.2 Advanced functionality
  - Program Iphase, Rdson and Tj temperature estimation
  - Program dc-bus capacitance Cdc value estimation
- Task 2.3 Integration, thermal testing and qualification of IPS-2
  - Hardware integration of IPS-2 unit using enhanced gate-drivers
  - Testing and demonstration of Iphase, Rdson, Tj, and Cdc estimation
- Task 2.4 Advanced functionality update
  - Program Iphase, Rdson and Tj temperature estimation in IPS-1
  - Program dc-bus capacitance Cdc value estimation in IPS-1
  - Testing and demonstration of Iphase, Rdson, Tj, and Cdc estimation
IMPACT

• Modularity of IPS concept combined with automated-manufacturing-oriented design of proposed IPS will expectedly favor multi-supplier IPS market development attaining economy of scales benefits

• IPS internal digital control and communication network will demonstrate a viable alternative to operating in the harsh EMI environment generated by SiC power semiconductors (main collateral effect of this technology)

➢ This is critical for modular systems as the EMI generated is directly proportional to the number of modules used, in this case IPS units
PUBLICATIONS

• “A 50kW Planar PCB-based Heavy Copper Coupled Inductor for FSBB,” submitted to ECCE 2022.

IP STATUS — Invention disclosures in preparation
1. “Buck-boost dc-dc converter high-efficiency and low EMI emissions current control scheme”
2. “IPS control and sensing communication network with sub-nanosecond synchronization”
THANK YOU

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SiC: Silicon-Carbide, semiconductor material
MOSFET: metal-oxide field-effect transistor
GD: Gate-driver, i.e., electronic circuit that controls the turn-on and turn-off of SiC power transistors
PTP: Precision time protocol
Mbps: mega bits per second
Msps: mega samples per second
PCB: printed circuit board
EMI: electromagnetic interference