Cost-Competitive, High-Performance, Highly Reliable Power Devices on Silicon Carbide

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State University of New York Polytechnic Institute

2021 DOE Annual Merit Review

This presentation does not contain any proprietary, confidential, or otherwise restricted information.

Project ID # elt247

Overview

Timeline

- Project start April 2019
- Project end March 2024
- Percent Complete: 40%

Budget

- BP2 total $333K: Federal $ 300K + cost share (10%)

Barriers

- Cost: the lack of device innovations and processing technologies
- Performance: need state-of-the-art f acility for tight design rules
- Reliability and ruggedness: trade off relationship with performance

Partners

- Sandia National Laboratories
- The Ohio State University
- Virginia Tech

Relevance – objectives / impact

Overall objectives in this project

- The primary objective of this project is to ensure that the next-generation of wide-bandgap devi ces of sufficient performance, reliability, and price to achieve the system-level DOE goals.

Objectives in previous period (BP2, FY2020-2021)

- Establishment of the process baseline for Gen2 MOSFETs.
- Evaluation of Gen2 MOSFETs;

  Performance; Ron,sp=5mohm-cm^2, Vth=2V, BV=1600V.

  Reliability and Ruggedness; Short Circuit SOA 2µs

Impact of research

- The successful development of the proposed device will bring in a highly efficient and reliable power electronics for electric drive trains.

Milestones – BP3

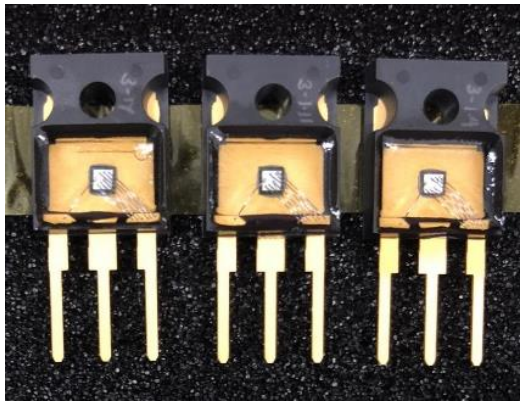
Milestone	Type	Description
Gen3 SiC MOSFET design	Technical	The cell and edge termination structures for MOSFETs and JBS diode integrated MOSFETs have been optimized; Optimized devices included in a single mask-set.
Gen3 SiC MOSFETs fabrication	Technical	Two engineering lots to make Gen3 devices completed; Implants conducted at RT; Self-aligned channel scheme optimized.
Gen3 SiC MOSFETs evaluation	Technical	Static performances have been characterized on-wafer; Reliabilities and ruggedness evaluated.
AlGaN/GaN HEMT device processing optimization	Technical	Various stages of devices processing are completed.
Improved static performance, Reliability assessment on Gen3 devices	Go/No Go	Performances of Gen3 SiC MOSFETs evaluated: BV = 1700V, Ron,sp = 4 mohm-cm2, Vth = 2V Short Circuit SOA 4µs; Tests on TDDB, HTGB, HTRB, dv/dt, 3Q diode behavior

Approach – CPR metrics

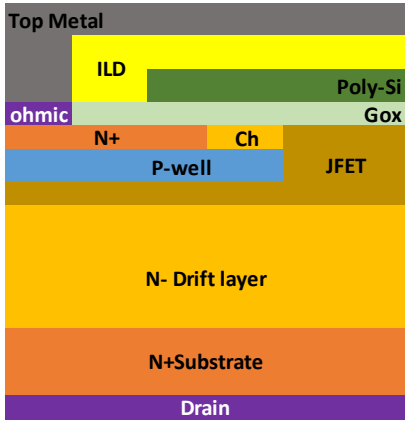
	on-resistance	chip price	blocking behavior	threshold voltage	short circuit capability	avalanche capability	HTRB	HTGB, Vth stability	dv/dt, switching behavior	BPD, SF- degradation	thermal management	others
short channel	+	+	-	-	-		-	-				
tight cell pitch	+	+			-							
self aligned channel	+	+	+	+				+				
narrow JFET region			+		+	+	+		+			
enhanced doping in JFET	+				-	-	-					
deep Pwell (so is JFET region)			+		+	+	+					
thinner gate oxide	+			-	-		-	-				
innovative gate oxide process	+	+		+	+			?		+		
unipolar diode integration		+							+	+		
inversion mode channel	-	-	+	+	+			+				
source doping reduction	-				+							
reduction in Wp+/Wn+	+	+			-	-						
Ringe based edge termination		-	-			-	-		+			
JTE based edge termination		+	+			+	+		-			
substrate thinning	+										+	
double sided package									+		+	
Ion implants @ RT		+								?		
W plug(high aspect ratio CT)	+										+	+
Striped cell design	-		+		+		+				+	

Technical Accomplishments and Progress

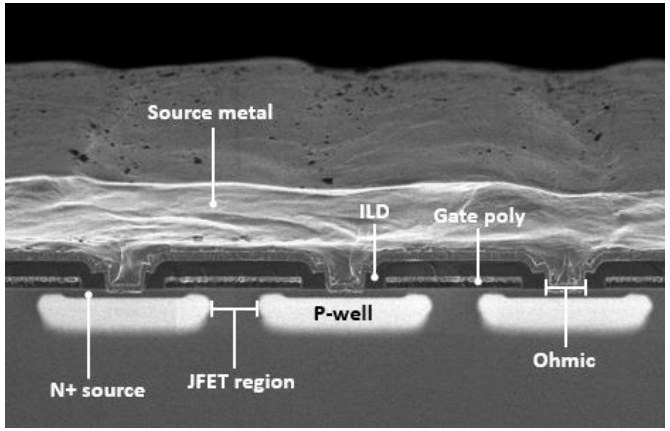
6 inch SiC wafer



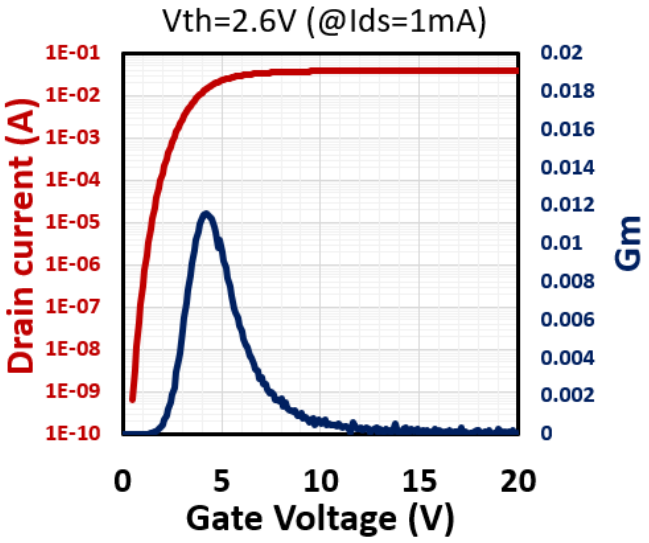
Packaged SiC MOSFETs



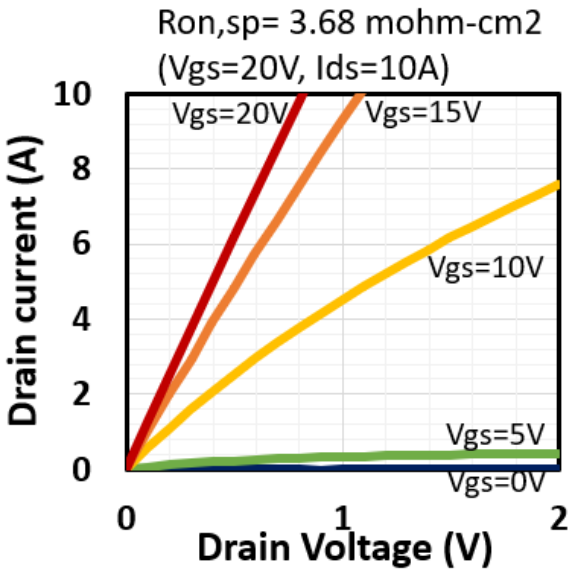
Cross-sectional view



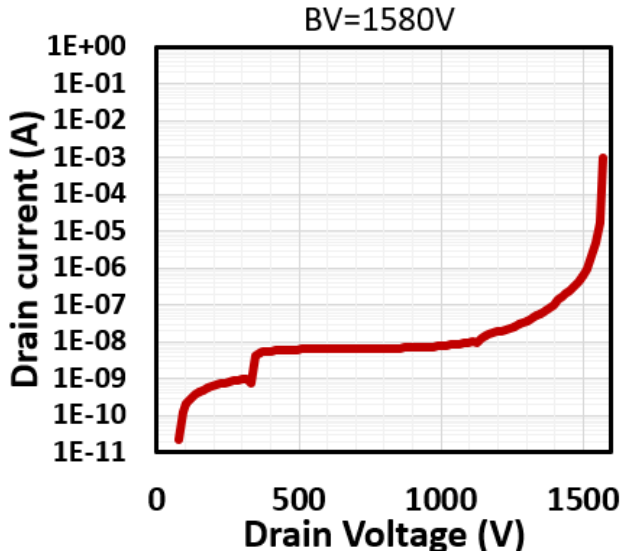
SEM image



Transfer characteristics

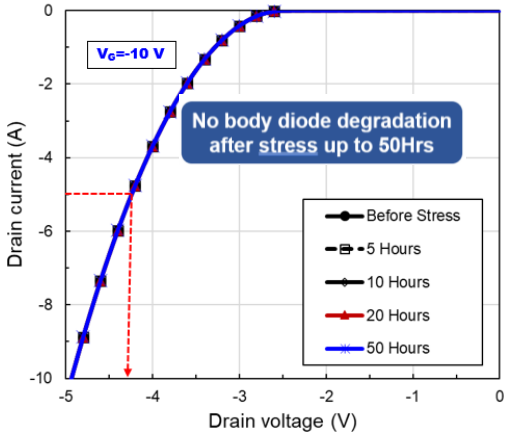


Output characteristics

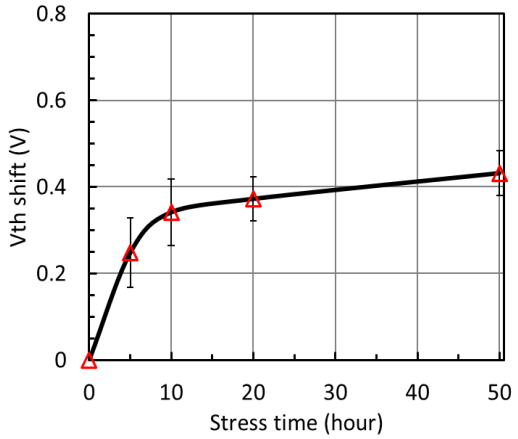


Blocking behaviors

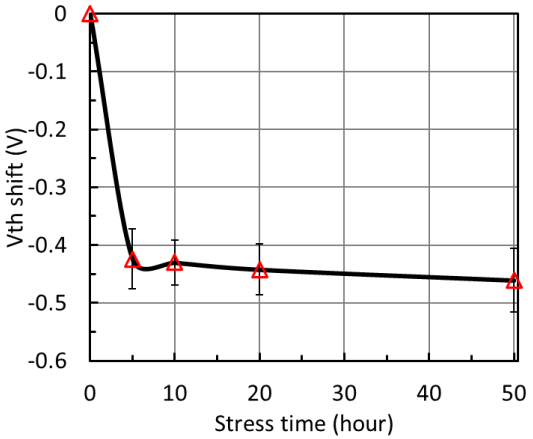
Technical Accomplishments and Progress



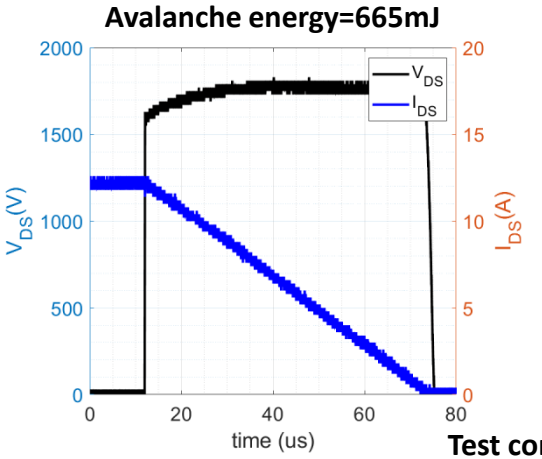
Body diode degradation



PBTI: Vgs=+20V

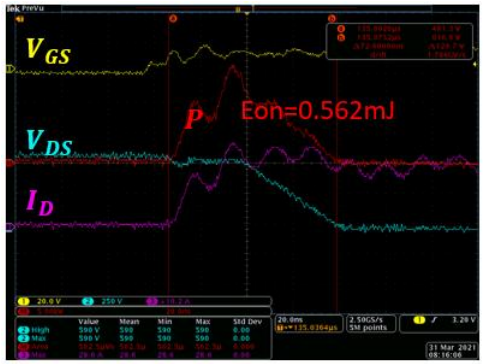


NBTI: Vgs=-10V

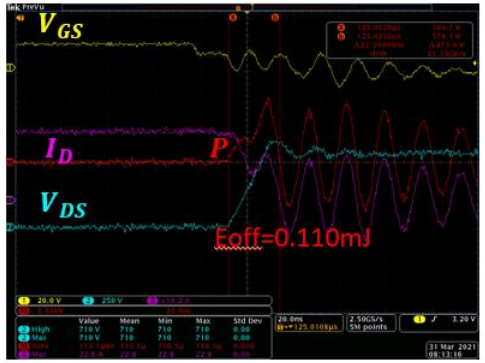


Avalanche energy

Test conditions
V_{DC}: 100V
L: 11mH

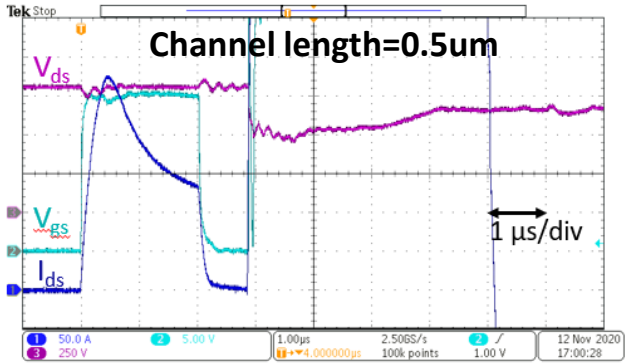


Switching Turn-on

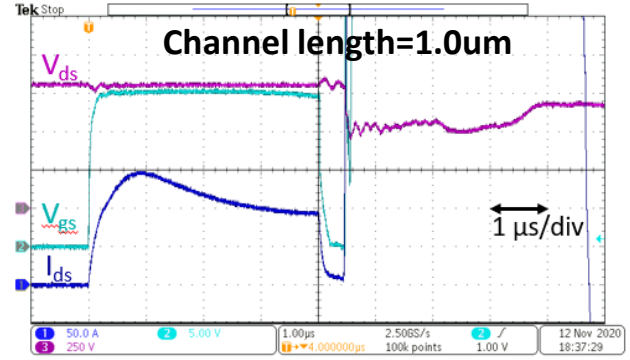


Switching Turn-off

Test condition: Resistor=10 ohm, Vgs=15V, Vds=~600V Id=~22A.



Short-circuit capability

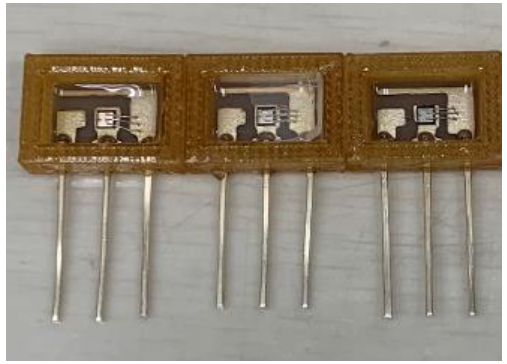


Short-circuit capability

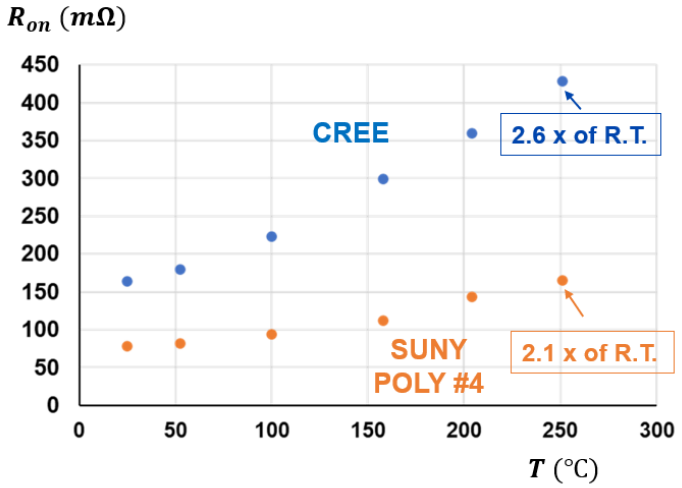
Test condition: Vgs=20V, Vds=800V.

Body diode, BTI, Avalanche, and SC were measured at OSU, Switching was measured at VT

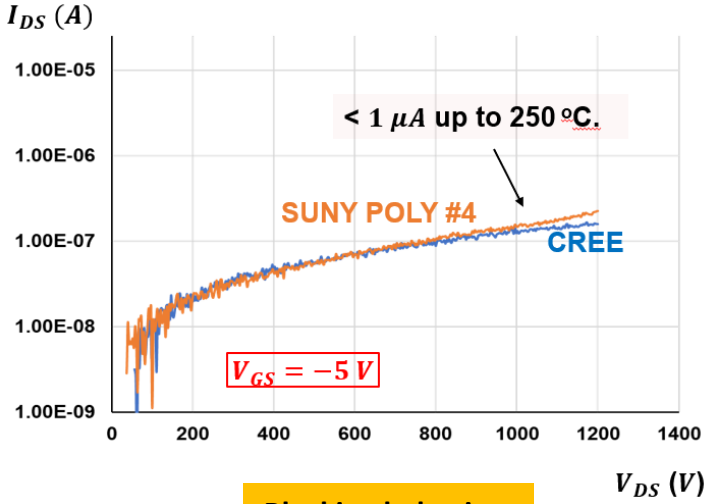
Technical Accomplishments and Progress



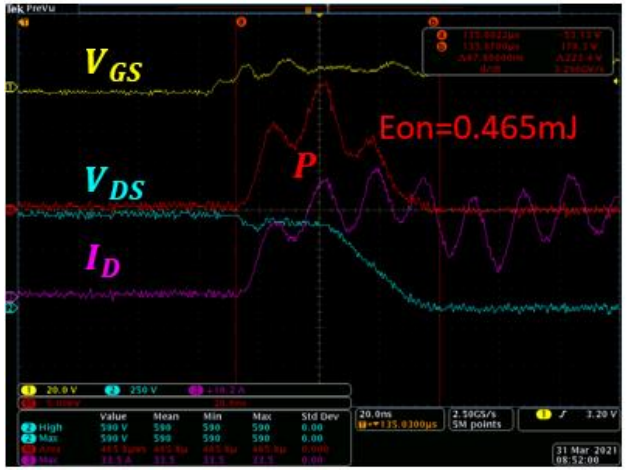
Packaged SiC MOSFETs for HT operation



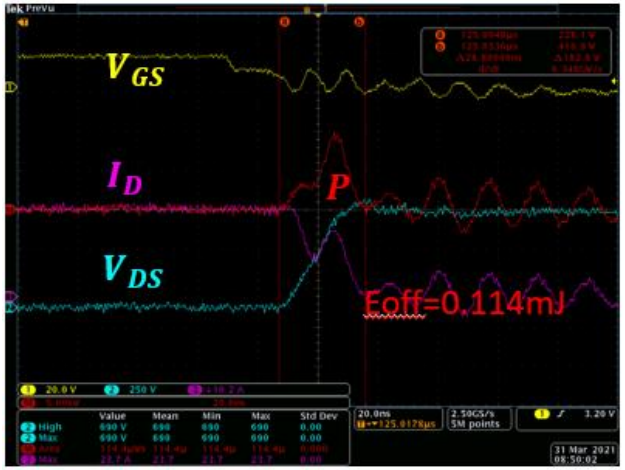
Output characteristics (Ron,sp)



Blocking behaviors



Switching Turn-on at 210 °C



Switching Turn-off at 210 °C

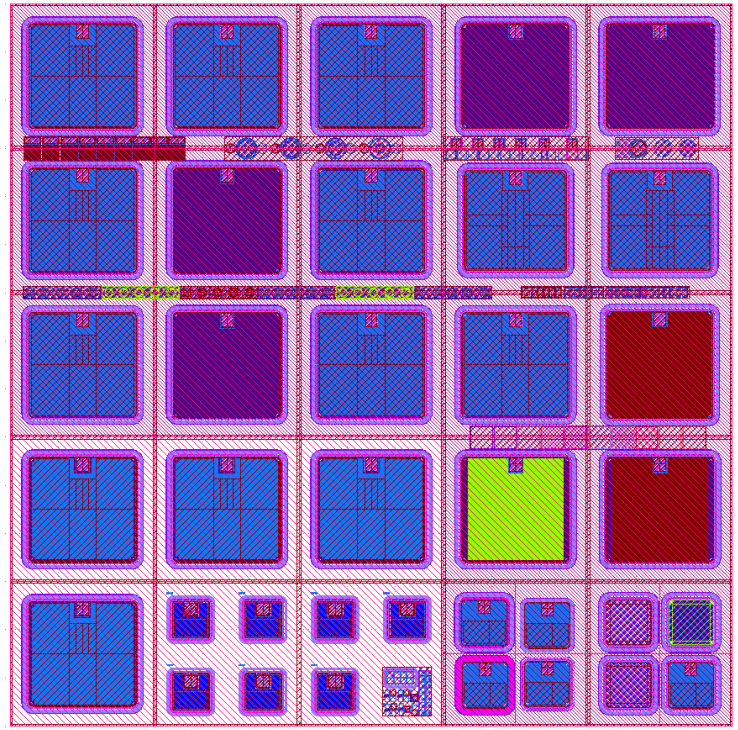
Test condition: Resistor=10 ohm, Vgs=15V, Vds=~600V Id=~22A.

VT packaged and measured MOSFETs

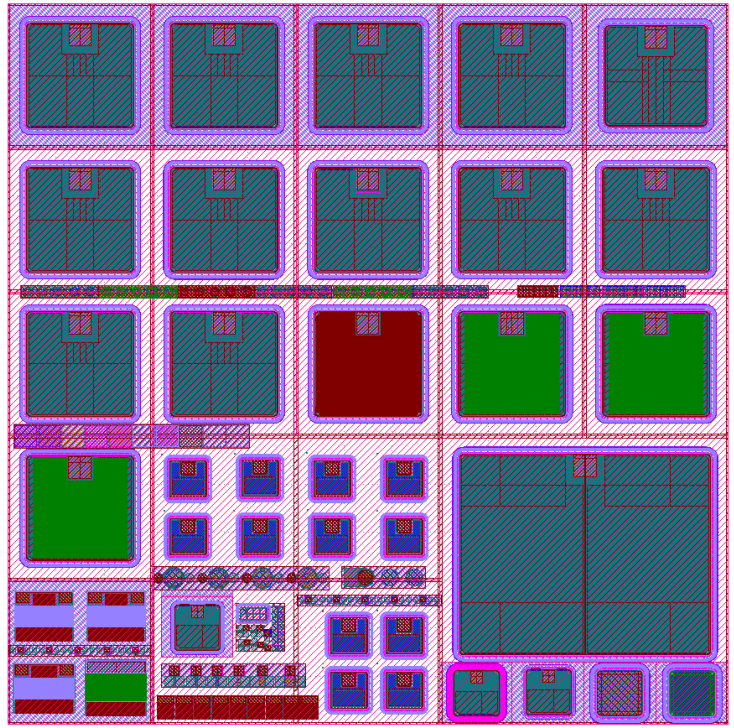
Technical Accomplishments and Progress

- **Mask design – floor plan for 1st and 2nd lot**

  - PiN diode, JBS diode, MOSFETs (different sizes), JBSFETs and test structures were included.
  - Mask design was taped out – design review by SiCamore engineers, kerf (process monitoring boxes) insertion was completed.



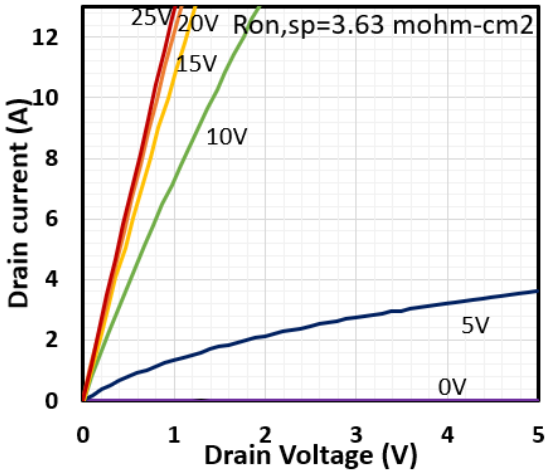
BP2-lot1



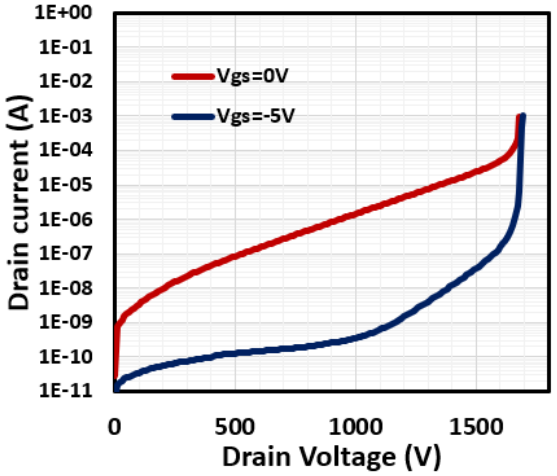
BP2-lot2

Technical Accomplishments and Progress

Lch=0.5um with Nominal Pwell

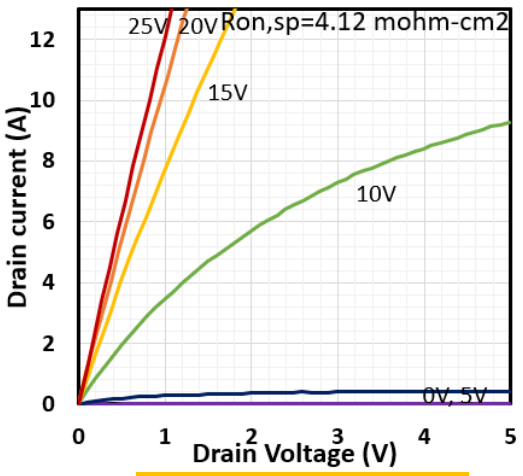


Output characteristics

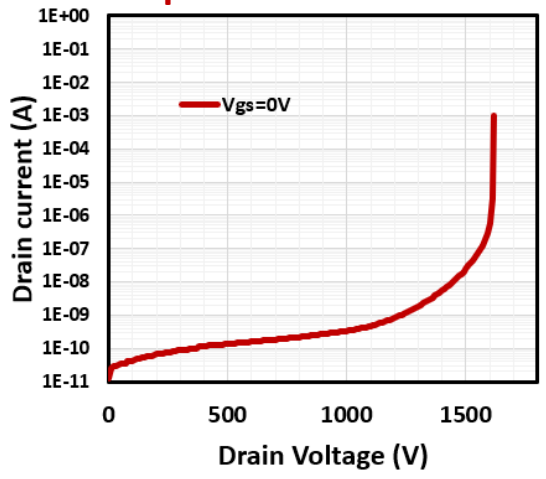


Blocking behaviors

Lch=0.5um with Deep Pwell

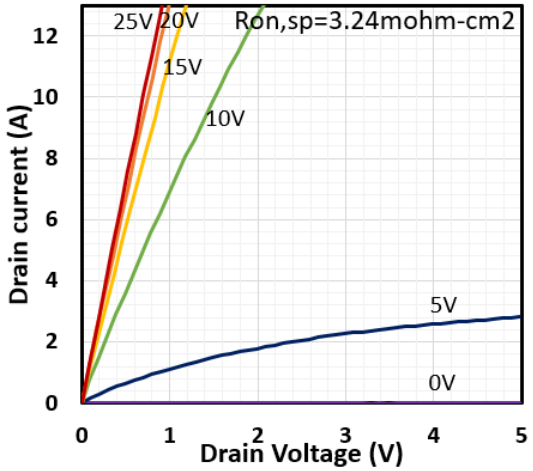


Output characteristics

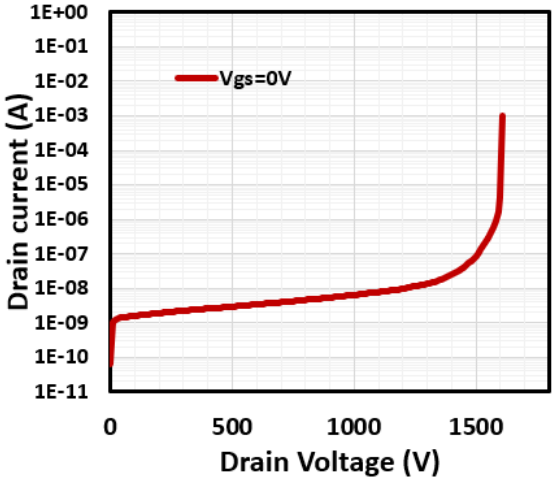


Blocking behaviors

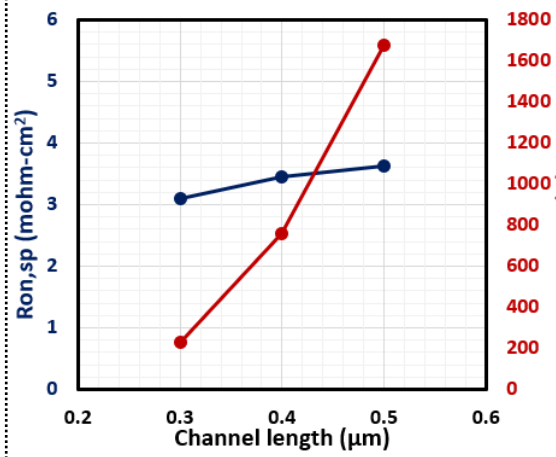
Lch=0.3um with Deep Pwell



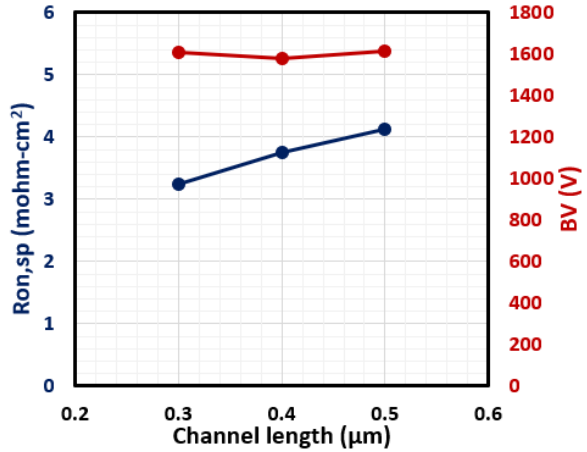
Output characteristics



Blocking behaviors



Summary of Nominal Pwell



Summary of Deep Pwell

Summary

Ron,sp (on-wafer)	BV (on-wafer)	Body diode degradation	PBTI/NBTI	Avalanche energy	SC SOA	Switching Turn-on/Turn-off
3.24 moho-cm^2	1610V	No degradation	Δ+0.45V/ Δ-0.45V	665mJ	>4us	0.562/ 0.110mJ

- Reliability and ruggedness tests were conducted on packaged devices from BP1 at RT and HT.
- The first lot in BP2 was completed; the 2nd lot is running at SiCamore.
- The static performance was significantly improved using deep Pwell structure.
- All aspects (CPR) need to be considered in a comprehensive research program.
- Strong team (fab and partner) was formed to accomplish the proposed goals.

Cost-Competitive, High-Performance, Highly Reliable Power Devices on Gallium Nitride

Principal Investigators: Shadi Sadvik

State University of New York Polytechnic Institute

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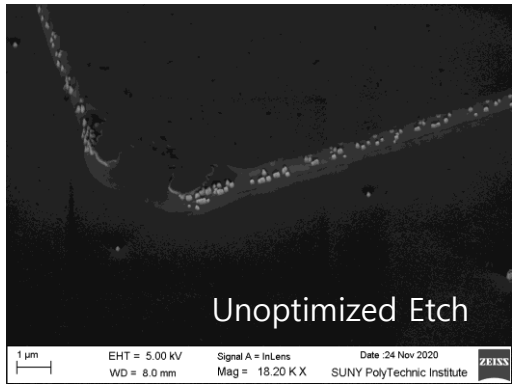
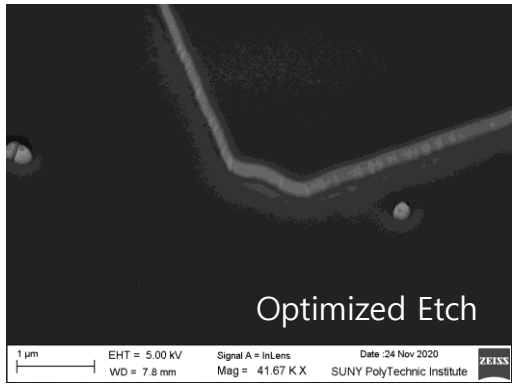
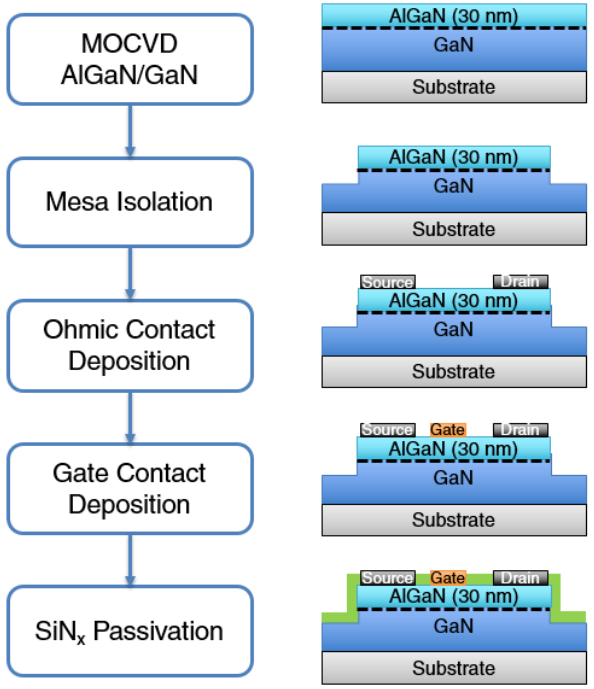
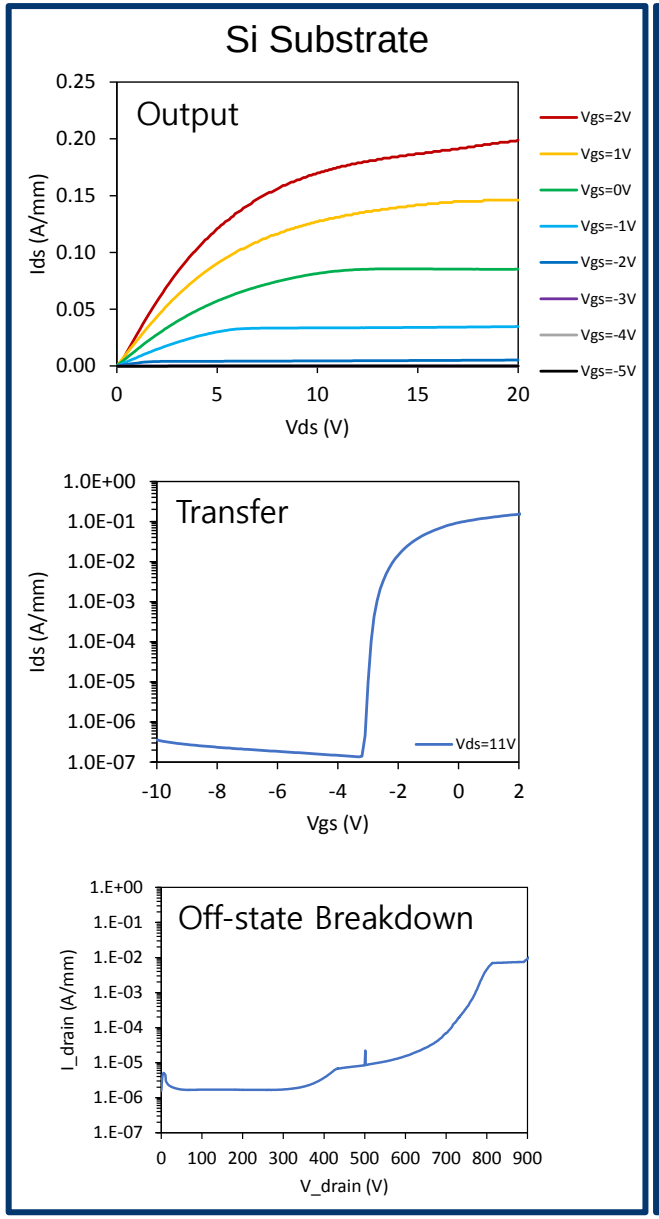
Project ID # elt247

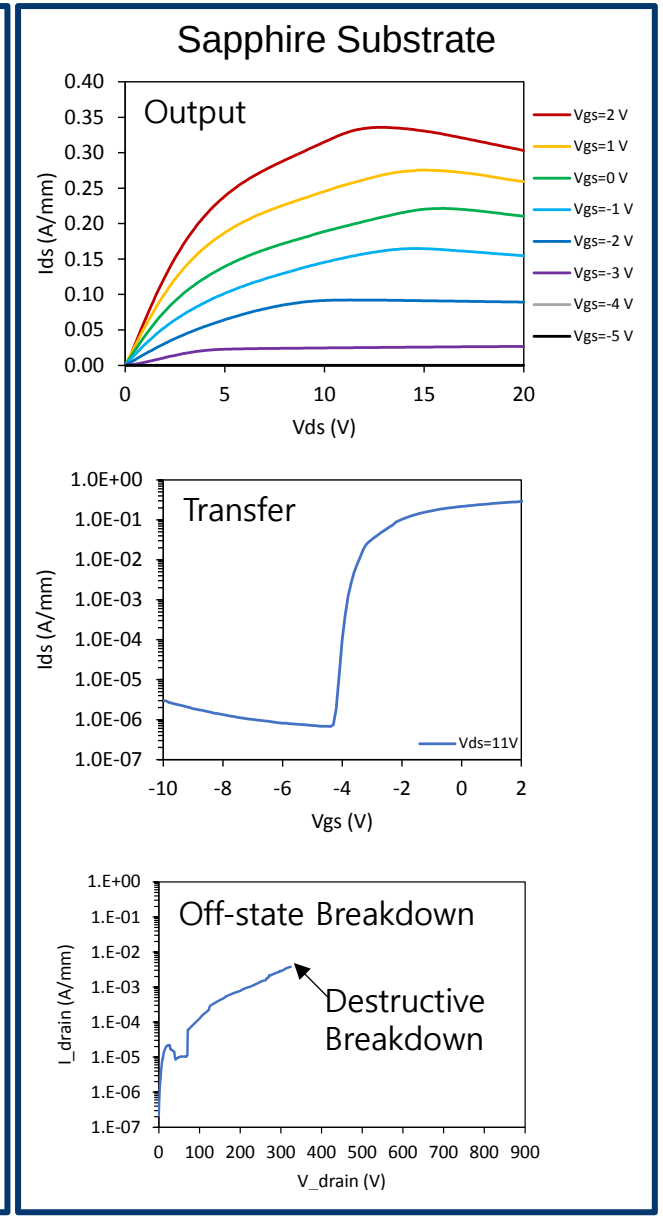
Progress: Processing Optimization and Breakdown Dependence on Substrate











- Poor device performance be due to unoptimized etch condition resulting in poorly defined mesa sidewalls
- Devices fabricated with optimized process resulted in low leakage and $I_{ON}/I_{OFF} > 10^5$
- Devices fabricated on Si substrate showed off-state breakdown 2x higher than devices fabricated on sapph ire substrate, at ~800V.

Technical Progress Summary and Future Work

- Improved etch process for mesa isolation drastically reduced leakage and improved gate control of fabricated HEMT devices
- Devices fabricated at the same time on Si and sapphire substrates demonstrated strong gate control and $I_{ON}/I_{OFF} > 10^5$
- Devices fabricated on Si substrate demonstrated off-state breakdown voltage ~800 V

- Semi-insulating bulk GaN substrates have been received
- New MOCVD carrier platter for 1.5" GaN substrates was been designed, ordered and received.
- Optimized HEMT growth and fabrication process will be performed on SI GaN substrates. Comparative device measurements and reliability testing will be conducted