Integration Methods for High-Density Integrated Electric Drives

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Overview

Timeline

- Start Date: *April 2019*
- End Date: *March 2024*
- Percent Complete: 40%

Budget

- Total project funding: *$1.5 million*
- Funding for FY21: *$300,000*
- Funding for FY22: *$300,000*

Barriers & Technical Targets

- **Single-chip Gate Drive**: Low-voltage, high-temperature (>200°C) SiC fabrication process; achieves 40-50% PCB volume savings
- **Power Modules**: Proven techniques for heterogeneously integrated power module (>200°C)
- **Sensing**: Highly compact, high temperature, noise immune, high bandwidth (>100 MHz) current sensing

Partners

- Virginia Tech
- Oak Ridge National Laboratory
- Stony Brook University

Any proposed future work is subject to change based on funding levels.

Relevance & Objectives

Overall Objective

To research, develop, and evaluate a heterogeneously integrated power module platform that will insert into a traction inverter system capable of the following:

Power Electronics Requirements	
Parameter	**Measure**
Cost ($/kW)	≤2.7
Power Density (kW/L)	≥100
System Peak Power Rating (kW)	100
Efficiency	>97%

FY 21 Objectives

- In-house Gen 1 SiC module fabrication and testing
- Reliability analysis and evaluation of Gen 1 module
- Integrated module validation with silicon gate driver
- High temperature SiC IC fabrication and unit test and evaluation
- System/converter level packaging design and system integration concepts
- High density current and voltage sensing

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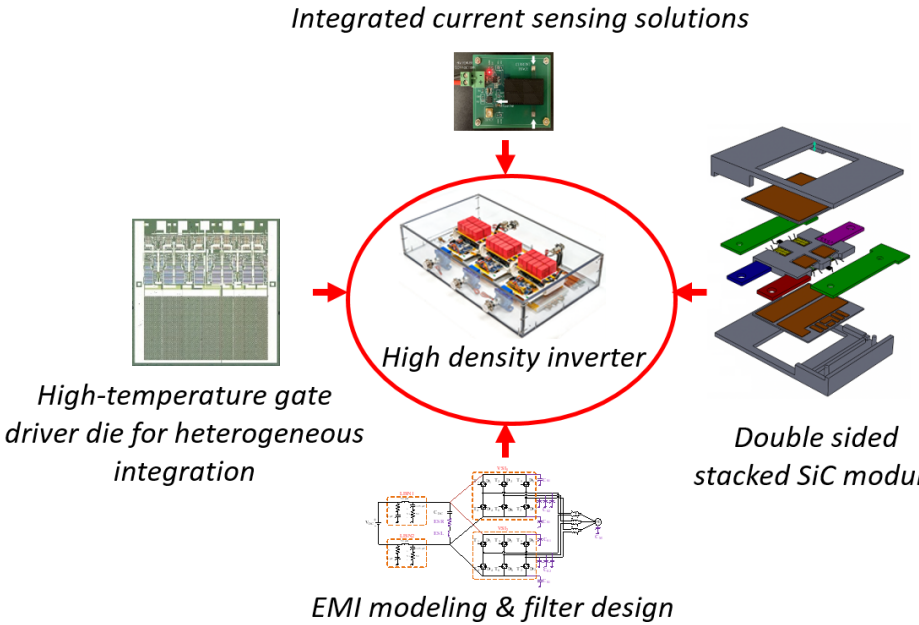
Approach / Strategy

Goal

The overall project goal is to research and develop a heterogeneously integrated power module platform. The research work involves both integrated circuit design and power electronic module packaging tasks.

Integration Motivation

- Smaller circuit parasitics (lower gate and power loop inductance) for increased efficiency
- Better control, EMI
- Higher power density
- Higher temperature operation
- Ultimately, higher reliability



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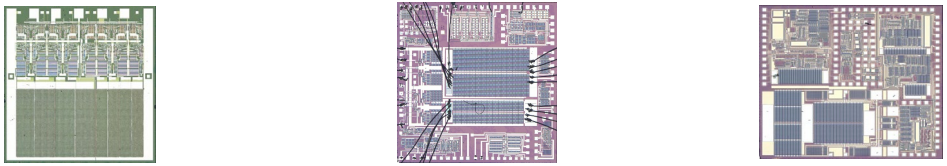
Milestones for FY21

Milestone	Type	Description
Module 3D modeling and parasitic extraction	Technical	Electrical parasitic extraction is complete, thermal performance is validated
Process and material system is validated	Technical	Process and material system is fixed
Module circuit simulation	Technical	Module in-circuit performance is validated
Motor drive system EMI modeling and basic EMI filter design	Technical	Working with motor drive design from ORNL, will develop companion EMI filter designs; will formulate filter integration plan into converter assembly layout
Go/No Go Decision Dummy module fabrication	Go/No Go	Dummy module fabrication and parasitic measurement. Design validated to support inverter target performance requirements.

Technical Accomplishments – FY21

Takeaway: Successful single-chip SiC gate driver die evaluation



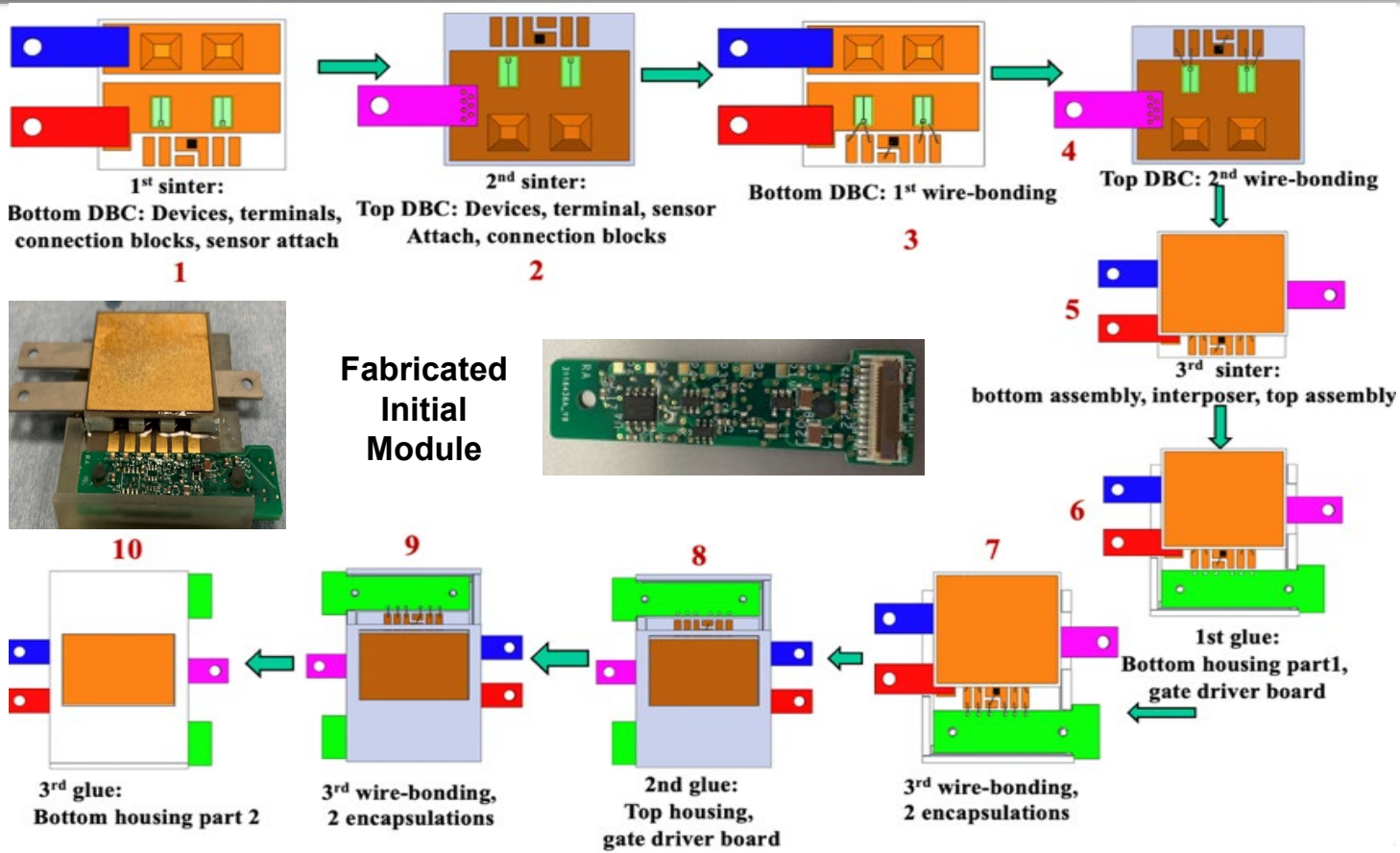
Die micrograph of SiC gate driver variant#1 (left), variant#3 (middle) and variant#4 (right). Die area 5 mm x 5 mm

Measured Performance Parameters for the SiC Gate Drivers at 200°C with 10 nF Load Capacitance

Parameters	Variant # 1	Variant # 3	Variant # 4
Driver current	2.1 A (sink)	4.14 A (sink)	4.19 A (sink)
	1.15 A (source)	2.65 A (source)	1.25 A (source)
Output voltage swing	~ 14.98 V to -3.97 V	~14.98 V to -3.99 V	~ 14.9 V to -3.99 V
Propagation Delays	472 ns (Falling)	564.3 ns (Falling)	136.6 ns (Falling)
	497 ns (Rising)	442 ns (Rising)	185.2 ns (Rising)
Rise and Fall Times	294 ns (Falling)	180 ns (Falling)	172 ns (Falling)
	687 ns (Rising)	402 ns (Rising)	529 ns (Rising)

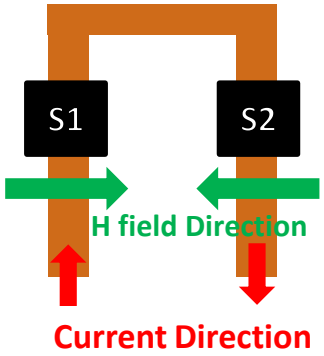
Technical Accomplishments – FY21

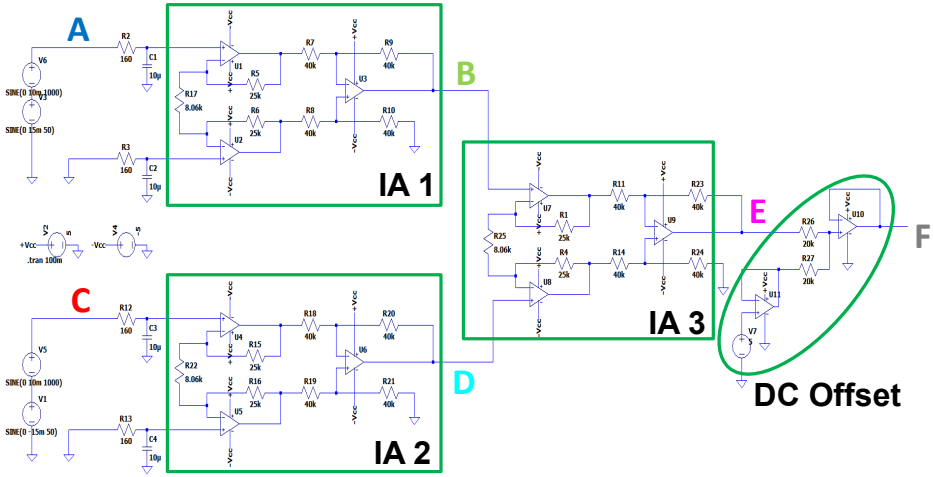
Takeaway: Fabrication flow for double-sided stacked power module



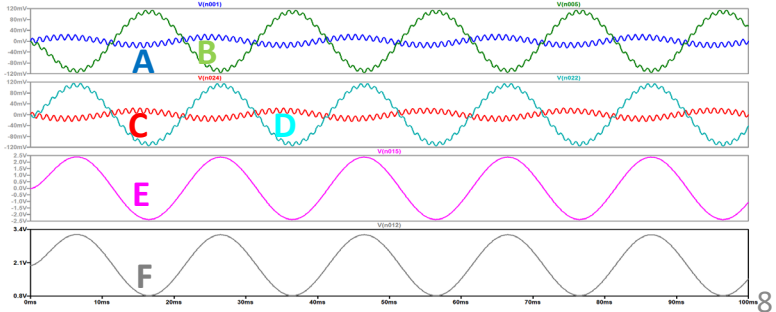
Technical Accomplishments – FY21

Takeaway: Integrable signal conditioning circuit for current measurement





- Three instrumental amplifiers included in the design
- DC offset circuit for shifting the output above 0 V to make output compatible with unipolar ADC in microcontroller
- Circuit can reduce the effect of external noise for accurate current measurement



Collaboration and Coordination with other Institutions

Virginia Tech

- Design of double-side cooled power module with DBC/IMS
- Processing and characterization of sintered-metal interconnect
- Packaging of high-temperature gate driver

Oak Ridge National Laboratory

- High performance liquid cooled heat sink design
- Insulated metal substrate development for single and double sided packaging
- System integration and evaluation

Stony Brook University

- Experiment and modeling investigation of integrated current sensing solutions
- Study of EMI modeling and EMI filter design

Proposed Future Work – FY 22

➢ **High Temperature Gate Driver Design for Heterogeneous Integration:**

- To design, fabricate and test next version of high-temperature gate driver with higher current sinking and sourcing capabilities and integrated protection features

➢ **High Power Density Power Module Design:**

- To design power module with integrated gate driver and decoupling capacitor
- Power module assembly and testing

➢ **Integrated Solutions for Power Module**:

- To implement the noise immune integrated current sensing method and signal processing circuits inside the power module

Any proposed future work is subject to change based on funding levels.

Summary

Approach

- To design a high power density power module
- Integration of high-temperature gate driver, decoupling capacitors, current sensing solutions and cooling technique into the module

Technical Accomplishments

- High temperature SiC gate driver bare die test and evaluation
- Development of fabrication process flow for double-sided stacked power module and dummy module fabrication
- Signal conditioning circuit design for current measurement with higher sensitivity and noise immunity

Future Plan

- To design and test next version of high-temperature, single-chip gate driver
- To design integrated power module with all the possible integration solutions studied for gate driver, decoupling capacitors, current and temperature sensors

Any proposed future work is subject to change based on funding levels

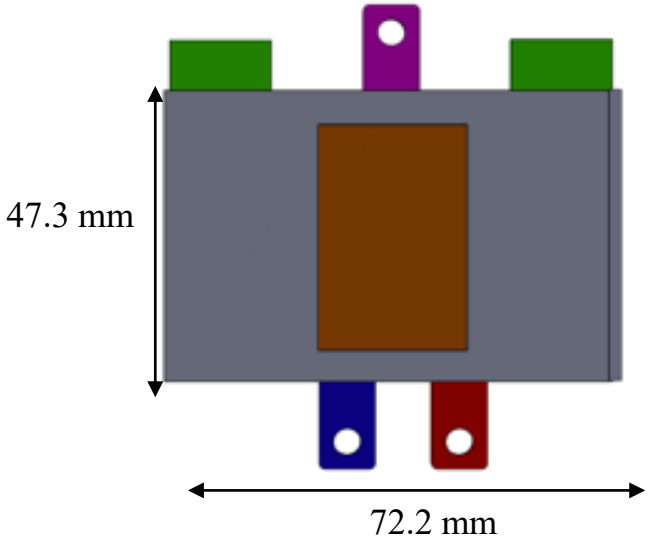
Technical Back – Up Slides

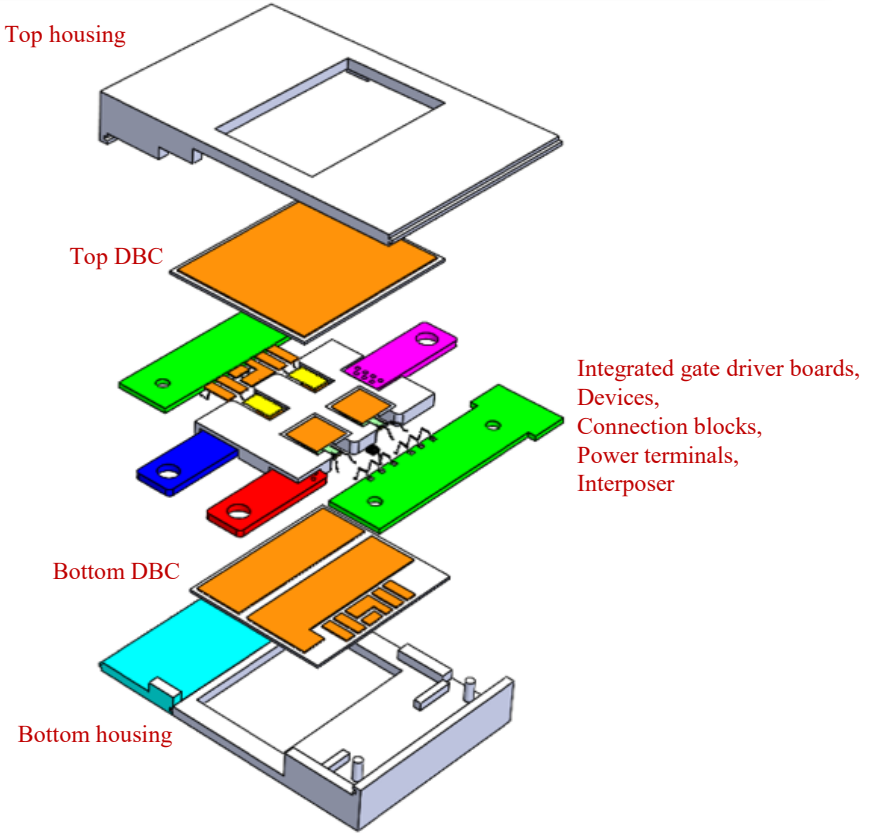
Technical Back-up Slides

Double-sided stacked power module design

Pros:
- Integrated gate driver module
- Better thermal performance

Cons:
- Complicated housing design
- Need gate electrode wire bonding





Top view and exploded view of the power module

Technical Back-up Slides

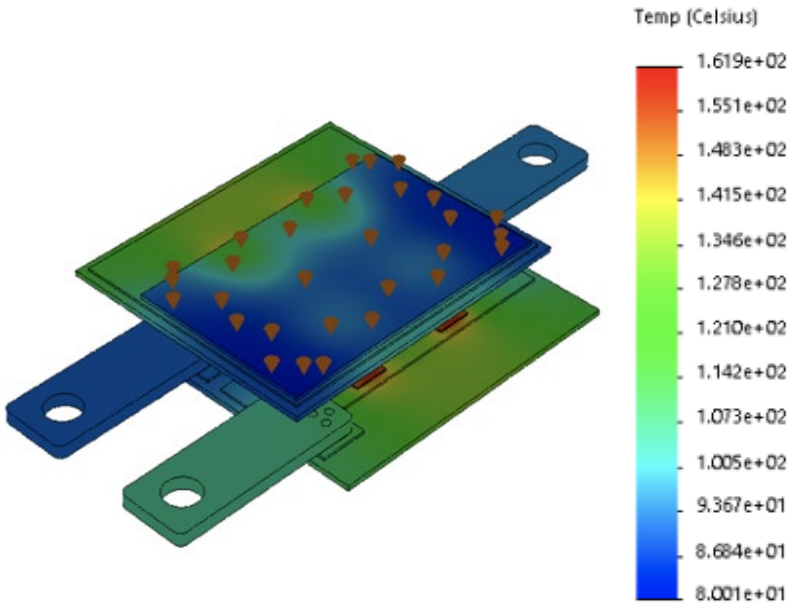
Electrical and thermal characteristics of the power module

Electrical characteristics

Specification	Value
Voltage	1200 V
Current	160 A @ T_j=160°C
Stray Inductance	6 nH

Thermal characteristics

Thermal Load	Value
Power (Per Item) (W)	145
Die Internal Resistance (mΩ)	13
Convection Coefficient (W/m²K)	10,000
Ambient Temperature (°C)	65
TIM Thermal Conductivity (W/mK)	9.6



Thermal simulation

Technical Back-up Slides

Performance comparison of GMR current sensors

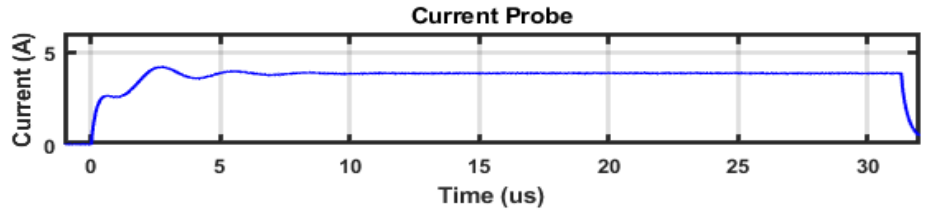
- Test results of two GMR current sensors from two different manufacturers
- Difference in rise time
- DS 10.2 from Tell-i follows the current probe accurately
- Error in ACS70331 from Allegro current measurement
- Undershoot in case of high di/dt has been predicted in ACS70331‘s datasheet
- Error of the ACS70331 current sensor can be compensated in less than 0.5 µS

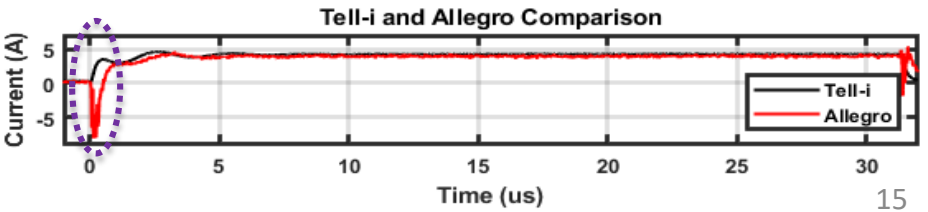
Tell-i GMR current sensor

Characteristic	Value
Bandwidth	DC-10MHz
Current Range	--10 A to 10 A
Output Offset Voltage	2.5V
Sensitivity	63.7 mV/A
Temperature	-40 to 125 ºC

Allegro GMR current sensor

Characteristic	Value
Bandwidth	DC-1MHz
Current Range	-5A to 5 A
Output Offset Voltage	1.5V
Sensitivity	200 mV/A
Temperature	-40 to 85 ºC

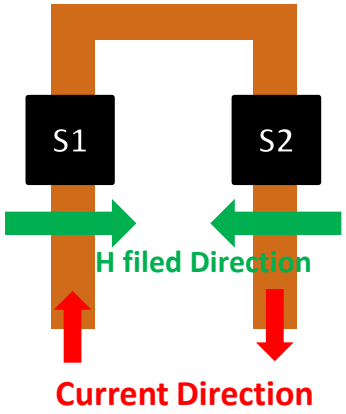


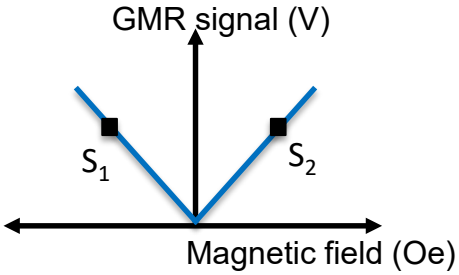


Technical Back-up Slides

Configuration of an accurate current measurement method

- Sensors can sense same magnitude of H-field with reverse direction
- Feeding sensors using instrumentation amplifier will result in:
  - $\Delta U=(K_{S1}.H_1+S_1.\Delta T+K_{S1}.H_{ext})-(K_{S2}.H_2+S_2.\Delta T+K_{S2}.H_{ext})$
  - $\Delta U=(K_{S1}+K_{S2}).H_1+(S_1-S_2).\Delta T+(K_{S1}-K_{S2}).H_{ext}$
  - $\Delta U=(K_{S1}+K_{S2}).H_1=(K_{S1}+K_{S2}).CI=SI$
  - *KS1* and *KS2*: Sensitivity of sensors
  - *S1.ΔT* and *S2.ΔT*: Effect of Temperature Fluctuation
  - *S*: Sensitivity of the Differential Measurement System
- Higher sensitivity and immunity from external noise and temperature fluctuation can be achieved





C. Mușuroi *et al*, "High Sensitivity Differential Giant Magnetoresistance (GMR) Based Sensor for Non-Contacting DC/AC Current Measurement," *Sensors (Basel, Switzerland),* vol. 20, *(1),* pp. 323, 2020.