Integrated Electric Drive System (Keystone Project #3)

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Overview

Timeline
- Start – FY19
- End – FY24
- 53% complete

Budget
- Total project funding
  - DOE share – 100%
- Funding for FY21: $420K

Barriers
- Integration of inverter and motor to achieve high power density electric drive
- Identification, evaluation, and integration of high energy density capacitor technologies
- Meeting DOE ELT 2025 integrated drive power density target of 33kW/L

Partners
- National Renewable Energy Laboratory (NREL)
- Sandia National Laboratories (SNL)
- Ames Laboratory
- ORNL team members: Shajjad Chowdhury, Emre Gurpinar, Tsarafidy Raminosoa, Gui-Jia Su, Jon Wilkins, and Burak Ozpineci
Project Relevance

• Overall Objective:
  – Research technologies that will allow the integration of the inverter with the motor resulting in a high-power density integrated traction drive
  – The project results from Keystone Projects #1 and #2 will be fed into this project for an iterative approach

• FY21 Objectives:
  – Assess feasibility of the proposed internal stator mount integration technique
  – Evaluate capacitor packaging techniques to improve electrical performance
  – Optimize power electronic substrate area to fit inside the outer rotor motor
<table>
<thead>
<tr>
<th>Date</th>
<th>FY 2021</th>
<th>Milestones and Go/No-Go Decision</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1</td>
<td>FY 2021</td>
<td><strong>Milestone:</strong> Experimentally evaluate high voltage PLZT capacitors</td>
<td>Completed</td>
</tr>
<tr>
<td>Q2</td>
<td>FY 2021</td>
<td><strong>Milestone:</strong> Optimize capacitor packaging to complement wide bandgap devices while keeping the electric drive power density within consortium target</td>
<td>Completed</td>
</tr>
<tr>
<td>Q3</td>
<td>FY 2021</td>
<td><strong>Milestone:</strong> Optimize power module area and identify cooling solutions for the inverter to integrate with the outer rotor motor</td>
<td>On track</td>
</tr>
<tr>
<td>Q4</td>
<td>FY 2021</td>
<td><strong>Go/No-Go Decision:</strong> If power module and heatsink fits inside the available volume then start designing other inverter components</td>
<td>On track</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Date</th>
<th>FY 2022</th>
<th>Milestones and Go/No-Go Decision</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1</td>
<td>FY 2022</td>
<td><strong>Milestone:</strong> Build a test setup to evaluate current sensors and select one to optimize volume</td>
<td>On track</td>
</tr>
<tr>
<td>Q2</td>
<td>FY 2022</td>
<td><strong>Milestone:</strong> Prototype and evaluate optimized substrate</td>
<td>On track</td>
</tr>
<tr>
<td>Q3</td>
<td>FY 2022</td>
<td><strong>Milestone:</strong> Develop a single-phase power module integrating, gate drivers, current and voltage sensors, busbars, and connectors</td>
<td>On track</td>
</tr>
<tr>
<td>Q4</td>
<td>FY 2022</td>
<td><strong>Go/No-Go Decision:</strong> If the developed module fit inside the motor, then start building the six-phase inverter for integration</td>
<td>On track</td>
</tr>
</tbody>
</table>
Approach/Strategy

• Assess internal dimensions for outer rotor motor for power electronics integration

• Identify required capacitor parameters and then design and characterize capacitor packages to fit inside the available space while optimized for performance

• Evaluate required cooling performance for the power module and estimate minimum dimensions to keep the device temperature within the manufacturer specified limits

Any proposed future work is subject to change based on funding levels
Technical Accomplishments – FY21

Cooling system design for the proposed integrated drive – ORNL and NREL collaboration

ORNL and NREL are working together to understand the impact of integrating inverter with the motor to achieve high power density target

**ORNL**
- Proposed internal stator mount integration solution to achieve DOE 2025 target
- Identified motor currents, voltages, and phase angles for the full operating range
- Estimated inverter losses based on 1.2kV SiC MOSFETs

**NREL**
- Developed cooling concepts for the proposed internal stator mount integration technique
- Designed heat exchanger for internal stator mount integration

**Internal stator mount integration**

**Inverter loss**

- Designed heat exchanger for motor and inverter cooling for internal stator mount integrated drive

**Bidzina Kekelia and Emily Cousineau – NREL**

2021 VTO AMR Peer Evaluation Meeting
Technical Accomplishments – FY21
Developed an analytical model of the outer rotor motor

Steady-state surface mount PM-motor model for loss estimation

When \( I_d = 0 \), Phase current

\[
T_e = \frac{3}{2} P \frac{2}{2} i_q \Psi_m
\]
\[
I = i_q = \frac{T_e \frac{2}{2} \frac{2}{3} P}{\Psi_m}
\]

Phase voltage

\[
V_d = i_d R \times L_d \frac{di_d}{dt} - \omega_e L_q i_q
\]
\[
V_q = i_q R \times L_q \frac{di_q}{dt} + \omega_e L_d i_d + \omega_e \Psi_m
\]
\[
V = \sqrt{(-\omega_e L_q i_q)^2 + (i_q R + \omega_e \Psi_m)^2}
\]

Power factor

\[
\varphi = 90 - \cos^{-1} \left( \frac{V_d}{V} \right)
\]

Results

Motor torque vs speed

Motor peak current

Motor power factor angle

Motor phase voltage

Maximum current [475A] and maximum phase angle occurs at 6.6kRPM at 100kW power.
Technical Accomplishments – FY21

Calculated inverter loss

Device selection and loss estimation for segmented inverter
- Selected 1200V, 17mohm SiC MOSFET dies
- Paralleled two devices to handle the required motor current
- Used datasheet conduction losses for loss evaluation
- Calculated switching losses using experimental results

Device parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Die</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Blocking voltage, $V_{DS}$</td>
<td>1200</td>
<td>V</td>
</tr>
<tr>
<td>$R_{DS} @ 150^\circ C$</td>
<td>19.5</td>
<td>mΩ</td>
</tr>
<tr>
<td>$I_{DS} @ 100^\circ C$ case</td>
<td>102</td>
<td>A</td>
</tr>
<tr>
<td>DC bus, $V_{dc}$</td>
<td>800</td>
<td>V</td>
</tr>
<tr>
<td>Switching, $f_{sw}$</td>
<td>30</td>
<td>kHz</td>
</tr>
<tr>
<td>Die temp, $T_j$</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Maximum estimated inverter loss is 2500W for a 100kW system. Including a safety margin, 3000W will be considered for cooling system design.

Technical Accomplishments – FY21

Identified cooling requirements of the power module

**Direct bonded copper (DBC) based power module**

- Designed a half bridge module considering two dies in parallel
- Utilized an AlN based ceramic insulator to achieve low thermal resistance
- Soldered SiC MOSFETs on the substrate

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**Image Description**

- Copper 0.3 mm
- SiC Chip – 400 W/cm²
- Solder
- AlN 150 W/m·K
- Thermal interface 0.25mm, 20 W/m·K

**DBC structure considered for FE simulation**

- Designed substrate to estimate required heat transfer coefficient (HTC)

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**The module requires 10kW/m²·K to keep the device temperature at 150°C.**
Technical Accomplishments – FY21

Evaluated capacitor current requirements

A segmented inverter reduces capacitor current stress significantly; thus, utilized for this project.

Segmented inverter

Capacitor current stress

Segmented inverter

Capacitor current FFT

DC link current components are at 120kHz for triangular modulation; thus, capacitance requirement will be minimum.
Technical Accomplishments – FY21

Estimated capacitance for the segmented inverter

Total capacitor current

\[ i_c = C \frac{dV}{dt} \]

\[ \int i_c \, dt = CV = Q \]

Required capacitance, \( C = \frac{\int i_c \, dt}{V} \)

Where, \( V \) is the ripple voltage which is defined by user, \( \int i_c \) is constant if load current, power factor, and modulation index are fixed

Required DC link capacitance various topologies and modulation techniques

<table>
<thead>
<tr>
<th>Topology</th>
<th>Modulation</th>
<th>Maximum RMS current for all frequency</th>
<th>Capacitor current frequency</th>
<th>Required Capacitance at 5% voltage ripple</th>
</tr>
</thead>
<tbody>
<tr>
<td>Segmented</td>
<td>Triangular</td>
<td>113 A</td>
<td>120kHz</td>
<td>15 ( \mu F )</td>
</tr>
<tr>
<td></td>
<td>Sawtooth</td>
<td>115 A</td>
<td>60, 180kHz</td>
<td>25 ( \mu F )</td>
</tr>
<tr>
<td></td>
<td>Bus clamped SVPWM</td>
<td>113 A</td>
<td>60kHz</td>
<td>21 ( \mu F )</td>
</tr>
<tr>
<td>Three phase</td>
<td>Triangular</td>
<td>198 A</td>
<td>60, 120kHz</td>
<td>38 ( \mu F )</td>
</tr>
<tr>
<td></td>
<td>Sawtooth</td>
<td>225 A</td>
<td>30, 60, 90kHz</td>
<td>82 ( \mu F )</td>
</tr>
<tr>
<td></td>
<td>Bus clamped SVPWM</td>
<td>204 A</td>
<td>30, 60kHz</td>
<td>73 ( \mu F )</td>
</tr>
<tr>
<td></td>
<td>Symmetrical SVPWM</td>
<td>198 A</td>
<td>60, 120kHz</td>
<td>35 ( \mu F )</td>
</tr>
</tbody>
</table>

Segmented inverter with triangular modulation requires a minimum of 15 \( \mu F \) capacitance and will have to handle 113A @ 120kHz frequency. High frequency operation will also ensure minimum capacitor losses.
Technical Accomplishments – FY20

Selected capacitor technology

<table>
<thead>
<tr>
<th></th>
<th>Film</th>
<th>PLZT</th>
<th>MLCC – Class II</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric</td>
<td>Metalized Polypropylene</td>
<td>PLZT</td>
<td>BaTiO$_3$</td>
</tr>
<tr>
<td>Temperature</td>
<td>105°C</td>
<td>150°C</td>
<td>125°C</td>
</tr>
<tr>
<td>Structure</td>
<td>Series Parallel</td>
<td>Parallel</td>
<td></td>
</tr>
<tr>
<td>Current handling capability</td>
<td>3 Amps @ 50 kHz, 85°C, 0 Amps @ 50 kHz, 105°C</td>
<td>8 Amps @ 50 kHz, 85°C, 6.5 Amps @ 50 kHz, 105°C</td>
<td>5 Amps @ 50kHz, 85°C, 3.5 Amps @ 50kHz, 105°C</td>
</tr>
</tbody>
</table>

PLZT capacitor has slightly higher volume than the MLCC for a given capacitance but can handle higher current, temperature, and has better reliability.
Technical Accomplishments – FY21
Characterized high voltage PLZT capacitor - experimental setup

Evaluation of PLZT capacitors requires a test rig with
- Two capacitors connected in series
- DC bias range of 0V – 1KV
- Temperature range -25°C – 150°C
- Frequency range 5kHz – 30MHz

High voltage measurement technique
Two port shunt through measurement

\[ V_S \]
2 capacitors in series
DC block
\[ R_C \]
\[ R_D \]
\[ V_{DC} \]
(0 – 1kV)
R_C = Charging resistor
R_D = Discharging resistor
V_{DC} = DC Bias voltage
Small signal = 1V p-p

Modified two-port-shunt-through method to characterize capacitors with high voltage bias

Technical Accomplishments – FY21
Characterized 800V PLZT capacitor – experimental results

- Impedance curves show the variation of capacitance at different bias voltages
- Maximum capacitance is 0.45 μF which is 40% less than datasheet capacitance value
- Minimum capacitance is 0.25 μF at -25°C and maximum is 0.45 μF at 75°C
- Equivalent series resistance (ESR) increases with DC bias but decreases with temperature; thus, high temperature operation is preferable
- Each capacitor can conduct 11Amps at 85kHz frequency

Minimum sixty (60) capacitors are required to achieve the 15 μF capacitance for the segmented inverter with sine triangular modulation scheme.
Technical Accomplishments – FY21

Optimized capacitor packaging – improved fill factor for circular design

- Designed a circular capacitor to fit each power module – six of them will be used in the segmented inverter
- Packaged considering 52mm x 52mm dimensions – circular capacitor

Circular capacitor package

- Exploded diagram of the designed circular package
- Cross section showing two identical current loops

Traditional flat capacitor package

- Flat capacitor boards containing 15 capacitors
- Cross section showing several current loops

Circular design has better flux cancellation due to overlapping current path and has improved fill factor than a traditional flat design (fill factor: 35% for circular and 27% for flat design)
Technical Accomplishments – FY21

Designed and assembled packaged capacitors

- Designed considering outer rotor motor dimensions
- Built two traditional flat boards for performance evaluation and comparison
- Assembled all three packages with 15 capacitors in parallel

Circular capacitor board components

- Connectors and terminals
  - DC+
  - DC-
  - Isolating sleeve
  - Screw

Assembled flat capacitor boards

- 3x5 arrays
- 5x3 arrays

Assembled circular capacitor board

- Top view
- Bottom view
- 13mm
- 52mm
Technical Accomplishments – FY21

Characterized circular capacitor

- Characterized for various operating voltages and temperatures
- Achieved best results at 800V bias and 100°C operating temperature

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volume</td>
<td>0.028L</td>
<td>Total 0.168L</td>
</tr>
<tr>
<td>Capacitance</td>
<td>4.2μF – 6μF</td>
<td>50kHz, 100°C</td>
</tr>
<tr>
<td>Theoretical current</td>
<td>More than 100 A</td>
<td>85kHz, 25°C [from datasheet]</td>
</tr>
<tr>
<td>Required current</td>
<td>20 A</td>
<td>Segmented inverter</td>
</tr>
<tr>
<td>Equivalent series resistance (ESR)</td>
<td>2.73mΩ</td>
<td>50kHz, 100°C</td>
</tr>
<tr>
<td>Equivalent series inductance (ESL)</td>
<td>3.78nH</td>
<td>10MHz</td>
</tr>
</tbody>
</table>

The designed capacitor has minimum capacitance of 25 μF and occupies only 0.17L volume for the segmented inverter.
Response to the Reviewer's Comments

• There is good collaboration. Would industry or university partners help the cause?
  • Thank you for your comment. We are currently collaborating with several national labs and universities within the consortium. We are also discussing with companies to start collaborations.

• Assessing the impact of stator heat on the inverter components will be a critical step toward successfully executing this concept architecture. Capacitor packaging will also be a key next step. So future plans as stated are sound.
  • Thank you for your comment. We are currently collaborating with NREL to assess the impact of stator heat flux on the inverter and presented some results showing the positive effect of higher temperature on capacitor parameters.

• The reviewer stated that this is a review of existing know-how and reports, followed by simulation and prototyping to obtain power-dense drivetrain system—it looks like an appropriate approach for this project.
  • Thank you for your comment. We are looking into component level volume minimization and tight integration techniques to minimize the overall traction drive volume. One of the major outcomes is the minimization of the DC link capacitor to 0.17L compared to 0.6 liter for 2016 BMW-i3’s traction drive capacitor.
## Collaboration

<table>
<thead>
<tr>
<th>Organization</th>
<th>Type of Collaboration</th>
</tr>
</thead>
<tbody>
<tr>
<td><a href="https://www.nrel.gov">NREL</a></td>
<td>Working on thermal analysis of the integrated electric drive systems</td>
</tr>
<tr>
<td><a href="https://www.sandia.gov">Sandia National Laboratories</a></td>
<td>Will provide wide bandgap device models and samples when they are available</td>
</tr>
<tr>
<td><a href="https://www.ameslab.gov">AMES Laboratory</a></td>
<td>Providing properties of newly developed magnetic materials for the traction motor drive.</td>
</tr>
</tbody>
</table>
Remaining Challenges

• Identify the optimum substrate area for the estimated inverter operating conditions
• Assess the feasibility of the proposed internal stator mount integration
• Identify a suitable place to integrate output current sensors, input voltage sensors, busbars, and identify low profile connectors for terminations
Proposed future work

• **Remainder of FY21**
  - Evaluate substrates to identify minimum substrate area for the estimated losses
  - Characterize the flat capacitor boards and identify current conduction capability of the designed capacitor packages

• **Future work – FY22**
  - Build a DBC based substrate to fit within the identified space inside the outer rotor motor
  - Characterize different current sensors, select one, and integrate with the inverter
  - Build and characterize a single phase leg power module

Any proposed future work is subject to change based on funding levels
Summary

• Relevance: The core function of this project is to research technologies that will allow the integration of inverter with the motor to meet DOE ELT 2025 power density target of 33kW/L for a 100kW integrated electric drive.

• Approach:
  – Identify ways to fit the inverter components inside the designed outer rotor motor to achieve tight integration
  – Characterize and package capacitors to identify promising capacitor technology for volume along with electrical performance optimization
  – Optimize substrate dimensions for the estimated inverter loss

• Collaborations:
  – NREL: Designing cooling structures for internal stator mount integration technique
  – Interactions are ongoing with Sandia and AMES

• Technical Accomplishments:
  – Identified available dimensions for inverter integration with outer rotor motor
  – Designed circular capacitor package with emerging PLZT based capacitor to optimize volume and performance
  – Estimated inverter losses for the designed outer rotor motor
  – Evaluated a DBC based substrate for the proposed integration method

• Future Work:
  – Complete the DBC based substrate analysis to evaluate minimum substrate area for the estimated inverter losses
  – Evaluate flat capacitor boards and identify current conduction capability of the designed packages

Any proposed future work is subject to change based on funding levels