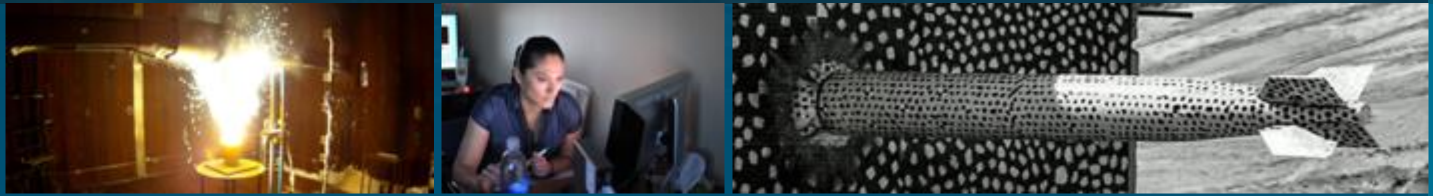
Development of Next-Generation Vertical GaN Devices for High-Power-Density Electric Drivetrain



Andrew Binder, Co-PI, Power Electronics

Sandia National Laboratories

June 22, 2021

Project ID: ELT210

Overview

Timeline

- Start – FY19
- End – FY23
- 50% complete

Budget

- Total project funding
  - DOE share – 100%
- Funding received in FY19: $550k
- Funding for FY20: $700k
- Funding for FY21: $695k

SUNY Poly
Albany Campus

Goals/Barriers

- **Device performance target = 1200 V/100A**
- Power Electronics Density = 100 kW/L
- System Power target > 100 kW (~1.2kV/100 A)
- Cost target for Electric Traction Drive system ($6/kW)
- Operational life of Electric Traction Drive system = 300k miles
- Barriers:
  - Relative immaturity of GaN-based vertical devices (performance/reliability)
  - Relative immaturity of new passive materials (performance/reliability)

Partners

- ORNL
- NREL
- SUNY – Woongje Sung
- Ohio State – Anant Agarwal
- Jim Cooper
- Jon Wierer – Lehigh University
- Project Lead: Sandia Labs, Team Members: Jack Flicker (Co-PI), Todd Monson, Bob Kaplar

Relevance and Objectives

Objectives

- Develop power electronics components to reach the power density targets of > 100 kW (~ 1.2 kV/100A) and 100 kW/L
- Power electronics performance targets enable overall system performance targets for the Electric Traction Drive system of 33 kW/L, $6/kW, and > 300k mile operation lifetimes
- **Third year objectives**:
  - GaN efforts focused on device design/simulation, process development, & Gen2 device demonstration
  - SiC efforts focused on COTS device evaluation, design improvement and device fabrication for automotive environments (led by consortium partners)

Impact

- Enabling advanced future Electric Traction Drive vehicles which contributes directly to clean energy transportation
- Wide bandgap (SiC and GaN) power devices enable higher power densities (reduced size and weight) and higher operating frequencies
- Higher operating frequencies enable size and weight reduction for passive devices (capacitors and inductors) in power circuits
- Efforts directly address technology barriers for power electronics and Electric Traction Drive power density targets

FY21 Milestones

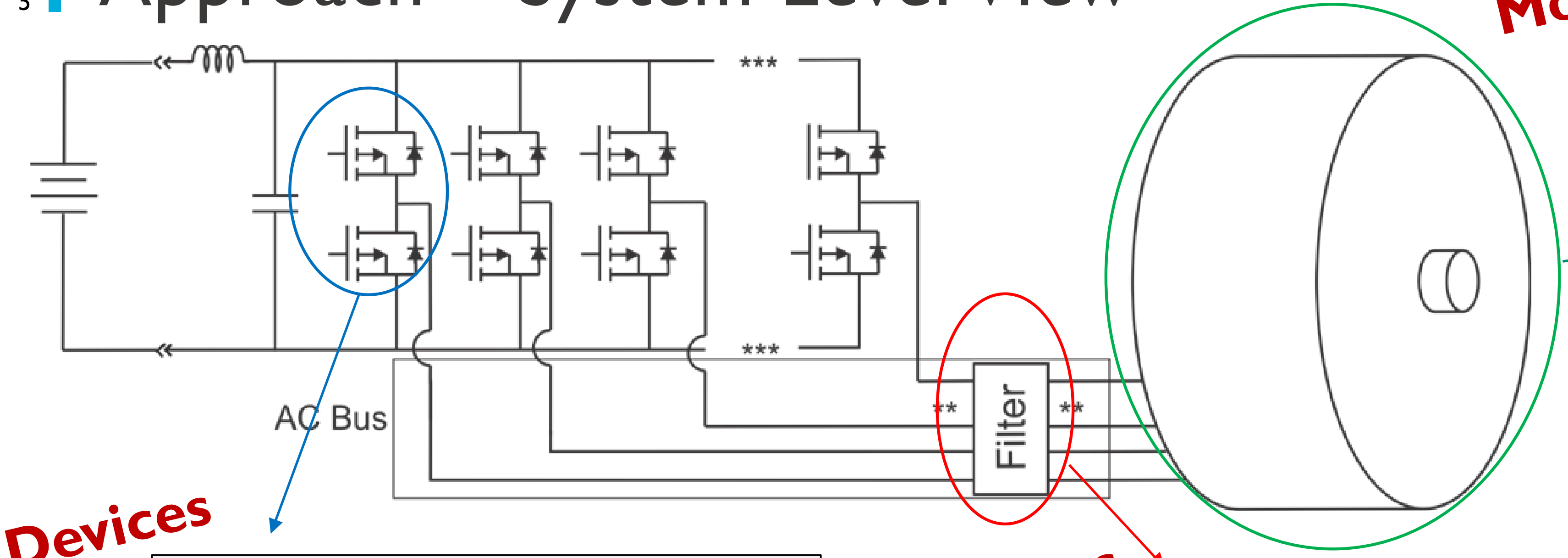
Milestone	Date	Status
Refine and calibrate device-level numerical models of vertical GaN MOSFETs. Refine and improve on 1st-generation vertical GaN MOSFET process and characterize performance.	9/2021	**On Track**
Refine and calibrate device-level numerical models of vertical GaN diodes. Refine and improve on 1st-generation vertical GaN Junction Barrier Schottky diodes and characterize performance.	9/2021	**On Track**
Evaluate existing designs for SiC JBS and MOSFET devices and determine feasibility for analog designs and fabrication process for v-GaN devices.	12/2020	**Complete**

FY22 Milestones (tentative)

Milestone
GaN MOSFET – Demonstrate 600 V reverse holdoff and 1.0 A forward current.
GaN JBS Diode – Demonstrate 1200 V reverse holdoff at less than 1 μA leakage and 1.0 A forward current.
Evaluate GaN devices in test bed using realistic usage scenarios as appropriate.

Any proposed future work is subject to change based on funding levels.

Approach – System Level View



Motors

- Increased power density
- Higher speed operation
  - Reduced size/weight

ELT216: Todd Monson
Iron Nitrides

ELT222: Jack Flicker
Ceramic Capacitors

Devices

- Higher critical elec. Field
  - Increased efficiency
- Higher frequency operation
  - Increased power density
  - Reduced size/weight

Passives

- Composite materials for improved inductors
- Improved capacitor lifetime, operating modes
- Higher frequency operation
- Reduced size/weight

System

ELT223: Jason Neely
Component Testing

- Characterization of devices, passives, and motors
- Sandia National Labs efforts span multiple levels within system design

Approach – Materials for Power Electronics

Stage 1:
SiC MOSFET + SiC Diode

Stage 2:
SiC MOSFET + GaN Diode

Stage 3:
GaN MOSFET + GaN Diode

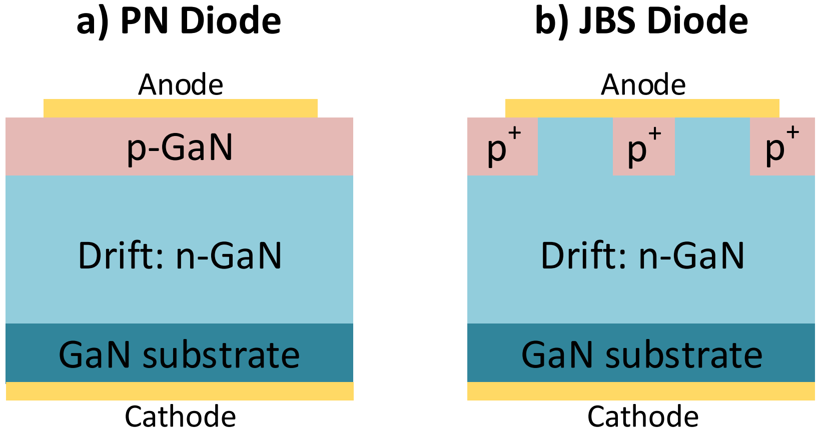
Device modeling, circuit simulation at each stage.

Characterization and evaluation of device technology in test bed at each stage.

Any proposed future work is subject to change based on funding levels.

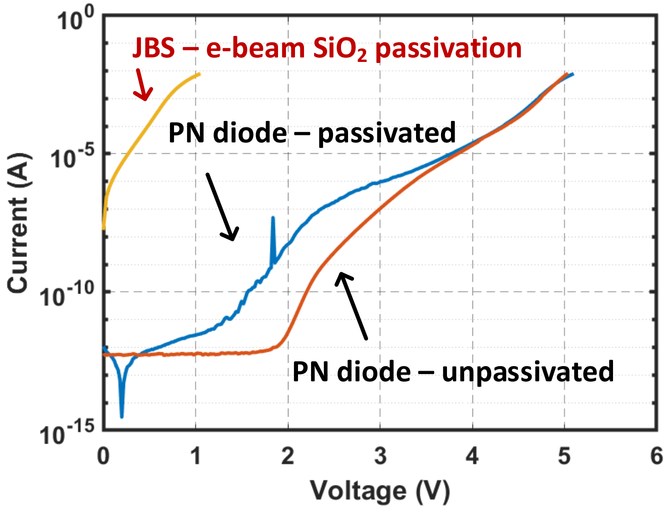
Technical Accomplishments and Progress – JBS Diode

- Previous JBS process demonstrated ~ 1.5 kV breakdown but had leaky reverse current
- Identified two components to JBS leakage
  - Surface leakage from passivation
  - Junction leakage from etch-and-regrowth
- Implemented PN diode experiments to focus on improving passivation and etch-and-regrowth processes
- Surface leakage can be eliminated by not including a passivation layer
  - Presently evaluating new passivation processes that do not add substantial leakage current
- Studying etch-and-regrowth processes to improve on process of record
  - Process of record remains the best approach out of many tried
  - Continuing to iterate to find a better result

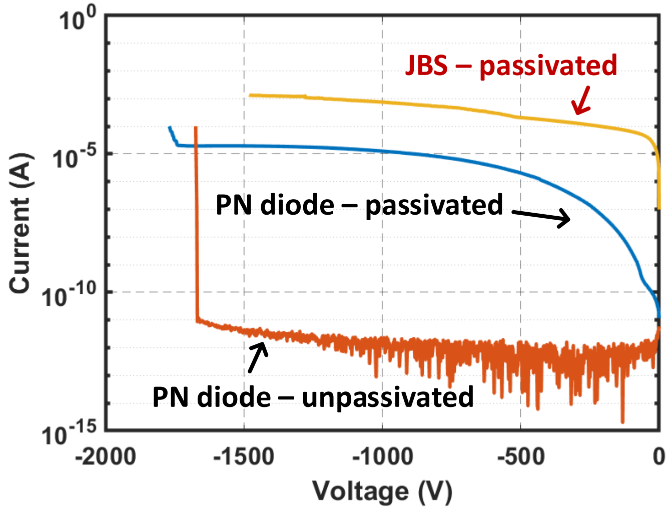

a) PN Diode

b) JBS Diode

Forward IV Diode Behavior

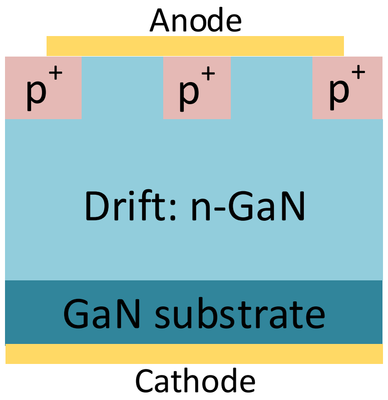


Reverse IV Diode Behavior



Technical Accomplishments and Progress – Schottky Diode

JBS Diode

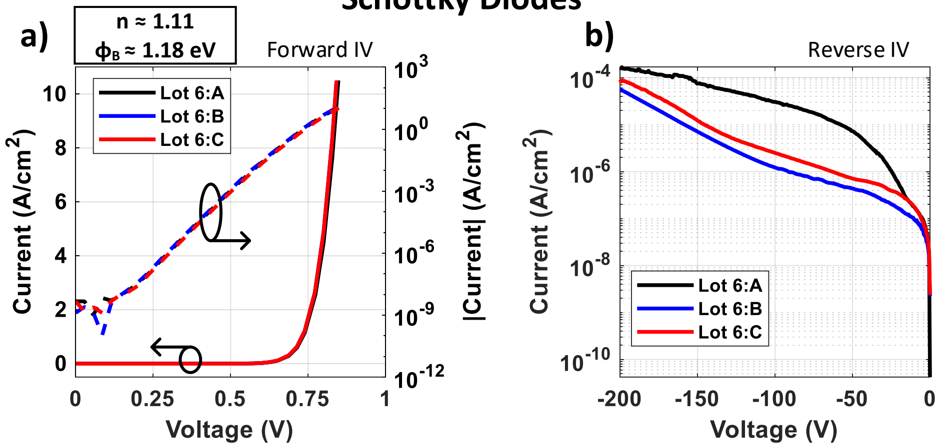


JBS

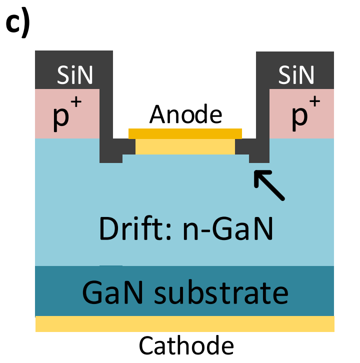
- Added JTE to improve breakdown characteristics
  - Effect is overshadowed due to junction and surface leakage
- Tested various surface treatments prior to regrowth
  - AZ400K plus UV-Ozone produced the best results

- Schottky test structures on JBS wafer lot showed good performance
  - Ideality factor and barrier height are aligned with expectations for Pd Schottky contact on GaN

Schottky Diodes



Schottky Test Structure

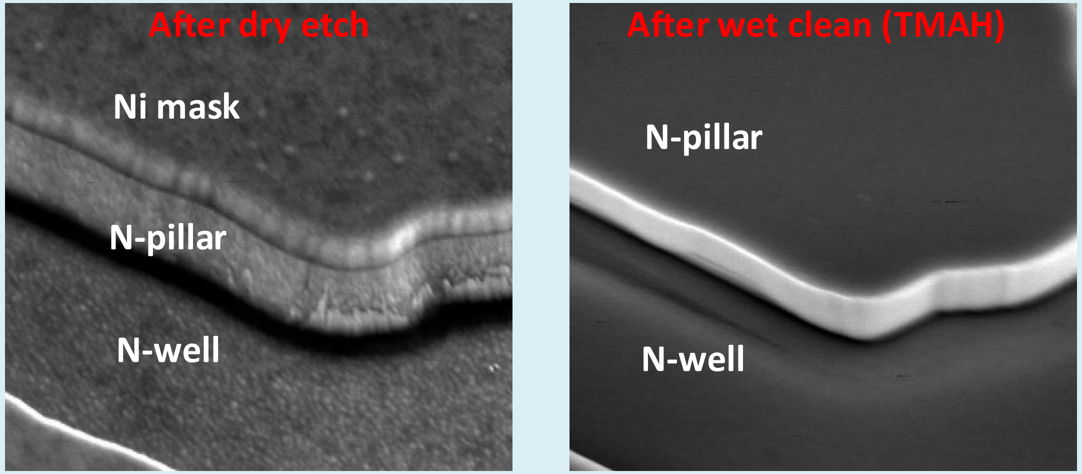


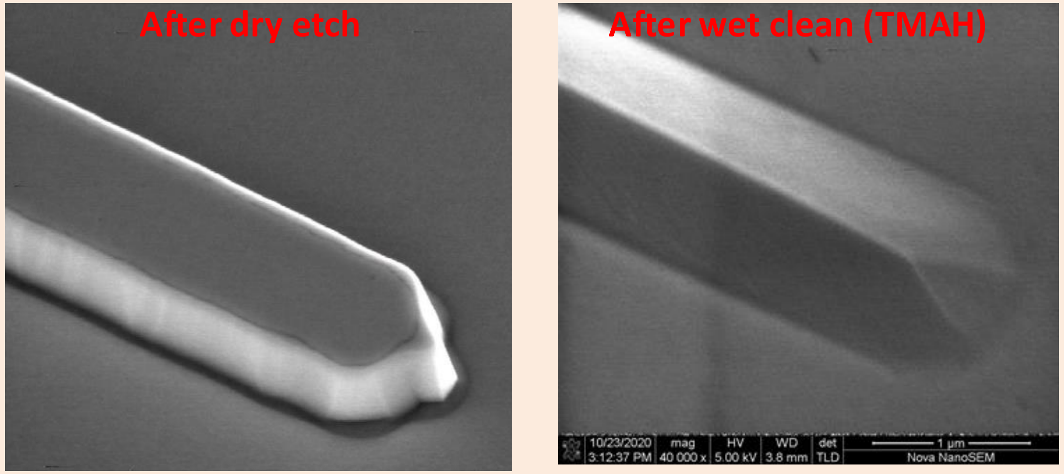
Technical Accomplishments and Progress – Process Development

- Developed and characterized new methods for forming JBS and MOSFET trenches
  - Tested various crystallographic etches (TMAH, AZ400K) and several masking methods
- Nickel masking proved important for maintaining feature integrity after crystallographic etch
- Vertical sidewalls can be obtained using AZ400K or TMAH elevated temperature etches

Process development of JBS etch process on GaICP tool

Ni Mask



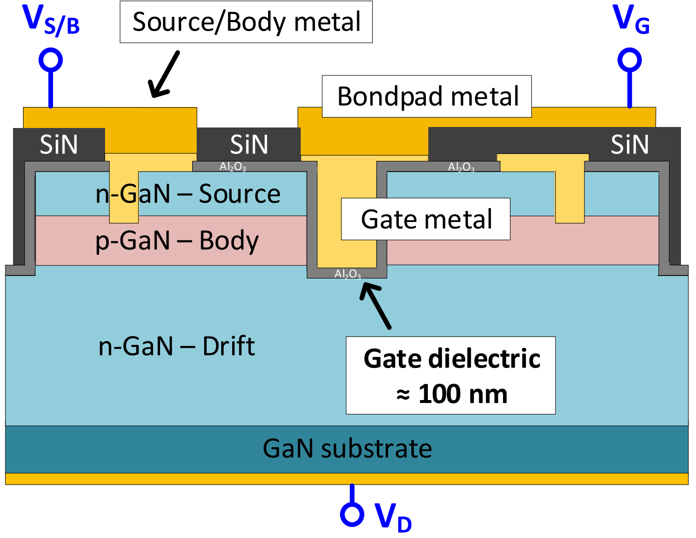


Photoresist Mask

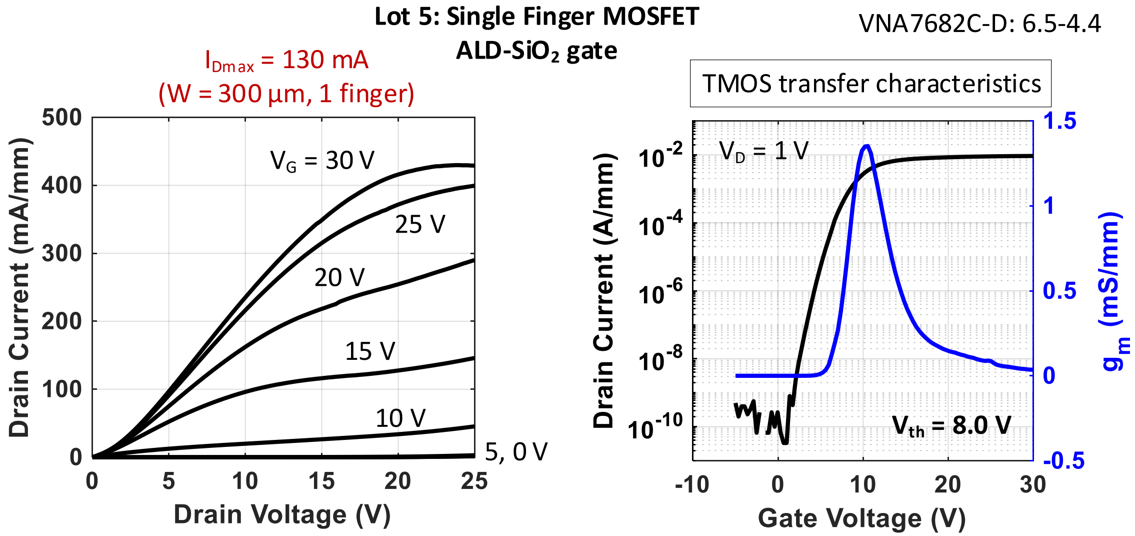
Technical Accomplishments and Progress - MOSFET

1st Gen Demonstrated

- Successfully demonstrated 1st Gen MOSFET on vGaN platform
  - Developed gate dielectrics for MOS platform
    - ALD-Al_2O_3 and ALD-SiO_2
  - Refined trench etch process for deep MOSFET trenches with vertical sidewalls



- Demonstrated 130 mA operation on a single finger device (300 µm gate width)
  - > 400 mA/mm
  - Four-finger devices capable of > 0.5 A operation



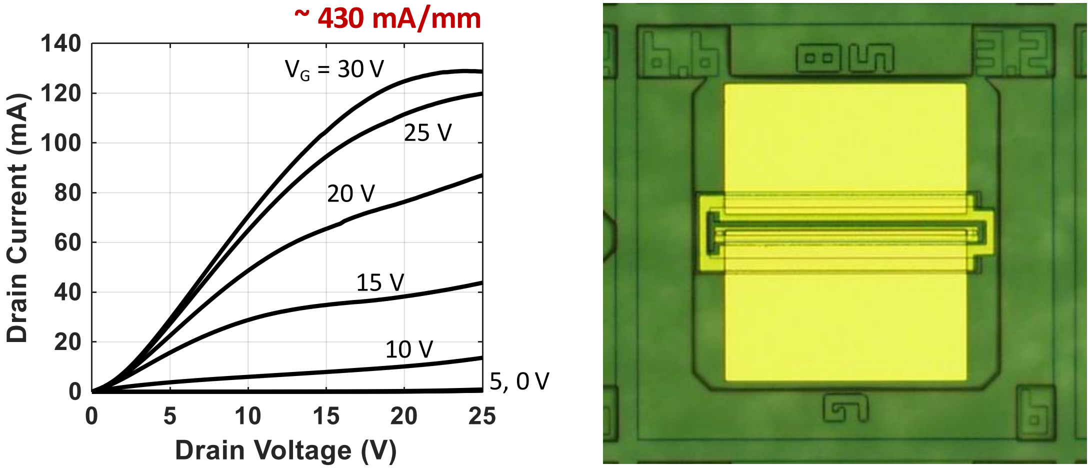
Technical Accomplishments and Progress – Current Scaling

- Using a multi-finger approach to scale to high current
  - Presently have single-finger and four-finger layouts
- Added experimental HEX-FET design to test a more compact layout

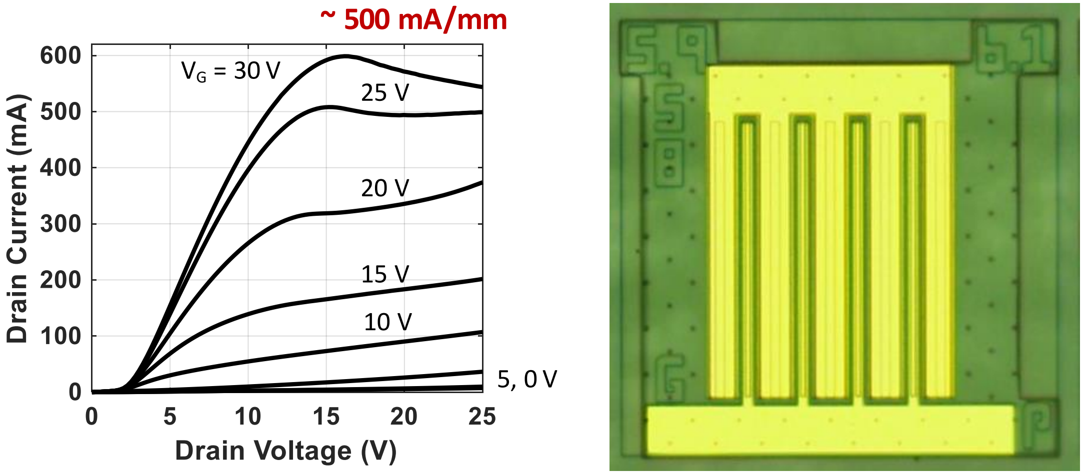
- Need **5 mm** device width → **2 A** operation
  - Based on Lot 5 performance (>400 mA/mm)
  - 7.5 mm → 3 A operation

- Updated MOSFET mask to increase device width for high current operation
  - W_G = 1.5, 4, 10 mm
- Expect to improve on 400 mA/mm performance for future lots

Single Finger MOSFET (W_G = 0.3 mm)



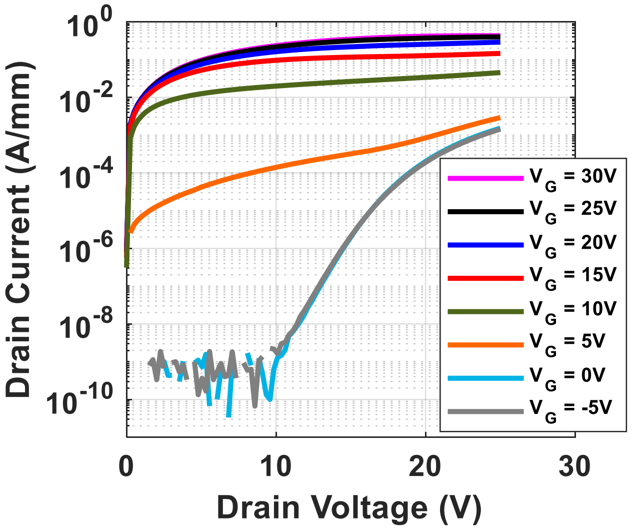
Multi-Finger (High Current) MOSFET (W_G = 1.2 mm)



Technical Accomplishments and Progress – MOSFET Breakdown

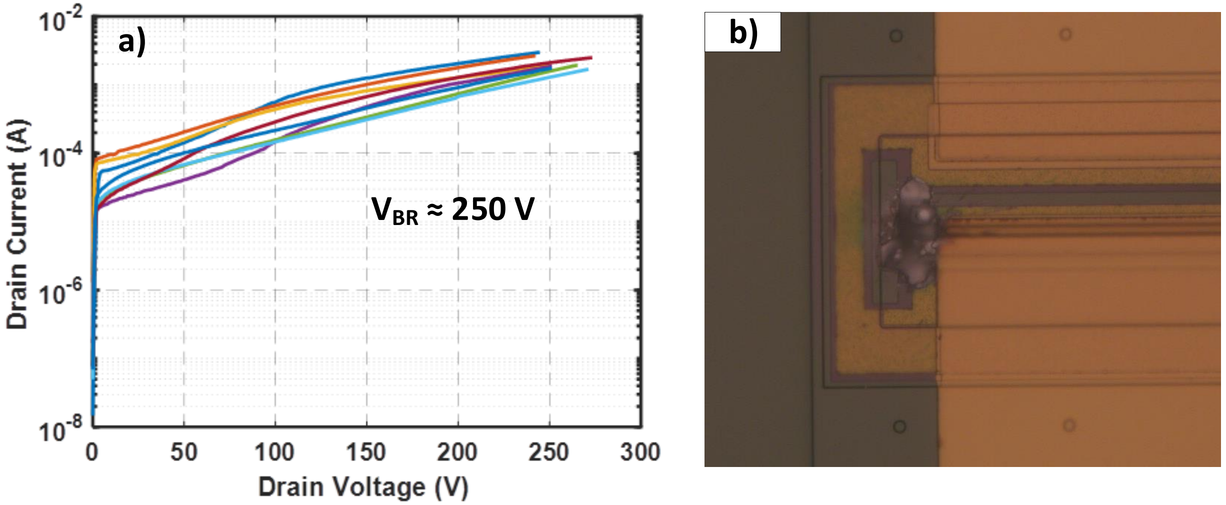
First gen. devices demonstrated issues with low bias leakage
  - Passivation leakage issue much like for JBS/PN diode
  - Using PN diode platform to improve passivation

Devices able to hold off ~ 250 V but at high leakage currents



- Devices show non-trivial threshold voltage shift depending on bias condition
  - Working on improving ALD dielectric and surface preparation strategies
  - Also working on etch damage removal methods for trench sidewalls

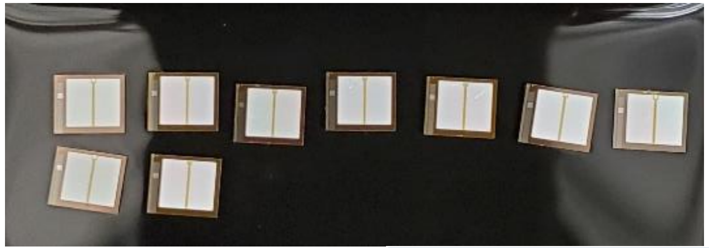
MOSFET Breakdown Result



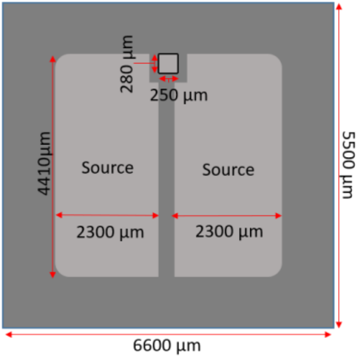
Technical Accomplishments and Progress – Testbed Development

- Need **rapid prototyping** for R&D devices
- Data on performance and reliability for input in future generations of components
- Realistically emulate operations and stressors that exist in end-use application but can be scaled in parameters (voltage, current, temperature, etc.) to suit intermediate maturity devices
- Developed brushless DC motor drive test-bed to evaluate performance of fabricated devices.
  - 1000 V, 10 A
  - Fully controllable voltage/current stress
  - Replicate motor dynamics

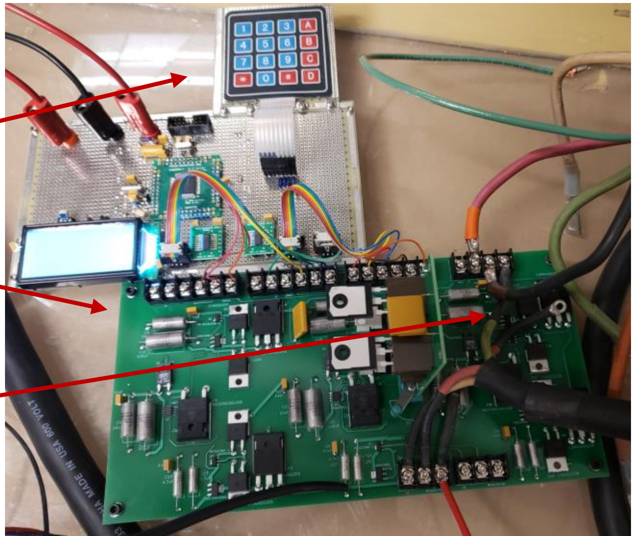
Jack Flicker - SNL



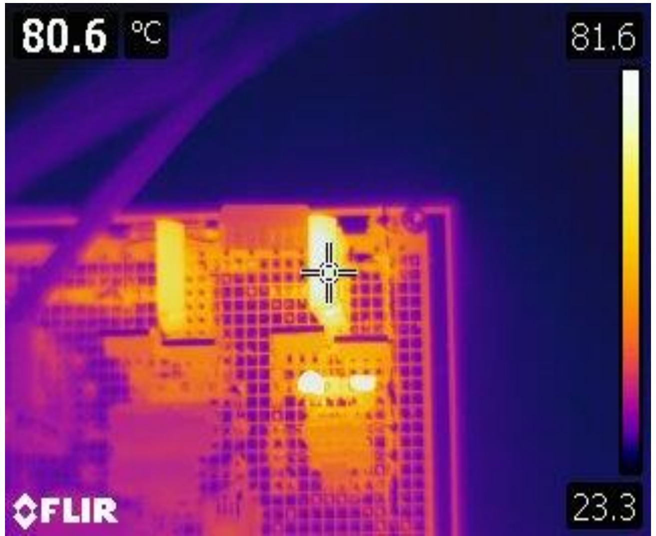
SUNY Fabricated SiC MOSFETs for testing in circuit



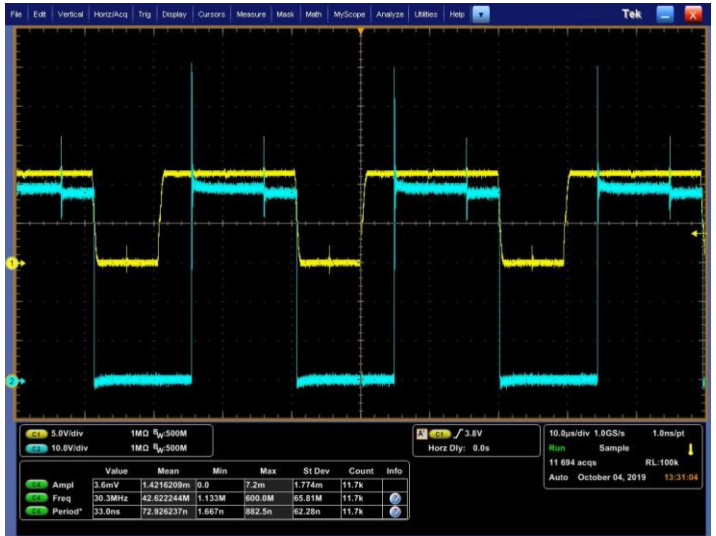
Fabricated Test Bed



Thermal Camera Image of Board



Oscilloscope Traces During Operation



C1 5.0V/div 1MΩ BW:500M
C2 10.0V/div 1MΩ BW:500M

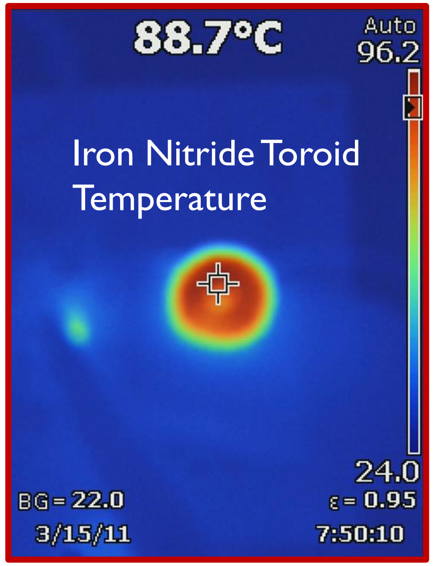
A' C1 ∫ 3.8V
Horz Dly: 0.0s

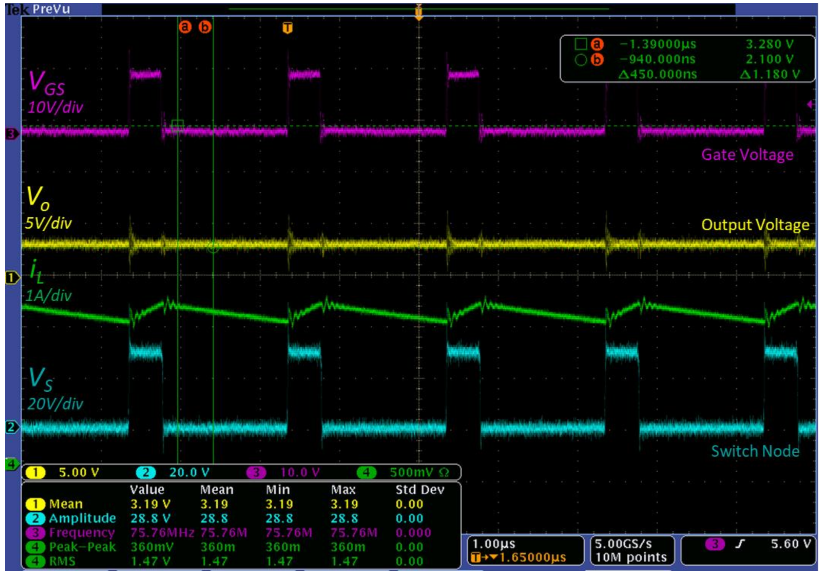
10.0µs/div 1.0GS/s 1.0ns/pt
Run Sample
11 694 acqs RL:100k
Auto October 04, 2019 13:31:04

	Value	Mean	Min	Max	St Dev	Count	Info
C4 Ampl	3.6mV	1.4216209m	0.0	7.2m	1.774m	11.7k	
C4 Freq	30.3MHz	42.622244M	1.133M	600.0M	65.81M	11.7k	?
C4 Period*	33.0ns	72.926237n	1.667n	882.5n	62.28n	11.7k	?

Technical Accomplishments and Progress – New Soft Magnetics

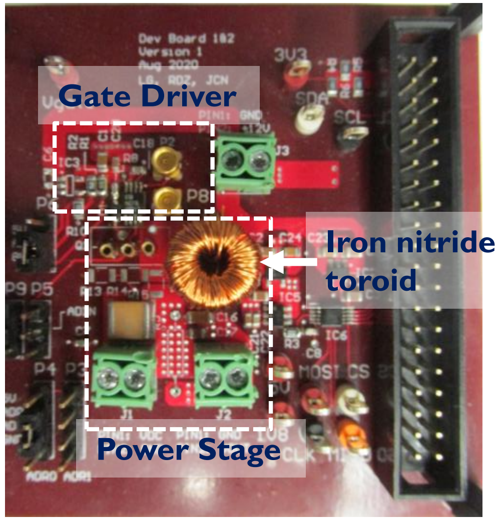
- Testing iron nitride/epoxy soft magnetic composites (SMCs) as a new inductor core material for high frequency electronics
  - **Higher magnetization (and power density), low loss, low cost**
- Iron nitride composite toroid sample has been evaluated in a hardware prototype
- Evaluation of the iron nitride composite material performance in comparison to other commercial core materials is in progress.



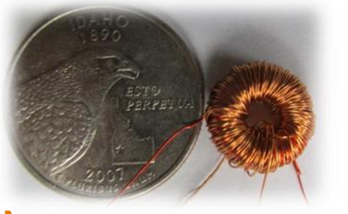


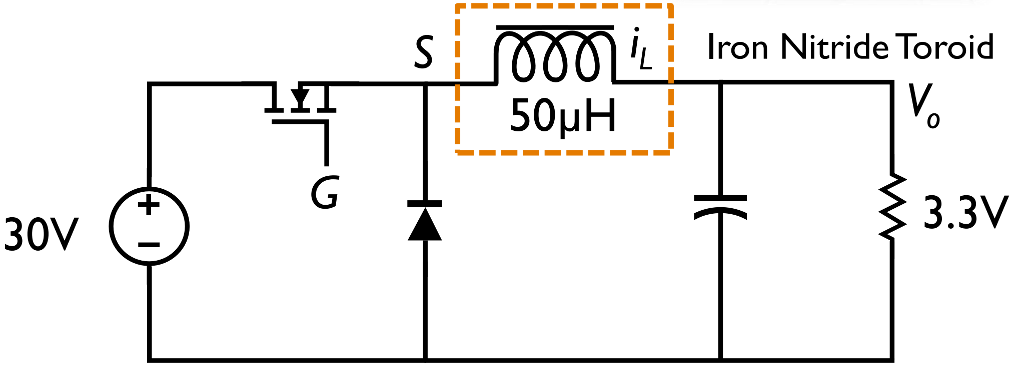
	Value	Mean	Min	Max	Std Dev
1 Mean	3.19 V	3.19	3.19	3.19	0.00
2 Amplitude	28.8 V	28.8	28.8	28.8	0.00
3 Frequency	75.76MHz	75.76M	75.76M	75.76M	0.000
4 Peak−Peak	360mV	360m	360m	360m	0.00
4 RMS	1.47 V	1.47	1.47	1.47	0.00

Buck Converter Prototype



ELT216: Todd Monson
Iron Nitrides

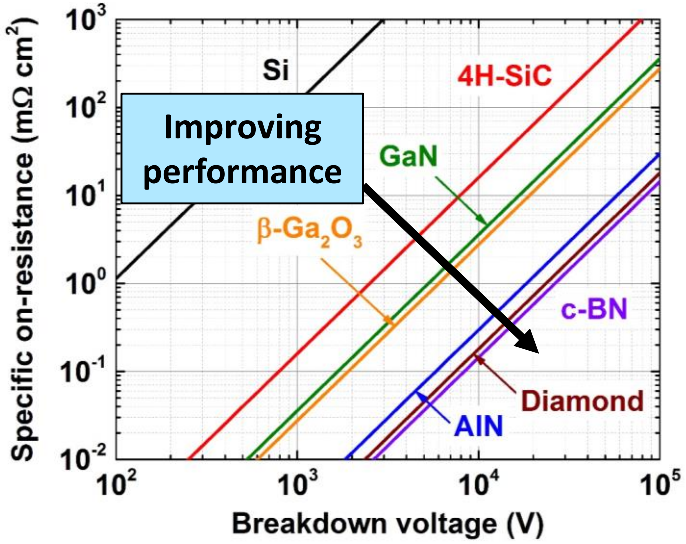




Responses to Previous Year Reviewers' Comments

- **What is the value proposition of vertical GaN devices?**
  - When GaN vertical devices reach full maturity we can expect up to 10x reduction in R_{on} by switching from SiC to GaN
  - Higher critical field means higher V_{BR}
    - Focusing on a reduction in V_{BR}^2/R_{on} to maximize performance

Smaller device area
- Lower gate capacitance → reduced switching losses
- More devices per wafer → reduced cost



- **Has any consultation been performed with chip manufactures and vehicle OEMs?**
  - Our consortium partners are using a commercial foundry for SiC devices. Discussions have been on-going to engage a foundry in the future for vertical GaN devices.
  - Automotive OEMs have been regularly engaged within the context of the Electrical and Electronics Tech Team
    - Open to suggestions on other approaches

Collaboration

Oak Ridge National Laboratory – Collaborating partner for Electric Traction Drive integration and evaluation. (Integrated drive)

National Renewable Energy Laboratory – Collaborating partner for Electric Traction Drive integration and evaluation. (Magnetic materials)

SUNY Poly
Albany Campus

State University of New York (SUNY) (Woongie Sung) – Fabricating SiC JBS diode integrated with MOSFETs.

Ohio State University (Anant Agarwal) – Designing for improved reliability for SiC electronics. Evaluate reliability and ruggedness of commercial and fabricated devices using realistic scenarios.

Jim Cooper– Working with OSU for SiC device evaluation. Working with Sandia for GaN power electronic device design and characterization. (Subcontractor)

Lehigh University (Jon Wierer) – Working with Sandia for design/simulation/modeling of GaN SB and JBS diodes. (Subcontractor)

Remaining Challenges and Barriers

GaN Devices:

- Immaturity of GaN devices requires multiple cycles of learning to develop and optimize device performance
  - Surface leakage related to passivation and junction leakage from etch-and-regrowth process are critical concerns at this stage
- Need to scale devices to higher operating currents
  - Primarily a function of process maturity and yield (substrate/wafer maturity)
- Device reliability needs to be evaluated
- GaN foundry cost models are in development

Proposed Future Research: GaN Devices

JBS

- Iterate to improve JBS diode performance against targets (1200 V/100 A)
  - Focusing on reducing reverse leakage current
    - Will require advances in etched-and-regrown junction performance as well as improved passivation quality.

MOSFET

- Iterate to improve GaN MOSFET performance against targets (1200 V/100 A)
  - MOSFET blocking state needs to be improved
    - Target 600 V blocking voltage, forward current of 1 A for next steps

System

- Combine GaN MOSFET and JBS diode in circuit for evaluation
  - Will require substantial maturation of MOSFET and JBS process before implementation in a circuit environment

Any proposed future work is subject to change based on funding levels.

Summary

- Leveraging the PN diode platform to inform on JBS and MOSFET efforts
  - Passivation studies, etch damage recovery, and low leakage pn junction regrowth can be studied more effectively on a simple PN diode
- Identified two key challenges for the JBS platform and are working to resolve surface and junction reverse leakage
- Demonstrated 1st Gen MOSFET with 10^7 on/off ratio, positive gate threshold voltage, and max 0.8 A drain current

- As device performance matures, we plan to evaluate their performance in a circuit environment
- Engaging with drive train team to ensure work is on track to meet program goals

Cycles of Learning