High-Voltage, High-Power Density Traction Drive Inverter (Keystone Project #1)

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Project ID: ELT209

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Overview

Timeline

- Start Date: FY19
- End Date: FY24
- 53% Complete

Barriers

- Passive components are bulky; DC bus capacitor takes 20% - 30% of inverter volume
- Meeting DOE ELT 2025 High Voltage Power Electronics Targets
  - Power Density: 100kW/L
  - Cost: $2.7/kW
  - Peak Efficiency: > 97%
  - Reliability: 300,000 mile lifetime or 15 years

Budget

- Total project funding
  - DOE share – 100%
- Funding for FY21: $550K

Partners

- Virginia Tech
- University of Arkansas
- National Renewable Energy Laboratory
- ORNL Team Members: Randy Wiles, Emre Gurpinar, Cliff White, Lincoln Xue

Any proposed future work is subject to change based on funding levels
Relevance – Project Objectives

Overall Objective:
- Develop technologies for next generation traction drive power electronic systems to achieve DOE ELT 2025 target of 100 kW/L
- Focus on traction drive inverter architecture, optimization of bus bar design, minimization of passive components

FY 2021 Objectives:
- Design and build 100 kW inverter prototypes
- Demonstrate technologies developed in the EDT Consortium
<table>
<thead>
<tr>
<th>Year</th>
<th>Quarter</th>
<th>Milestones and Go/No-Go Decision</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>FY2021</td>
<td>Q1</td>
<td><strong>Milestone</strong>: Evaluate and down select SiC MOSFETs and gate drive solutions developed at ORNL and consortium partners.</td>
<td>Completed</td>
</tr>
<tr>
<td></td>
<td>Q2</td>
<td><strong>Go/No-Go Decision</strong>: Design a busbar and a heat sink using genetic algorithm (GA) based optimization tools. If the design can meet the inverter requirements start designing an inverter package.</td>
<td>Completed</td>
</tr>
<tr>
<td></td>
<td>Q3</td>
<td><strong>Milestone</strong>: Design an inverter control board with form factor best fitting to the inverter design.</td>
<td>On-track</td>
</tr>
<tr>
<td></td>
<td>Q4</td>
<td><strong>Milestone</strong>: Build a 100kW segmented SiC MOSFET inverter prototype.</td>
<td>On-track</td>
</tr>
<tr>
<td>FY2022</td>
<td>Q1</td>
<td><strong>Milestone</strong>: Perform functional verification tests of the inverter built in FY21.</td>
<td>On-track</td>
</tr>
<tr>
<td></td>
<td>Q2</td>
<td><strong>Milestone</strong>: Perform full load tests.</td>
<td>On-track</td>
</tr>
<tr>
<td></td>
<td>Q3</td>
<td><strong>Milestone</strong>: Refine inverter designs (Gen-2).</td>
<td>On-track</td>
</tr>
<tr>
<td></td>
<td>Q4</td>
<td><strong>Go/No-Go Decision</strong>: Build Gen-2 100kW prototype.</td>
<td>On-track</td>
</tr>
</tbody>
</table>

Any proposed future work is subject to change based on funding levels.
Goal: Increase traction drive power electronics system power density to meet DOE ELT 2025 targets (100kW/L) by focusing on power inverter architecture research and bus bar designs for reduction of passive components

• Inverter architecture to reduce capacitor requirements:
  – Multiphase inverter (asymmetrical six-phase)
  – Segmented inverter arrangement

• Increase DC bus voltage (800V+):
  – Better utilize SiC switching devices’ inherently higher voltage ratings
  – Reduce the size of SiC dies (lower cost)
  – Reduce phase and DC bus current
  – Evaluate impact of insulation requirements

• Optimize DC bus bar designs:
  – Direct cooling of DC bus bars
  – Embedded and distributed capacitors
Approach

Use segmented inverter to reduce the DC bus capacitance

**Segmented inverter**
- Separate inverter switch dies and stator windings into two sets of drive unit
- No changes needed in control of the motor except modifying the pulse width modulation (PWM) scheme
- Interleaving the switching timings to reduce the DC bus ripple current

![Standard 3-phase inverter](image1)

![Segmented 3-phase inverter](image2)

Reduction of capacitor ripple current with interleaved switching for carrier-based PWM methods

![Optimal zero vector placement in space vector (SV) PWMs](image3)

Capacitor ripple current vs modulation index, showing >50% reduction with the segmented inverter.
Technical Accomplishments – FY20

Performed a comparison study of open winding and segmented drives

• Comparison of open winding and segmented drives

<table>
<thead>
<tr>
<th></th>
<th>Segmented Drive</th>
<th>Open Winding Drive*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear</td>
<td>Over modulation</td>
<td>Linear</td>
</tr>
<tr>
<td>Phase max voltage</td>
<td>$\frac{V_{dc}}{\sqrt{3}}$</td>
<td>$\frac{2V_{dc}}{\pi}$</td>
</tr>
<tr>
<td>Phase current rating</td>
<td>$I_m$</td>
<td>$I_m$</td>
</tr>
<tr>
<td>Inverter rating</td>
<td>$\sqrt{3}V_{dc}I_m$</td>
<td>$\frac{6V_{dc}I_m}{\pi}$</td>
</tr>
</tbody>
</table>

*Not usable due to zero sequence currents

• Open winding drive
  – Better utilizes DC bus voltage but unable to fully utilize Si/SiC devices’ current capability
  – Leads to an inverter rating reduction by 13% for the same amount of Si/SiC
  – Requires one additional current sensor
  – Can use interleaving to significantly reduce the DC bus ripple current, still generate 15% to 100% higher ripple compared to the segmented inverter
  – Presents paths for 3rd harmonics from the inverter and/or motor back EMFs to generate zero sequence currents

Open stator winding drive configuration using a single DC source
Technical Accomplishments – FY20

Evaluated the DC bus ripple currents in open winding drives for various PWM schemes and compared to segmented drives

- PWM schemes for open winding drives
  - Bipolar switching with 120 degree phase shift
  - Unipolar switching
  - Interleaving to reduce ripple current

Interleaving can significantly reduce the DC bus ripple current, still 15% to 100% higher than in the segmented inverter

Symmetrical SV modulation

Bus clamp SV modulation

Comparison of DC bus ripple current for SV PWMs with interleaving vs segmented drive
Technical Accomplishments – FY21

Design and demonstrate 100kW segmented inverters using technologies developed in the EDT Consortium

• Major tasks and roles
  – Power module: ORNL, VT, U of A
  – Gate drive and sensing: ORNL, VT, U of A
  – DC bus and capacitor: ORNL
  – Control: ORNL
  – Thermal management: ORNL

<table>
<thead>
<tr>
<th>Inverter Ratings</th>
</tr>
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<tbody>
<tr>
<td>Vdc (V)</td>
</tr>
<tr>
<td>800</td>
</tr>
<tr>
<td>Power (kW)</td>
</tr>
<tr>
<td>100</td>
</tr>
<tr>
<td>143kVA at pf=0.7</td>
</tr>
<tr>
<td>Efficiency (%)</td>
</tr>
<tr>
<td>98</td>
</tr>
<tr>
<td>Coolant flow rate (L/min)</td>
</tr>
<tr>
<td>10</td>
</tr>
<tr>
<td>WEG, 50/50</td>
</tr>
</tbody>
</table>

• Current sensing
  – COTS sensors for Gen-1
  – Gen-2: parasitic voltage drop based current sensing and protection (VT); Giant magnetoresistance (GMR) based DC/AC current measurement (U of A)

Cree SiC MOSFET CPM3-1200-0013A
  - 1200V
  - 102A @100°C
  - 13mΩ @25°C, 21mΩ @175°C

Parasitic voltage drop based current sensing (VT)

GMR-based current measurement (U of A)
Technical Accomplishments – FY21

Developed PLECS loss model for the Cree SiC MOSFET die, CPM3-1200-0013A

• Comparison of conduction losses
  – MOSFET-only, MOSFET with body-diode, and body-diode in the 3rd quadrant

  ![Graph showing comparison of conduction losses](image)

• Switching losses derived from CPM3-1200-0016A in TO-247-4L package

  ![Graph showing switching losses](image)
Technical Accomplishments – FY21

Simulated switch losses for thermal design

- Losses per switch in the segmented inverter
  - Po=100kW
  - fsw=30kHz
  - Bus-clamped/symmetrical SVPWM

- Bus-clamped SVPWM reduces switching loss significantly over symmetrical SVPWM

- Diode conduction in 3rd quadrant depends on power factor and switching scheme

Bus-clamped SVPWM will be adopted for inverter efficiency enhancement
Technical Accomplishments – FY21

Designed heat sinks for the VT power module using the ORNL GA-based optimization tool

- Loss in each chip: 150 W
- Coolant inlet: 65 °C and (10/6) L/m flow rate

- VT double-side cooled SiC phase leg module: two Cree SiC MOSFET dies, CPM3-1200-0013A

\[
\begin{align*}
\text{Chip Tjmax: } & 153.3\degree\text{C, 155.93}\degree\text{C} \\
\text{Pressure drops: } & 749.27\text{Pa, 749.27Pa} \\
\text{Coolant outlet Tmax: } & 74.89\degree\text{C, 74.17}\degree\text{C}
\end{align*}
\]

Ver. 1: 17.28x13.46x4.22mm

Ver. 2: 13.46x17.28x6.5mm (54% increase in volume over Ver. 1)

FEA results using COMSOL
- Chip Tjmax: 153.3°C, 155.93°C
- Pressure drops: 749.27Pa, 749.27Pa
- Coolant outlet Tmax: 74.89°C, 74.17°C
Technical Accomplishments – FY21

Derived a lumped thermal impedance model for the VT power module and simulated MOSFET junction temperature fluctuation

- Simulation results at Po=100kW, fsw=30kHz, pf=0.7 indicating >15°C reduction in Tjmax with bus-clamped SVPWM over symmetrical SVPWM

<table>
<thead>
<tr>
<th>Symmetrical SVPWM</th>
<th>Bus-clamp SVPWM</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET conduction loss</td>
<td>MOSFET conduction loss</td>
</tr>
<tr>
<td>Switching loss</td>
<td>Switching loss</td>
</tr>
<tr>
<td>Diode conduction loss</td>
<td>Diode conduction loss</td>
</tr>
<tr>
<td>Total loss</td>
<td>Total loss</td>
</tr>
<tr>
<td>MOSFET junction temperature</td>
<td>MOSFET junction temperature</td>
</tr>
<tr>
<td>MOSFET current</td>
<td>MOSFET current</td>
</tr>
<tr>
<td>Diode current</td>
<td>Diode current</td>
</tr>
</tbody>
</table>

Rth

<table>
<thead>
<tr>
<th></th>
<th>Die #1</th>
<th>Die #2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rth</td>
<td>0.12250</td>
<td>0.05911</td>
</tr>
<tr>
<td>Cth</td>
<td>0.34422</td>
<td>0.04304</td>
</tr>
</tbody>
</table>

PLECS thermal model
Technical Accomplishments – FY21

Completed a 100kW inverter design using the VT phase leg modules

- The inverter design is promising in meeting the power density and efficiency targets (100kW/L, 97%)

167x64x82mm ~0.88L

Photo of VT SiC power modules (29.5x20.5x4mm)

DC bus capacitor board with low inductance bus bar design using TDK ceralink capacitors, 60µF, 228Arms @105°C

Outlet manifold
Current sensors (LEM HCF300-S)
Gate driver
Capacitors
Inlet/outlet manifold design ensuring an even flow distribution to the 12 heat sinks

Inlet manifold
Phase outputs
Six double side cooled phase leg modules
**Technical Accomplishments – FY21**

Completed heat sink design using the ORNL GA-based optimization for use with the U of A SiC power modules for a 100 kW segmented inverter

- Selected four candidates for detailed FEA evaluations
- Results: maximum junction temperature $T_{j,\text{max}} < 152^\circ \text{C}$, pressure drop < 356 Pa
- Confirmed in FEA correction of imbalance in $T_{j,\text{max}}$ with flow rate adjustment

\[ f_{1} = (1 + k_{f}) * f_{\text{rated}}, \quad f_{2} = (1 - k_{f}) * f_{\text{rated}} \]

- Flow rate adjustment with offset $k_{f}$

Heat sink convection coefficient vs volume for the GA-based optimization design iterations

Heat sink convection coefficient vs volume for the GA-based optimization design iterations

Maximum junction temperature distribution

Heat sink

- $T_{j,\text{max}}$ vs flow rate offset

Heat sink #2: 36.82x23.6x5.33 mm

SiC #1, #2

SiC #3, #4
Response to Previous Year Reviewers’ Comments

• **Reviewer:** The reviewer looked forward to hearing about the follow-up regarding comparative evaluation between the segmented inverter drive and the open-end winding dual inverter drive concept.

  **Response:** We have conducted a comprehensive study of the bus voltage and device utilization and DC bus ripple current in the open winding drives for various modulation schemes as well as comparison to the segmented inverter.

• **Reviewer:** Efficiency evaluation is not observed as an accomplishment nor stated to be part of the future work.

  **Response:** Meeting the inverter efficiency target is our goal and we have specified in our prototype design at 98%, which is the scalability target in the Wide Bandgap Advanced Integrated Power Module 2025 Technical Guidelines. In addition to the loss reduction coming along with the use of wide band gap devices, we are also using the bus-clamped space vector modulation in the segmented drive to further reduce the switching losses.

• **Reviewer:** Looking forward to seeing the outcomes of 100 kW prototype.

  **Response:** We have completed a 1\textsuperscript{st} design for 100kW segmented inverter, which looks promising in meeting the power density and efficiency targets, and plan to experimentally validate the design in FY22.
Collaboration and Coordination with Other Institutions

<table>
<thead>
<tr>
<th>Institution</th>
<th>Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virginia Tech</td>
<td>• Requirements for inverter power modules</td>
</tr>
<tr>
<td></td>
<td>• Power module for inverter design</td>
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<td>University of Arkansas</td>
<td>• Requirements for inverter power modules</td>
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<td></td>
<td>• Power module for inverter design</td>
</tr>
<tr>
<td>National Renewable Energy Laboratory</td>
<td>• Incorporate thermal management research results into inverter designs</td>
</tr>
<tr>
<td></td>
<td>• Validate inverter thermal designs</td>
</tr>
</tbody>
</table>
Remaining Challenges and Barriers

- Impact of higher DC bus voltage on the system insulation requirements needs to be evaluated
- Rapid prototyping of unconventional heat sink and manifold designs
- Integration of current sensing and protection into gate drivers
Proposed Future Research

• FY 2021
  – Complete control board design
  – Complete an inverter design using the UArk phase leg modules
  – Build a 100kW inverter

• FY 2022
  – Test and evaluate the inverter built in FY21
  – Refine inverter designs with integrated current sensing and gate drives

Any proposed future work is subject to change based on funding levels
Summary

• **Relevance:** Reducing inverter DC bus components will remove some of the barriers in inverter designs to achieve the ELT 2025 targets of 100kW/L and 300,000 mile lifetime.

• **Approach:** Develop inverter topologies, increase DC bus voltage, and investigate direct bus cooling to minimize the inverter DC bus design.

• **Collaborations and Coordination with Other Institutions:** Virginia Tech, University of Arkansas, NREL.

• **Technical Accomplishments:**
  – Evaluated the open winding drive and conducted a comparison study against the segmented drive.
  – Completed a 100kW segmented inverter design using VT double side cooled SiC phase-leg modules.
  – Completed liquid heat sink design for use with the U of A SiC phase-leg modules.

• **Future Work:**
  – Build and test 100kW high voltage segmented inverters.
  – Evaluate inverter designs to identify gaps (if any) against the DOE ELT 2025 targets.
  – Refine the designs to incorporate the latest developments.

Any proposed future work is subject to change based on funding levels.