



Commercial Thin Film Research Overview

Photovoltaics Track

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Solar Energy Technologies Office

Overview

- **Introduction to Commercial Thin Films**
- Current Research Topics in Cadmium Telluride
- Current Focus Areas in Copper Indium Gallium Selenide
- Summary of High Level Goals for Commercial Thin Films



Commercial Thin Film Technologies

Image Credit: First Solar



Cadmium Telluride (CdTe)

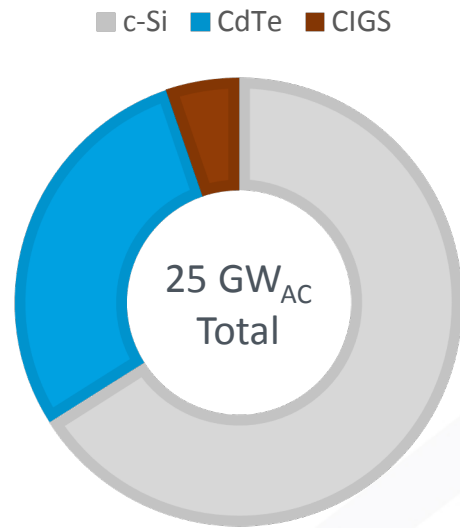
Image Credit: Solar Frontier



Copper Indium Gallium Selenide (CIGS)

Commercial Thin Film Technologies

A Few Thin Film Highlights



US Utility Scale Fleet as of 2019,
Including ~30% Thin Film Capacity

(Data from the 2019 Utility Scale Solar Report from
Lawrence Berkeley National Lab)

Image Credit: Solar Power World

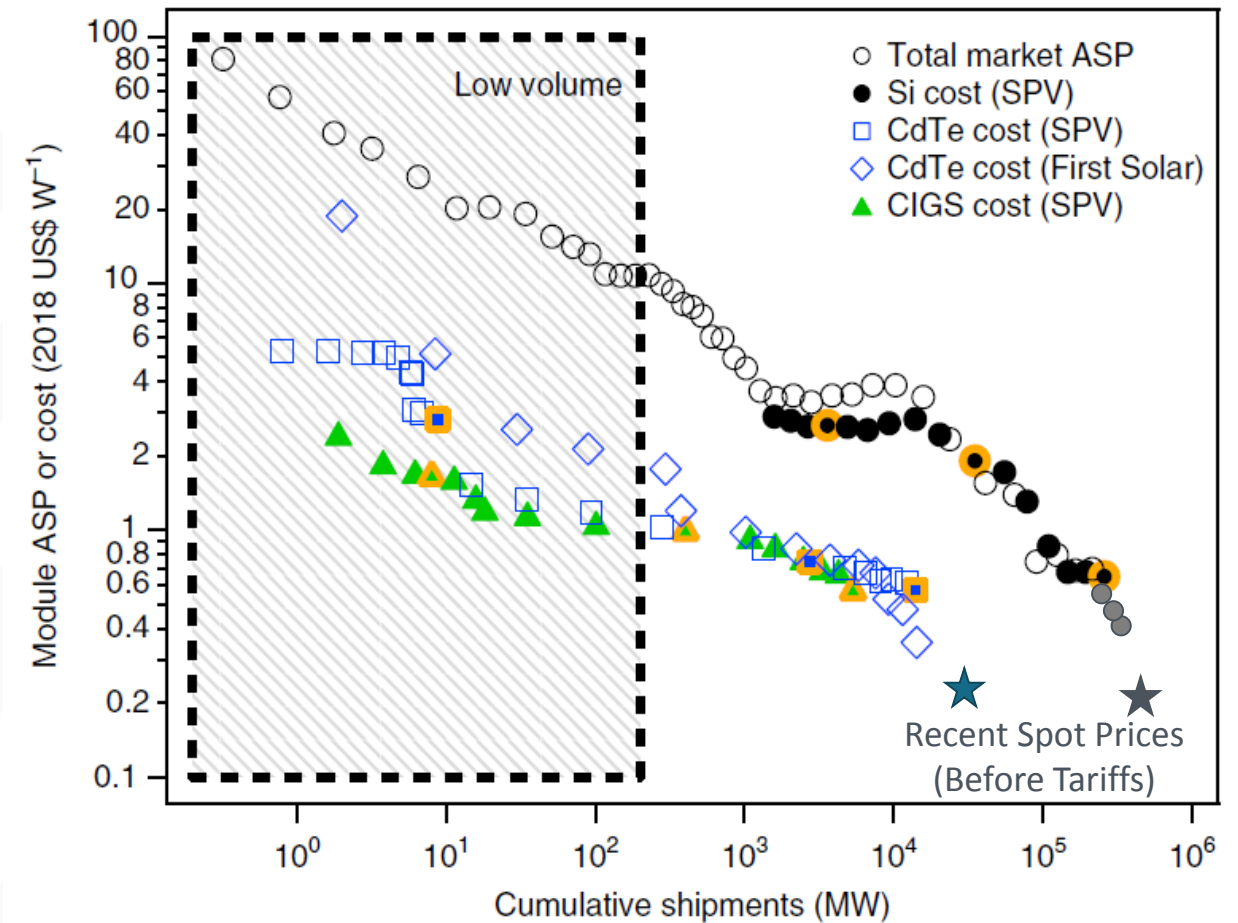
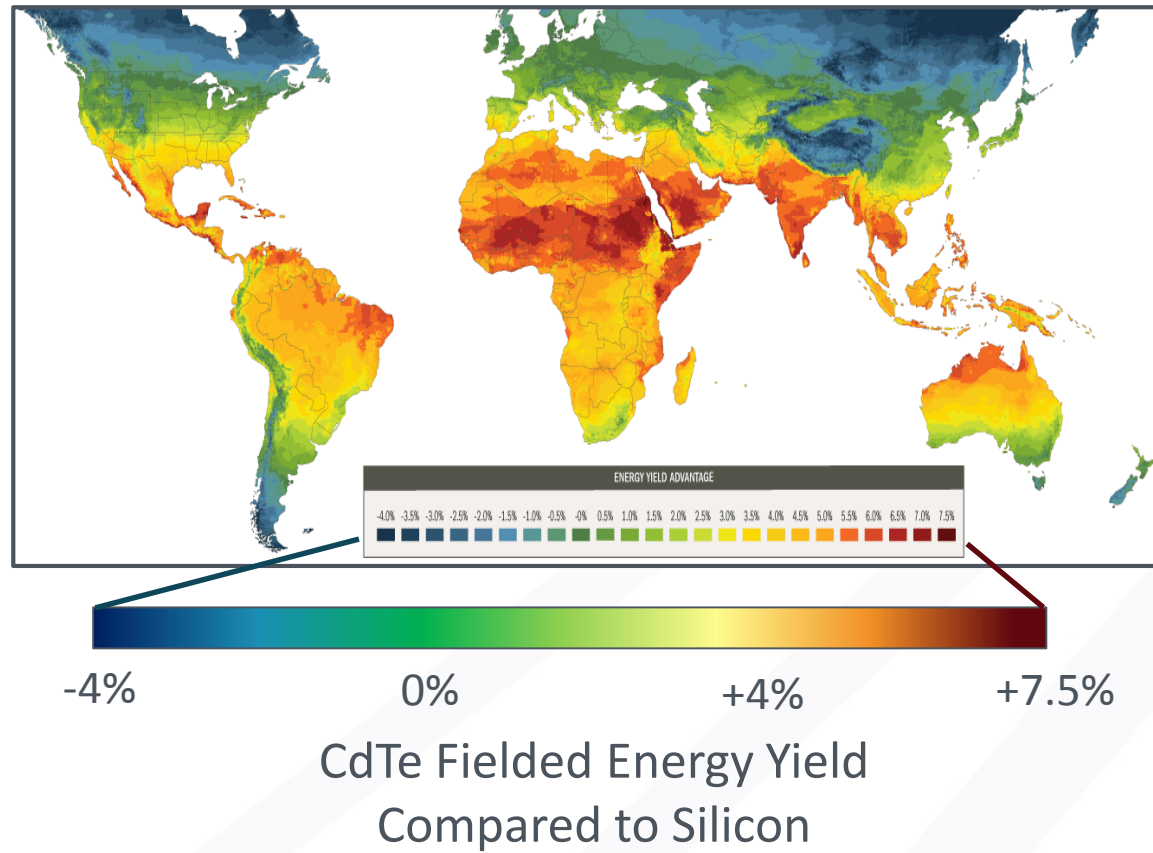


- CdTe (First Solar) Currently Represents the Majority of Domestic Cell Manufacturing Capacity.
- Raw Materials can be Converted into Completed Thin Film PV Modules in just a Few Hours.
- First Solar's Estimated Cell and Module Manufacturing Labor Intensity was Roughly 50% Lower than Canadian Solar's in 2018/19 (0.9 FTE/MW vs. 1.8 FTE/MW)

The Potential for Cost Advantages

Figure Credit: Reese and Haegel et al. 2018, *Nature Energy*, 3, 1002–1012

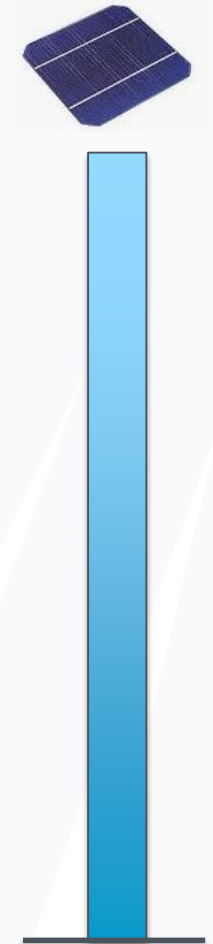
Image Credit: First Solar



Global Thin Film Market Update

≈ 150 GW/yr Supply Chain

≈ 10 GW/yr
Supply Chain



**Continuous Technology Advances are Needed in
Order for Thin Films to Maintain Competitiveness**

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CdTe Performance Targets

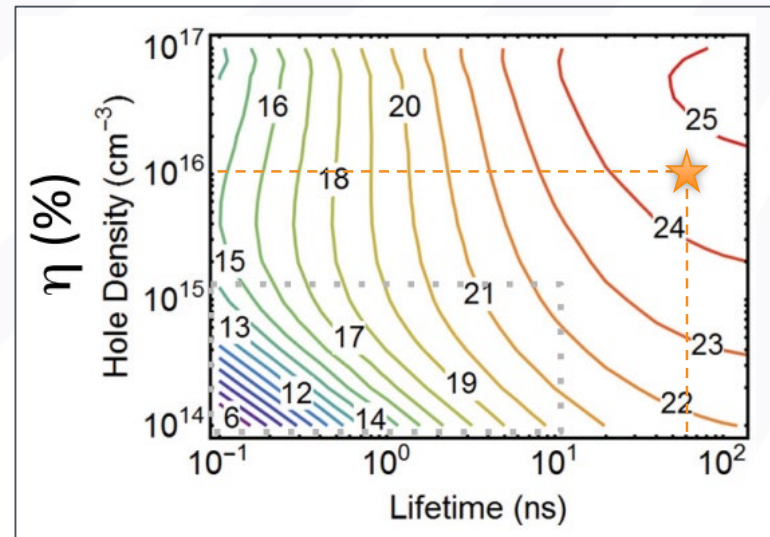
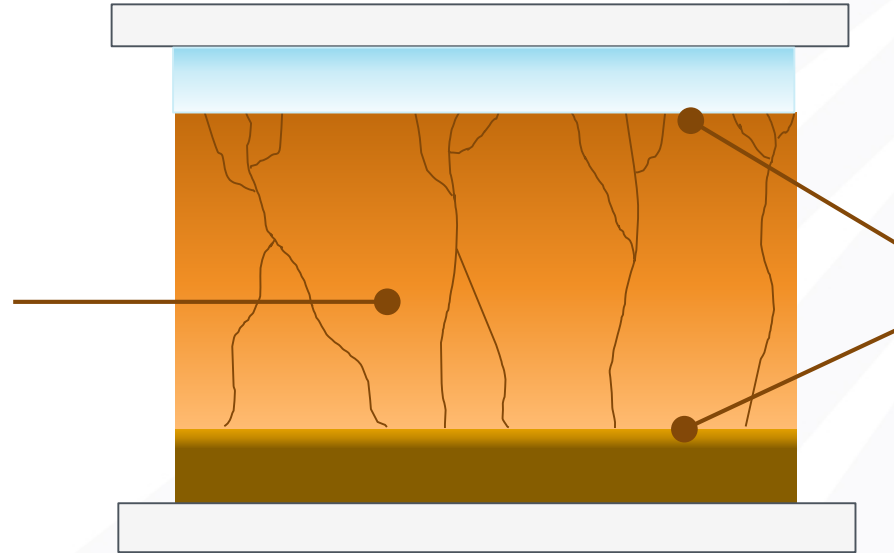
Absorber

Current Status

Cu Doping	GrV Doping
10^{14} cm^{-3}	10^{16} cm^{-3}
1 μs	10 ns

24% Efficiency Goals

Low Doping	High Doping
10^{15} cm^{-3}	10^{16} cm^{-3}
3 μs	50 ns



Contacts

Current Status

Front SRV	Rear SRV
10^2 cm/s	10^5 cm/s

24% Efficiency Goals

Front SRV	Rear SRV
10^2 cm/s	10^2 cm/s

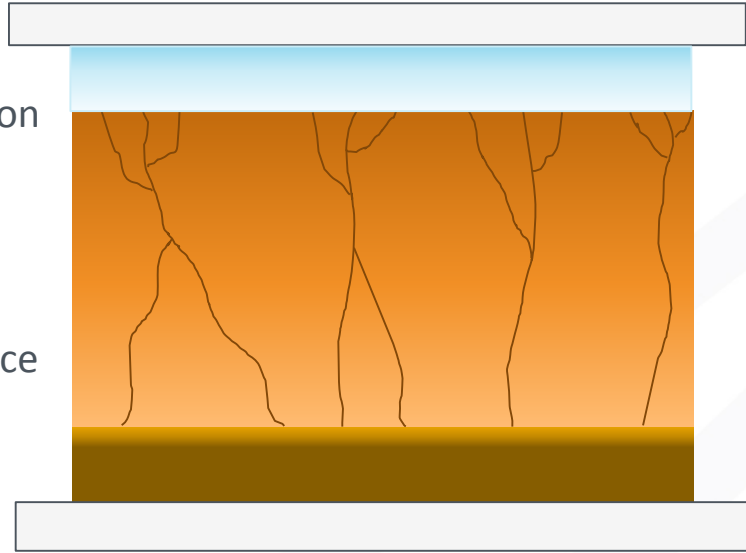
CdTe Research Areas

Front Barrier and TCO

Copper-Doped CdSeTe

Front Interface and Junction

Rear Contact and Interface



CdTe Layer Formation
and Post-Treatments

Bulk Loss
Mechanisms

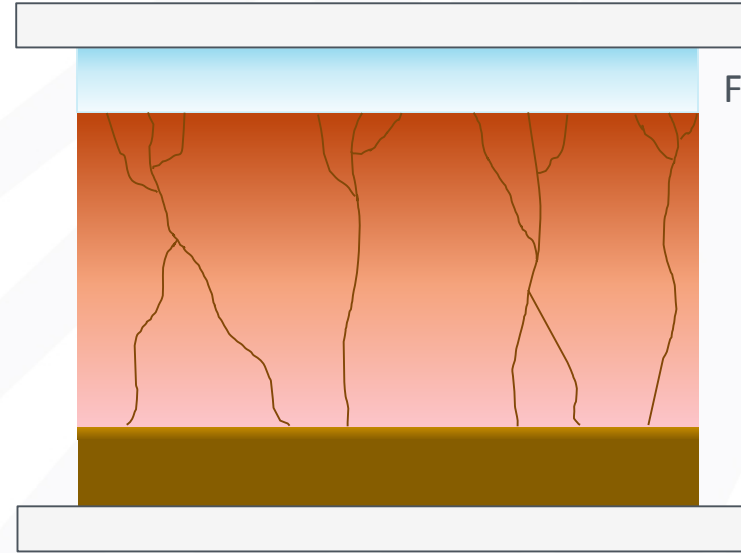
Rear Metallization
and Barrier

Group V-Doped CdSeTe

Front Barrier and TCO

Front Interface and Junction

Rear Contact and Interface



Bulk Loss
Mechanisms

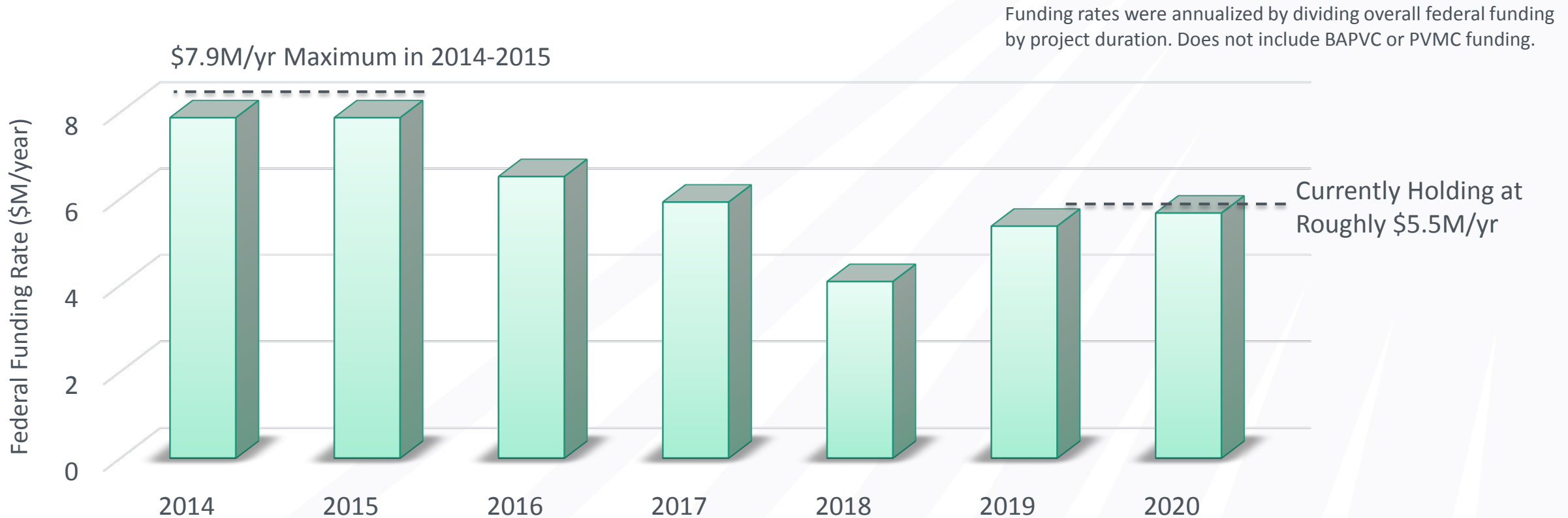
CdTe Layer Formation
and Post-Treatments

Rear Metallization
and Barrier

CdTe Research Areas



Approximate CdTe Historic Federal Funding Levels



➤ Annual Funding Estimates are Approximate, and can vary Significantly based on how Projects are Sorted.

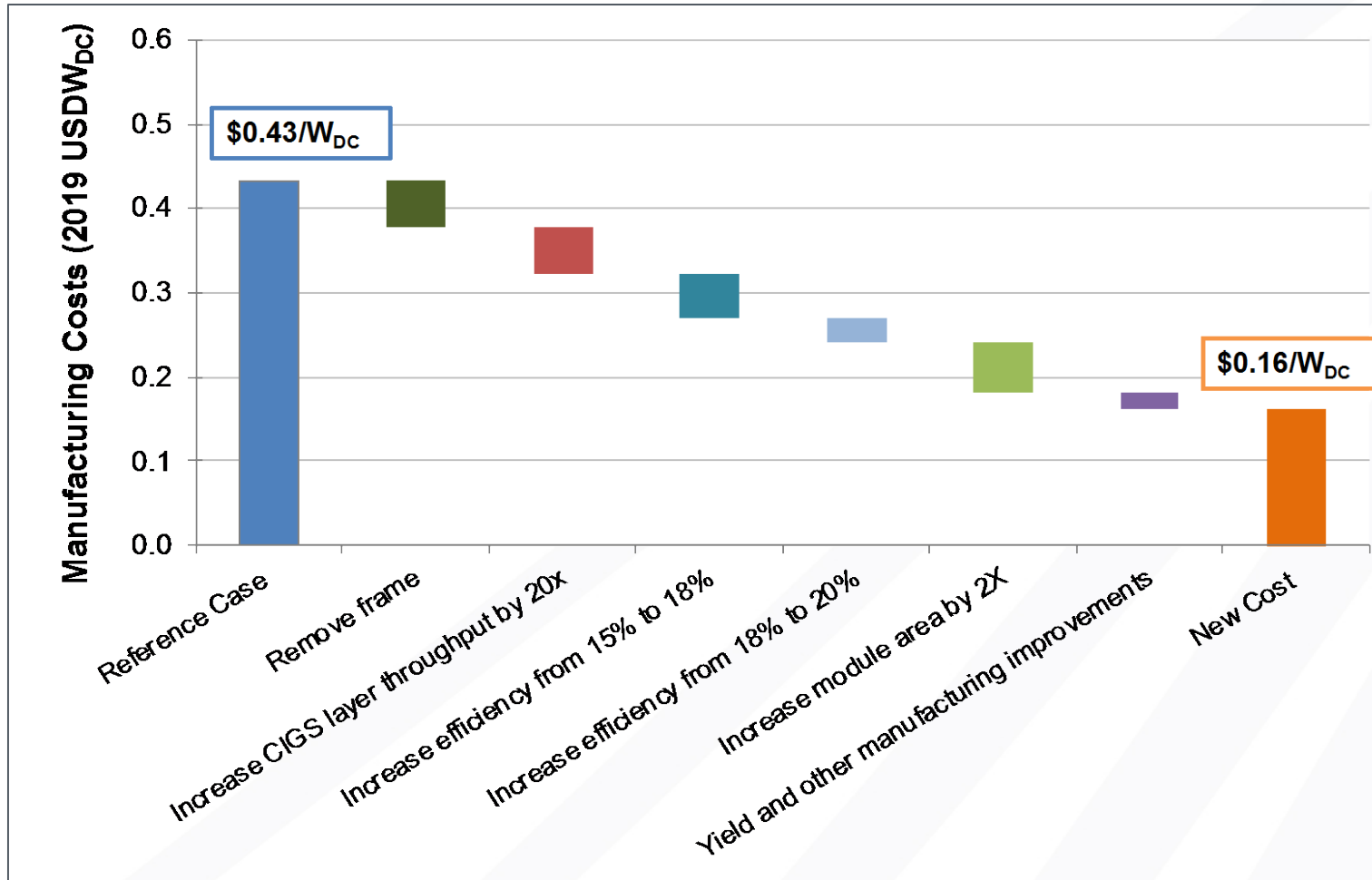
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CIGS Research Overview

Figure Credit: NREL Strategic Energy Analysis Center, *Draft Analysis*



Front Barrier and TCO

Front Interface and Junction

CIGS Layer Deposition
and Post-Treatments

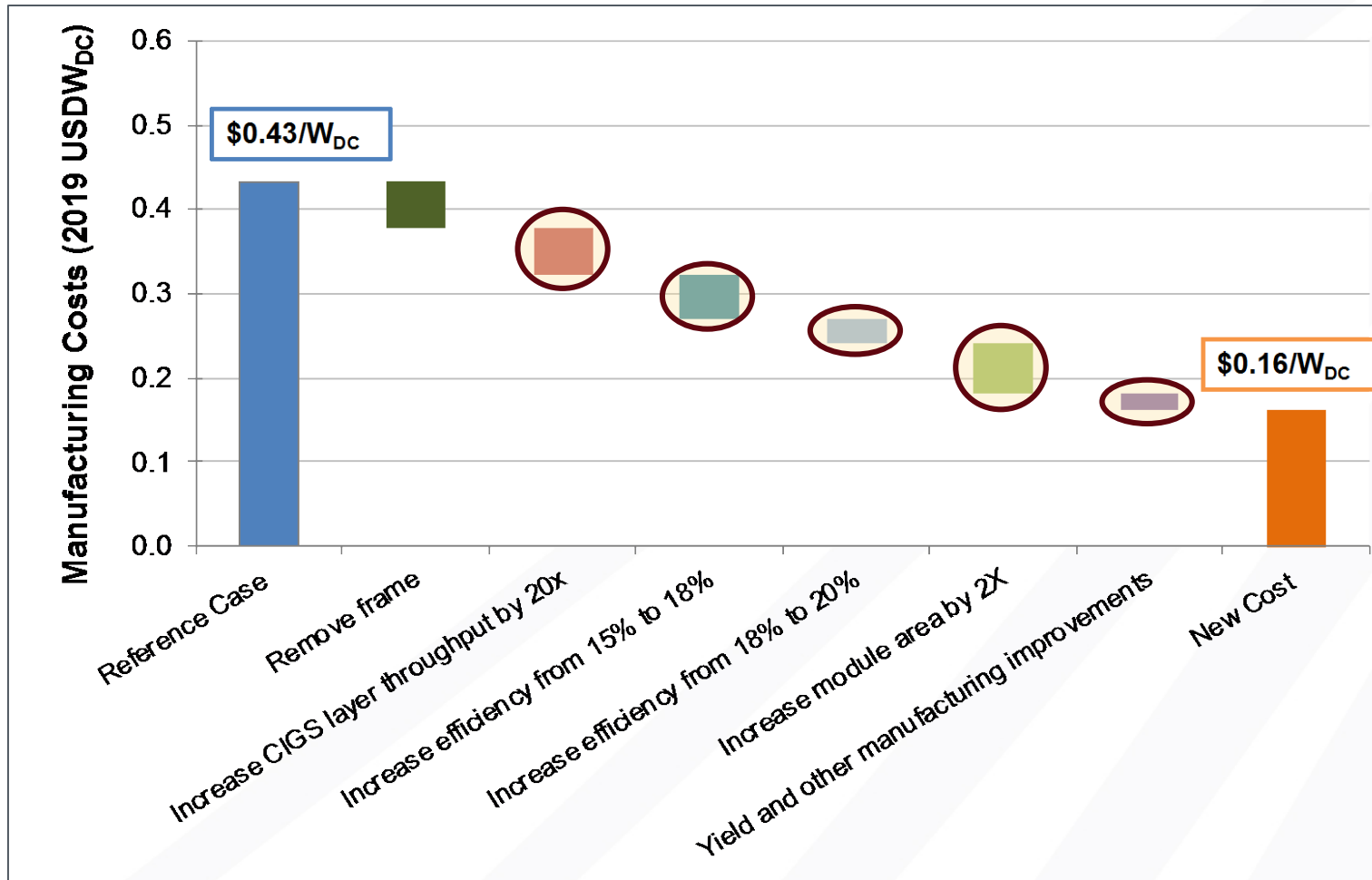
Rear Contact and Interface

Bulk Loss Mechanisms

Rear Metallization and Barrier

CIGS Research Overview

Figure Credit: NREL Strategic Energy Analysis Center, *Draft Analysis (Preliminary)*



Cu(In,Ga)Se₂ module technologies face significant challenges in high quality, large area absorber fabrication.

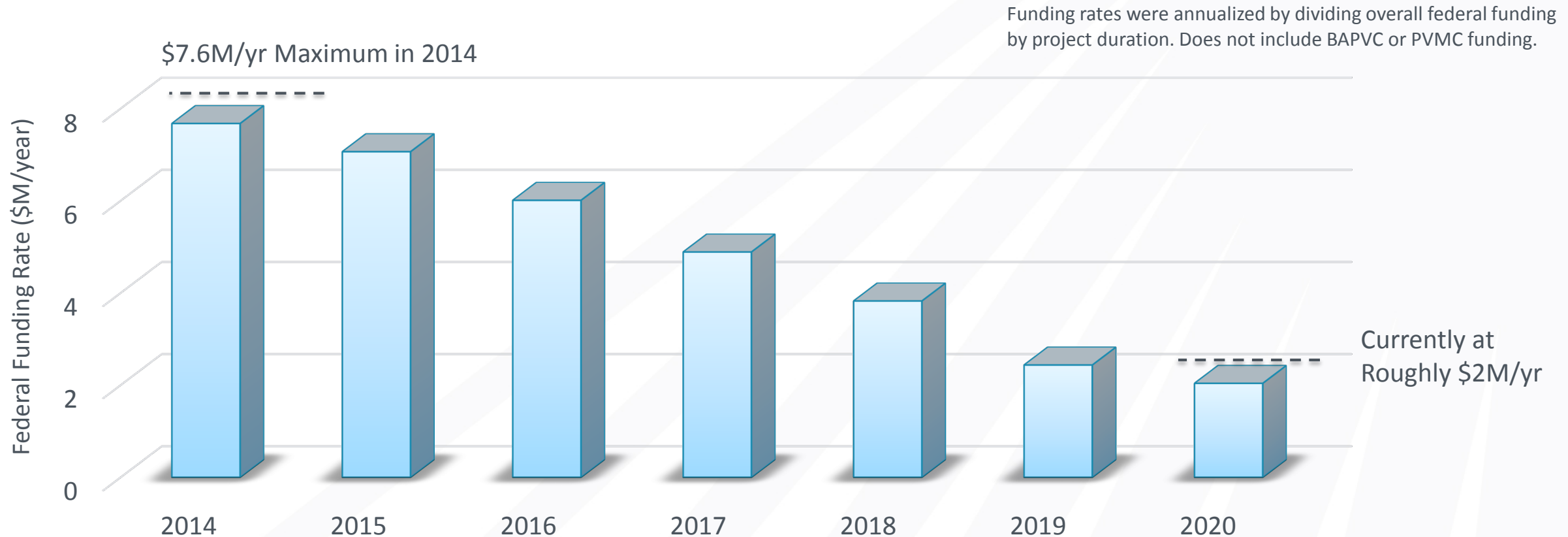
CIGS Layer Deposition
and Post-Treatments



Bulk Loss Mechanisms



Approximate CIGS Historic Federal Funding Levels



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Summary of High Level Goals

Cadmium Telluride (CdTe)

- ❖ Increase cell efficiency without increasing manufacturing cost or reducing service lifetime.
- ❖ Identify new materials and architectures that will continue to expand the roadmap for future technology improvements.



Image Credit: First Solar

Copper Indium Gallium Selenide (CIGS)

- ❖ Develop and improve manufacturing methods that undercut the $\$/W_{DC}$ costs of industry-leading cell and module technologies.
- ❖ Identify use cases that value flexibility, light weight, or substrate fabrication architectures.



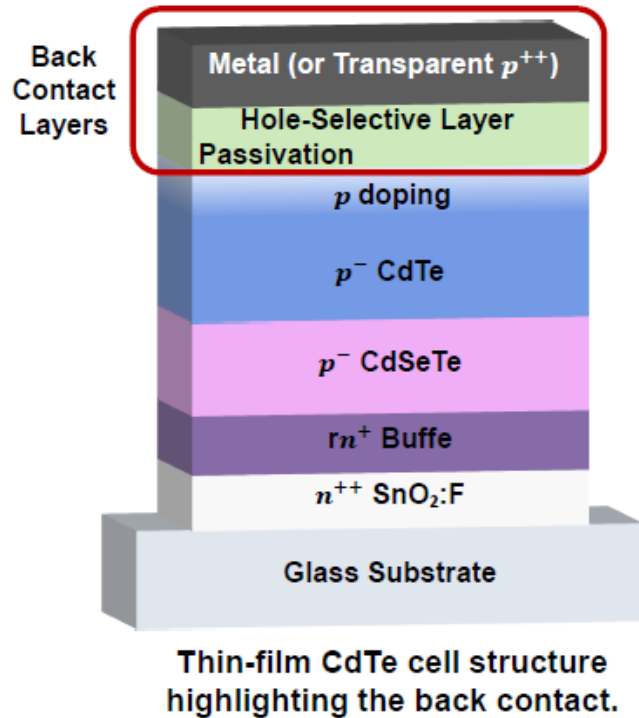
Image Credit: Solar Frontier

THANK YOU!

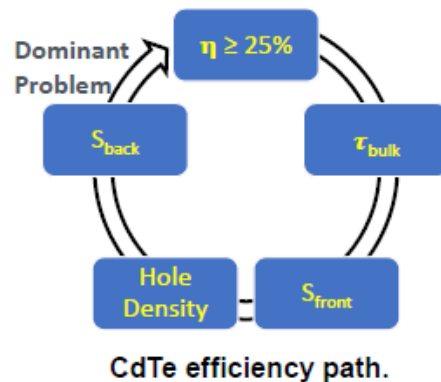
...QUESTIONS?



Highlights for SETO2 8974 (CSU, Sites)

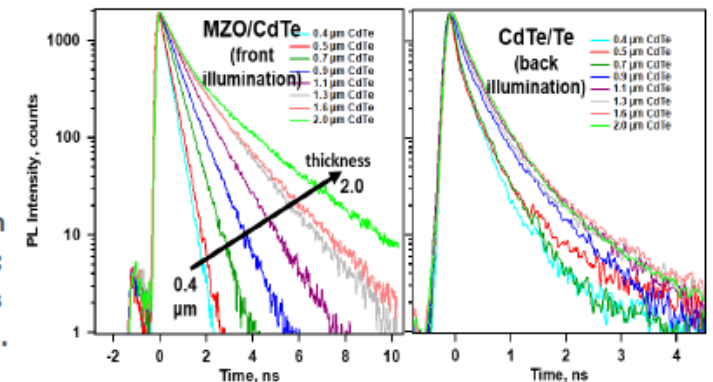
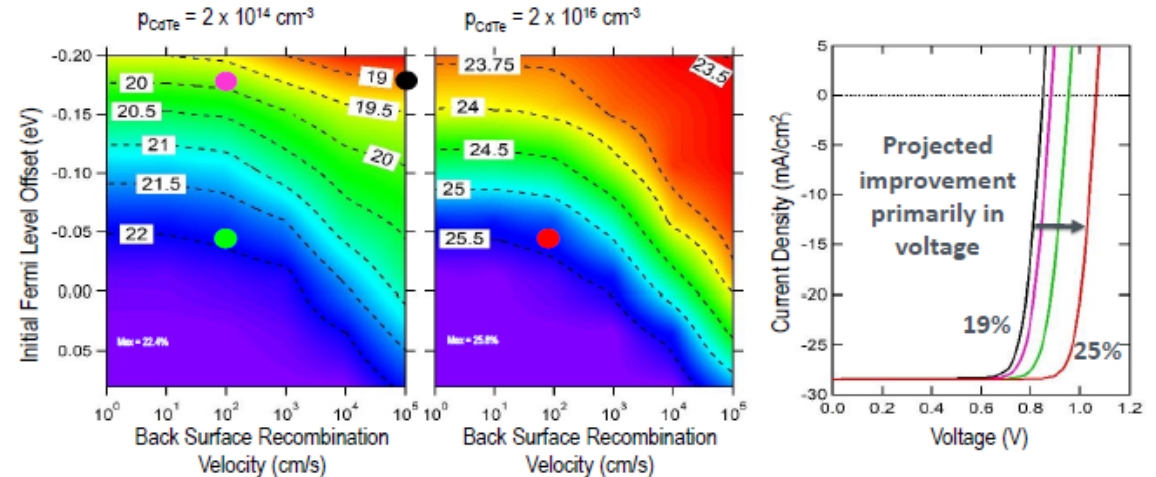


Strategy is to start from current baseline (black dot), reduce back-surface recombination (pink dot), reduce the initial Fermi-level offset (green dot), and increase the absorber carrier concentration (red).



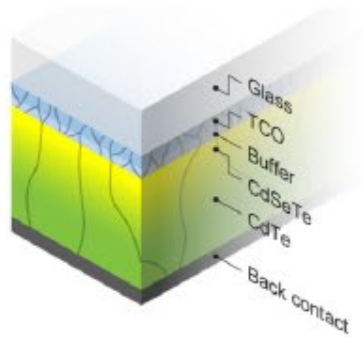
CdTe efficiency issues are being systematically addressed. Back contact remains the dominant problem.

Evidence: back-illumination TRPL recombination is low; front-illuminated increases dramatically with thickness.

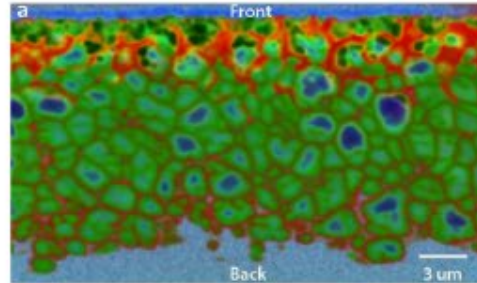


Additional project contributors: University of Toledo; First Solar, Inc.; National Renewable Energy Laboratory; University of Illinois at Chicago

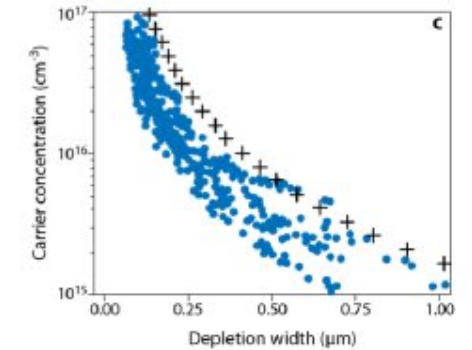
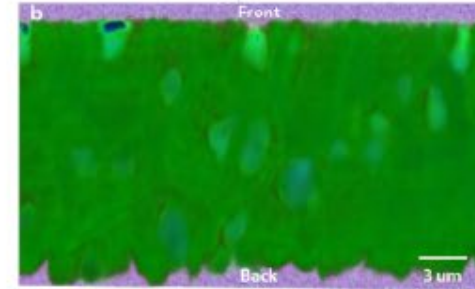
Highlights for Lab Call19-21 34353 (NREL, Metzger)



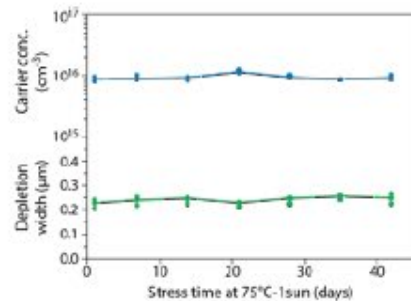
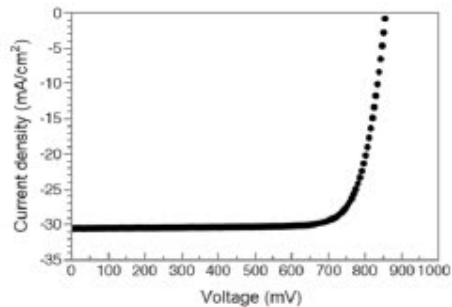
Schematic of a typical CdTe solar cell. The thin (3 μm) absorber is deposited in seconds on a glass/TCO substrate.



— V_{Te}
— Undoped
— Deep states

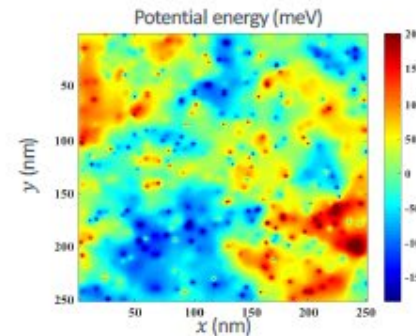


Thin film solar cells usually have poor carrier concentration control. CdTe was no different and limited to ca. 10^{14} cm^{-3} , well below the $10^{16} - 10^{17} \text{ cm}^{-3}$ ideal. The state-of-the-art dopant, Cu moves and creates stability issues. We shifted to placing group V elements (P, As, Sb) on the Te lattice site. Cathodoluminescence shows (a) ex-situ processes are non-uniform, (b) in-situ group V doping is uniform, (c) and hole density can now reach $10^{16} - 10^{17} \text{ cm}^{-3}$.

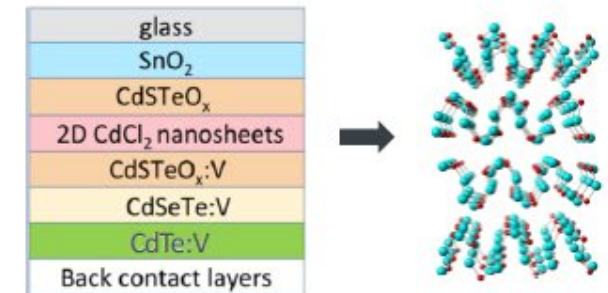


For the first time cells can be made by manufacturing methods without Cu. The efficiency has reached 21%, and the energy yield is greater than state-of-the-art cells. The approach also removes CdTe's largest stability issue, Cu doping.

Additional project contributors: University of Illinois at Chicago, First Solar



The 10^{18} cm^{-3} GrV incorporation needed today creates potential fluctuations, decreasing V_{oc} . We are researching dopants, defects, and new methods.

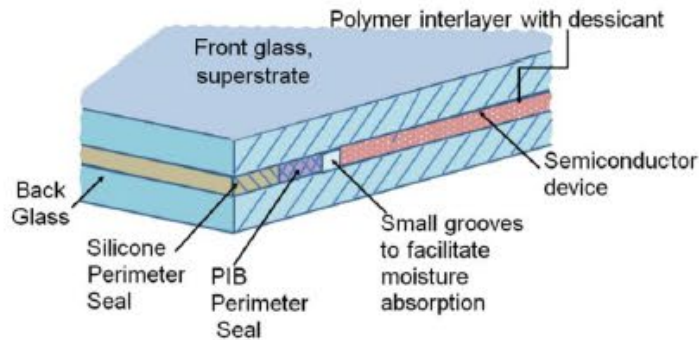


Planar, atomically smooth cleaves have provided seminal interface discoveries. We are reengineering the buried p-n interface to enhance performance.

Nature Energy, 4, 837

Highlights for PVRD2 8161 (CSU, Barth)

New Module Architecture

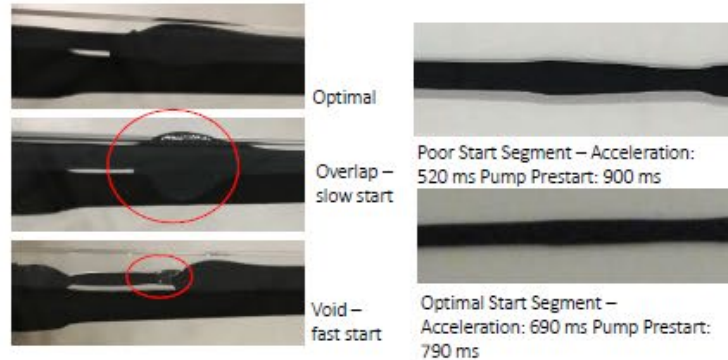


Encapsulation Prototype Tool

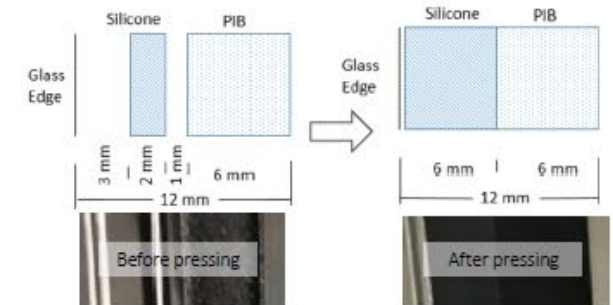


Additional project contributors: Sam Ellis, Tushar Shimpi, Larry Maple

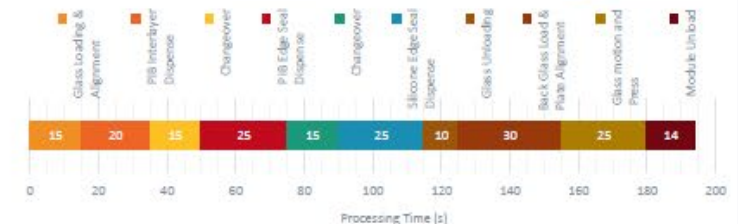
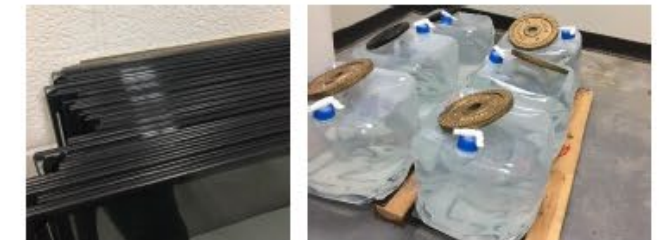
Dispense Optimization



Edge Seal



Quality & Speed Milestone

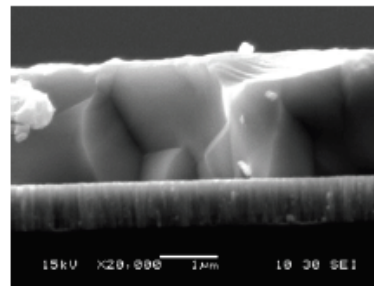
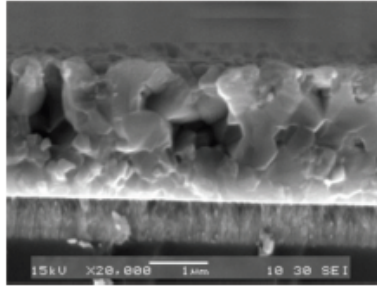


Highlights for PVRD 7551 (CSM, Rockett)

Dramatic improvement in grain structure & device performance

3 stage process:

Stage 1: 350°C, III-rich
Stage 2: 400°C, Cu-rich
Optional anneal (+5 min)
Stage 3: 400°C, III-rich
12 min total time.

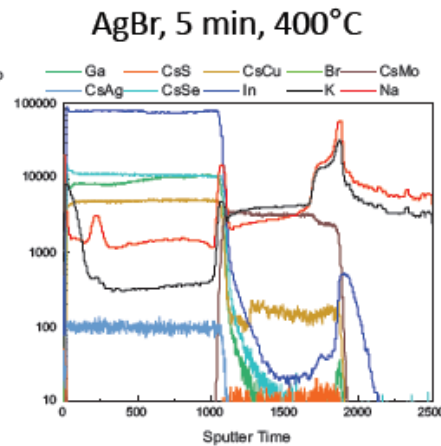
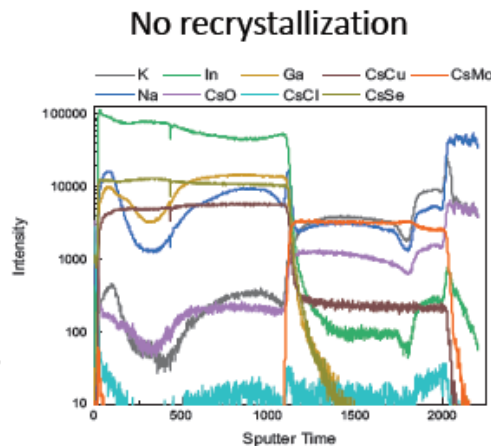


SIMS Profile:

Sharp interfaces retained.

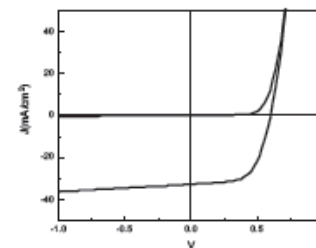
Ga profile lost in recrystallization.

Good results with AlCl_3 ex-situ anneal.
Also exploring CuCl and InCl_3 .

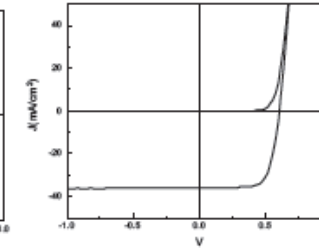


	Voc(mV)	Jsc(mA/cm ²)	FF(%)	η(%)
Reference	599	32.6	55.6	12
AgBr	605	35.9	72.2	15.7

No recrystallization



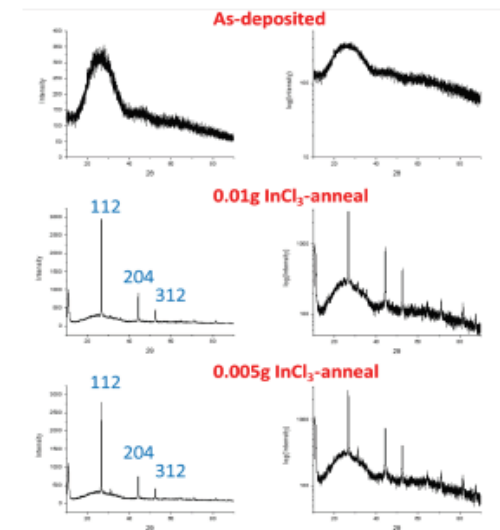
AgBr, 5 min, 400°C



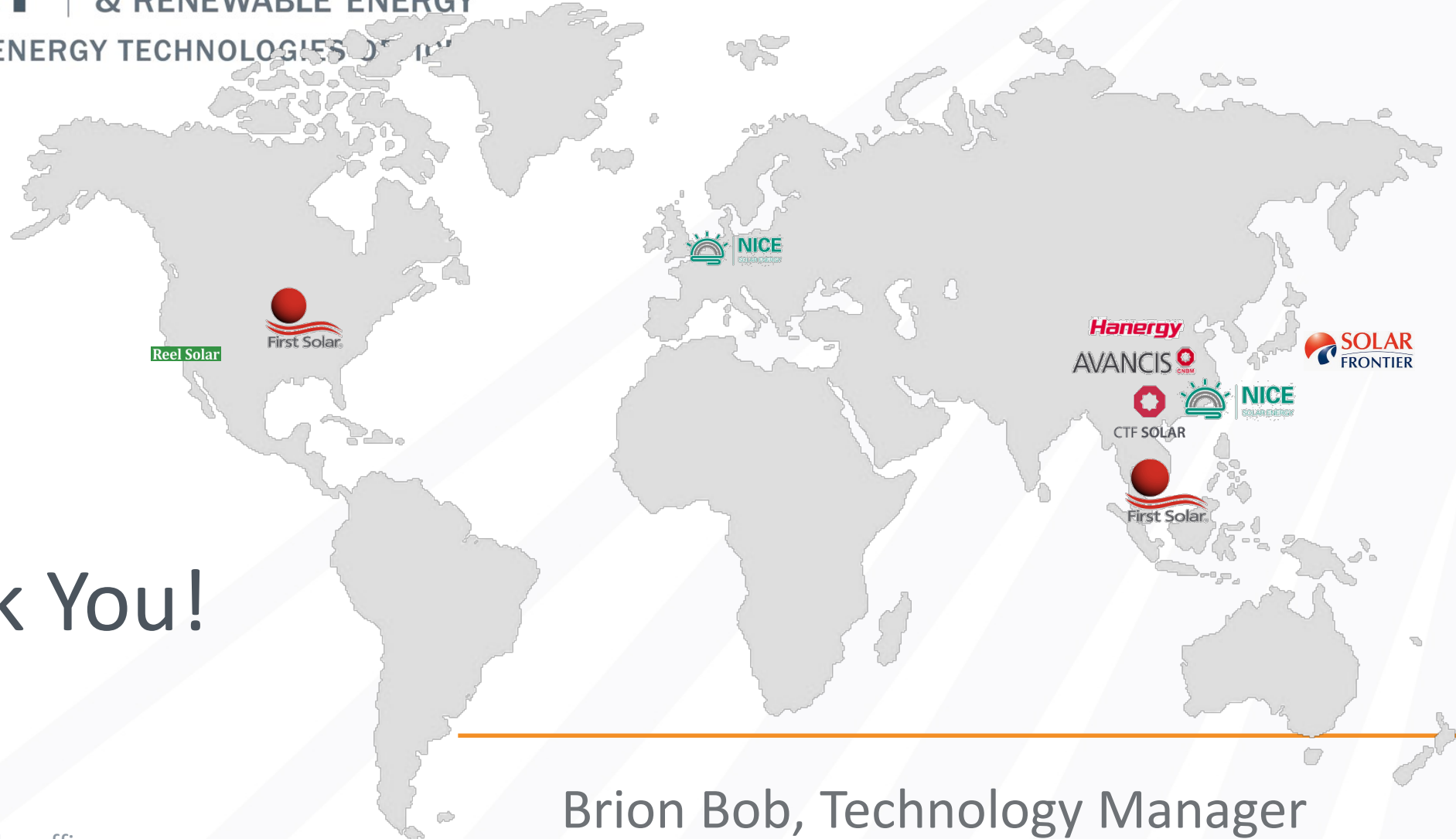
Reduced voltage-dependent collection, reduced series resistance, improved current, improved voltage & fill factor

Further improvements expected with corrected Ga profile & alkali halide PDT.

Recrystallization of initially amorphous material deposited at room temperature shows potential for even higher rates and lower temperatures



Additional project contributors: Sylvain Marsillac, ECE Department, Old Dominion University, Norfolk, VA



Thank You!