Sandia National Laboratories

Task 4: Adaptive Protection for Inverter Dominated Ugrids

PRESENTED BY

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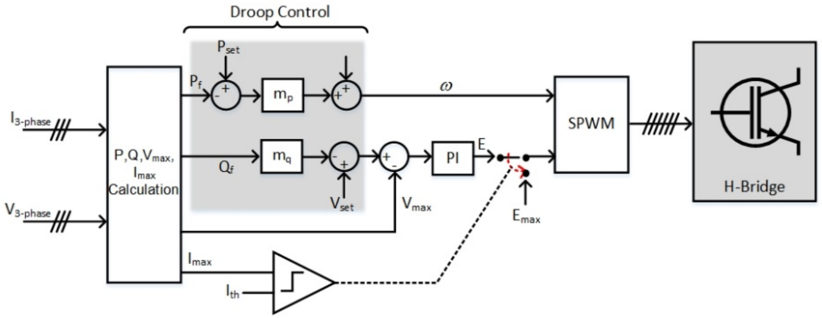
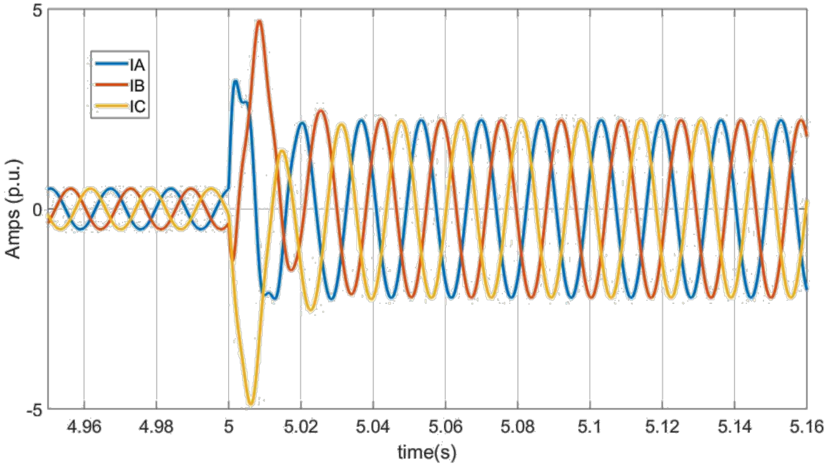
Task 4: Recent Accomplishments

- Modeling of grid forming inverters for protection studies
  - Collaboration with New Mexico State University
- Installing, testing, and validating designs using PHIL
  - Demonstration at DETL
- Adaptive protection design
  - Collaboration with Clemson University
  - Demonstration at DETL



Publications:

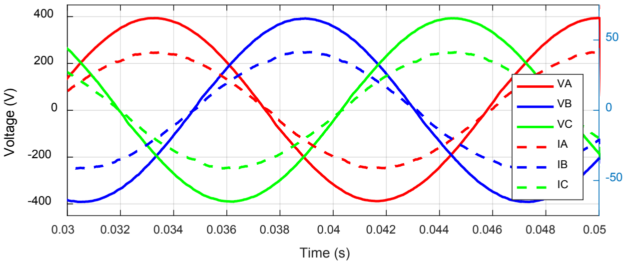
- "Simulation of Grid-Forming Inverters Dynamic Models using a Power Hardware-in-the-Loop Testbed"," IEEE Photovoltaic Specialists Conference (PVSC), 2019.
- "Grid-forming Inverter Experimental Testing of Fault Current Contributions," IEEE Photovoltaic Specialists Conference (PVSC), 2019.
- "Realistic Microgrid Test Bed for Protection and Resiliency Studies," North American Power Symposium (NAPS), 2019.



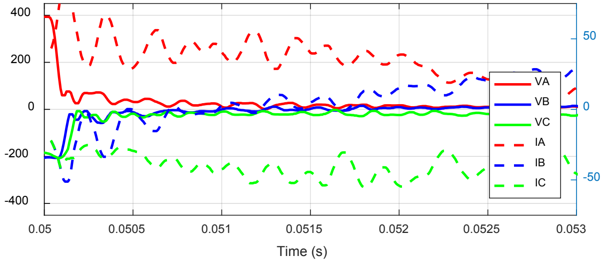
Inverter Short-Circuit Models

- It is important to have accurate models of inverters for dynamic studies and protection coordination
  - Initial spike (~0.1ms) depends on filter cap, system impedance, and pre-fault condition
  - Transients during control actions, lasting 2-8ms
  - Steady-state fault current based on the current limiter
- Models are challenging to develop because there are stark differences between manufacturers, single vs. three-phase inverters, PV vs. energy storage vs. grid forming inverters.

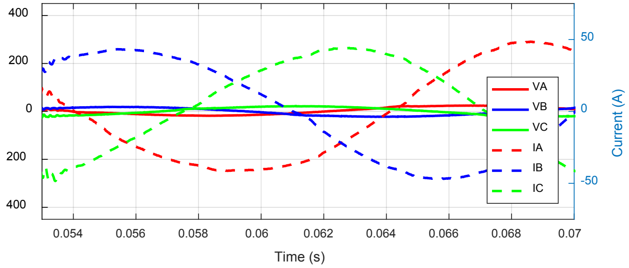
Pre-fault



Transient Fault Response

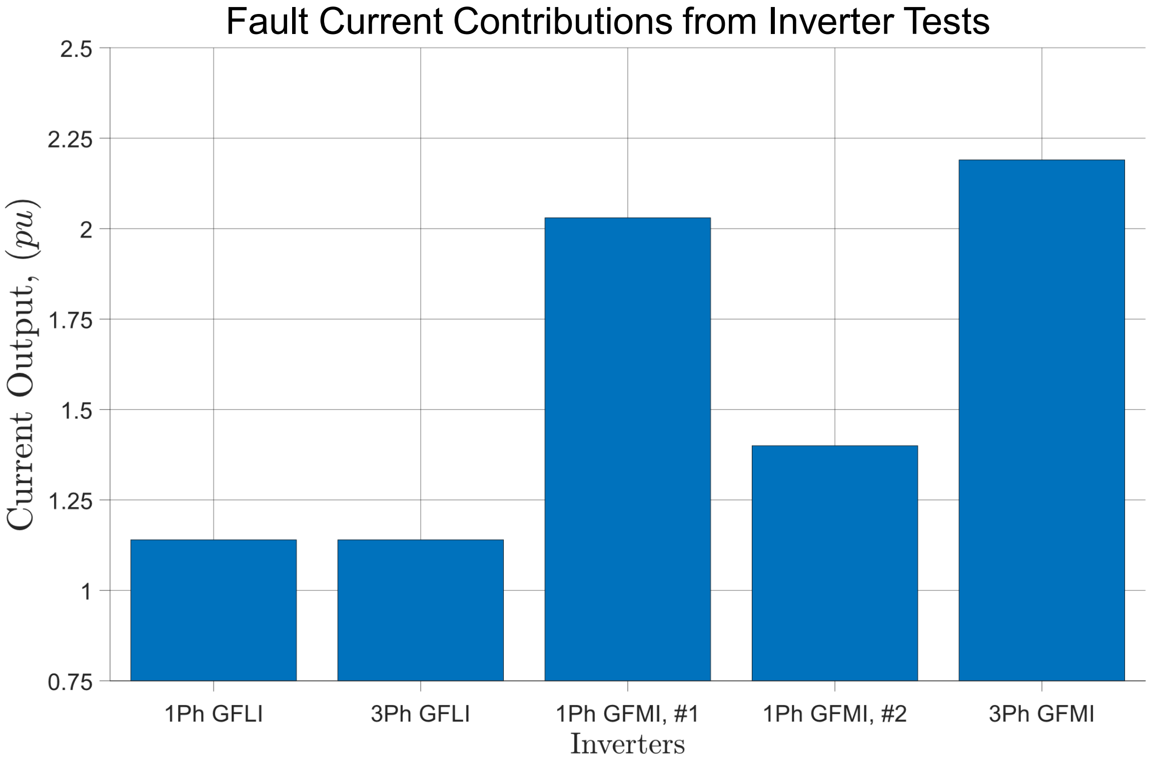


Steady-State Fault Response



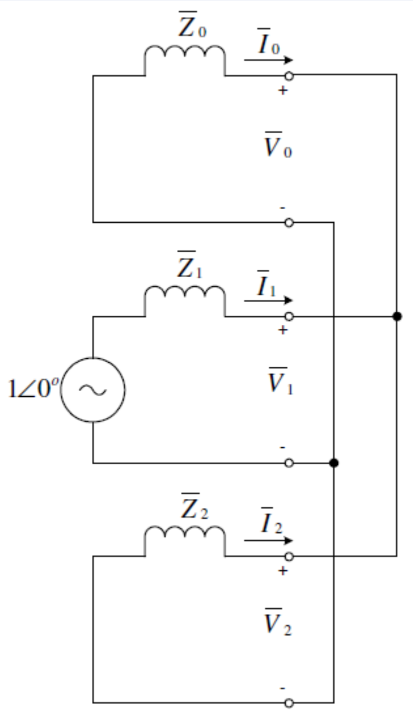
Inverter Tests - Fault Characterization

- Best way to fully characterize inverters for all transient and steady-state time scales is through testing (Sandia's DETL)
- Grid-following inverters (GFLI) generally have very low fault current contributions (1.1-1.2 of their rated current)
- Grid-forming inverters (GFMI) can deliver 2x the rated current for about 60 seconds

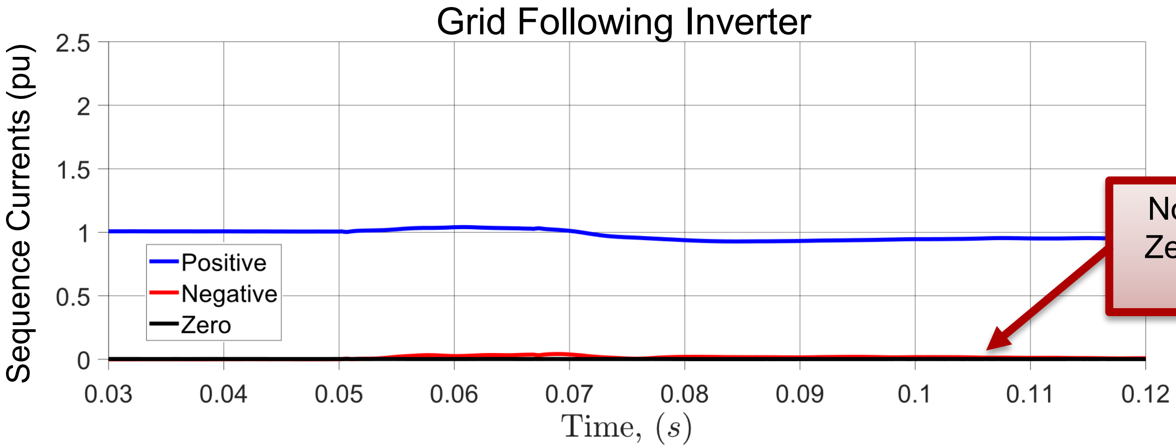


Inverter Tests – Double-Line-to-Ground Fault

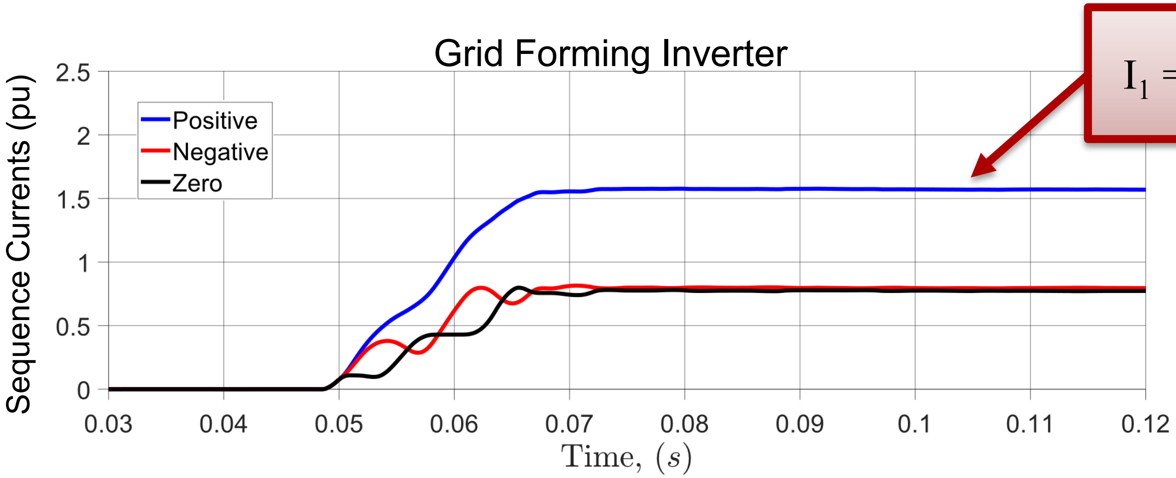
Double-Line-to-Ground Fault Diagram



$$V_0 = V_1 = V_2$$
$$I_1 = -(I_0 + I_2)$$


Grid Following Inverter

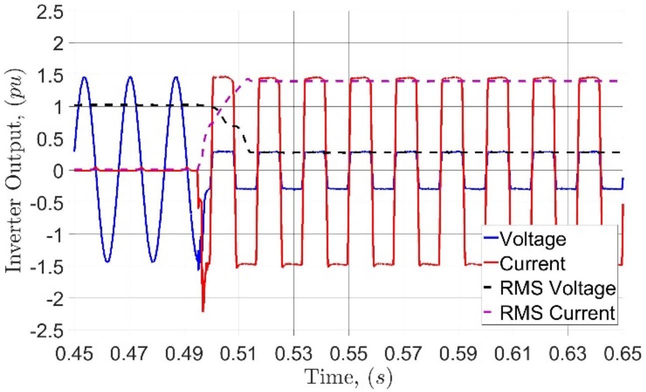
No Negative or Zero Sequence Current


Grid Forming Inverter

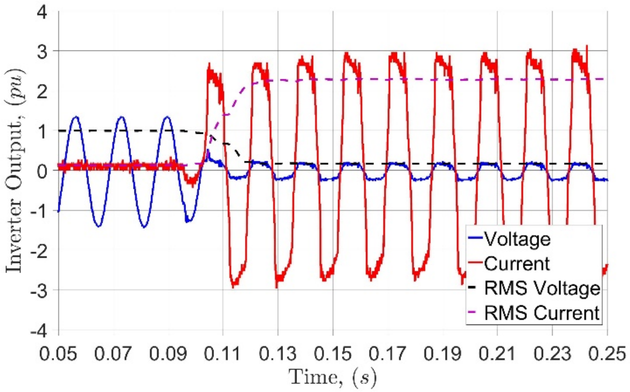
$I_1 = -(I_0 + I_2)$

Inverter Controls – Fault Current Limiter

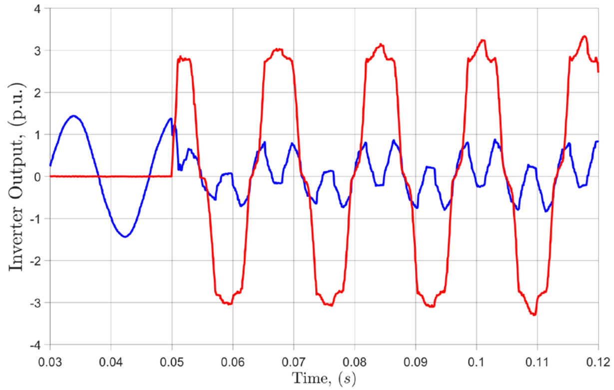
- Fault current contribution from inverters is determined by the inverter current limiting control
- Each inverter and manufacturer have different magnitudes of fault current, but they also produce different types of fault current
  - Controlling current magnitude (sine wave) vs. controlling instantaneous current at the H-bridge (square wave) vs. hysteresis control
  - Speed of PLL (GFLI) or droop controls (GFMI)



GFMI clipping current output during fault without peaking



GFMI clipping output current during with peaking



GFMI curtailing current output during with hysteresis control

Installing, testing, and validating designs using Power Hardware in the Loop (PHIL)

Demonstration of resilient nodes based on the framework.

Initial demonstration using PHIL at Sandia DETL

- Grid-forming inverters (GFMI) have been integrated into DETL for demonstration
- This collection of single-phase and three-phase, solar GFMI and battery GFMI, and different vendors allows us to demonstrate different systems and test how various inverter designs will perform:
    - OutBack Power
    - Schneider Electric
    - Princeton Power Systems
    - SMA
    - ABB

Simulation of Grid-Forming Inverters Dynamic Models using a Power Hardware-in-the-Loop Testbed.

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Abstract — **Modern power grids include a variety of renewable Distributed Energy Resources (DERs) as a strategy to comply with new environmental and renewable portfolio standards (RPSs)**

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peer-to-peer coordination between devices. This is typically accomplished by the use of droop control schemes in frequency and voltage [7].

Recently, a workshop related to GFMIs for low inertia power systems [8] gathered members of academia, researchers of national laboratories, utility engineers, and representatives of inverter and protective relaying manufacturers. In this workshop, presenters addressed the state-of-the-art in GFMI power electronics, reliability, and control. Furthermore, design engineers of protective relaying equipment expressed their concerns about the negative influence of the Phase Locked Loop (PLL) of GFLIs in terms of protection, loss of synchronism, and inability to supply negative sequence current during fault scenarios. Even though protective relay manufacturers are able to design protective relays for both types of inverters either at transmission or distribution level [9], [10]; design engineers clearly expressed their preference towards protection of GFMIs scenarios, since these inverters inherently behave in a similar way as synchronous machines without the need of PLL for synchronization purposes.

To date, almost all GFMI behavior and incident operational benefits have been shown in simulation. More research into hardware demonstration is needed. While demonstration of GFMI in application environments is ideal, it is difficult to tractable test hardware in a wide variety of operation conditions. Power Hardware-In-Loop (PHIL) is a hybrid simulation/hardware testbed that can apply simulated grid conditions to actual hardware. It is a flexible, high fidelity extension of simulation results that are more tractable to implement for a wide variety of operating conditions than a pure hardware testbed.

Even with a very broad and in-depth analysis of the benefits of GFMIs, topics about testing such devices using PHIL are often not discussed. While there is abundant literature that explain the different methods of interfacing GFLIs using PHIL interfaces [11], [12], [13], [14], [15], the process of interfacing GFMIs using PHIL interfaces presents its own challenges in terms of stability and control. These challenges, so far, have not been properly addressed in literature.

This paper presents simulation results of two GFMI simulation models interfaced with physical GFLIs using a PHIL setup. The main idea behind these simulations is to recognize and understand the intrinsic dynamics of the simulation models in terms of transient stability, voltage and frequency regulation, and load sharing capabilities. Results of the PHIL tests will

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Grid-forming Inverter Experimental Testing of Fault Current Contributions

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Abstract — **Historically, photovoltaic inverters have been grid-following controlled, but with increasing penetrations of inverter-based generation on the grid, grid-forming inverters (GFMI) are gaining interest. GFMIs can also be used in microgrids that require the ability to interact and operate with the grid (grid-tied), or to operate autonomously (islanded) while supplying their corresponding loads. This approach can substantially improve the response of the grid to severe contingencies such as hurricanes, or to high load demands. During islanded conditions, GFMIs play an important role on dictating the system's voltage and frequency the same way as synchronous generators do in large interconnected systems. For this reason, it is important to understand the behavior of such grid-forming inverters under fault scenarios. This paper focuses on testing different commercially available grid-forming inverters under fault conditions.**

Index words: grid-forming, distributed energy resources, fault, microgrid.

I. INTRODUCTION

With increasing penetrations of inverter-based generation on the grid, largely coming from PV and energy storage distributed energy resources (DER), the grid support functions and inverter capabilities, such as volt-var, frequency-watt (FW) and ride-through (RT) capabilities, continue to become more critical with an ever-expanding list of capabilities to ensure grid stability under generation variability. Added to this list are grid-forming inverters (GFMI) that have the capability to provide their own voltage and frequency reference and island from the main grid. Similar to the desire to protect an area electrical power system (EPS), it is also desired to ensure that the devices connected to a microgrid remain healthy after a fault occurrence. However, unlike other distributed energy resources (DER), inverters use various control schemes that vary between manufacturers. Therefore, the dynamic responses of GFMI during fault conditions are not fully known and can vary significantly between devices. Applying faults to GFMIs from a variety of manufacturers is necessary to quantify the degree of difference and similarity to fault response. Using the Low Voltage RT (LVRT) requirement from IEEE 1547-2018, a fault will be defined as condition that causes the GFMI to output a voltage level below 88% of the nominal voltage (V_{nom}).

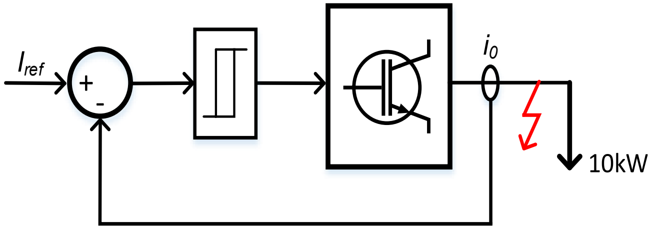
Although DERs are not required to have the functionality required by IEEE Std 1547-2018 [1] while operating on an islanded microgrid, some of these functionalities are beneficial when an inverter is tied to a low inertia system, primarily the FW function. This functionality allows for proper load sharing of grid-following inverters (GFLI) when tied to a droop control GFMI. However, with LVRT capabilities enabled, when a fault occurs that causes the output voltage of the GFMI to be reduced to less than 50% of $V_{nom,}$ any GFLI would go into a momentary cessation if the event lasts longer than 5 cycles. This event would also require other DER such as synchronous generators to cease to energize after 10 cycles. This could result in driving the voltage even lower as the overall injection of current would be only that of the devices without these capabilities enabled. Additionally, with GFLIs operating with their frequency RT capabilities enabled the inverters are susceptible to nuisance trips if the circuit load is not properly balanced with a droop control GFMI controlling the voltage frequency. Any frequency outside of 58.5 – 61.2 Hz must trip after 5 minutes of continuous operation, and any frequency outside of 56.5 – 62 Hz must trip within 10 cycles. This can lead to further issues within the microgrid.

Due to the low inertial characteristics of a microgrid, fault causing events, such as damage to power lines, are more detrimental to the system [6]. A fault condition in the microgrid could lead to the load demand exceeding the maximum production of the DERs capacity. When the GFMIs experiences these type of scenarios, the inverter reduces its voltage output due to the reduced grid impedance, [4].

With the high current demand of an inductive motor start up, it is desired that a GFMI be capable of providing current above its rated value for a short duration to supply the increased current draw from the inductive motor start and keep voltage reduction in the microgrid to a minimum. While conventional GFLI may only inject 1.1 to 1.2 p.u. current during a fault, GFMIs that utilize energy storage can be designed (either via controls, for short duration events <10 cycles or hardware for longer duration) to be capable of outputting current levels 2 to 3 times greater than their rated outputs during an overload condition. In order reduce low voltage events due to inductive motor starts, as well as to properly coordinate the protection system, understanding the fault current characteristics of GFMIs is very important [2]-[9].

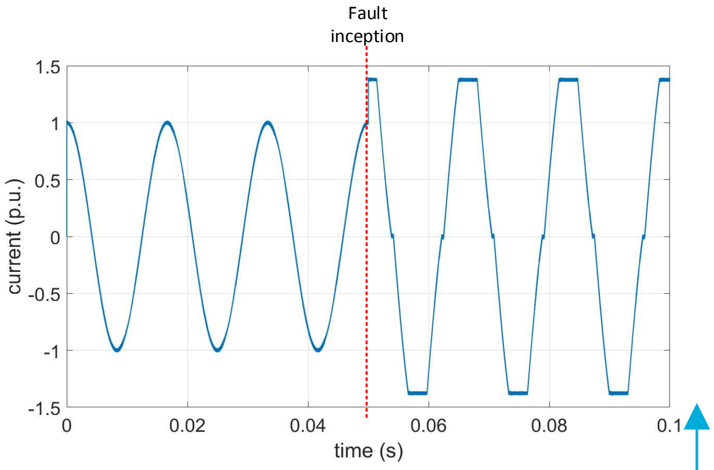
This paper is organized in the following manner. Section II describes the basic configuration of a microgrid and how the GFMI was subjected to fault conditions. Section III contains

Validation of Grid-Forming Inverter Simulation



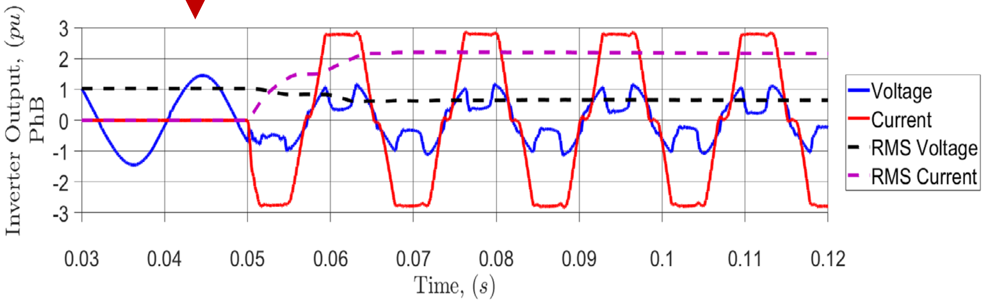
- Control switching scheme based on hysteresis
  - facilitates the four-quadrant operation of the inverter as an AC current source into a grid regulated for voltage and frequency
  - hysteresis comparison implemented by using output current of the inverter

- Validated against real GFM
  - fault applied at the terminals of the inverter supplying rated power (10 kW) at a time of 0.05 s
- Fault behavior shows a good qualitative match to the experimental fault behavior
  - inverter current saturates in a near square wave behavior
  - characteristic shoulder at a current of 0 p.u
- Further work is ongoing to implement full closed loop control



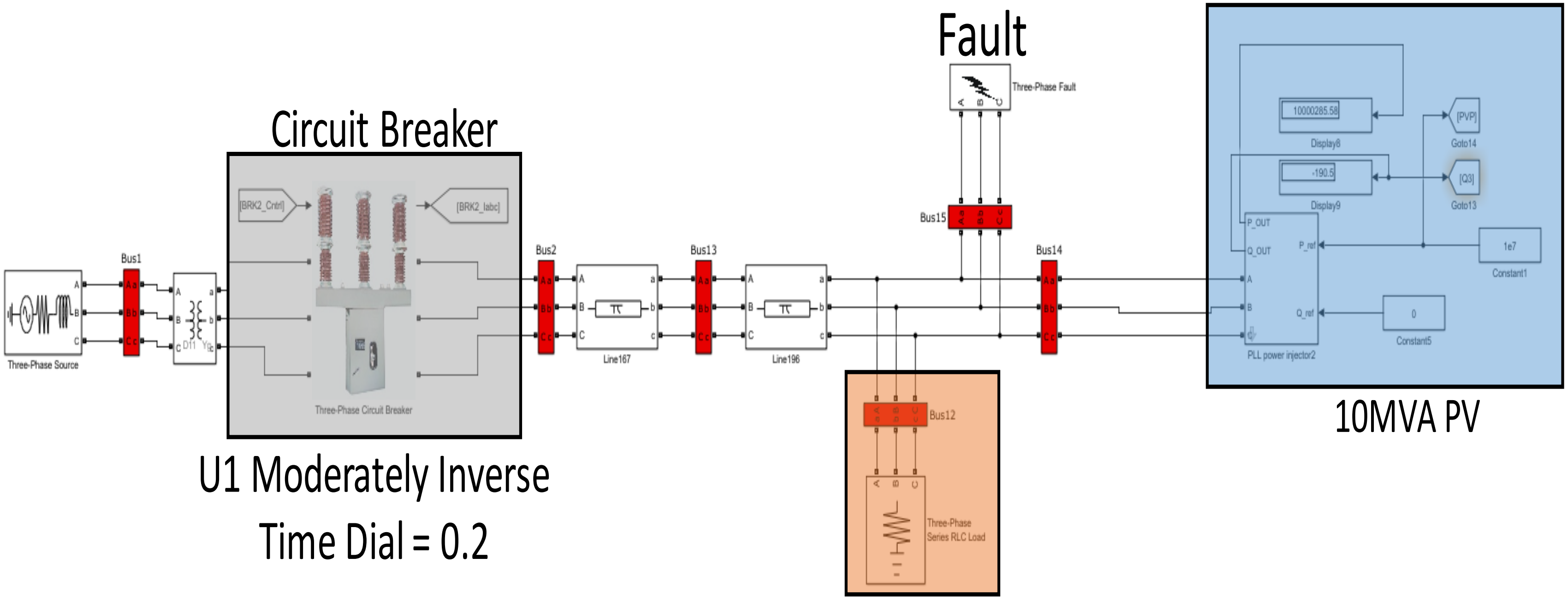
Experimental

Simulated



Designing adaptive protection schemes for inverter-dominated microgrids.

Test System in Simulation



Fault

Circuit Breaker

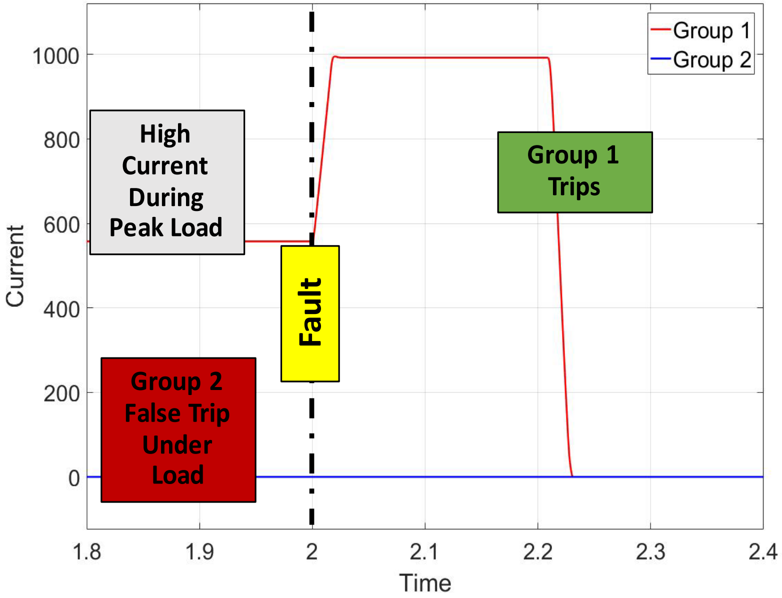
U1 Moderately Inverse

Time Dial = 0.2

10MW Load

10MVA PV

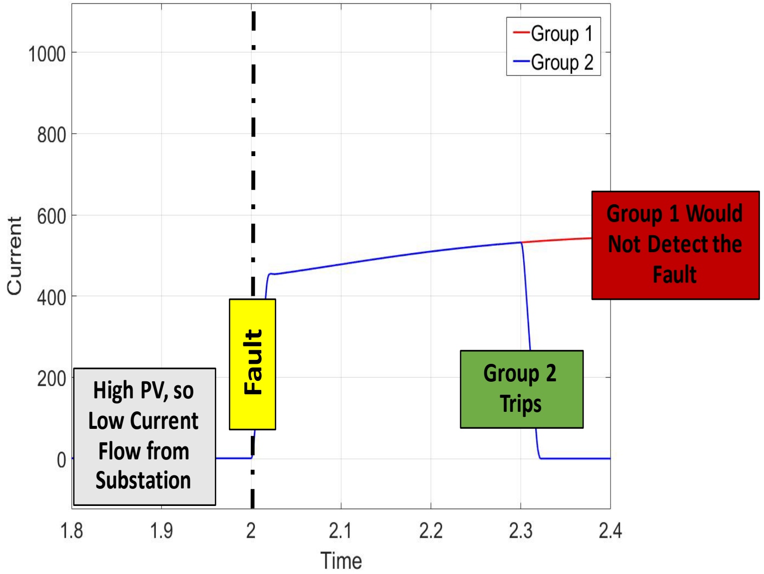
Designing adaptive protection schemes for inverter-dominated microgrids



High Current During Peak Load

Group 1 Trips

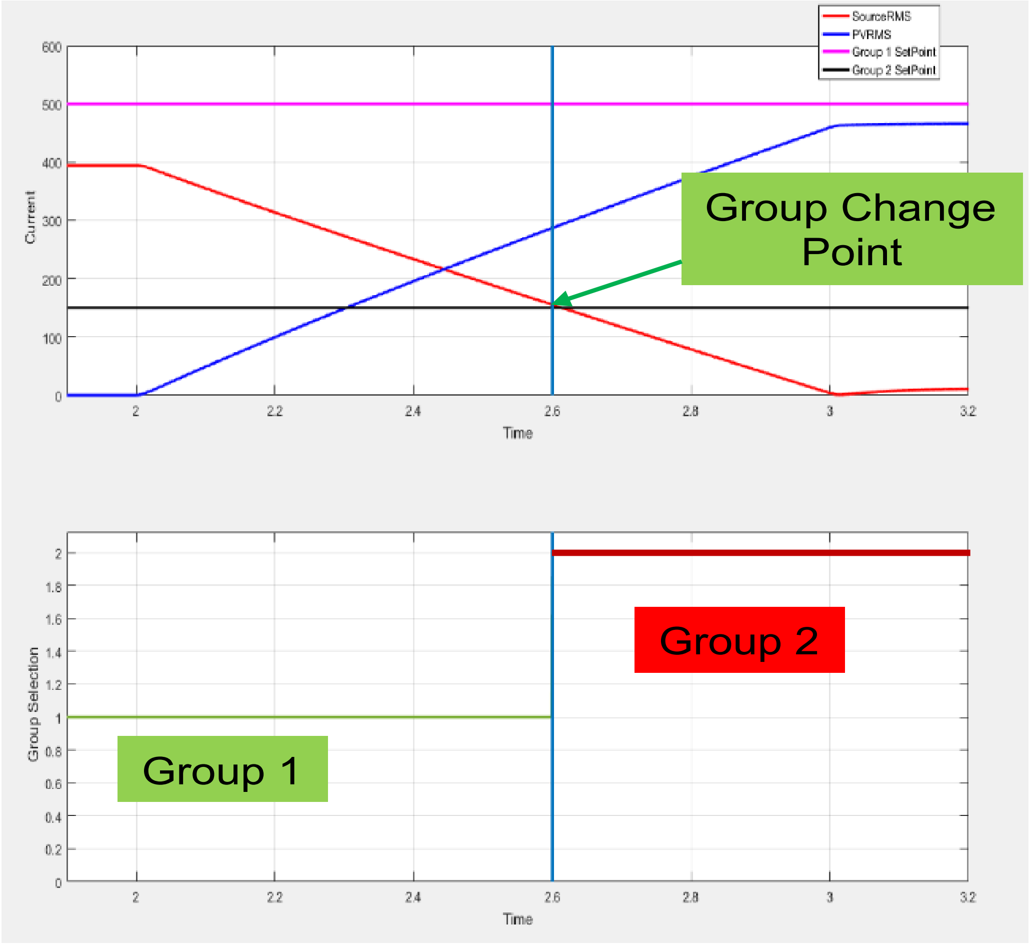
Group 2 False Trip Under Load



Group 1 Would Not Detect the Fault

High PV, so Low Current Flow from Substation

Group 2 Trips



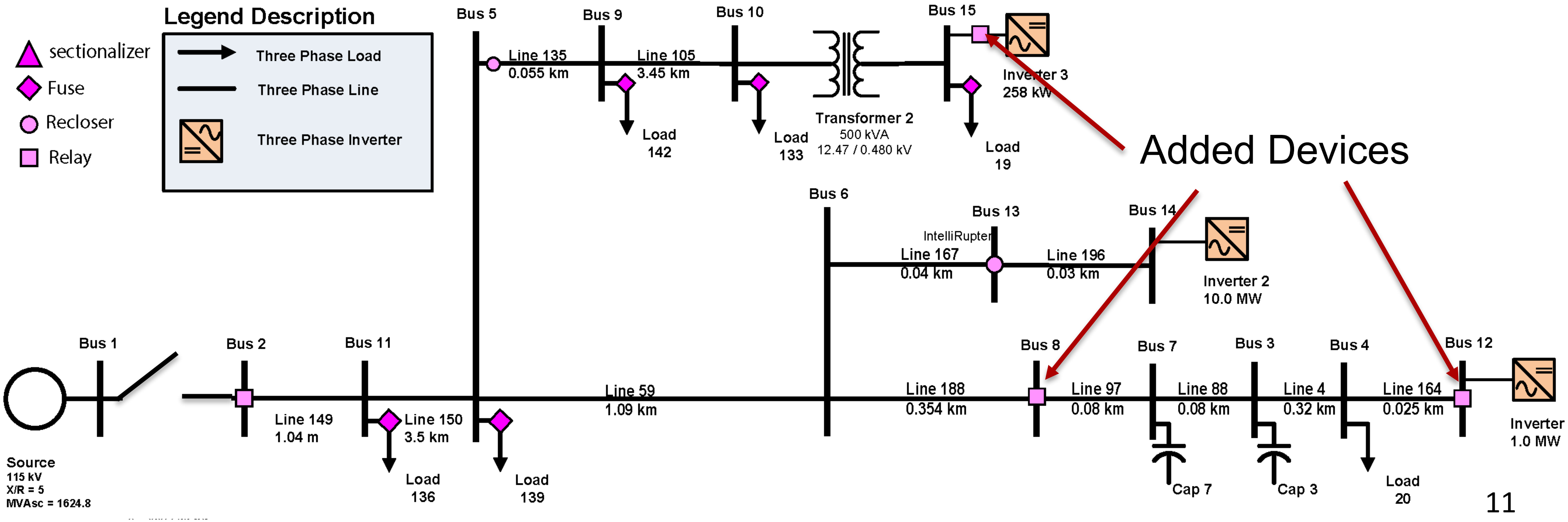
Group Change Point

Group 2

Group 1

Protection System Changes for Islanding

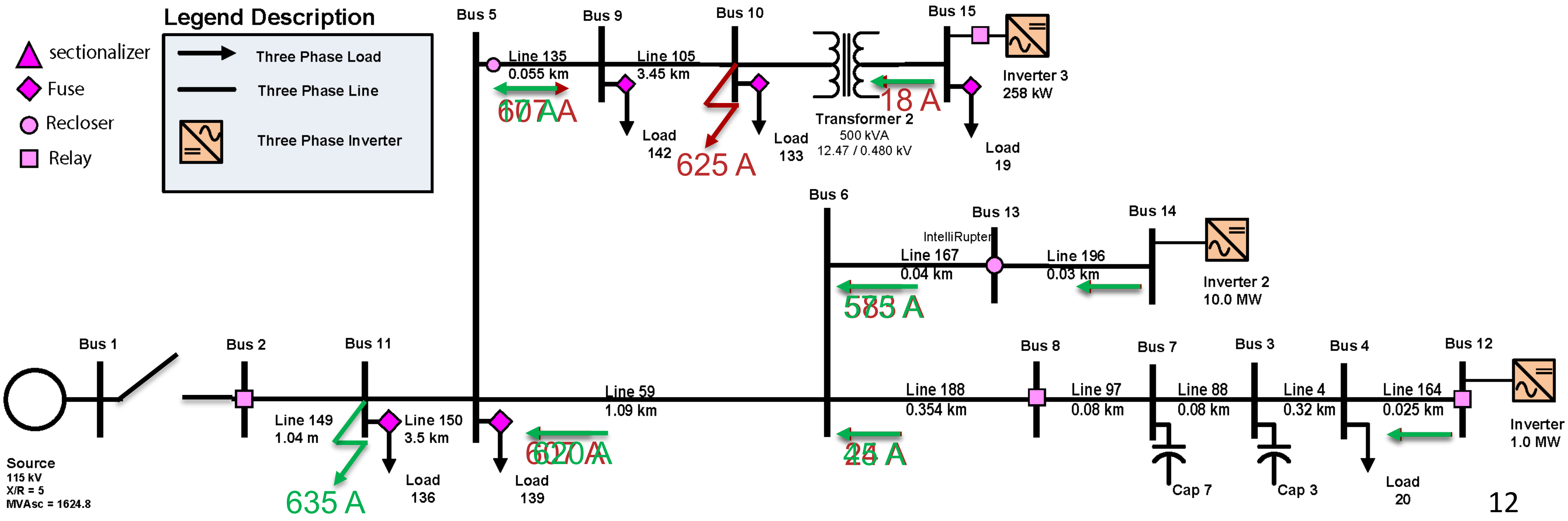
- Must add protective devices to the generation (instead of self protection when grid connection is lost)
- Sectionalizers must be removed because it cannot be coordinated with multiple fault paths



Added Devices

Adaptive Protection Scheme for Microgrids

- Protection scheme must change with microgrid operation mode (Different setting for grid-connected and islanded mode)
  - Lower trip setting for islanded mode to operate for limited fault currents.
  - Different coordination scheme for the changed network topology.
- Direction dependent coordination curves for forward and reverse
  - Different trip setting depending on the direction of fault current.
  - Recloser is backed up by Relay at Bus 15 for Forward direction fault (green)
  - Recloser is backed up by IntelliRupter & Relay at bus 8 in reverse direction fault (red)



National Grid Test feeder for protection studies

- 13 KV class feeder with voltage regulator, recloser and fuses. Multiple voltage regions on feeder connected by step up/down transformers.
- CYME model that will be converted for use in HIL
- Adaptive protection design
  - Move design and testing from sample IEEE test feeder and simplified local feeder to the NG Test Feeder.
- Data gathering on types of existing DER on feeder and data for the substation model ongoing.