SOLAR ENERGY TECHNOLOGIES OFFICE
U.S. Department Of Energy

Power Electronics Program Kickoff

# PV Inverter Systems Enabled by Monolithically Integrated SiC based Four Quadrant Power Switch (4-QPS)

FREEDM systems center

NC STATE UNIVERSITY

Topic area: TA-1
Control No: 1740-1612

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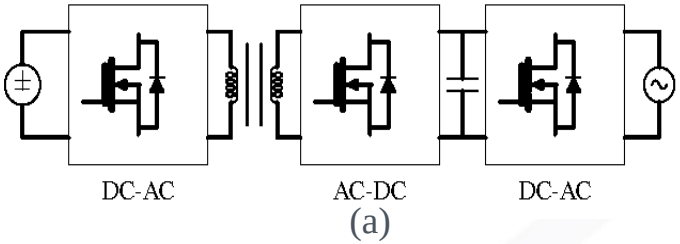
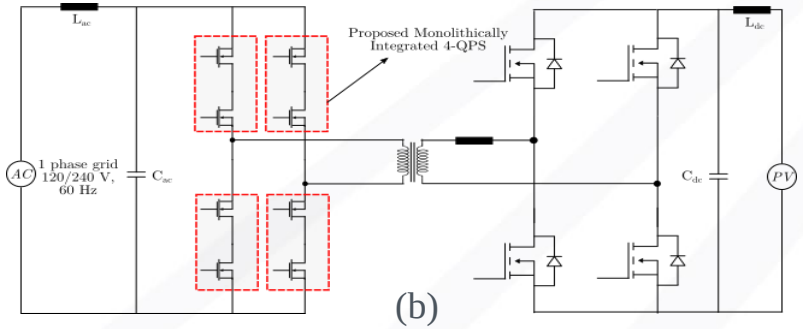
Jayant Baliga (co-PI)
Douglas Hopkins (co-PI)

# Project Goal and Approach – 3 Areas

- Cyclo-converter based 1-phase and 3-phase grid connected PV inverter enabled by Monolithically integrated SiC 4-QPS at 1200V, 10-25A
  * Advanced packaging of single switch module and 3-phase switch module




- **Elimination of DC electrolytic capacitors**
- Capacitors required are filter capacitors which are film capacitors (small VA rated, available for high ripple current with low ESR)
- All switches shown can be SiC 4-QPS – hence standardized modules

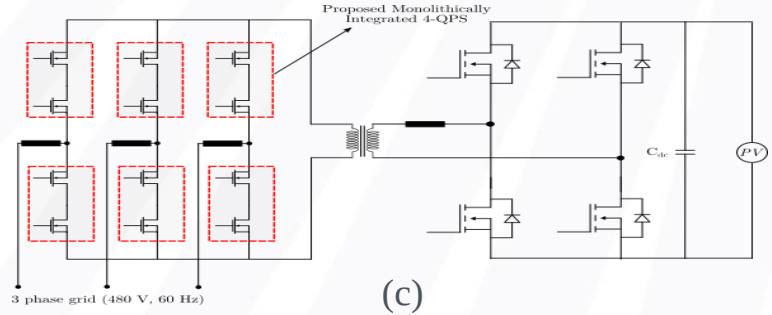
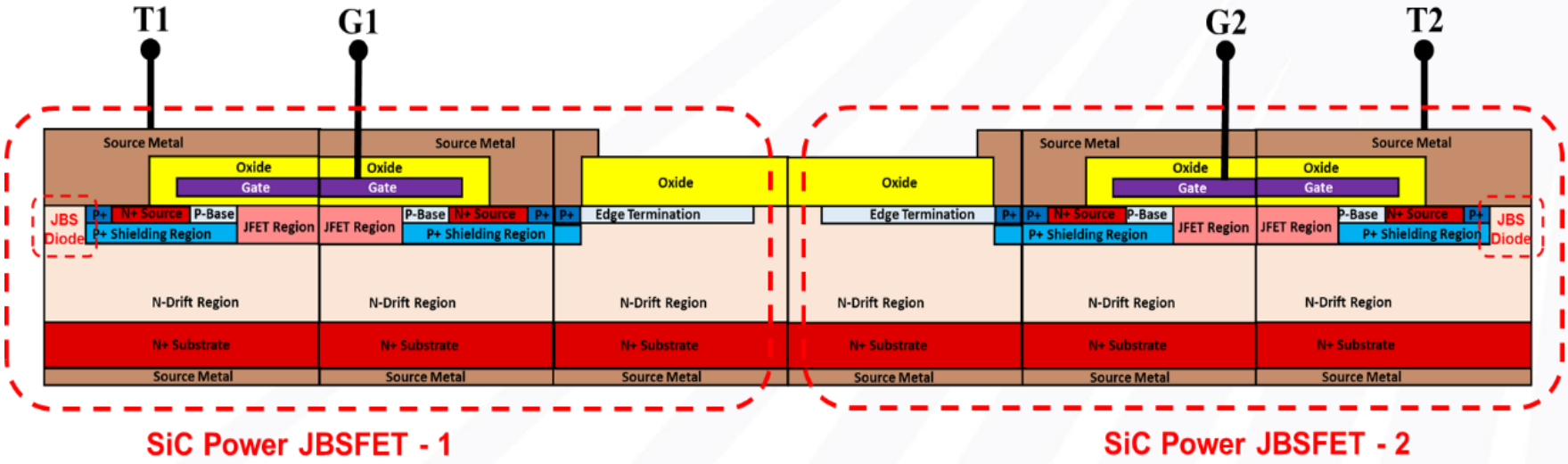



**Figure 1:** (a) Conventional power architecture for DC-AC conversion, (b) High-frequency link single phase inverter using 4-QPS enabled cyclo-converter (c) High-frequency link 3-phase inverter using 4-QPS enabled cyclo-converter.

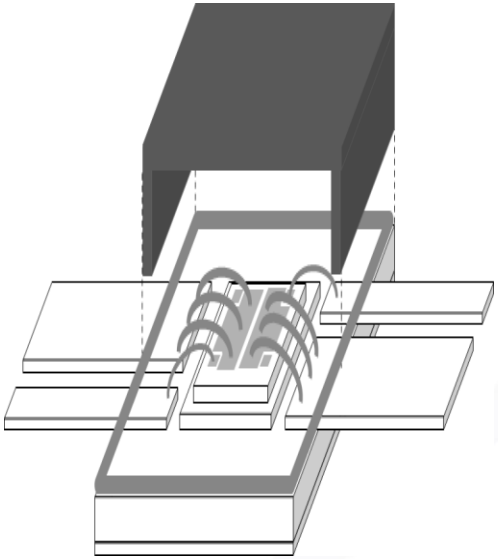
# Proposed SiC Bi-Directional FET – BiDFET (or 4QPS)

- Monolithically integrated SiC based 4-QPS at 1200V and 10-25A

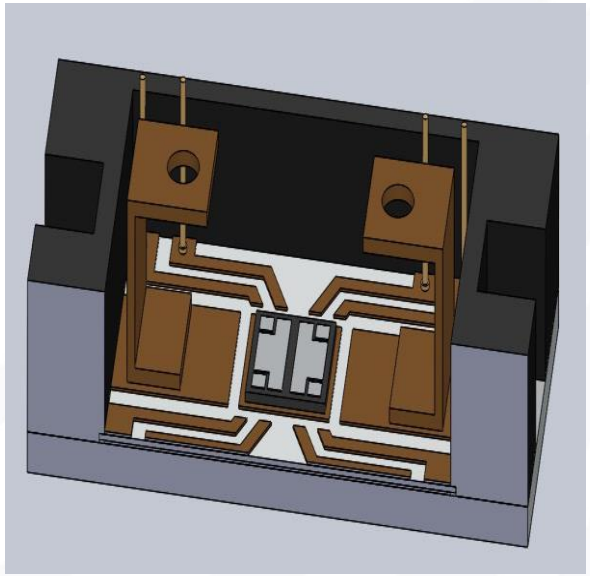


# Proposed Packaging of BiDFET (or 4-QPS)

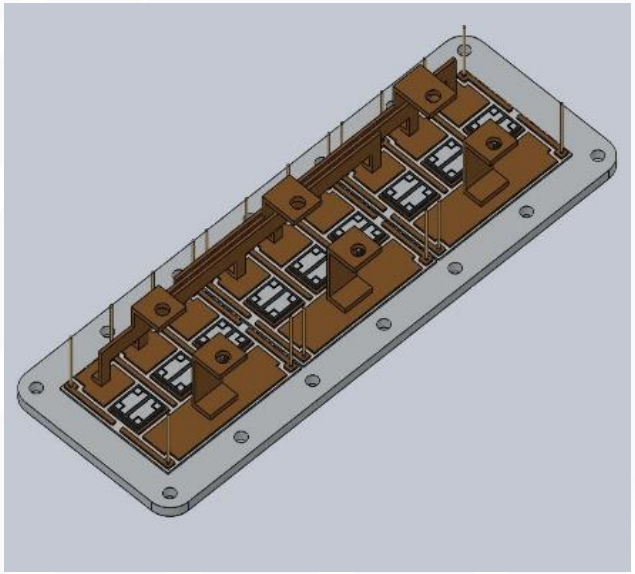
*Advanced Packaging of BiDFET rated 1200V and 10-25A*



(a)



(b)



(c)

(a) High performance planar tab package and layout (b) Single switch module with housing and baseplate (c) Three phase switch module with baseplate

# Program Tasks and Research Outcomes

- Task 1: Overall Project coordination and Project management – [Bhattacharya (SB)]
- Task 2: BiDFET (or 4-QPS) device design, fabrication (X-Fab), testing – [Baliga]
  - Scale-up to high current with lowest Rds_on at 1200V

- Task 3: Packaging and Module (PREES Lab) – [Hopkins]
  - Module with single switch and 3-phase switch to meet standards
  - Module with paralleled dies and suitable for higher temperature (175C)

- Task 4: PV - 1ϕ AC Grid Connected Converter Hardware Prototype at 1.5 kW (FREEDM Lab) - [SB]
  - Gate driver design and operation for BiDFET (or 4-QPS) – high frequency (200kHz), short circuit protection, with diagnostics and prognostics features
  - Control of grid connected converter system (with low inertia)
  - Investigate grid support functions

- Task 5: PV 3ϕ AC Converter Hardware Prototype at 15 kW Scale (FREEDM Lab) – [SB]
  - Control of grid connected converter system (with low inertia), grid support functions

# Proposed Technology Target Level of Performance

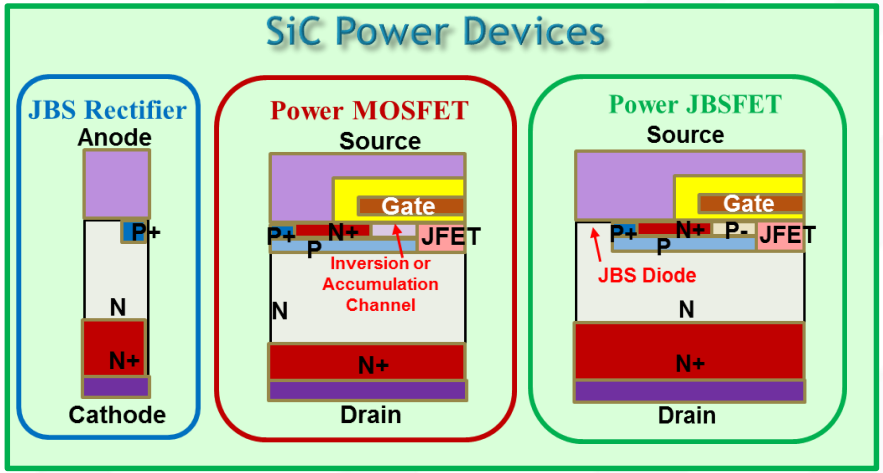
| | Technical and Market Specifications | | | |
|---|---|---|---|---|
| | Current State of Art 1ϕ two stage PV inverter (Residential) | **1ϕ 4-QPS enabled PV inverter (Residential)** | Current State of Art 3ϕ two stage PV inverter (Commercial) | **3ϕ 4-QPS enabled PV inverter (Commercial)** |
| **Cost** | >$0.1/W | **<$0.05/W** | >$0.08/W | **<$0.04/W** |
| **Efficiency** | 95% | **98% - 98.5%** | 95% | **98% - 98.5%** |
| **Power Density** | 5W/in3 | **12W/in$^3$** | 3W/in$^3$ | **12W/in$^3$** |
| **Reliability** | 10 years | **>20 years** | 10 years | **>20 years** |
| **Interoperability** | IEEE, ANSI, NERC Compliant | **IEEE, ANSI, NERC Compliant** | IEEE, ANSI, NERC Compliant | **IEEE, ANSI, NERC Compliant** |
| **Baseload PV Plant Operation Capability** | No | **No** | No | **No** |
| **Power Rating** | 1.5kW | **1.5kW** | 15kW | **15kW** |
| **Grid Interconnection Voltage** | 240V | **240V** | 480V | **480V** |

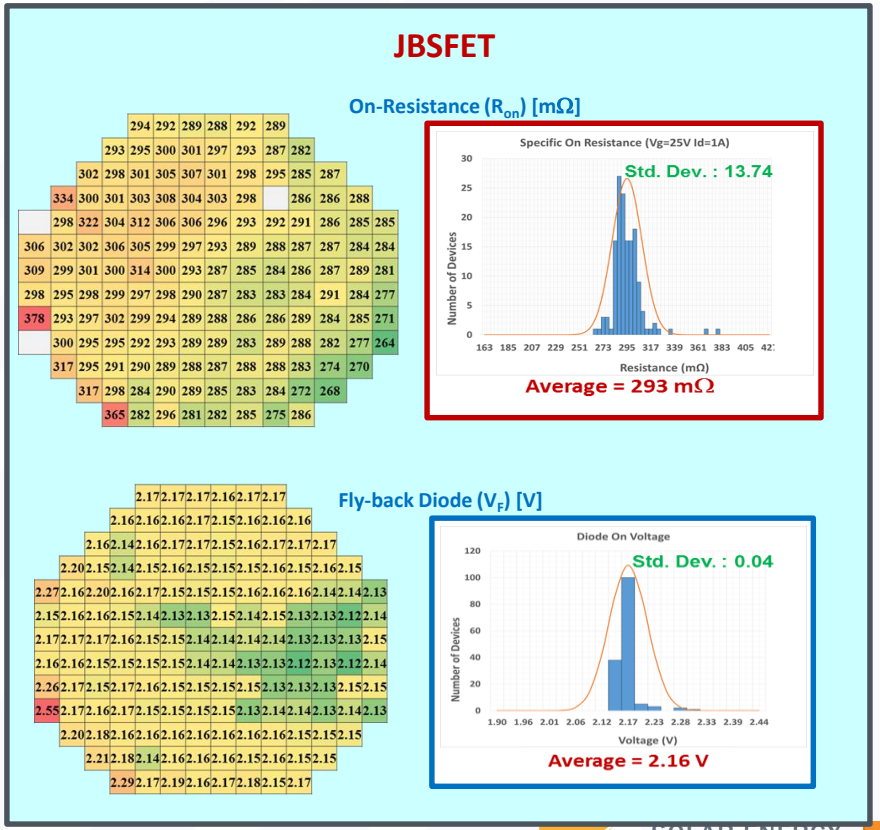
**Table 1:** Technical and market performance criteria specifications for current state of the art solar inverters at both residential (1.5 kW) and commercial (15 kW) scale as compared to the proposed solutions to satisfy proposal requirements

# NCSU PRESiCE Manufacturing Technology

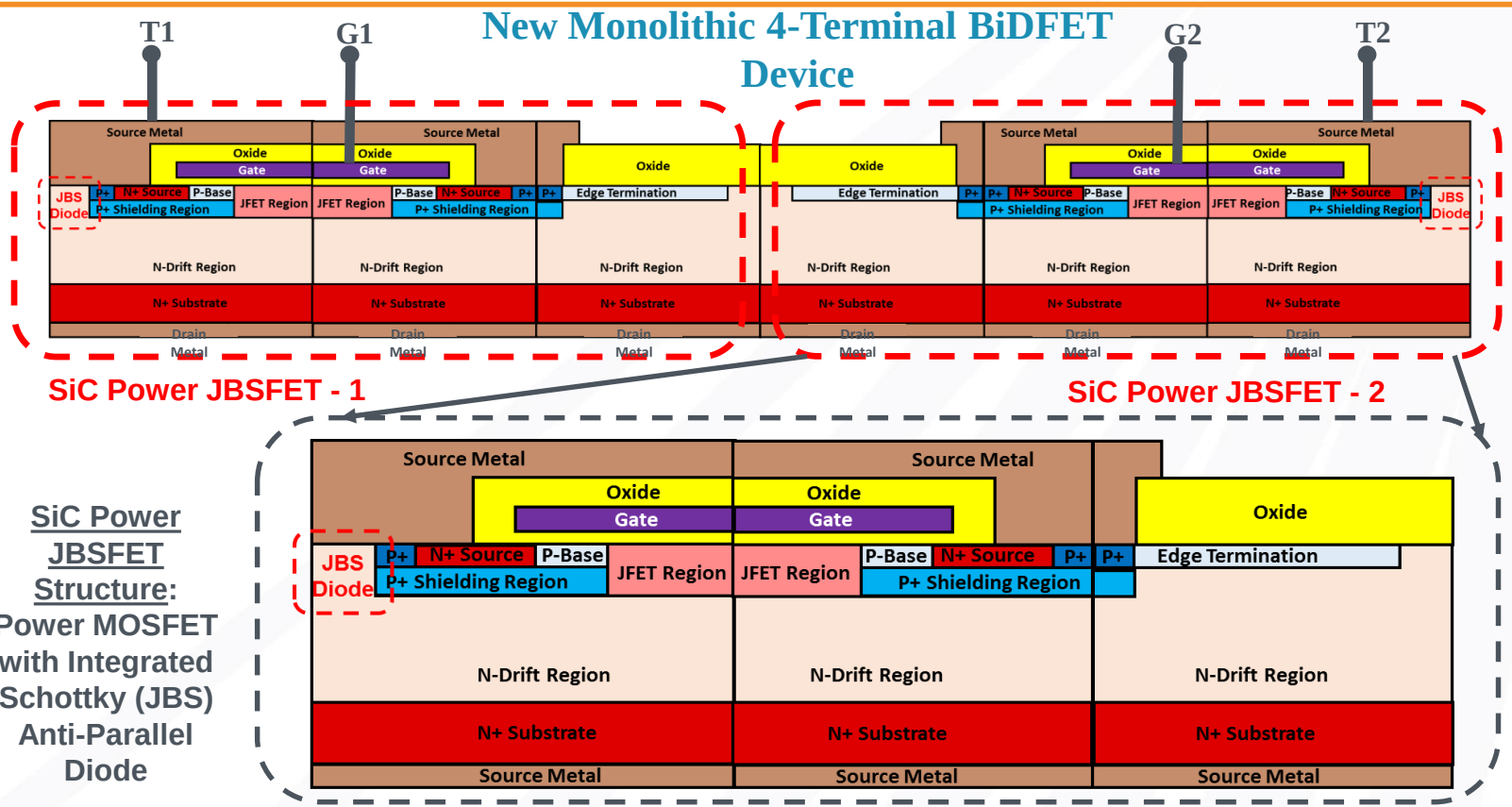
## PRESiCE: PRocess Engineered for manufacturing SiC Electronic-devices

- NCSU Process has been established at a high volume 6 inch wafer foundry (X-Fab, TX)
- Multiple lots have been run and process control demonstrated with wafer maps and statistical distributions



# Proposed SiC Bi-Directional FET – BiDFET (or 4QPS)



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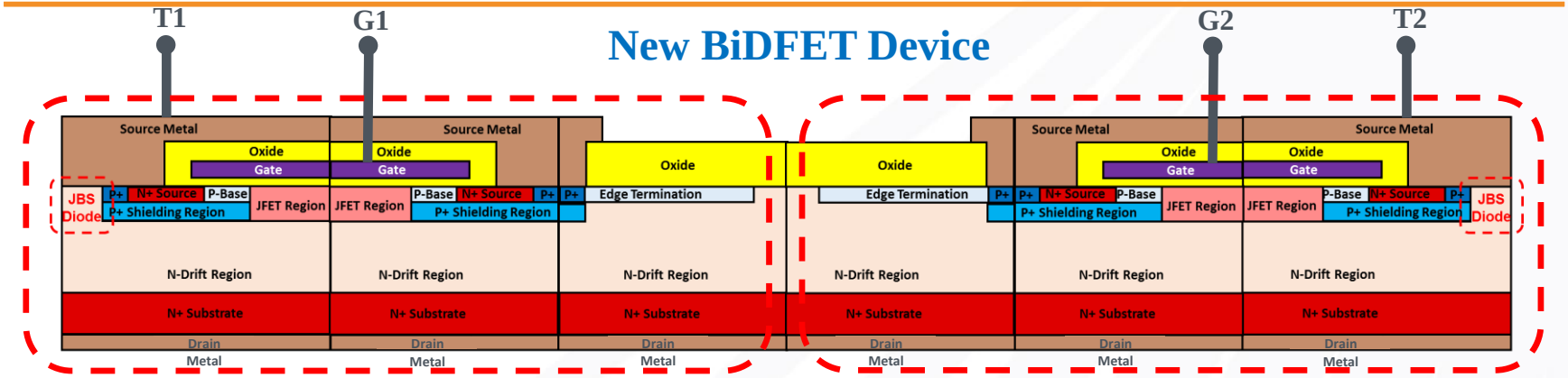
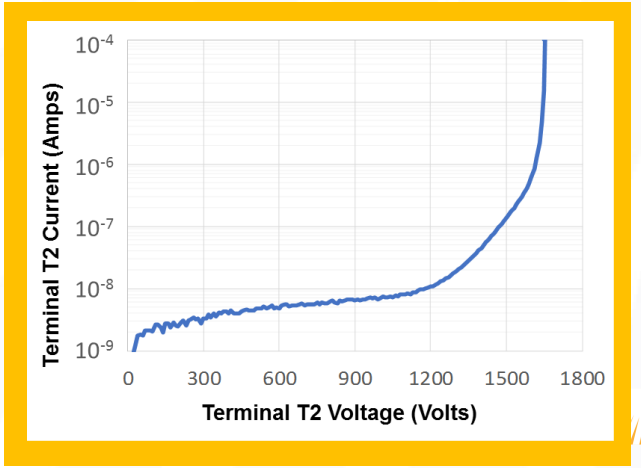



## Operation in First Quadrant

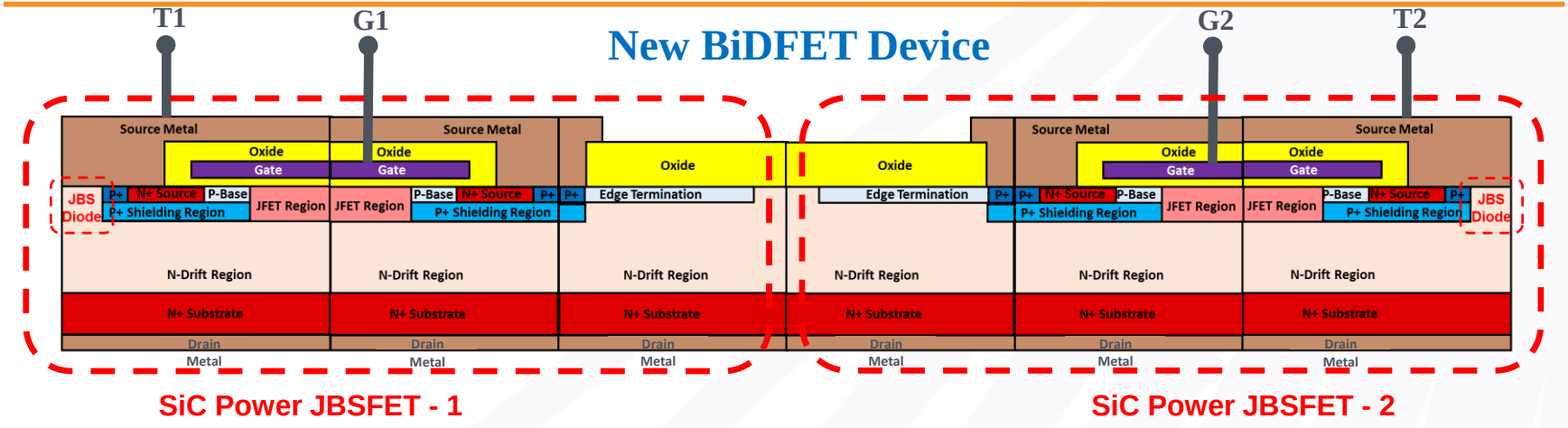
- T1 is Reference Electrode for BiDFET
- Positive bias on Electrode T2
- JBSFET-1 Blocks Voltage if V(G1-T1) = 0
- Blocking Voltage = 1650 V
- Low leakage current in spite of Schottky Contact

W. Sung and B.J. Baliga, "Monolithically Integrated 4H-SiC MOSFET and JBS Diode (JBSFET) using a Single Ohmic/Schottky Process Scheme" IEEE Electron Device Letters, Vol. 37, No. 7, pp. 1605-1608, Oct. 2016



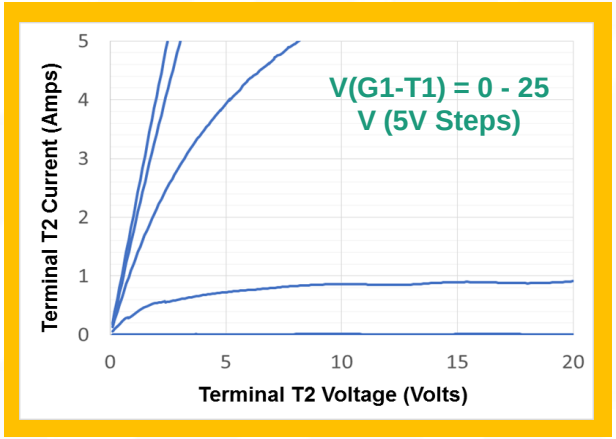

Similar Characteristics in Third Quadrant

# Proposed SiC Bi-Directional FET – BiDFET (or 4QPS)




## Operation in First Quadrant

- T1 is Reference Electrode for BiDFET
- Positive bias on Electrode T2
- Gate Bias for JBSFET-2: V(G2-T2) = 25 V
- Current flows through channel within JBSFET-2
- Gate Bias for JBSFET-1 Varied (5 V steps to 25 V)
- On-state Resistance = 0.5 Ω – Can be reduced with larger active area.
- Current Saturation with good Safe-Operating-Area

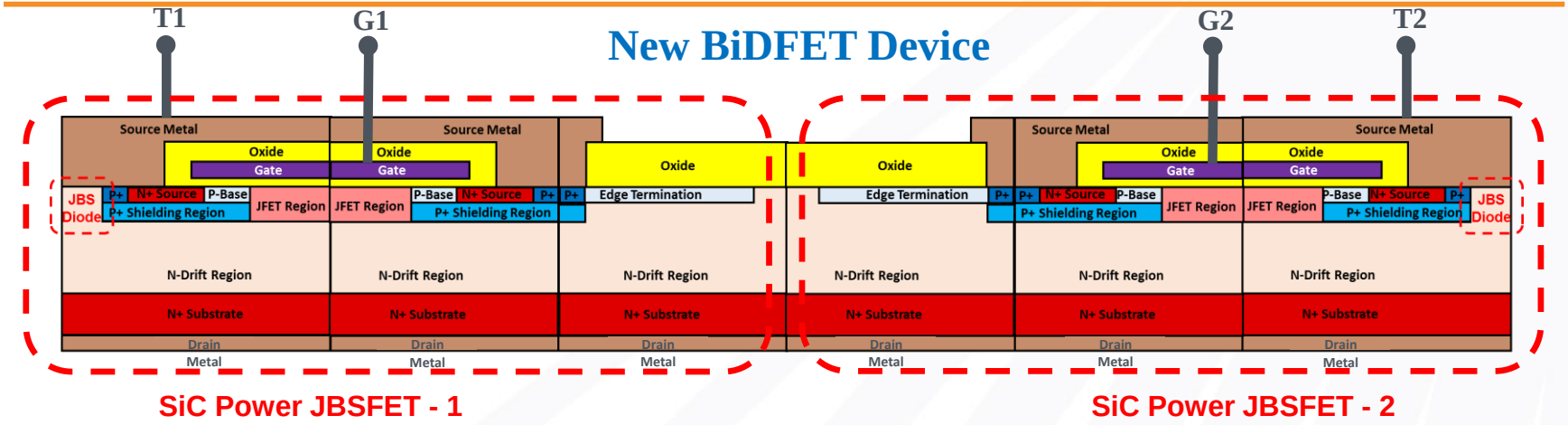



Similar Characteristics in Third Quadrant

**Ron = 0.5 Ω**

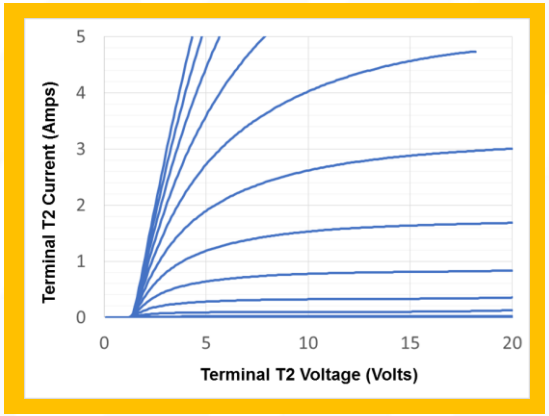
**Small Devices**

# Proposed SiC Bi-Directional FET – BiDFET (or 4QPS)




## Operation in First Quadrant

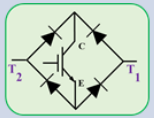
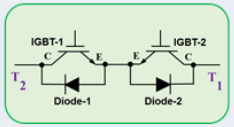
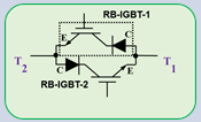
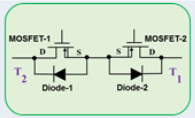
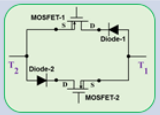
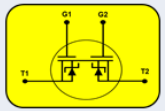
- T1 is Reference Electrode for BiDFET
- Positive bias on Electrode T2
- Gate Bias for JBSFET-2: V(G2-T2) = 0 V
- Current flows through JBS Diode within JBSFET-2
- Gate Bias for JBSFET-1 Varied (2 V steps to 26 V)
- Knee is observed at 1.5 V in output characteristics.
- Current Saturation with good Safe-Operating-Area




**Similar Characteristics in Third Quadrant**

V(G1-T1) = 0 - 26 V
(2V Steps)

# BiDFET Comparison with Alternative Device Options

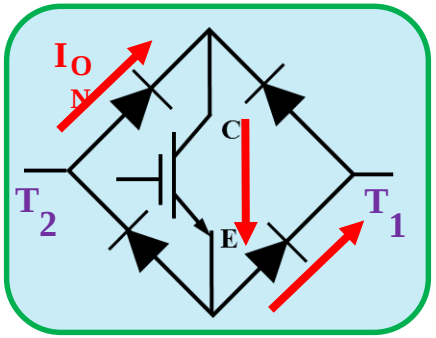
| AC Switch Option | | | Number of Devices & Packages per Leg | On-State Voltage Drop |
|---|---|---|---|---|
|  | Si Devices | Case (a) | 5 | 3.5 V |
|  | Si Devices | Case (b) | 4 | 2.5 V |
|  | Si Devices | Case (c) | 2 | 2.0 V |
|  | SiC Devices | Case (d) | 4 | 1.25 V |
|  | SiC Devices | Case (e) | 4 | 1.25 V |
|  | SiC BiDFET | | 1 | 0.5 V |

- **Assumptions:**
- Si Diode On-State Voltage Drop = 1.0 V
- Si Asymmetric IGBT On-State Voltage Drop = 1.5 V
- Si Symmetric (RB) IGBT On-State Voltage Drop = 2.0 V
- SiC Diode On-State Voltage Drop = 1.0 V
- SiC MOSFET On-State Voltage Drop = 0.25 V

**Scale up device area in Proposed Project**

# Bi-Directional Switches – Previously Proposed

Case (a)




P.W. Wheeler, J. Rodriguez, J.C. Clare, L. Empringham, and A. Weinstein,

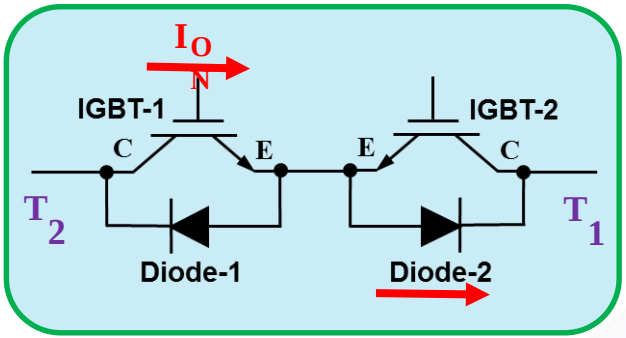
"Matrix Converters: A Technology Review",

*IEEE Trans. Industrial Electronics*, vol. 49, no. 2, pp. 276–288, April 2002.

- **Si Diode Bridge with Asymmetric blocking Si IGBT**
- 5 Discrete Components
- 5 Packages – Cost and Space
- On-State voltage drop = 3.5 V
  - two Si diode voltage drops (~ 2 V) plus the Asymmetric Si IGBT voltage drop (~ 1.5 V)
- High switching losses of the Si IGBT
- Level-Shift of Gate Voltage required

# Bi-Directional Switches – Previously Proposed

Case (b)




K. Tazume, T. Aoki, and T. Yamashita,

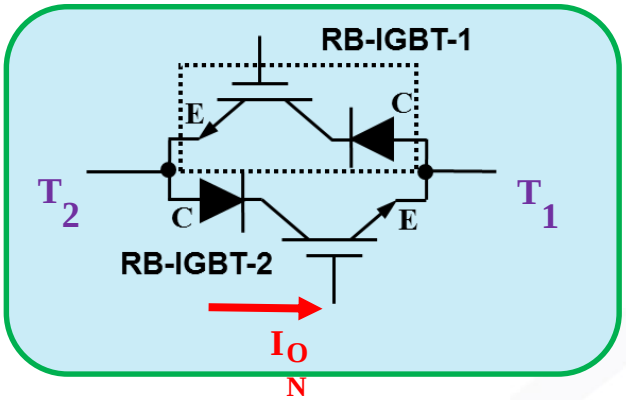
"Novel Method for Controlling a High-Frequency Link Inverter using Cycloconverter Techniques,"

IEEE Power Electronics Specialists Conf., pp. 497–502, May 1998

- **Series Emitter-connected Asymmetric blocking IGBTs with Fly-back diodes**
- 4 Discrete Components
- 4 Packages – Cost and Space
- On-State voltage drop = 2.5 V
  - one Si diode voltage drop (~ 1 V) plus the Asymmetric Si IGBT voltage drop (~ 1.5 V)
- High switching losses of the Si IGBT
- Level-Shift of Gate Voltage required

# Bi-Directional Switches – Previously Proposed

Case (c)

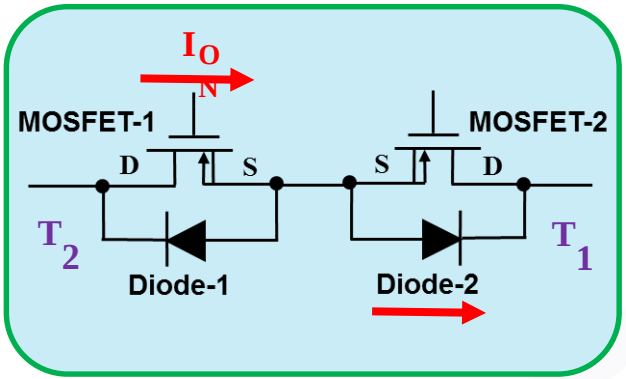



M. Takei, T. Naito, and K. Ueno, "Reverse Blocking IGBT for Matrix Converter with Ultra-Thin Wafer Technology," IEE Proc. Circuits, Devices, Systems, Vol. 151, pp. 243–247, June 2004.

- **Back-to-back Reverse blocking Si IGBTs**
- 2 Discrete Components
- 2 Packages
- On-State voltage drop = 2.0 V
  - High voltage drop of Reverse Blocking Si IGBT
- High switching losses of Reverse Blocking Si IGBT
- Level-Shift of Gate Voltage required

# Bi-Directional Switches – Previously Proposed

Case (d)




S. Safari, A. Castellazzi, and P. Wheeler,

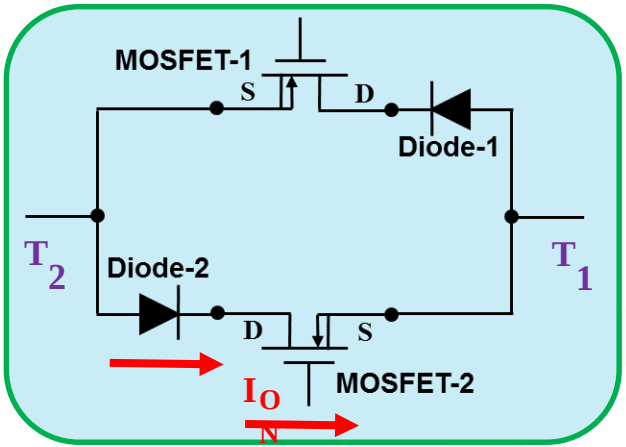
"Experimental and Analytical Performance Evaluation of SiC Power Devices in the Matrix Converter,"

IEEE Trans. Power Electronics, Vol. 29, pp.2584–2596, May 2014

- **Series Source-connected SiC power MOSFETs with Anti-Parallel Diodes**
- 4 Discrete Components
- 4 Packages – Cost and Space
- On-State voltage drop = 1.25 V
  - one SiC diode voltage drop (~ 1 V) plus SiC MOSFET voltage drop (~ 0.25 V)
- Low switching losses of SiC MOSFET
- No Level-Shift of Gate Voltage required

# Bi-Directional Switches – Previously Proposed

Case (e)



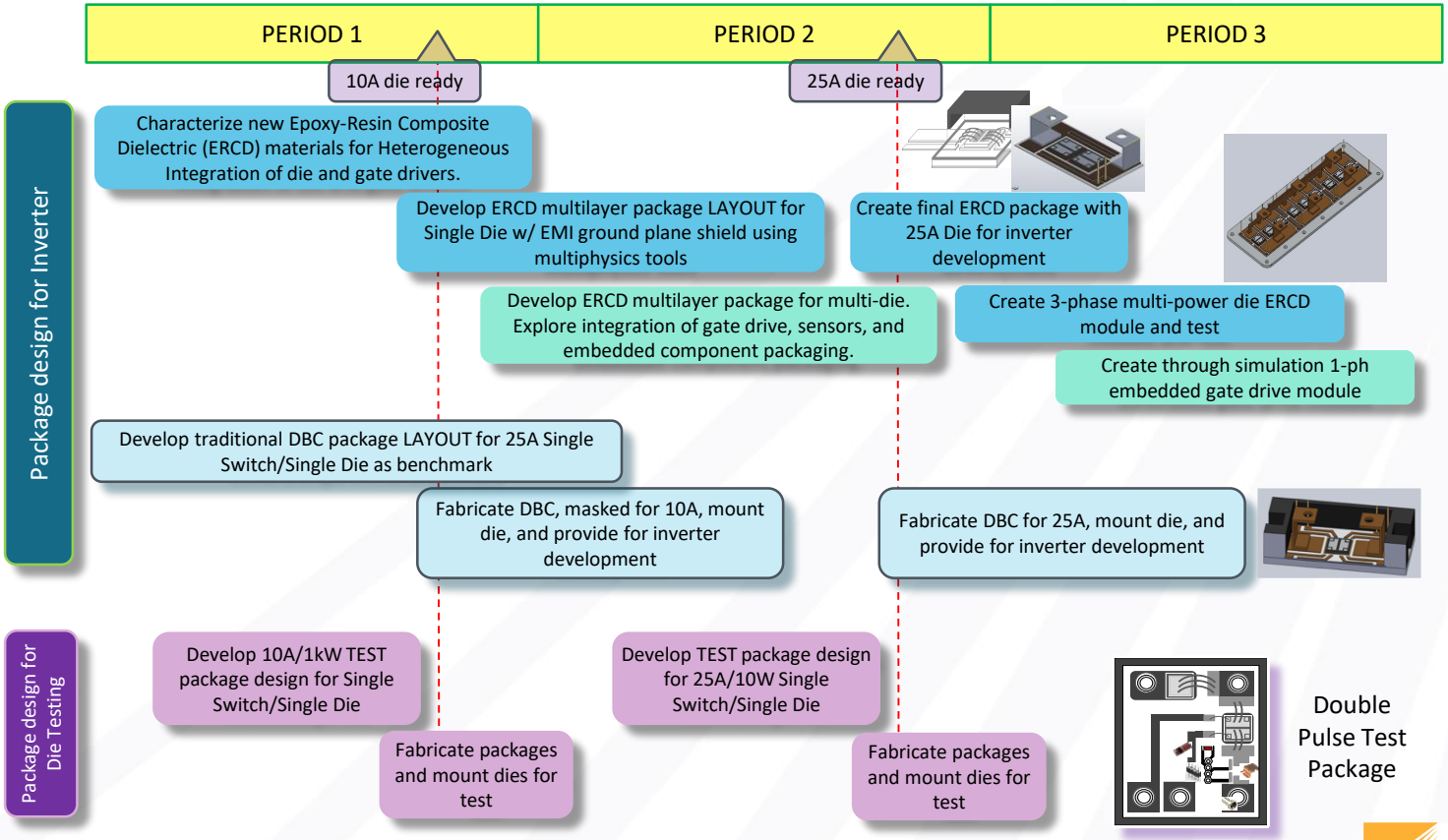

H.F. Ahmed, H. Cha, A.A. Khan, J. Kim, and J. Cho,

"A Single-Phase Buck-Boost Matrix Converter with only Six Switches and without Commutation Problem,"

IEEE Trans. Power Electronics, Vol. 32, pp.1232–1244, February 2017

- **Back-to-back SiC Power MOSFETs with Series Reverse blocking Diodes**
- 4 Discrete Components
- 4 Packages – Cost and Space
- On-State voltage drop = 1.25 V
  - one SiC diode voltage drop (~ 1 V) plus SiC MOSFET voltage drop (~ 0.25 V)
- Low switching losses of SiC MOSFET
- Level-Shift of Gate Voltage required

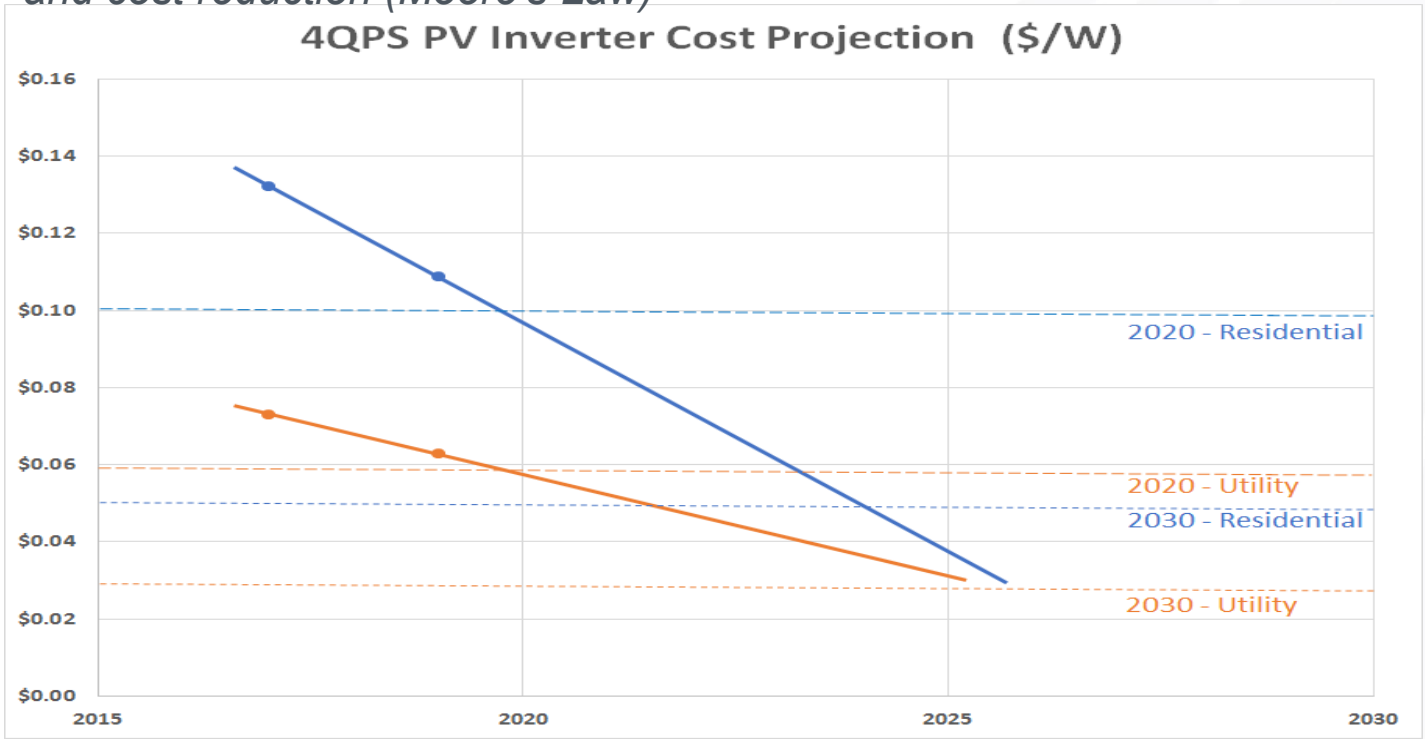
# Advanced Packaging Timeline




Two types of packaging needed:
(1) Advanced Packaging for Inverters
(2) Packaging for new-device test

# Extrapolated Cost Projection

*Meet and exceed DOE Targets – potential for further with technology improvements and cost reduction (Moore's Law)*



# Potential Impact of the Proposed Technology

- Highly compact, high efficiency, cost-effective solar PV inverter with safe failure modes.
- BiDFET (or 4-QPS) enables new power converter topologies – such as cyclo-converters and “buck” converter topologies with inherent short circuit and current protection
- BiDFET (or 4-QPS) enables new grid connected power converter (SST) for renewable energy integration which require a “buck” function with desirable short circuit and current protection
- Higher reliability and redundancy in conventional grid tied solar PV inverter – due to elimination of DC electrolytic capacitors.
- Key Technical challenges: Control and Commutation challenges exist in Cyclo-converter based circuits (employ ZVS and ZCS since “series” diode commutation implies ZVS, ZCS switch turn-off

# Advanced Package Development for Heterogenously Integrated Power (HiP)

New tech is in AI & IoT, which require Heterogeneous Integration at the Package Level, i.e. System in Package (SiP)

PREES has been working with RISHO KOGYO CO., LTD. as a development partner in applying new high-thermal conductivity (10W/mK), Epoxy-Resin Composite Dielectric (ERCD) based laminates to power packaging.

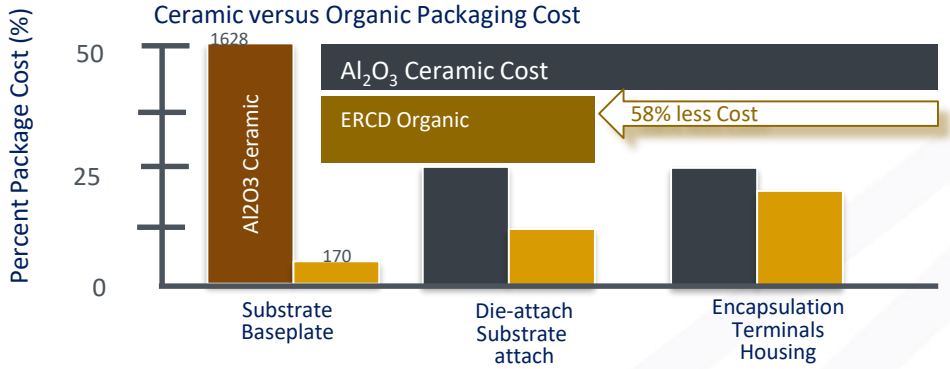
- The laminates have high BV (>5.5kV/100µm), operate at >250˚C, have low modulus for high reliability, and can be layered to embed components.

The new laminate approach brings Heterogeneous Integration to power packaging and develops new fundamental concepts for others to develop highly integrated power electronic systems.

The proposed work has three thrusts:

- Use of traditional packaging development to support low-risk 4-QPS device testing and inverter development
- Use of advanced packaging to develop Novel 4-QPS SiPs for PV inverter applications by creating multilayer EMI shielding in Single-Chip, and Multi-Chip (3-ph) Modules
- Developing ground rules through the characterization of materials and processes, and multi-physics modeling for embedding sensors and gate drives, i.e. Heterogeneously Integrated Power (HiP). [Physical demonstration of HiP is beyond scope and funding.]

# Enabling Low Cost and Safety




Enabling Low-Cost Power Modules

Substrate and baseplate account for *half of the packaging material* cost. Therefore, the choice of technology in ceramic substrates or baseplates can have a great impact on final power module cost. Approximately, 25% of the cost is related to die-attach or substrate attach material. Rest of the cost is divided between encapsulation, terminals and housing.

*Power Module Packaging: Material Market and Technology Trends 2017* ,Yole Development

EMI and Safety are primary factors in future Power Modules.

- Multilayer structures possible with organic substrates (ERCD) allow embedded ground planes to limit ground currents, i.e. conducted EMI and fault / trip conditions, in the PV system.
  - Versatility of organic laminates will enable many new packaging structures once fundamentally characterized for power electronics applications
- Thin structures, needed for high thermal conductance, can challenge 480V system level IEC and UL safety standards (e.g. insulation level, partial discharge, etc.). New ERCD materials have a higher voltage capability: DBC ceramic has 20kV/mm vs ERCD 55kV/mm
  - High PD resistance reduces aging, and enables denser multi-level packaging further enabling higher HI levels of components, sensors, and subsystems.

# Advanced Package Development for Heterogenously Integrated Power (HiP)

Well Accepted – To continue on the path of Moore's Law, the electronics industry is aggressively moving to "Heterogenous Integration" (HI) of components, sensors, and subsystems into package (SiP)

- To have Power Electronic Systems partake in the 'next electronics revolution;', power electronics packaging cannot continue with ceramic-based systems
- New Organic Materials, e.g. Epoxy-Resin Composite Dielectrics, can meet or exceed all requirements of power packaging, except thermal conductance of AlN & BeO.
  - → $250^0$C continuous operation
  - → Equal capability for hierarchal soldering of sintering attachment of die
  - → Direct attachment of Cu-clad dielectric to Al and Cu baseplates (not possible with cer.)
  - → Higher reliability at the Cu/insulator interface due to lower modulus
  - → 10W/mK that exceeds thermal conductance of $Al_2O_3$ for thicknesses of 80-120µm
  - → Breakdown/aging voltage > 5.5kV/100µm (measured), versus 2kV/100µm
  - → Multi-layering, embedding of components, sensors and die (not possible with cer.)

*This work develops fundamental characterizations and simple demonstration of ERCD power packaging, and directly supports new developments in HI*

# Capabilites – PREES Lab

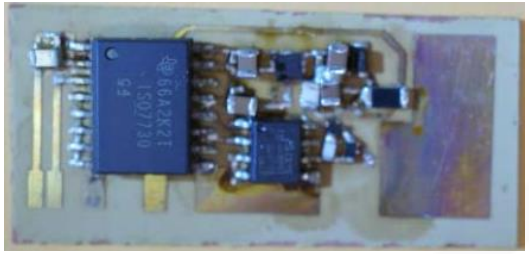
## Epoxy-Resin Composite Dielectric (ERCD) Material

Laminate thickness is down to 80µm giving a thermal conductance is 3X greater than DBC Alumina, or allowing 3X higher power dissipation (10W/mK)

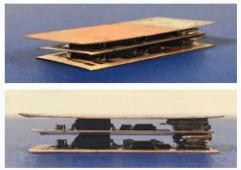
As an organic, the low modulus provides >10X reliability over ceramic-DBC

Most important – cost is 10X lower

| Parts | Thick-ness (µm) | Thermal Conductivity W/m·K | Unit Thermal Resistance $m^2 \cdot ^oC/W$ | Cost Estimation $ / $m^2$ |
|---|---|---|---|---|
| ERCD | 80 | 8 | $1 \times 10^{-5}$ | 170 |
| $Al_2O_3$ | 254 | 23 | $1.104 \times 10^{-5}$ | 1628 |
| AlN | 254 | 170 | $1.49 \times 10^{-6}$ | 5892 |



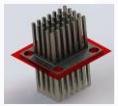
Gate driver circuits together with isolator and LDO on ERCD

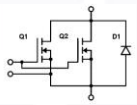


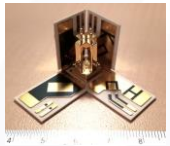
Stacked two-layer half bridge module on ERCD

Laboratory for Packaging Research in Electronic Energy Systems (PREES)

PREES CERAMIC MODULES







# Q & A