Directions in Power Electronics for Photovoltaics

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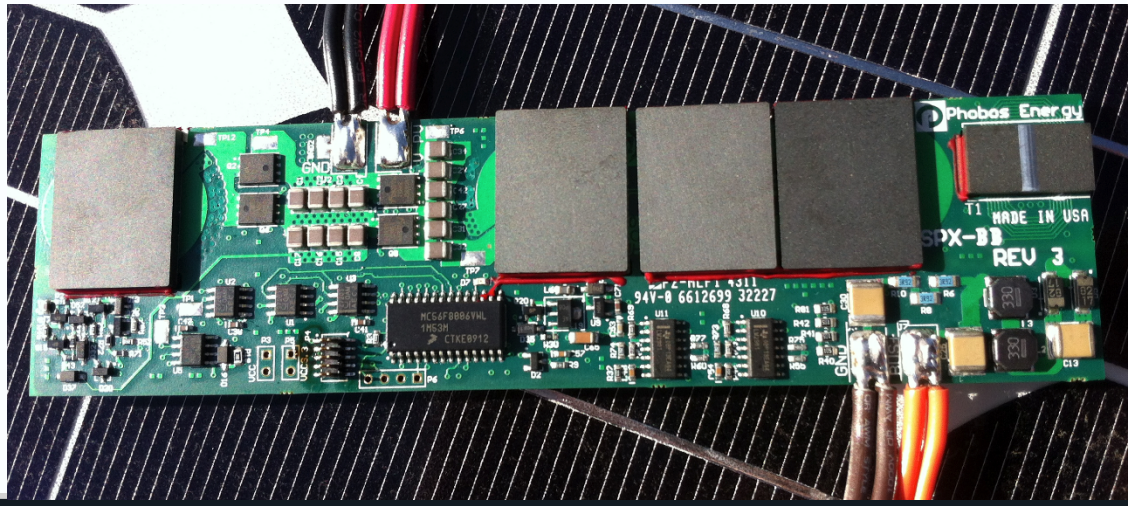


“String” Inverters

- Small size and weight leads to simple installation, low BOS cost
- 1000+ VDC input, three-phase AC output
- Opportunities to increase power and voltage without increasing size and weight?
- Opportunities to reduce BOS cost and reduce inverter $/W
- Improved PV inverter technologies through WBG power semiconductors and inverter circuit architectures

Advancing power converter technology

With new wide bandgap power semiconductor device technologies, there are new opportunities for disruptive and transformative advances in power electronics.

Areas ripe for focus include:

- Converter circuit topologies and architectures
- Resonant and soft switching techniques
- Control techniques
- System architectures and system design
- Enabling complex power circuits and their performance improvements via recent advances in packaging and interconnect technologies

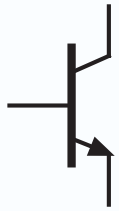
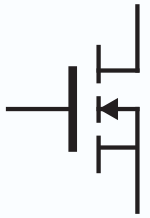
New approaches that combine advances in multiple sources are more likely to lead to transformative results

Brute-force replacement of Si devices with WBG devices offers limited improvement in converter metrics

Key metrics: cost, application-specific loss, size and weight.

Historical Disruptions in Power Semiconductors

Si BJT to Si MOSFET: 1980's, 10 V to 1000 V

Device		1980	1990
Si BJT		Dominant 20 kHz	Supplanted by MOSFET Still cheaper than MOSFET, but inferior system size and cost
Si MOSFET		Emerging Too expensive DC losses too large	Dominant 100 kHz Reductions in magnetics size and cost

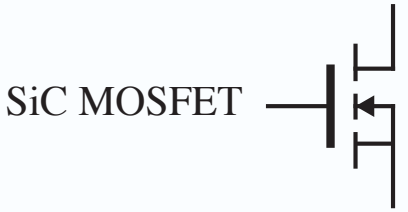
Why:

1. Reduced ac loss of MOSFETs allowed 5x increase of frequency
2. Availability of good ferrite materials at 100 kHz, so 5x reduction of magnetics size and/or loss

New applications became feasible, new circuit designs were developed, converter systems were optimized in different ways to take advantage

Next Disruption in Power Semiconductors

Si IGBT to SiC MOSFET: 600 V to 10 kV(?)

Device	Now	Ten years (?)
	Dominant 10 kHz	Supplanted by SiC MOSFET Still cheaper than SiC, but inferior system size and cost
	Emerging Too expensive DC losses too large	Dominant 100 kHz Reductions in magnetics size and cost

Why:

1. Reduced ac loss of MOSFETs allowed 5x increase of frequency
2. Availability of good ferrite materials at 100 kHz, so 5x reduction of magnetics size and/or loss

Feasibility of new applications, development of new circuit designs, optimization of converter systems in new ways to take advantage

Power Converter Metrics

Cost

- Generally measured in $/W
- For research projects, other related metrics may be more appropriate:
  - Total semiconductor area, mm^2/kW (Don't just count transistors)
  - Total magnetics core and copper volumes
  - Total capacitor energy or apparent power

Loss

- Efficiency h or $Q = P_{out}/P_{loss}$
  - Peak efficiency is not very meaningful
  - Weighted loss in realistic scenario: CEC efficiency
  - Worst-case maximum loss, or *Q* at rated output power

Size

- Volumetric power density, measured in W/in^3 or kW/L
- Gravimetric power density is measured in kW/kg
- Impact of size on BOS cost

Efficiency improvement: incremental or transformative?

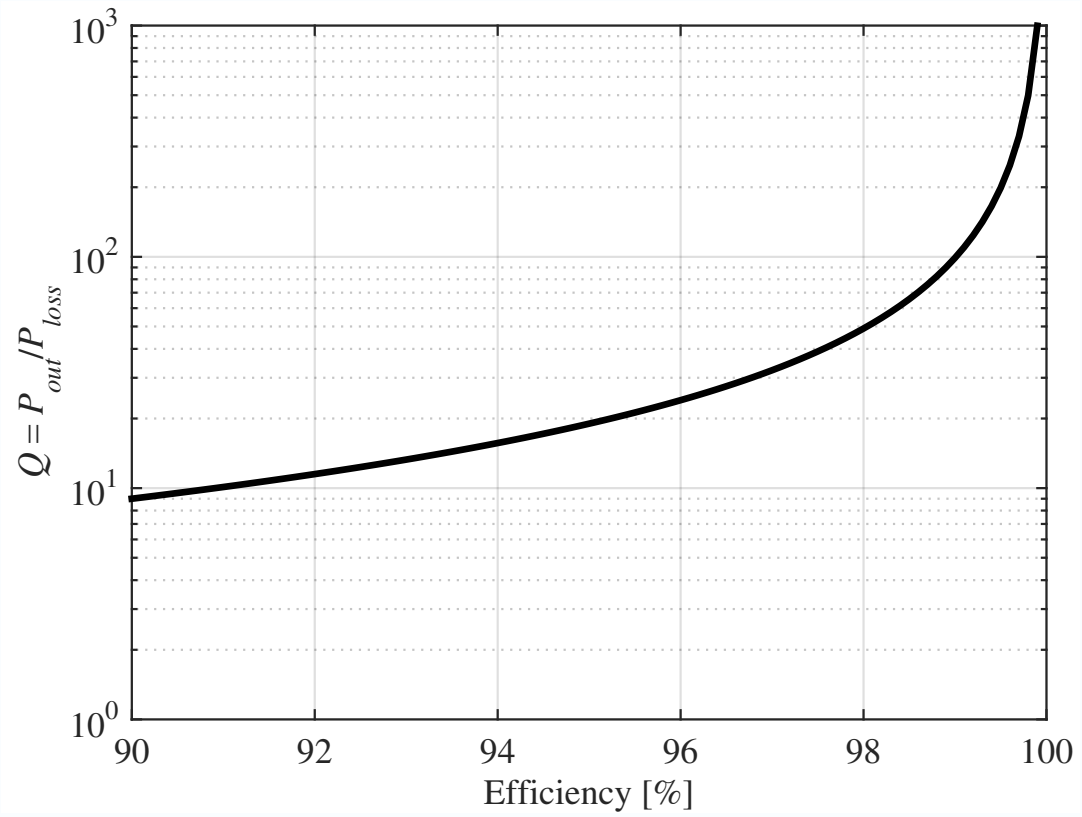
How significant is a 1% gain in efficiency?

$$\eta = \frac{P_{out}}{P_{in}}$$

$$P_{loss} = P_{in} - P_{out} = P_{out}\left(\frac{1}{\eta} - 1\right)$$

- P_{loss} determines size and weight of the inverter enclosure
- Converters generally are loss-limited, and technologies that can produce large output power while incurring small loss result in small size and low cost

$$Q = \frac{P_{out}}{P_{loss}} = \frac{\eta}{(1-\eta)}$$



For a given limited P_{loss}, increasing Q increases available output power, and hence also the specific cost ($/W)

Trends in Converter Circuit Topologies and Control

Complex converter topologies

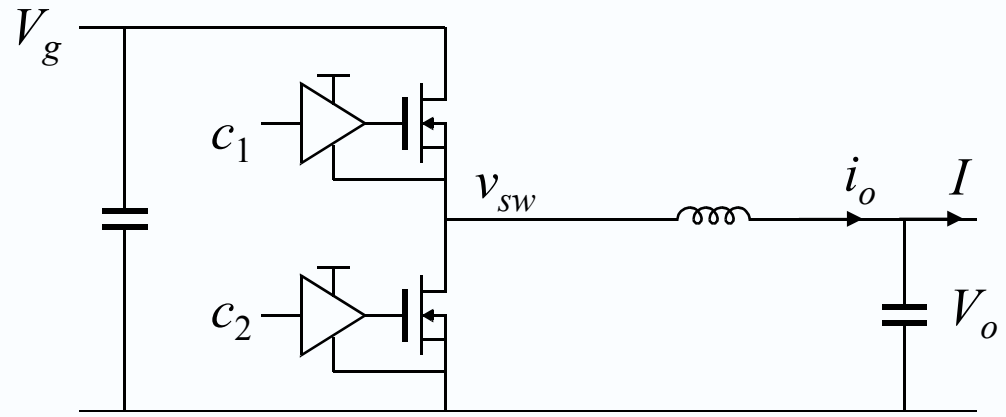
- Current scaling: multi-phase topologies
- Voltage scaling: multi-level topologies
- Modularity and multilevel modular converters
- Efficient indirect power processing: composite architectures that employ dissimilar modules

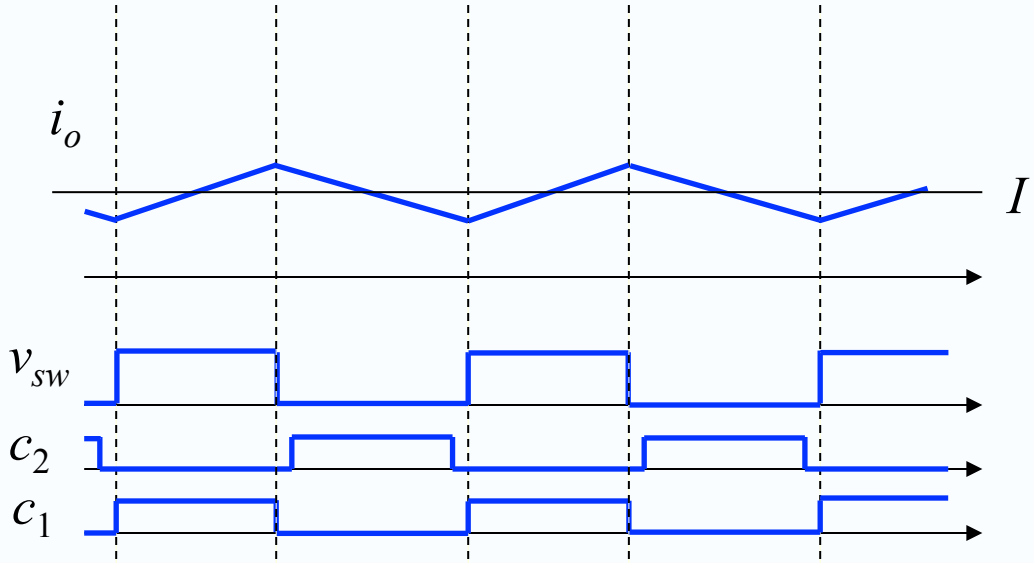
These approaches can lead to significant improvements in power density, efficiency, and performance

Enablers for complex converter architectures

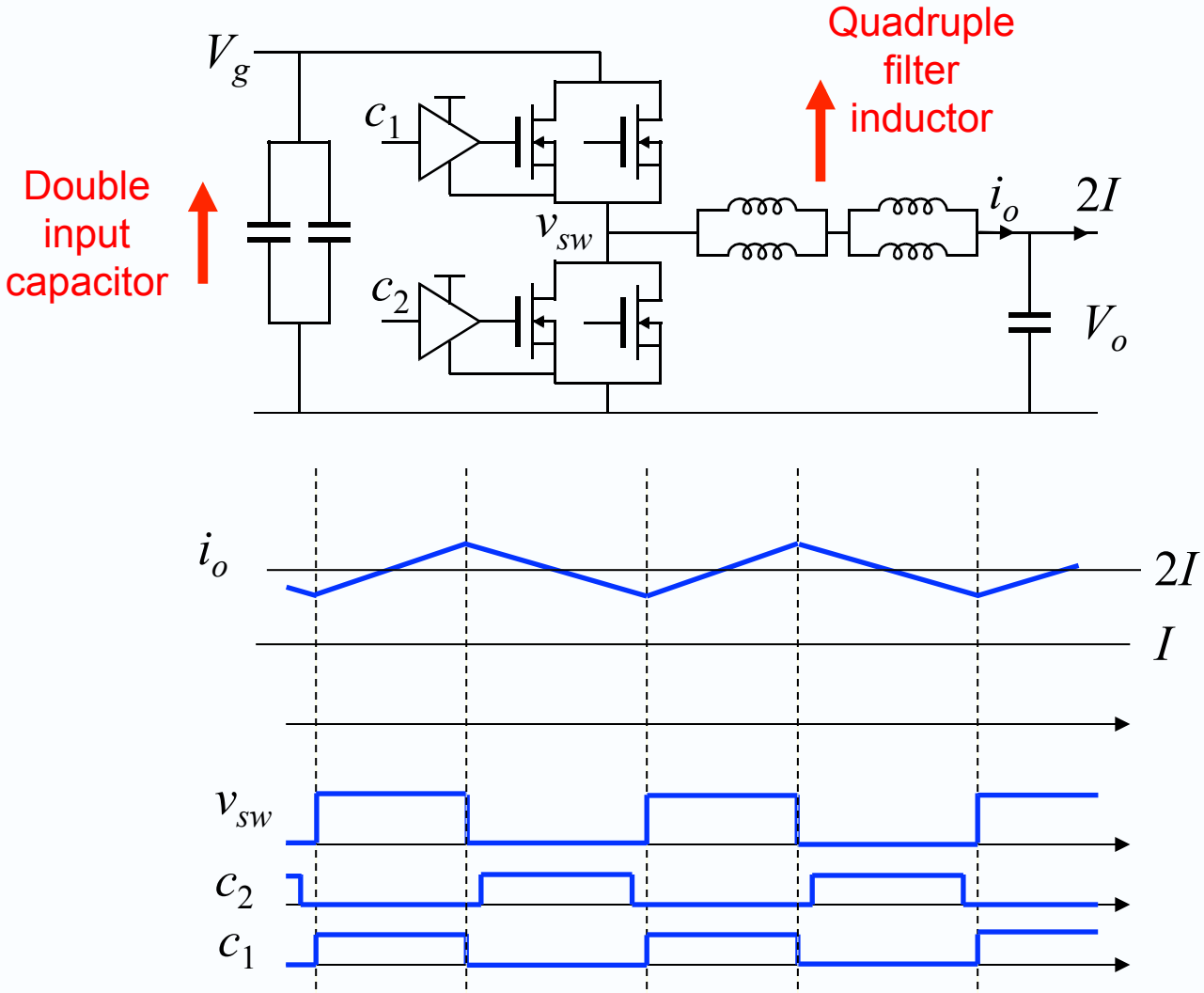
- Control techniques including autonomous module control and efficiency maximization via passthrough modes
- Packaging and complex interconnects

Goal: scale current by a factor of 2 in the basic half-bridge (buck or boost) module

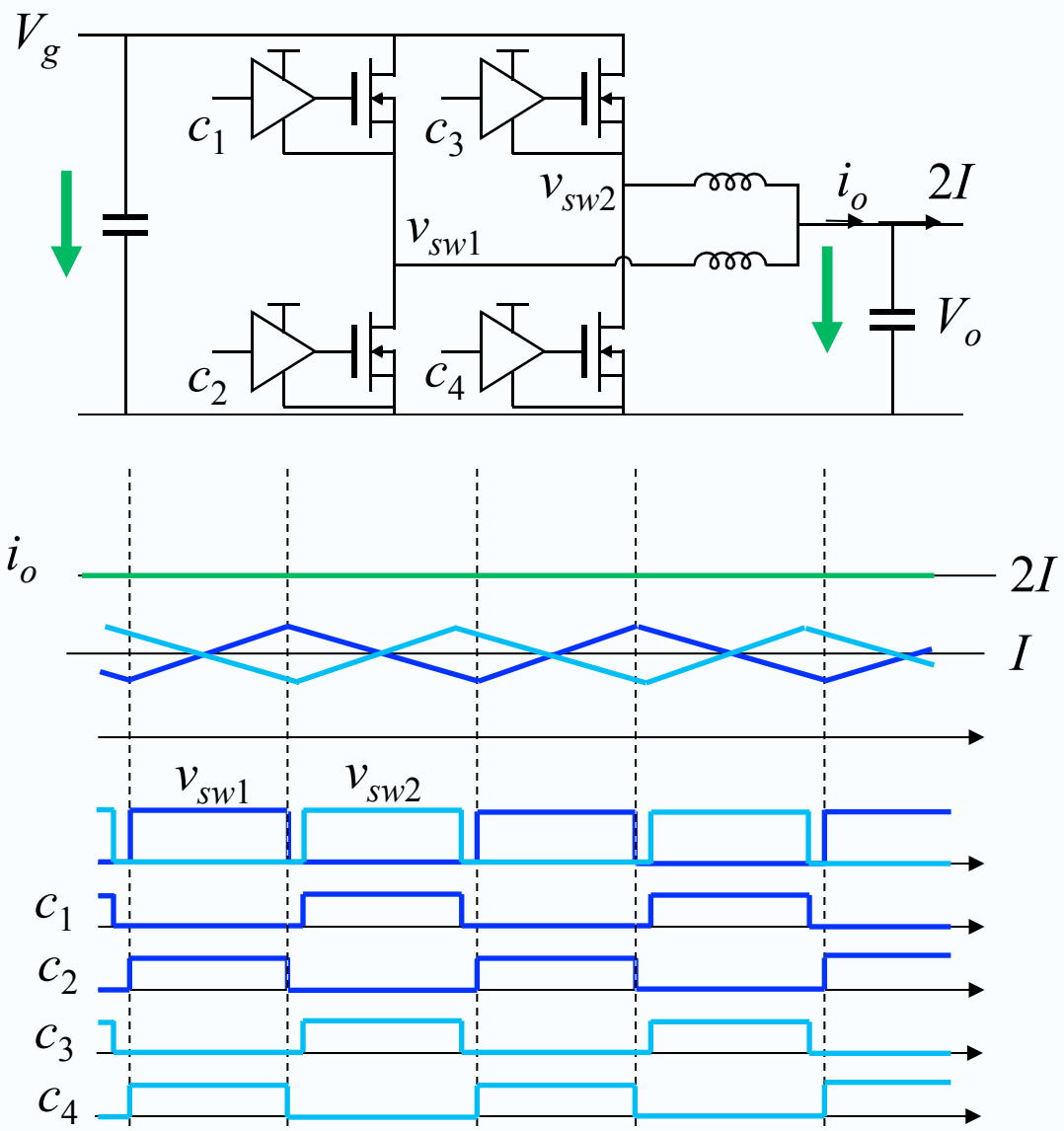




Approach 1: just double semiconductor device area

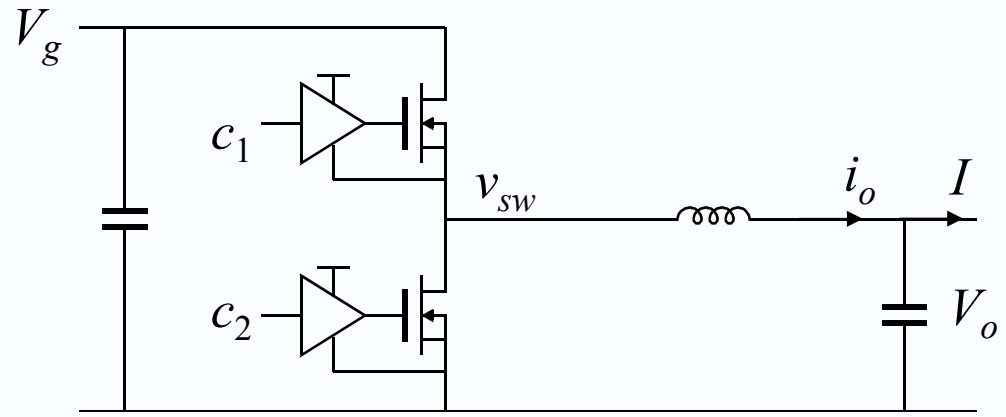


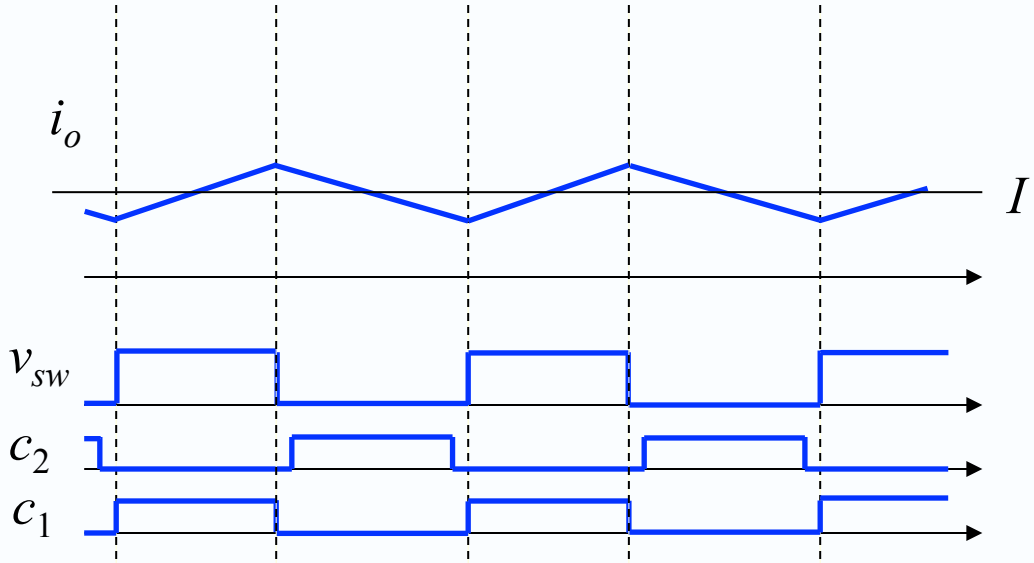
Approach 2: interleaved 2-phase converter



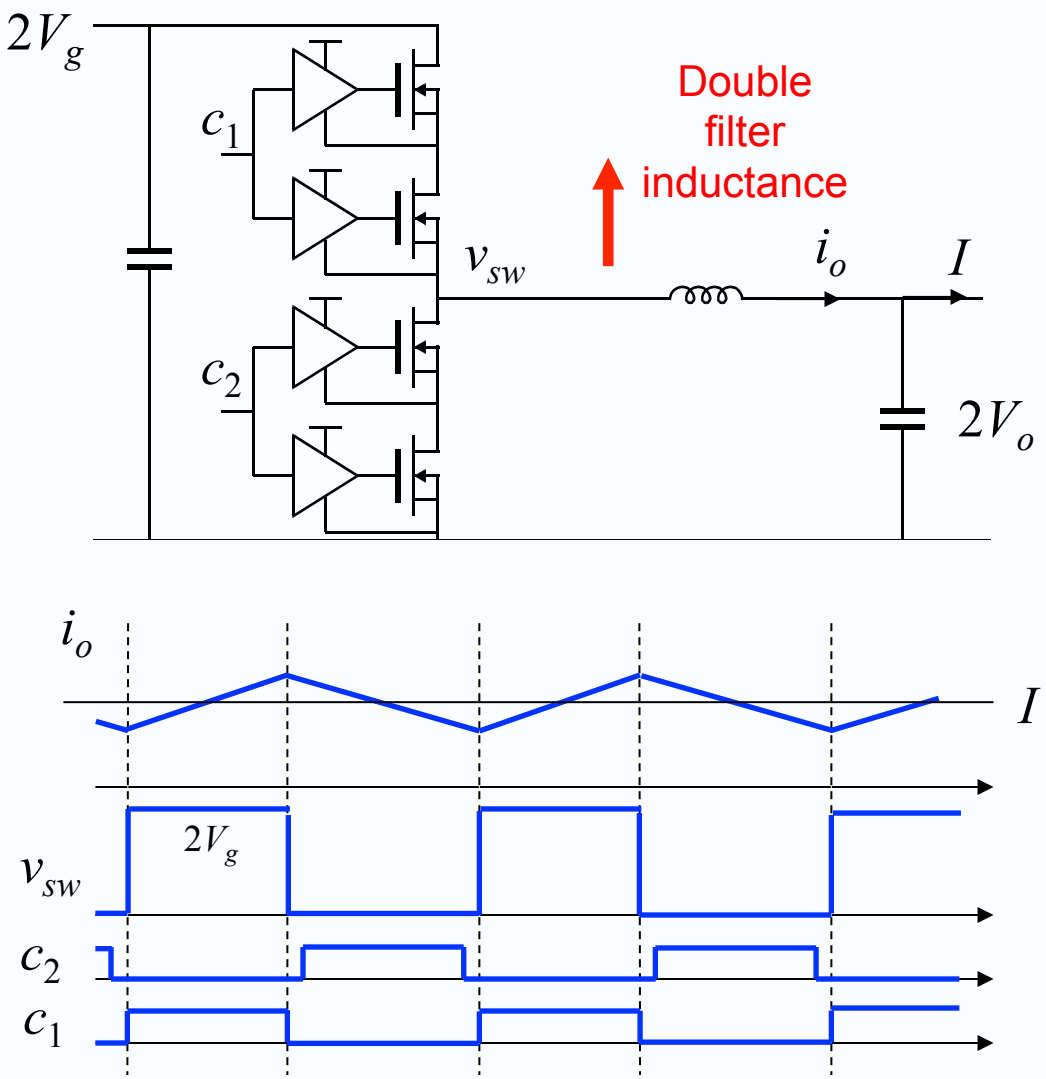
- Substantially reduced input and output ripples
- Same semiconductor area used more effectively
- Requires more complex control
- Requires more complex power interconnects

Goal: scale voltage by a factor of 2 in the basic half-bridge (buck or boost) module



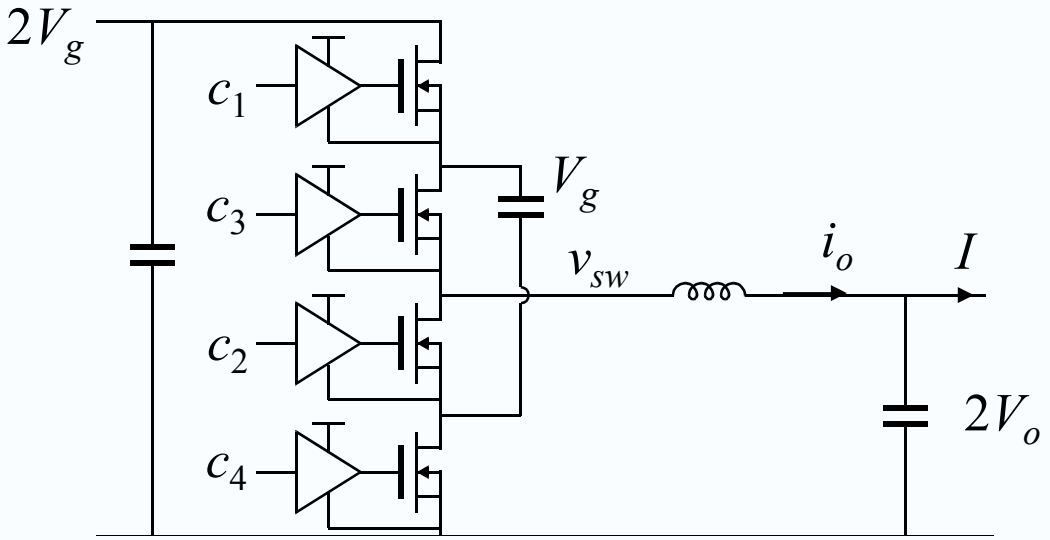


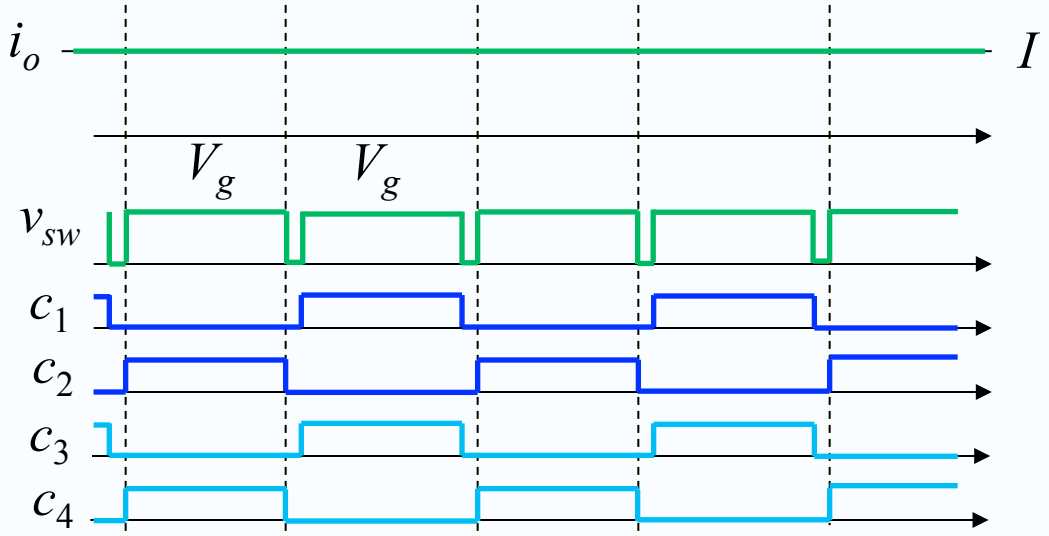
Approach 1: just stack devices in series



- Series stacking of devices is very difficult in practice
- Just replacing devices with 2x higher breakdown voltage is more practical, but requires larger semiconductor area

Approach 2: multi-level conversion

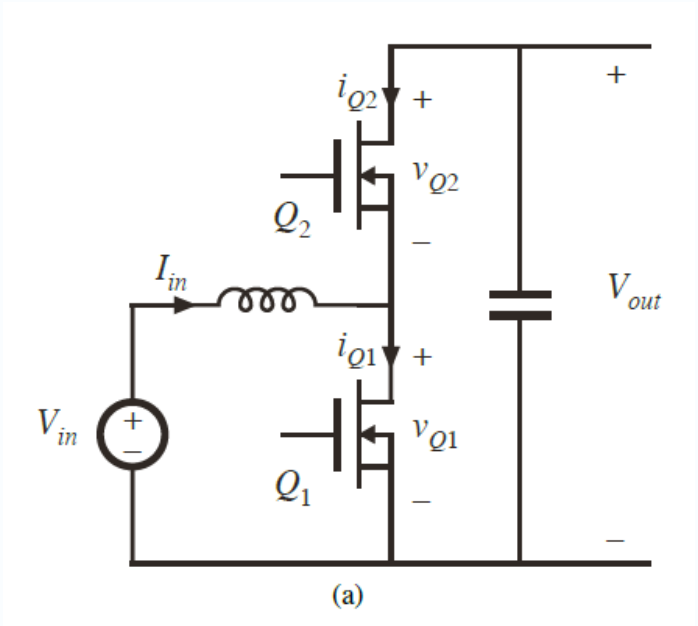


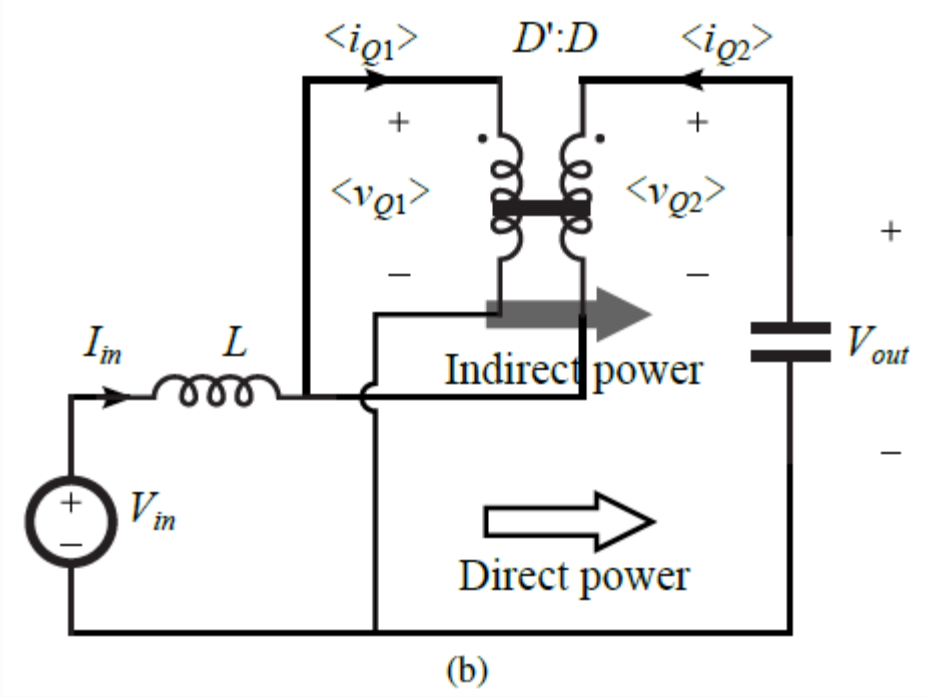


- The switched-node voltage has 3 possible levels: $2V_g$, V_g, and 0
- The switching-node voltage frequency equals 2fs
- Switches exposed to half voltage stress
- Much reduced filter inductance
- More complex interconnects, more complex control
- Numerous modular multi-level topologies have been investigated

Beyond multi-phase/multi-level modular topologies

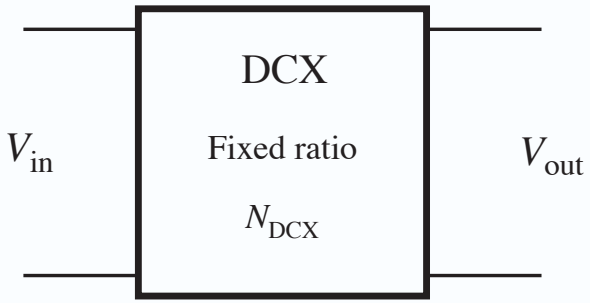
- Losses in power converters are associated with indirect power processing





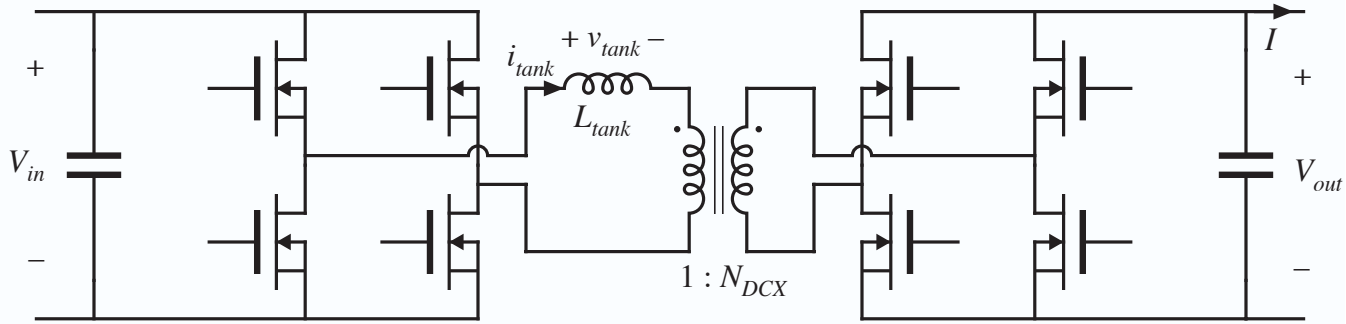
- Traditional converter topologies, such as boost do not process indirect power efficiently: switching devices are exposed to full voltage and current levels
- How can indirect power be processed more efficiently?

“DC Transformer” (DCX) concept

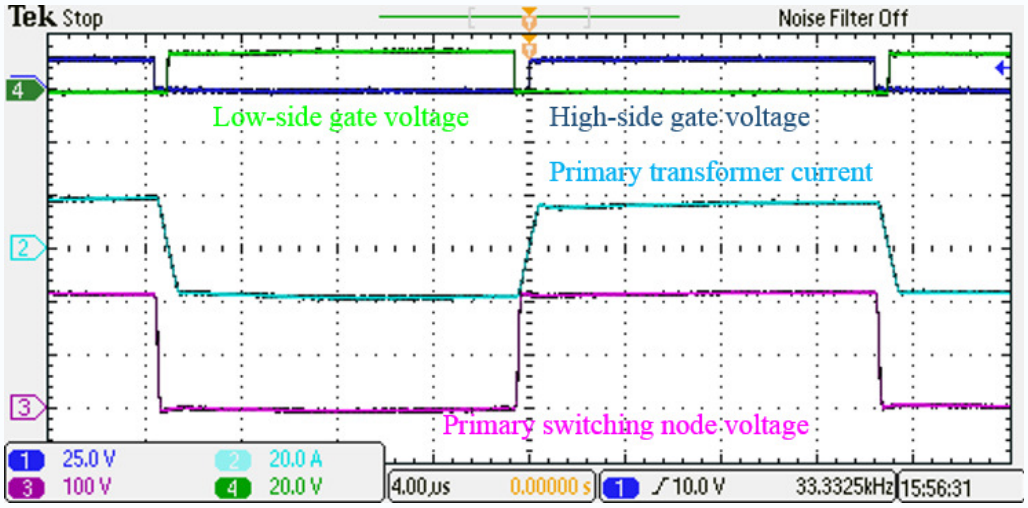


The ***DC Transformer*** (DCX): an isolated converter block that can change voltage by a fixed ratio, and process indirect power with very high efficiency

Example: ***Dual Active Bridge*** circuit: a DCX with bidirectional power flow. Efficiency is very high when optimized for fixed voltage ratio



- Low RMS currents
- Low switch current stresses
- Low input and output ripples
- Zero-voltage switching of all devices



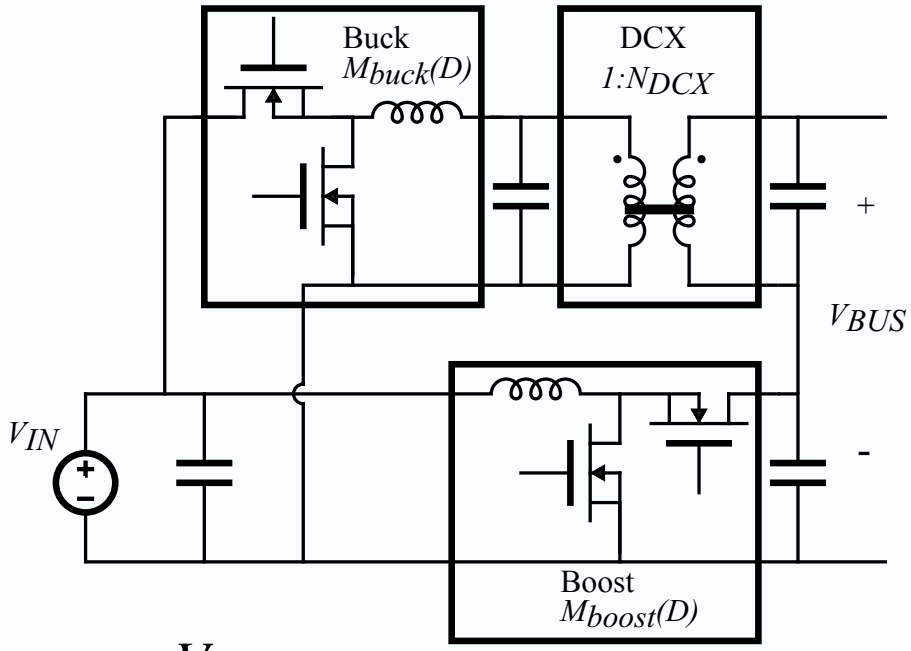
Beyond multi-phase/multi-level modular topologies

Concept:

- Use ultra-efficient DCX modules to process most of indirect power
- Combine *dissimilar* modules to achieve desired conversion characteristics and regulation capabilities

Example: Boost Composite Converter

Boost Composite Converter Architecture



$$M = \frac{V_{out}}{V_{in}} = M_{buck}N_{DCX} + M_{boost}$$

Dissimilar partial-power converter modules:

- Same total silicon area
- Total film capacitor size reduced by 3x
- Significantly lower loss at high boost ratios
- Significantly reduced partial-power loss

Dominant loss mechanisms are addressed:

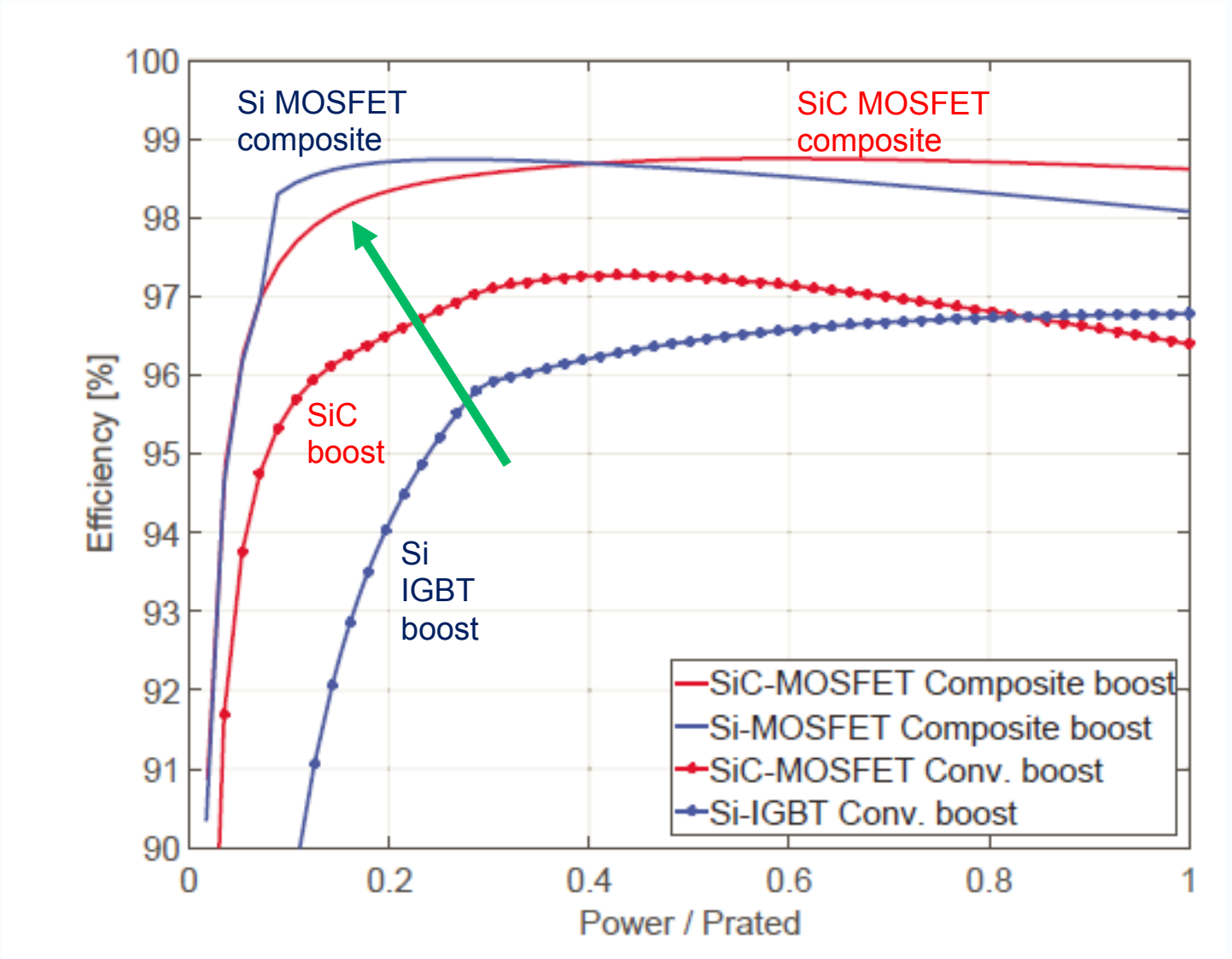
- Use of pass-through modes to minimize AC losses
- Use of ultra-high-efficiency DC Transformer (DCX) module to convert most of the indirect power

1. H. Chen, K. Sabi, H. Kim, T. Harada, R. Erickson, and D. Maksimovic, "A 98.7% Efficient Composite Converter Architecture with Application-Tailored Efficiency Characteristic," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 101-110, Jan. 2016.
2. H. Chen, H. Kim, R. Erickson and D. Maksimovic, "Electrified Automotive Powertrain Architecture Using Composite DC-DC Converters," *IEEE Transactions on Power Electronics*, 2016.

Effect of Converter Topology on Capacitor Size

- Capacitor size and cost generally is proportional to the applied AC rms current
- Capacitor rms current is independent of switching frequency
- Capacitor rms current depends on the converter circuit topology and the operating point
  - Operation of boost converter at high duty cycle leads to high capacitor rms current
  - Multilevel modular converter approaches increase capacitor requirements
  - Operation of boost or buck modules at near-passthrough points, or operation of DCX modules, leads to reduced capacitor requirements
- It is possible to significantly reduce total system capacitor requirements, through fundamentally sound improvements to converter topology

Efficiency comparison (250-to-650 V, 15 kW)



Summary of converter technologies: EV drivetrain boost example

Converter	Si-IGBT Conventional boost	Si-MOSFET Composite boost	SiC-MOSFET Conventional boost	SiC-MOSFET Composite boost
Switching frequency	10 kHz	20 kHz	240 kHz	240 kHz
CAFE efficiency	94.3 %	98.2 %	96.9 %	98.3 %
CAFE Q factor	22.2	55.3	34.7	58.6
Magnetic volume [mL]	343	372	136	82

- Brute-force device replacement in the conventional boost converter yields relatively small improvements in efficiency and converter *Q*, and no improvements in capacitor size
- **Composite architecture + SiC devices = transformative improvement**
  - Composite architecture addresses fundamental loss mechanisms
  - SiC enables increased switching frequency and much reduced magnetics size
  - In the composite architecture, SiC yields very high peak and average efficiency, much higher converter *Q*, and very high power density

Conclusions

New WBG semiconductor power devices can enable new opportunities for disruptive and transformative advances in power electronics, but new device technologies must be combined with advances in converter circuits and control. Areas ripe for focus include:

- Converter circuit topologies and architectures
- Control techniques
- System architectures and system design
- Enablement of more complex power circuits via interconnect and packaging

Brute-force replacement of Si devices with WBG devices offers limited improvement in converter metrics

Suggested ways to measure cost:

- Total semiconductor area, mm^2/kW (Don't just count transistors!)
- Total magnetics core and copper volumes
- Total capacitor energy or apparent power
- Effect of inverter size and weight on installation cost

Reduction of BOS (installation) cost via improved WBG+topologies:

- Maintain low size and weight of string inverters and increase P_{out}/P_{loss}
- Increased cost of WBG devices could be offset by reduced magnetics cost and reduced installation cost