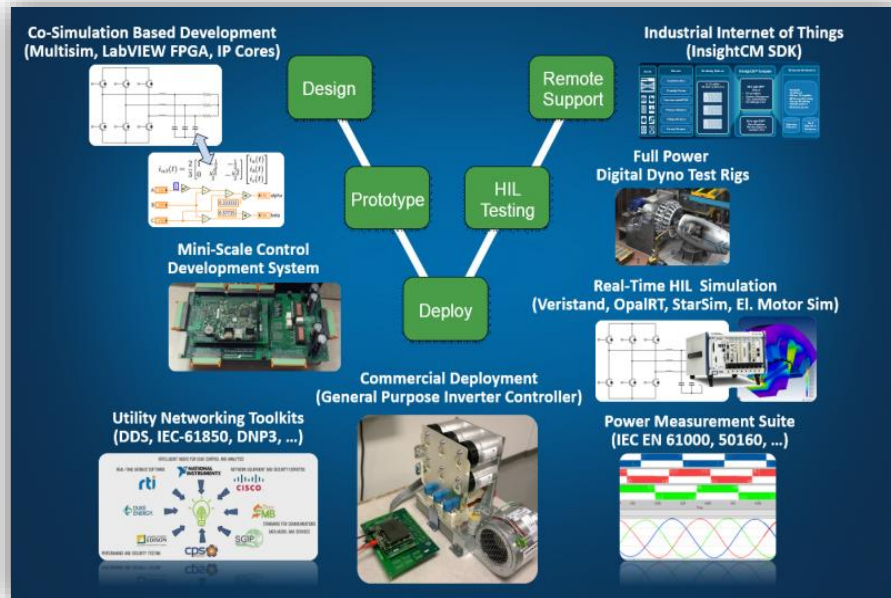
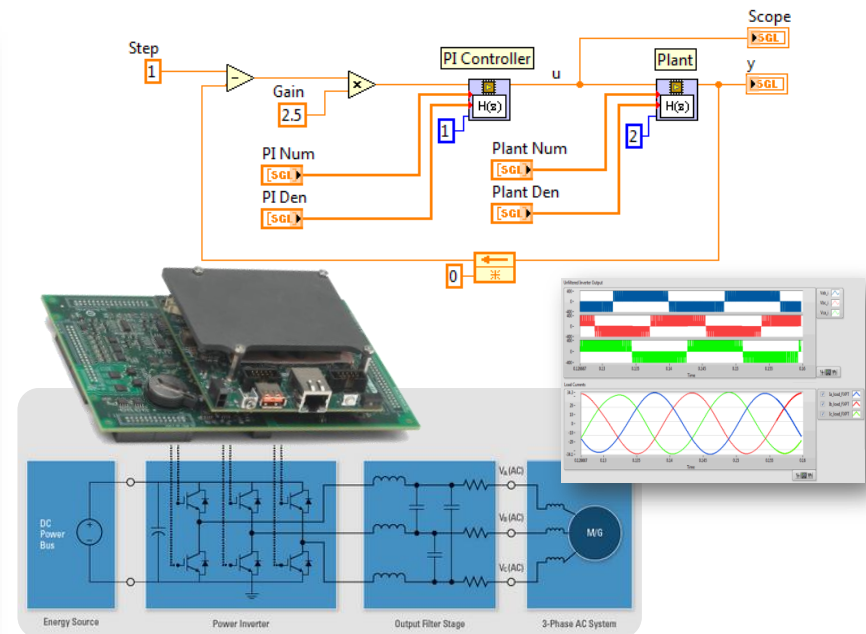


Enabling High-Penetration Solar PV *Control Systems*



Complete Toolchain for Control Design,
HIL Verification and Deployment



NI General Purpose Inverter Controller



*Brian MacCleery – Principal Product Manager for
Clean Energy Technology, National Instruments,
Member IEEE*

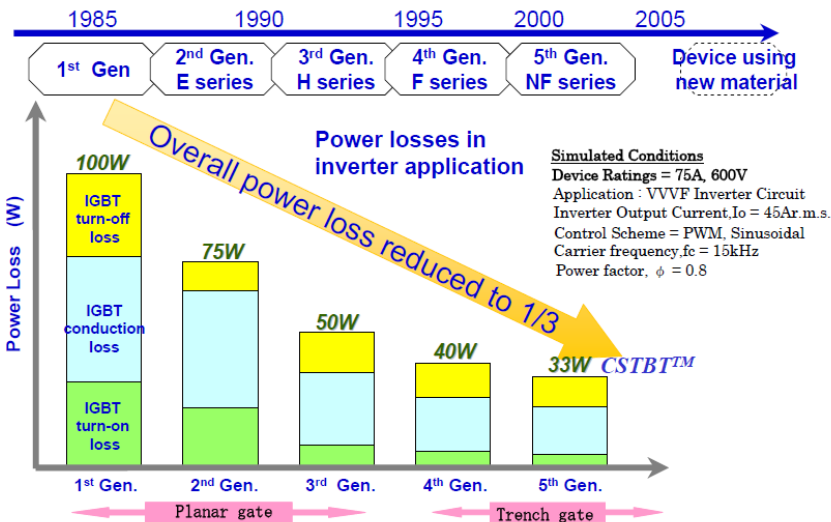
You Can Forecast Any Technology in 5 Minutes with Two Data Points

- Requirements:
 - Two data points for performance/\$ vs. year
 - Divide the technology metric by dollars (i.e. kW/\$, (kW/in³)/\$)
- Formulas:
 - $CAGR = \ln(v2/v1)/dT$
 - $v2 = v1 * \exp(CAGR * dT)$
 - Doubling time: $dT = \ln(2)/rate$
- Where:
 - CAGR is the Compound Annual Growth Rate
 - v1 is the value at date 1
 - v2 is the value at date 2
 - dT is the time interval in years

Example: IGBT Module Energy Efficiency



Reduction of IGBT operation losses



Year	Waste Heat (W/100 kW)		Power Electronics Module Efficiency
1980	5975	1980	94.0%
1990	3222	1990	96.8%
2000	1738	2000	98.3%
2010	937	2010	99.1%
2020	505	2020	99.5%
2030	272	2030	99.7%

$$CAGR = \frac{\ln(v_2/v_1)}{dT}$$

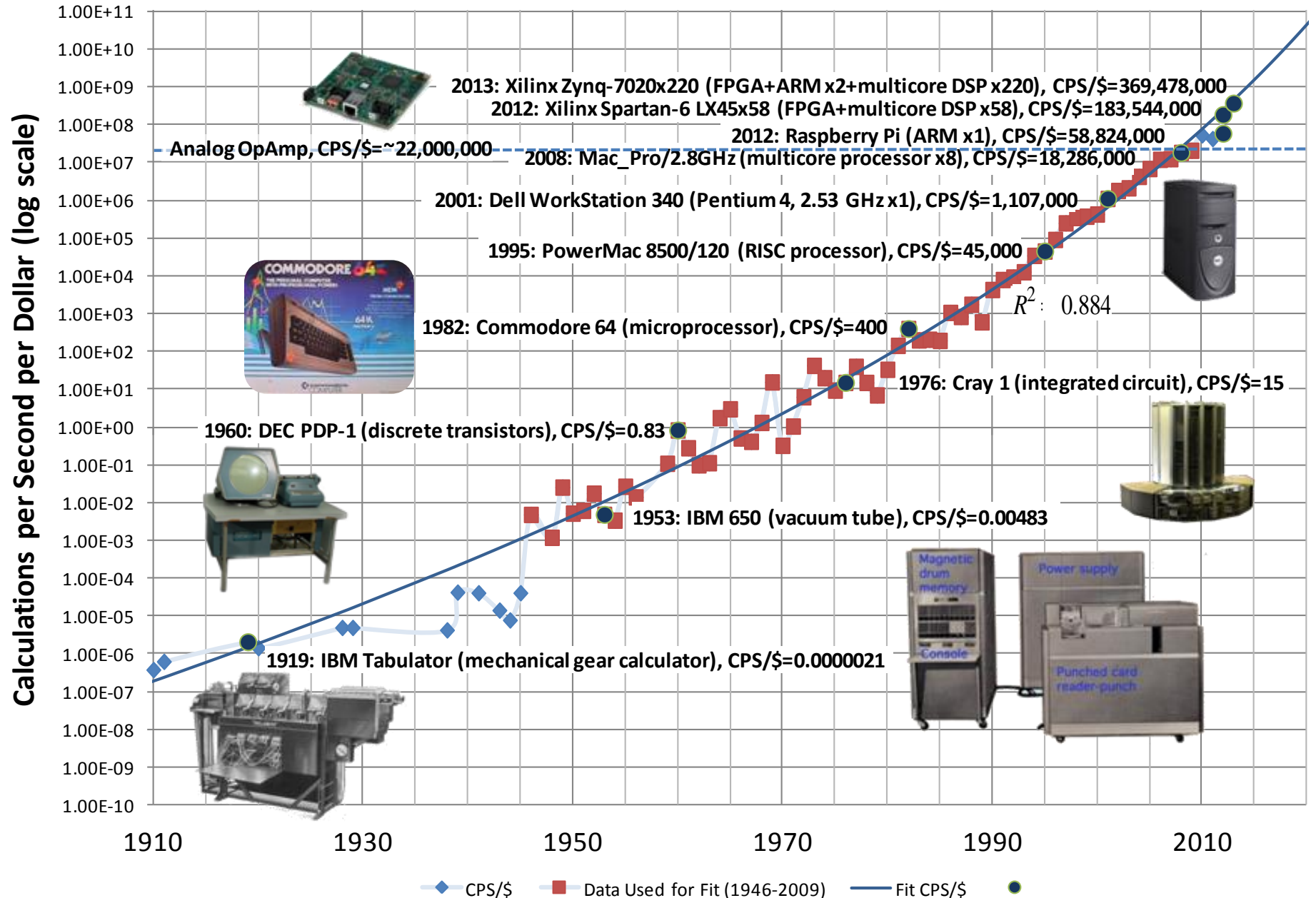
$$v_2 = v_1 * \text{EXP}(CAGR * dT)$$

Doubling time: $dT = \ln(2) / \text{rate}$

Data Source for Curve Fit:
Mitsubishi-Powerex Melcosim Version 11.04.01

Power Electronics Module Energy Efficiency (power loss)			
	13.5 kW Inverter Loss (W)	Year	Inverter IGBT Efficiency
1983	670.2	1983	95.0%
1998	265.4	1998	98.0%
Delta	0.40	15	
CAGR	-6.2%		
Doubling Time	-11.22		

Computing Performance Per Dollar: 1910-2020



Myth: “Renewable Energy Power Electronics Destabilizes the Grid”

- It is not the inherent nature of power electronics that is causing grid stability issues (e.g. low inertia, high THD)
- It is not the non-dispatchable nature of renewable energy that is causing grid stability issues
- My opinion: Operating inverters as current sources is the root of the problem

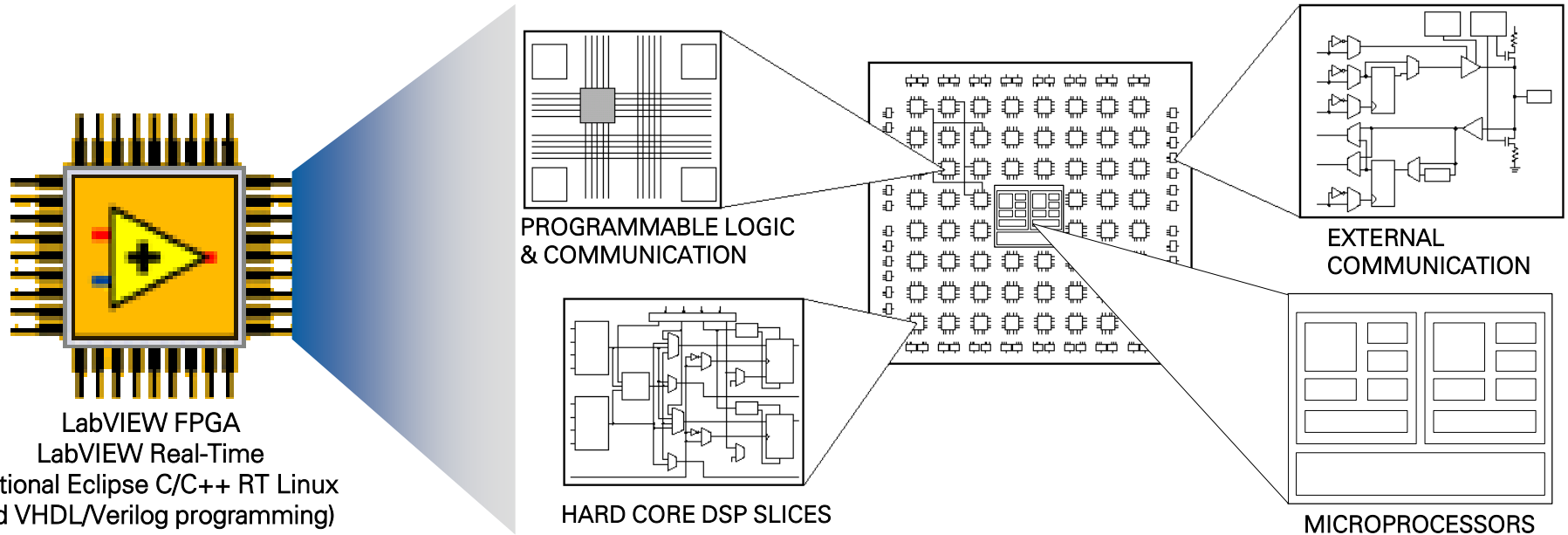
The fact that inverters are not allowed to regulate voltage and frequency (closed loop) is the root cause of the problem

- It is time for inverters to actively regulate voltage and frequency
 - It is not technically difficult.
 - We recently demonstrated that new Ethernet Time Sensitive Networking (TSN) technologies can be utilized for phase alignment. (NI recently filed patents on this approach.)
- It does require some sacrifice
 - It will mean more automatic curtailment. However, this change has already happened with passive open loop 'voltage regulation' standards.

The control systems for wide bandgap power converters will run in “FPGA” hardware

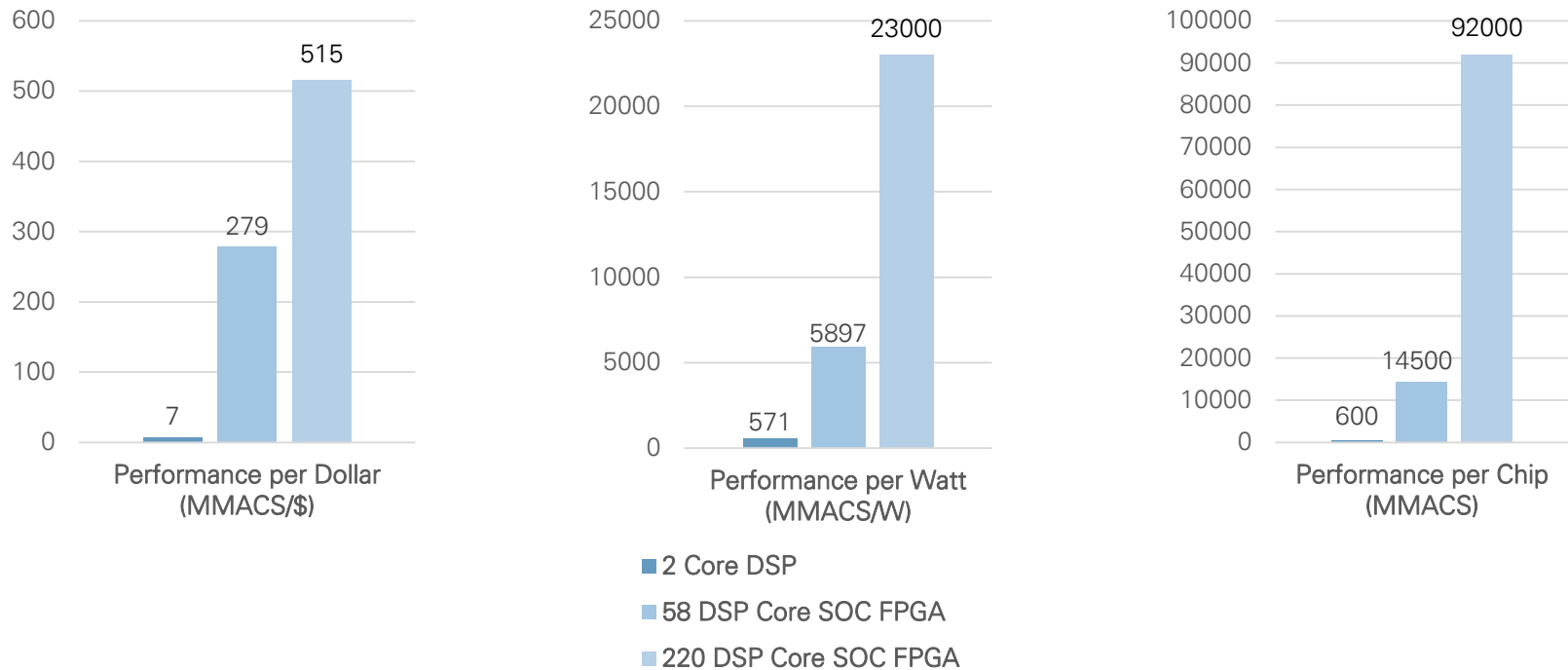
- Modern “FPGA” chipsets are not what you might think
 - They are hybrid chipsets with embedded DSP cores, programmable logic fabric and (sometimes) ARM microprocessors.

FPGA, DSPs, Microprocessors have merged into a Reconfigurable System-on-Chip (RSOC)



“In the past it took us several times longer for a full custom design for a DSP-based circuit board prototype, which then had to be redesigned for volume commercialization after the field trials. We could not have loop frequencies above about 40 kHz, even with a highly skilled DSP programmer. With FPGA, everything is truly running in parallel so I don't have timing problems... We can now have commercial hardware out for field testing in 3 months.” – [Eaton Corporation](#)

Traditional DSP vs. System-on-Chip (SOC) FPGA



	Performance Ratio (Spartan-6/DSP)	Performance Ratio (Zynq-7020/DSP)
MMACS per Chip	24	94
MMACS per Watt	10	31
MMACS per Dollar	40	69

MMACS = Multiply-accumulate operations per second
(measure of DSP computing performance)

Modern “FPGA” chipsets are not what you might think

- They are programmed graphically with high level control design tools that require no knowledge of Verilog or VHDL
- Algorithms run in floating point math
- The entire power electronics control algorithm runs in the hybrid FPGA/DSP fabric.
- They are capable of closed loop control at rates over 1 MHz
- They are powerful enough that full digital twin real-time simulation models can be embedded in the control chip

LABVIEW FPGA MODEL BASED ALGORITHM DEPLOYMENT TOOLS

LABVIEW FPGA

Implementation:

Single Precision Floating Point

Performance:

2.95 microseconds

339 times faster than real-time

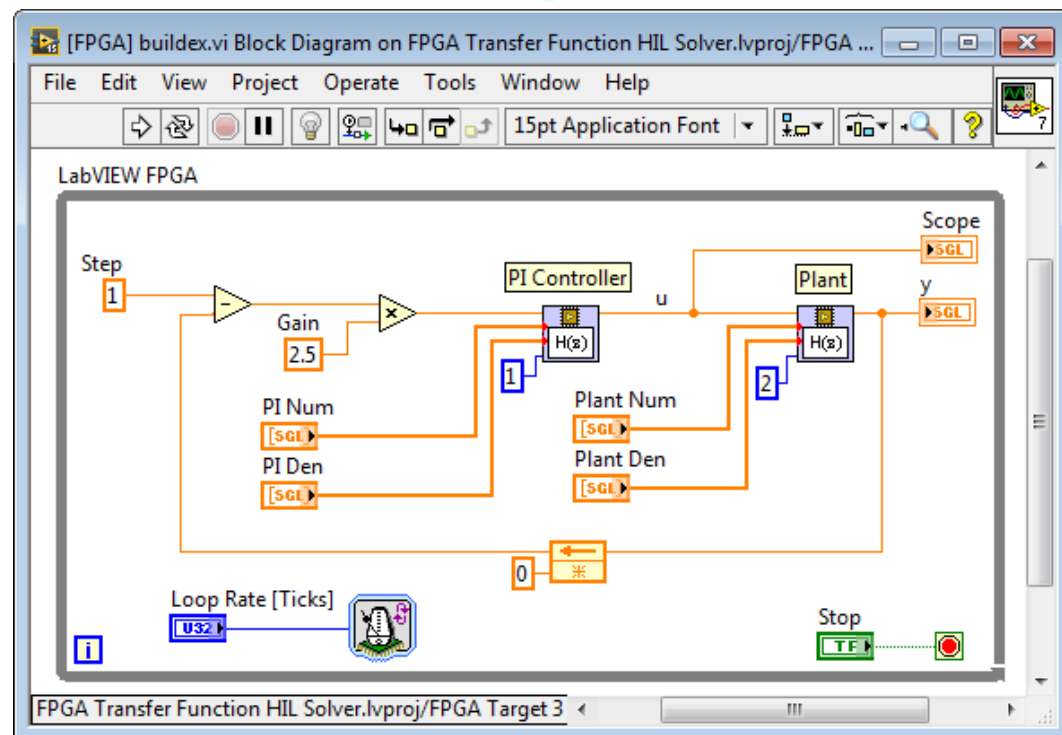
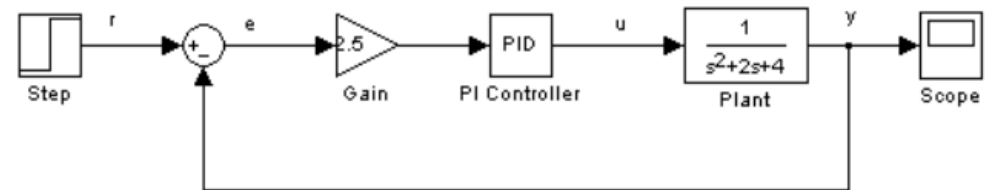
FPGA Resources (Spartan-6 LX45):

Slice Registers: 3.6% (1953 out of 54576)

Slice LUTs: 11.1% (3018 out of 27288)

DSP48s: 34.5% (20 out of 58)

Block RAMs: 0.0% (0 out of 116)



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[Download the LabVIEW FPGA Floating Point Toolkit](#)

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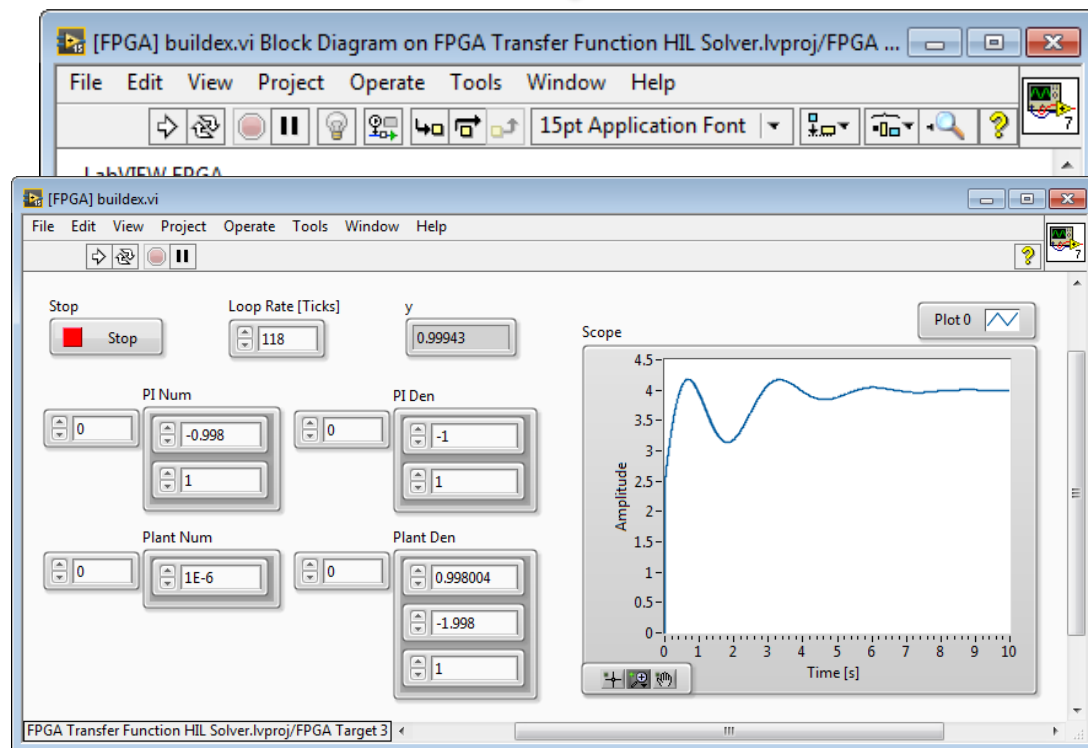
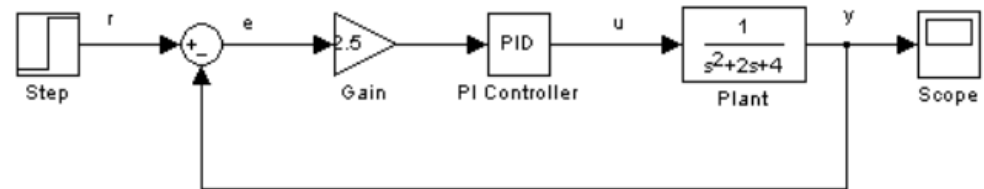
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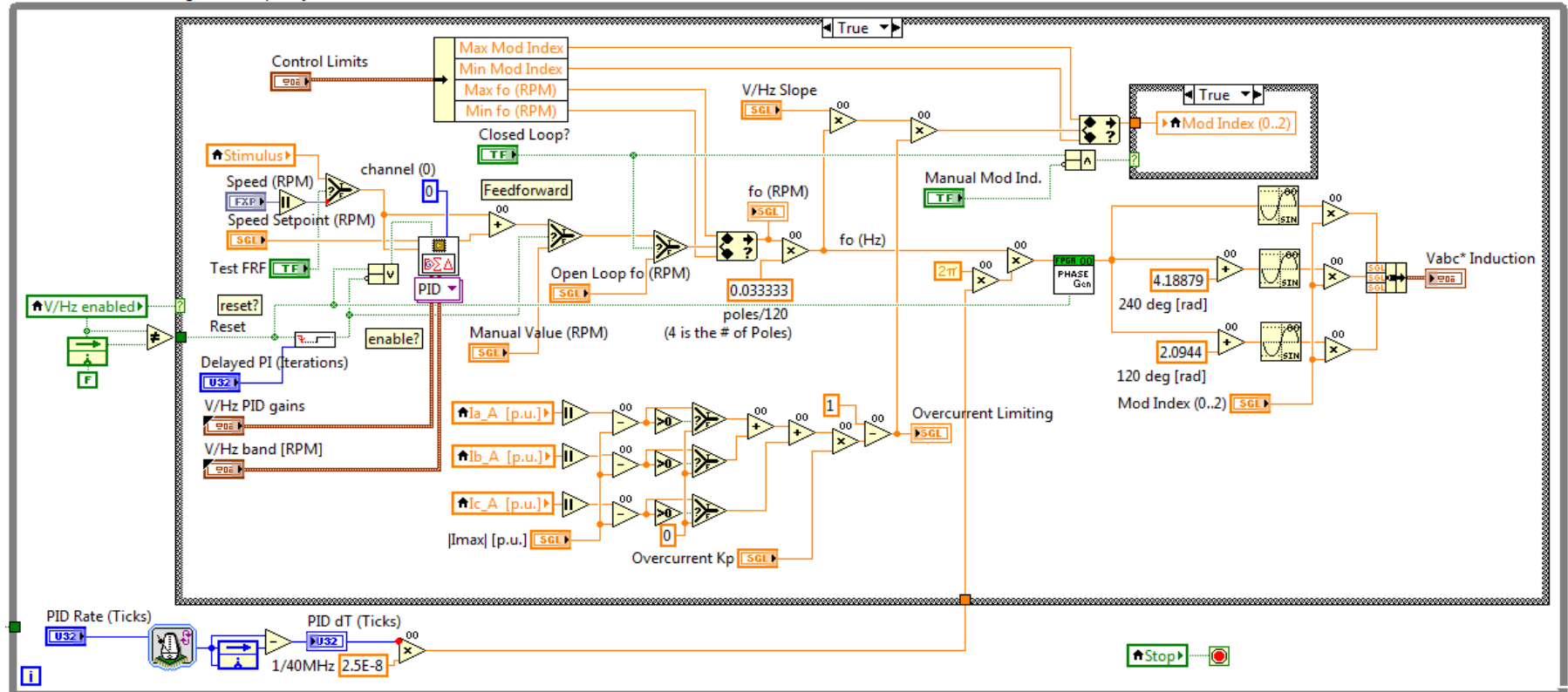


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[Download the LabVIEW FPGA Floating Point Toolkit](#)

FPGA Floating Point Control

AC Induction Motor Voltage over Frequency (V/F) Control



There is a lot the embedded control system can do to reduce cost, weight and size

- There are significant low hanging fruit opportunities for cost reduction through advanced control IP

TOTAL LIFETIME COST REDUCTION THROUGH ADVANCED IP

TIME SENSITIVE NETWORKING
TIME LOCKED GRID SYNCHRONIZATION

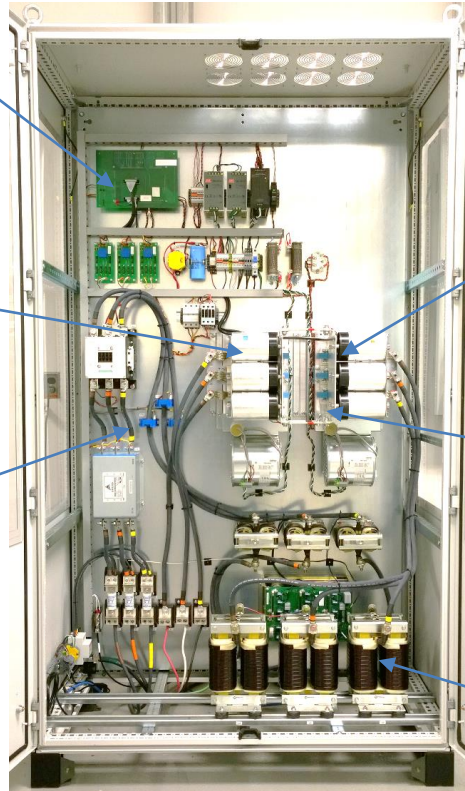
PROGNOSTICS
DIGITAL TWIN SELF-SIMULATION

RELIABILITY
ADVANCED CURRENT LIMITING

IGBT LIFETIME EXTENSION
ACTIVE JUNCTION TEMPERATURE
REGULATION

ADVANCED CONTROL
VIRTUAL SYNCHRONOUS MACHINE

**LINE REACTOR COST/WEIGHT
REDUCTION**
ACTIVE FILTERING



[Browse case studies folder](#)

There is a lot the embedded control system can do to reduce cost, weight and size

- There is a tremendous low hanging fruit opportunity for improvements in the control systems that primarily have not been done due to the performance limitations of old chipsets and the arduous nature of the way they were programmed
- Traditionally the circuit design, magnetics, thermals and control algorithms are optimized individually

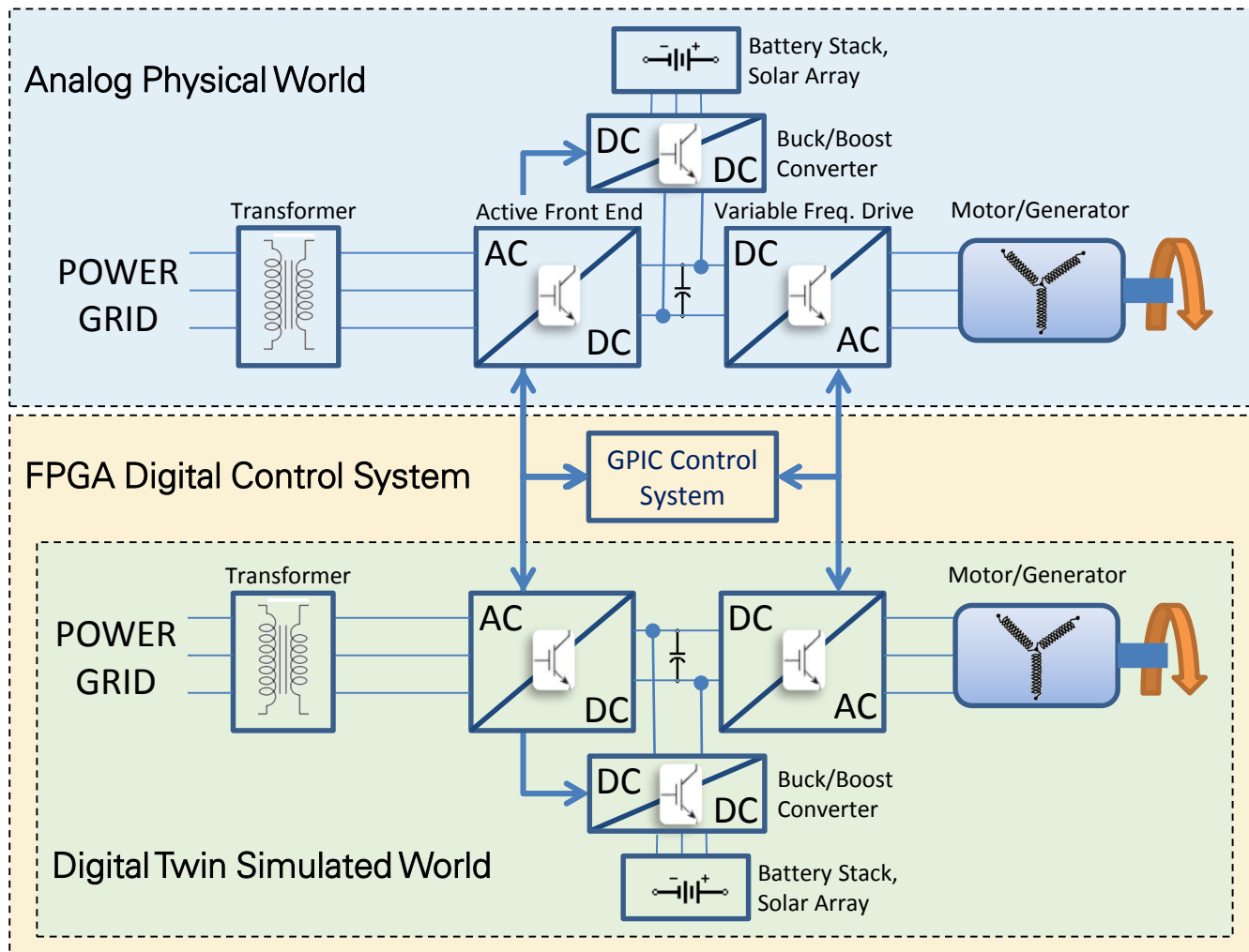
Embedded Real-Time Digital Twins

- Use of digital twin real-time simulation models embedded in the control system

Drivers:

- Business need to add new control objectives for properties that cannot be directly measured (i.e. transistor lifetime extension and wear leveling)
- Business need for self diagnostics and prognostics (equipment condition health monitoring)

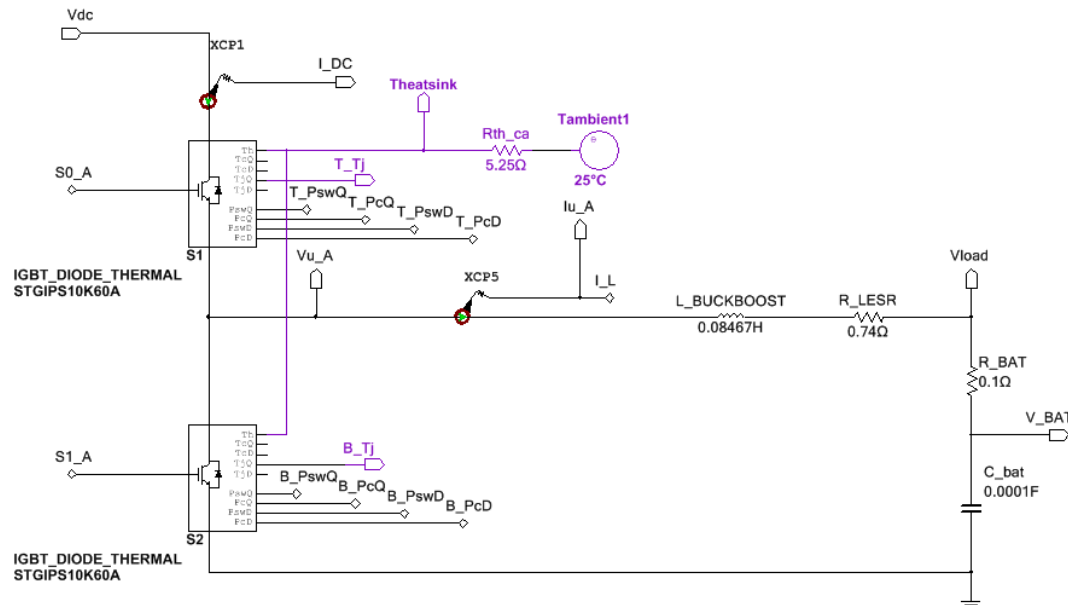
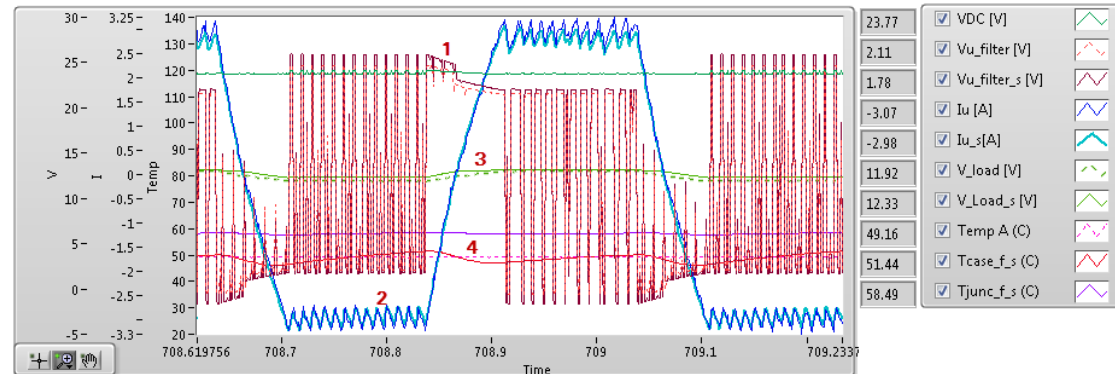
FPGA BASED CONTROL SYSTEM WITH LOCAL REAL-TIME DIGITAL TWIN



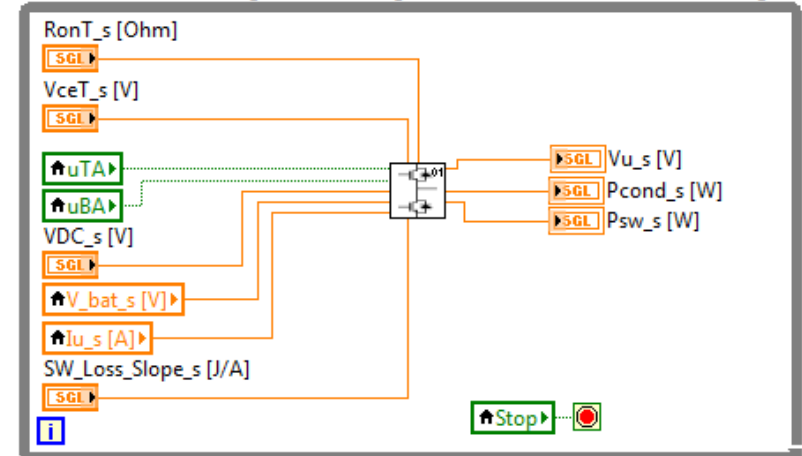
Buck-Boost Energy Storage Converter with Embedded Real-Time Digital Twin for Active Junction Temperature Regulation

1. IGBT half-bridge output voltage (red)
2. Battery Charge/Discharge Current (blue)
3. Battery Terminal Voltage (green)
4. Case Temperature (red)

SINGLE IGBT HALF-BRIDGE DATA (PHYSICAL MEASUREMENT vs. DIGITAL TWIN)



LabVIEW FPGA Half-Bridge Converter Digital Twin w/ Conduction and Switching Losses



DIGITAL TWIN APPLICATIONS BY STAKEHOLDER

- **SYSTEM DESIGN TEAM**

- **Model Validation:** Continuous online validation of the model during field deployments closes the loop with the design team and confirms or rejects the assumptions on which their design decisions are based.
- **Design Optimization:** Digital twin models combined with advanced machine learning algorithms facilitates design optimization that spans the boundaries between the physical system design and the control algorithms to satisfy multiple design objectives. Example: Optimize the design for energy efficiency, cost reduction, and uptime

DIGITAL TWIN APPLICATIONS BY STAKEHOLDER

- **CONTROL DESIGN TEAM**

- **Observer-based Control:** Many internal states in cyber-physical systems cannot be physically measured but are modeled in the digital twin and can be used as feedback signals for control. Example: IGBT junction temperature active regulation
- **Delay Removal:** Time delays are very problematic for control systems and can be removed in the digital twin model. “Zero delay” digital twin signals can be used as feedback signals for control. Example: Zero delay temperature control
- **Automatic Online Re-Tuning:** The digital twin model combined with advanced machine learning algorithms can be used to find the optimal tuning gains that satisfy multiple linear and non-linear control objectives. Example: Simultaneous tuning of cascaded control loops for setpoint tracking, stability, and IEEE 1547 compliance objectives.
- **Predictive Control:** Faster than real-time digital twin models can be used to explore multiple control strategies before committing to one

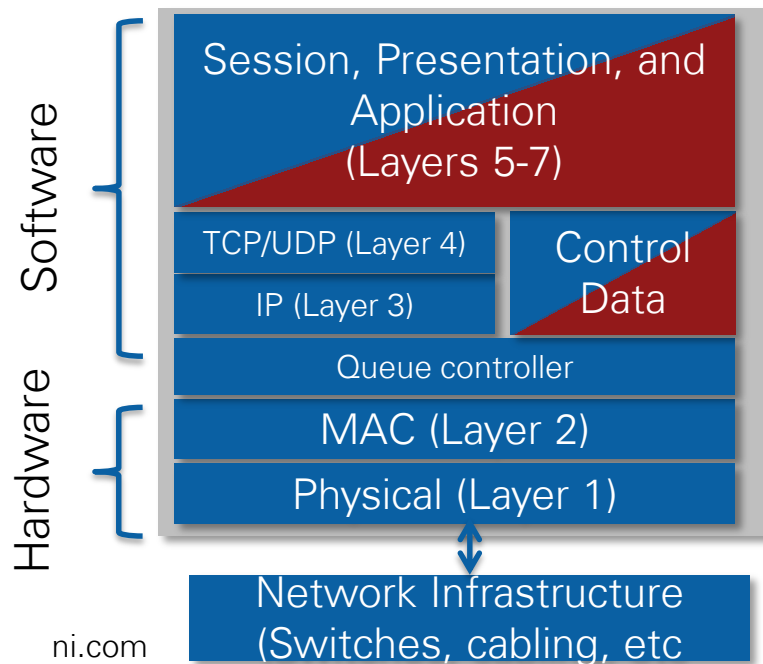
DIGITAL TWIN APPLICATIONS BY STAKEHOLDER

- **OPERATIONS & MAINTENANCE TEAM**

- **Prognostics:** A mismatch between the physical system response and the digital twin may indicate a problem. The digital twin endows the control system with an expectation for the system response, enabling problems to be detected long before a failure occurs.
- **Lifetime Extension:** Digital twins can include models for component lifetime, which can be incorporated in the control strategy to extend lifetime and increase reliability.

Ethernet Time Sensitive Networking

- Emergence of new timing, synchronization and deterministic communication capabilities standard Ethernet (true standards)



Key technology vendors are driving:

- Intel
- Broadcom
- Marvell
- Cisco

Key industrial, embedded, and automotive vendors are participating to drive requirements

■ Custom HW or SW
■ Standard HW or SW

Time Sensitive Networking: Key Elements



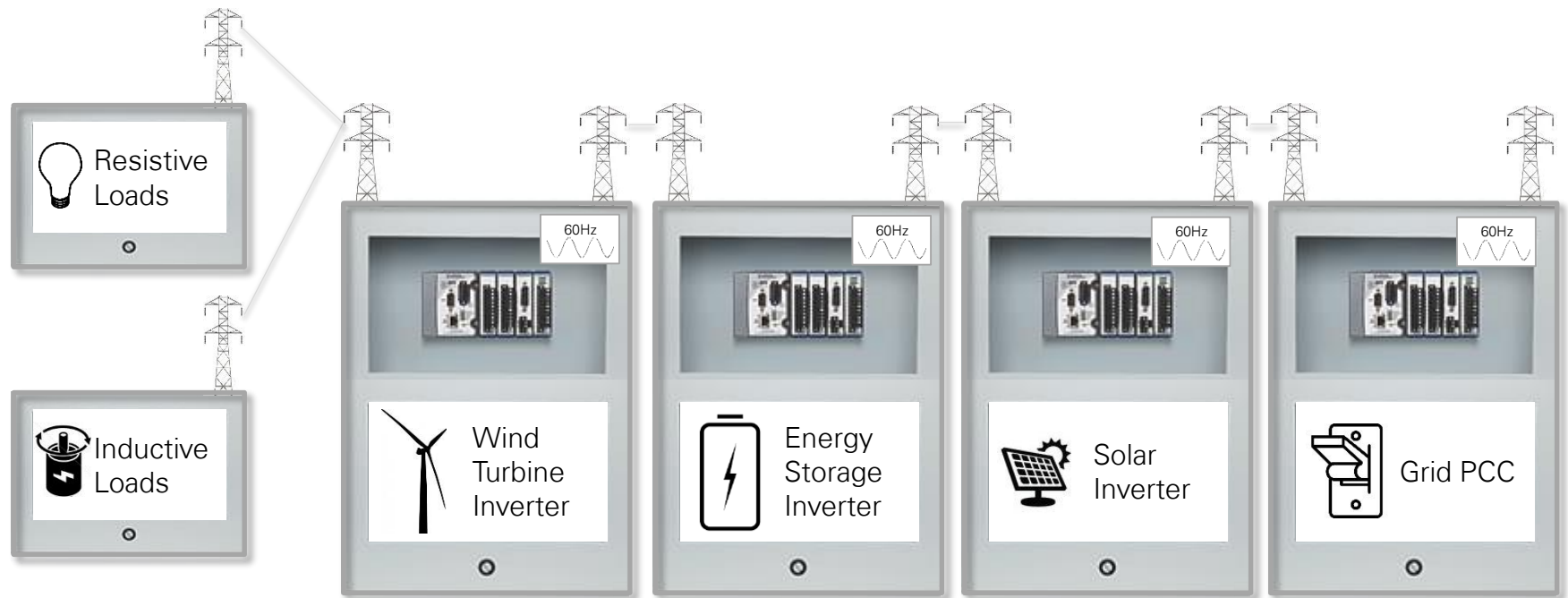
Standard	Area	Title
IEEE 802.1ASrev, IEEE 1588	Timing & Synchronization	Enhancements and Performance Improvements
IEEE 802.1Qbu & IEEE 802.3br	Forwarding and Queuing	Frame Preemption
IEEE 802.1Qbv	Forwarding and Queuing	Enhancements for Scheduled Traffic
IEEE 802.1Qca	Path Control and Reservation	Path Control and Reservation
IEEE 802.1Qcc	System Configuration	Enhancements and Performance Improvements
IEEE 802.1Qci	Time Based Ingress Policing	Per-Stream Filtering and Policing
IEEE 802.1CB	Seamless Redundancy	Frame Replication & Elimination for Reliability

...

Additional Enhancements to Come

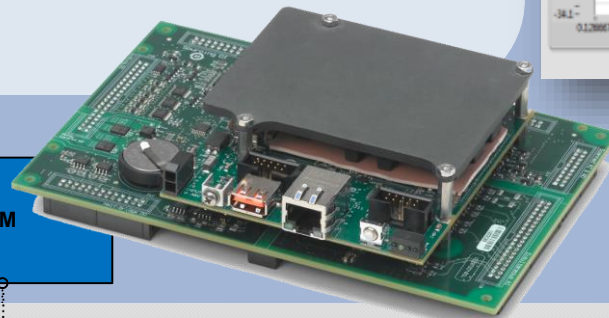
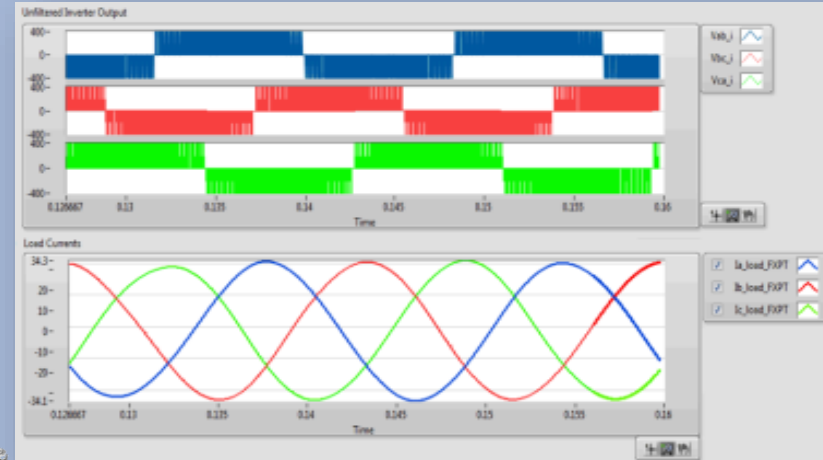
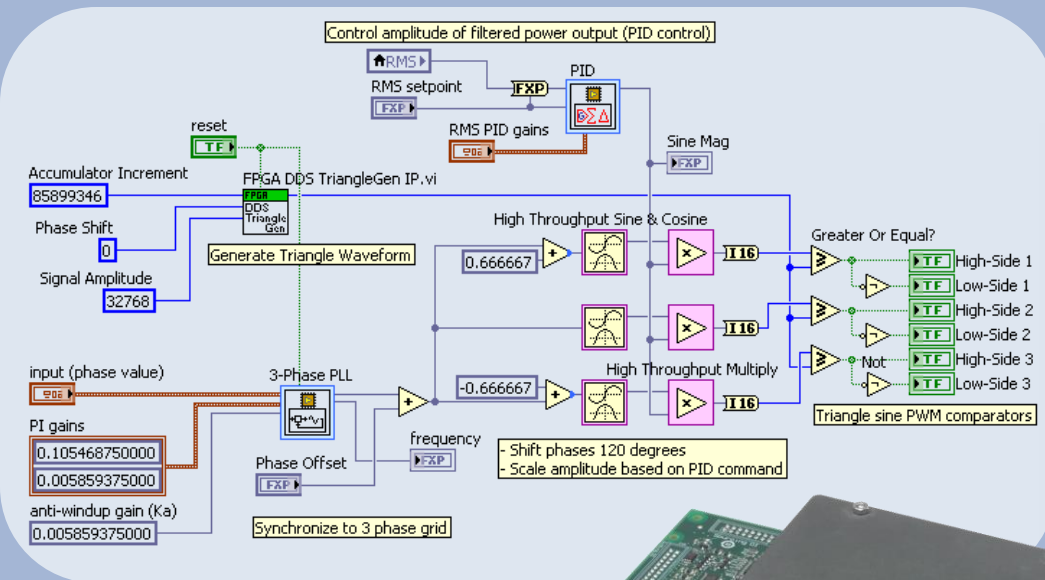
100 Percent Power Electronics Microgrid Demonstration

Ethernet Time Sensitive Networking (TSN)

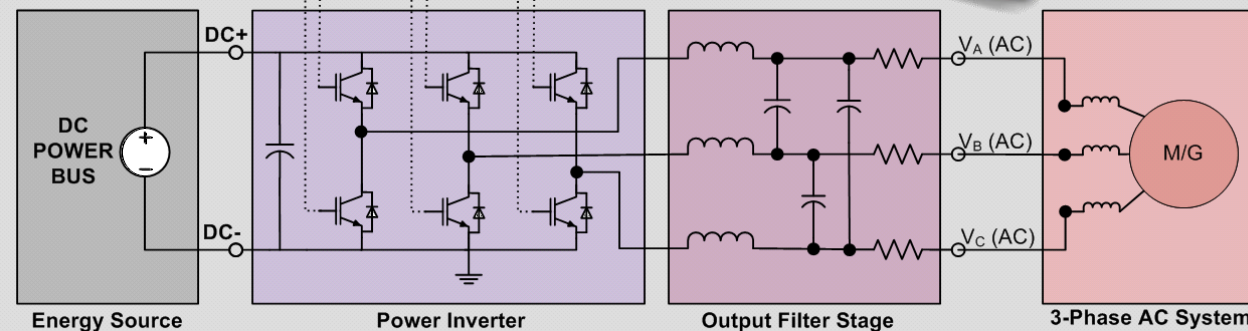


Also compatible with Virtual Synchronous Machine (VSM) control (Zhong)

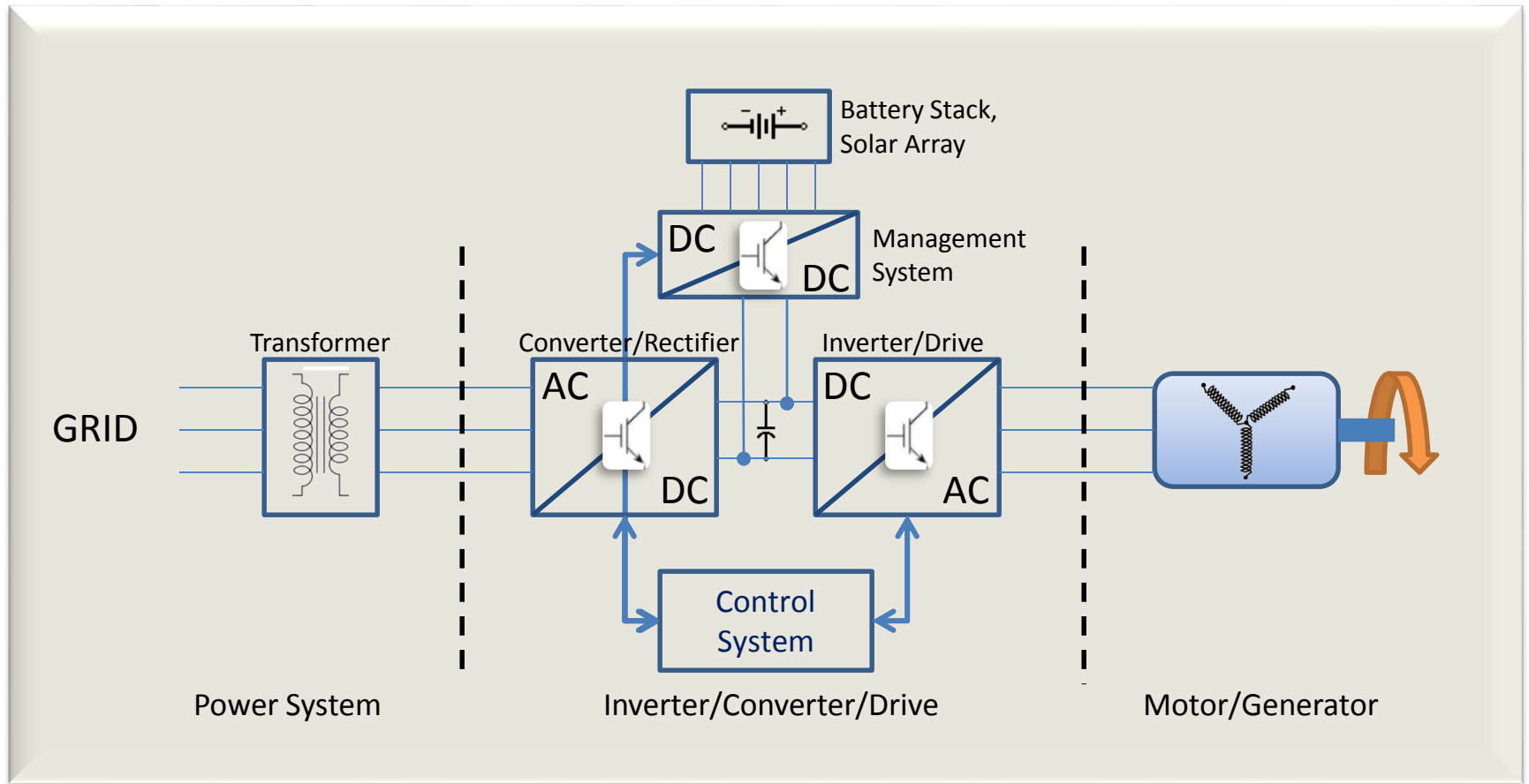
NI Single-Board RIO General Purpose Inverter Controller (GPIC)



NREL
NATIONAL RENEWABLE ENERGY LABORATORY

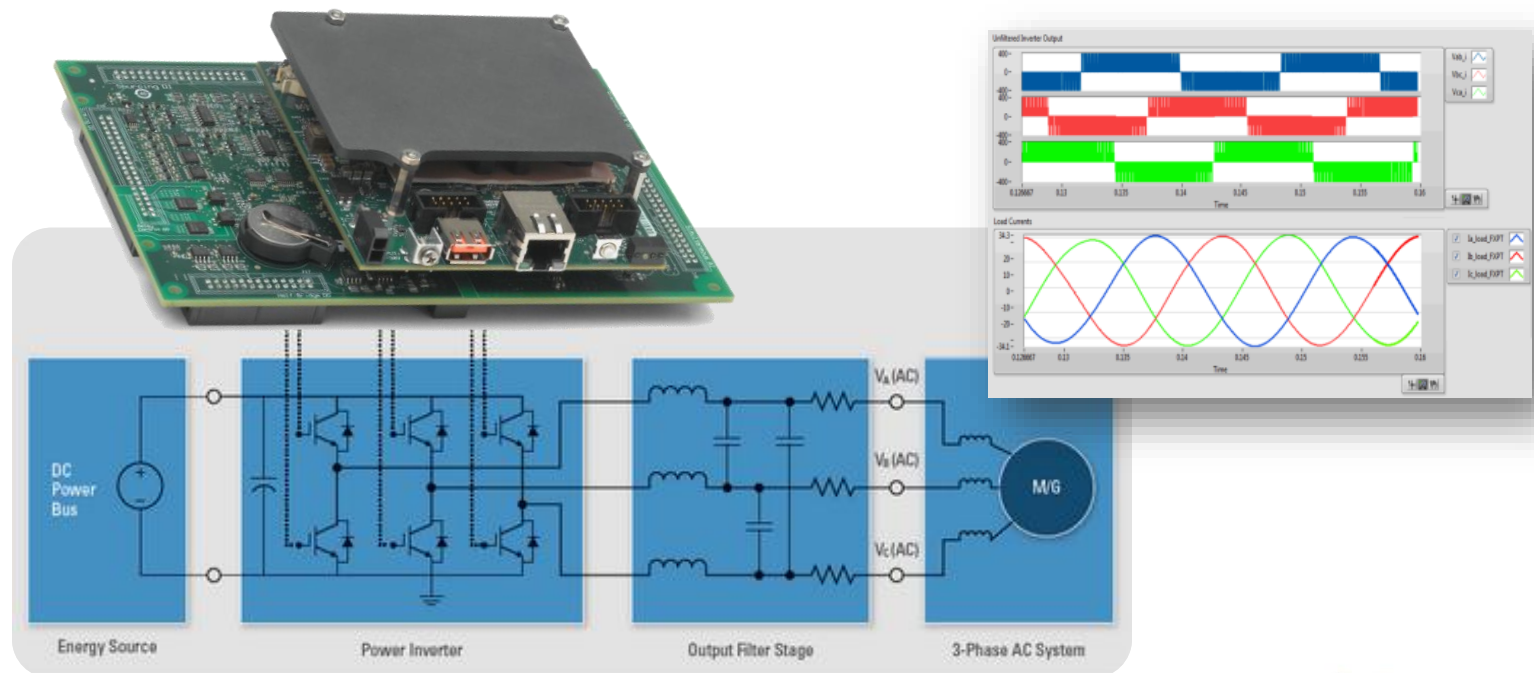


Typical GPIC Power Conversion Applications



NI Single-Board RIO General Purpose Inverter Controller (NI GPIC)

- Industry-proven embedded control and I/O system for OEM power conversion equipment
- FPGA Reconfigurable System-On-a-Chip (RSOC) technology with 220 DSP cores: 69x higher performance per dollar than traditional DSPs
- Quadruples the productivity of embedded design teams: 114-person-month average reduction in development cost

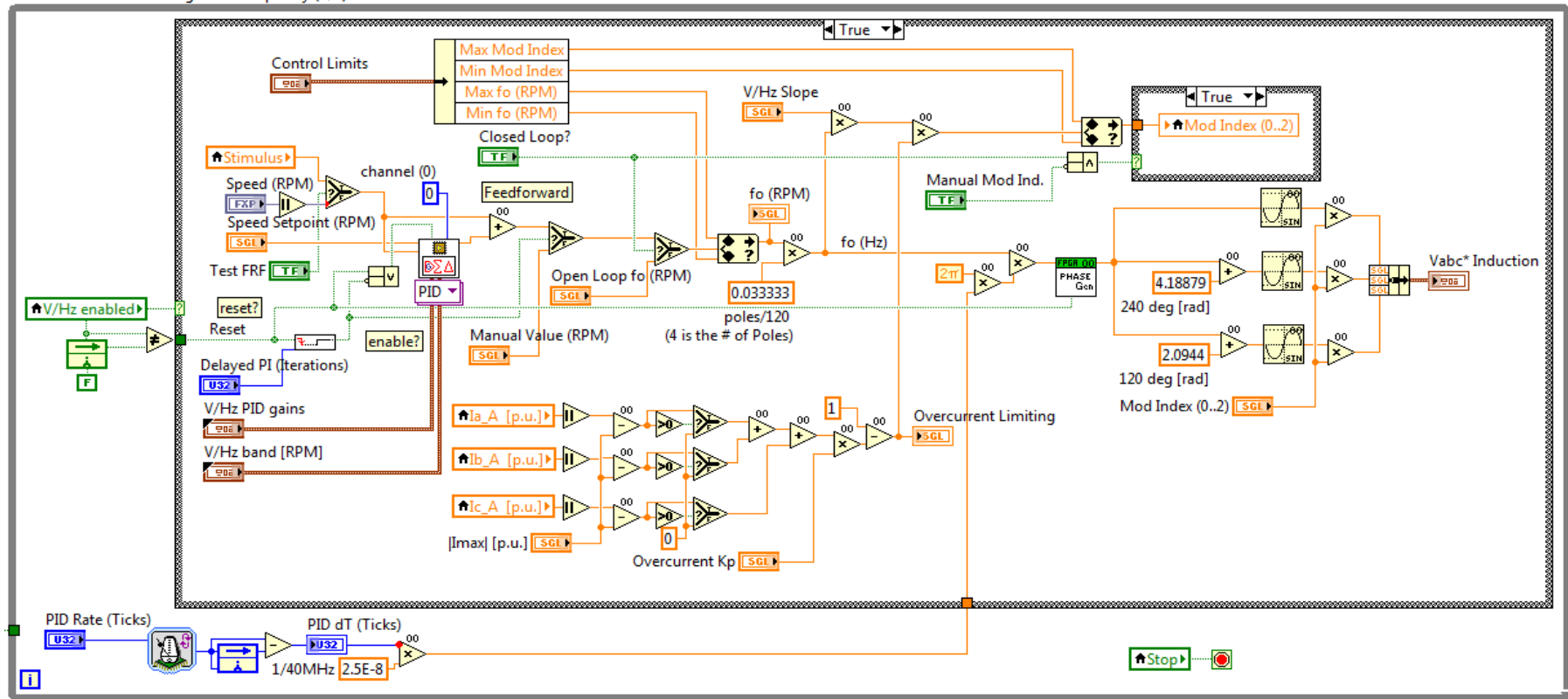


[Download Case Studies](#)

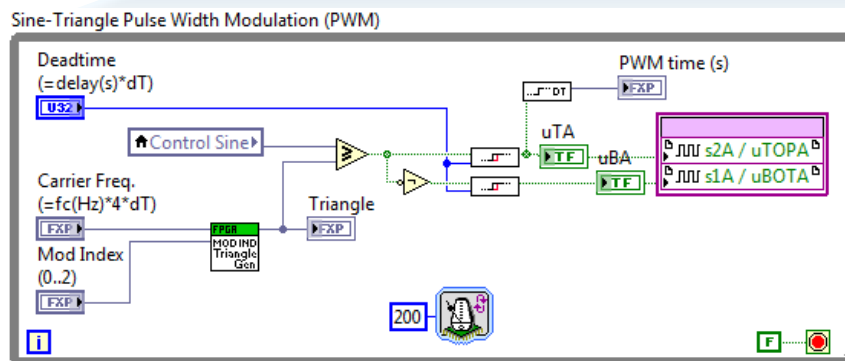
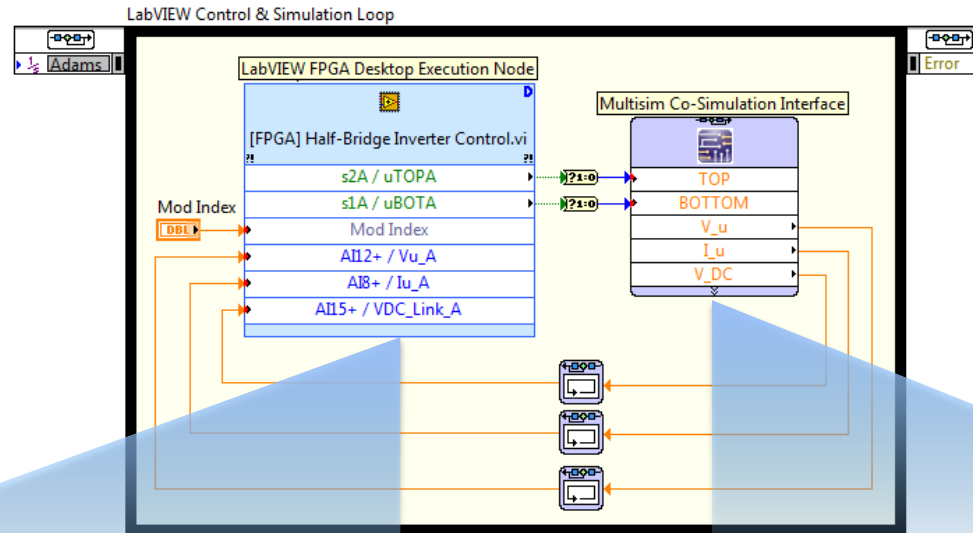
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- Reconfigurable System-On-a-Chip (RSOC) technology with 220 DSP cores: 69x higher performance per dollar than traditional DSPs
- Complete toolchain quadruples the productivity of embedded design teams: 114-person-month average reduction in development cost

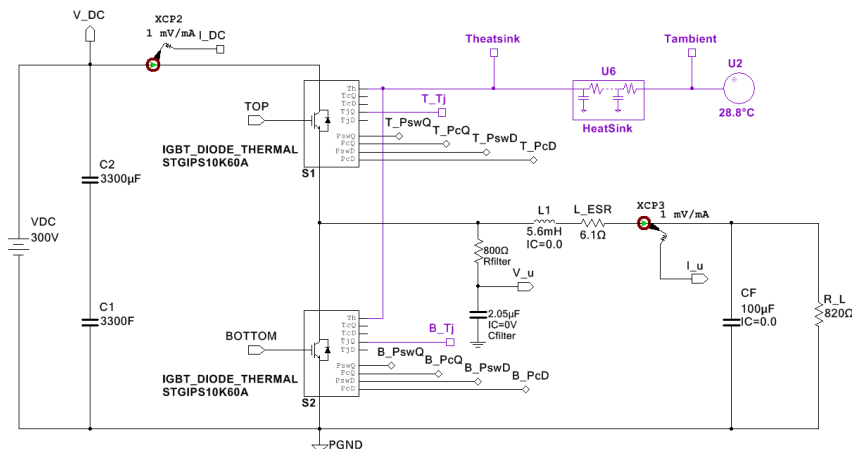
AC Induction Motor Voltage over Frequency (V/F) Control



Co-Simulation Based FPGA Control Design

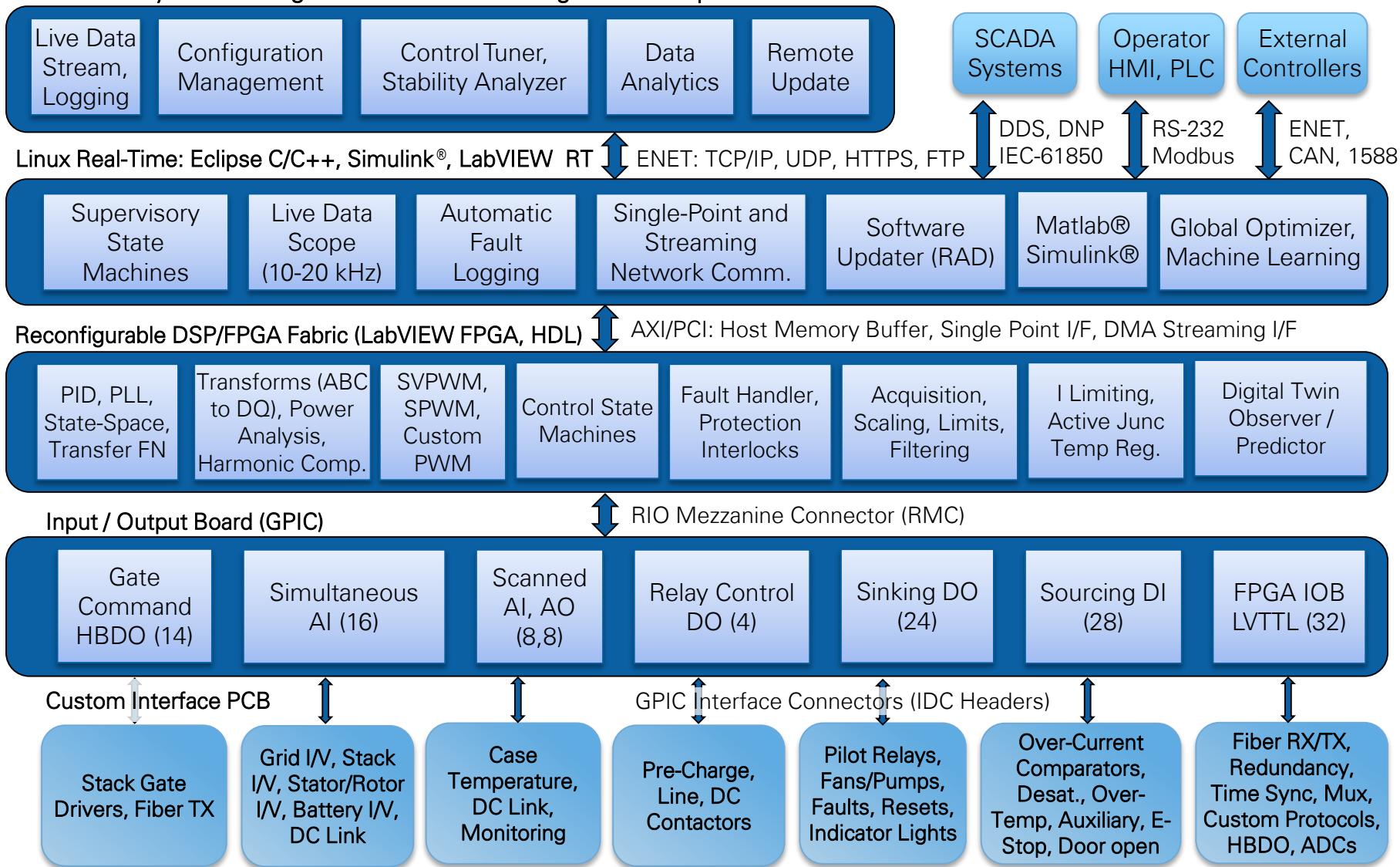


**Time
Adaptive
Synchronized
Co-Simulation
(TASCS)**



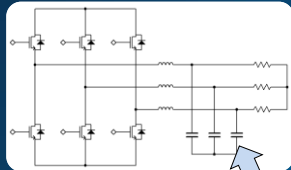
Hardware/Software Architecture Map

Remote System Management Utilities for Design Team & Operators



Complete Power Electronics Control Design Toolchain

Co-Simulation Based Development
(Multisim, LabVIEW FPGA, IP Cores)



$$i_{\alpha\beta}(t) = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix}$$

A: 0.333333 alpha
B: 0.57735 beta
C: 0.57735 beta

Mini-Scale Control
Development System



Design

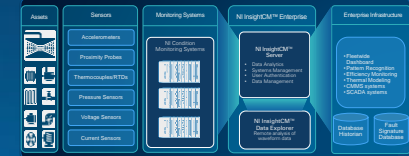
Prototype

Deploy

HIL
Testing

Remote
Support

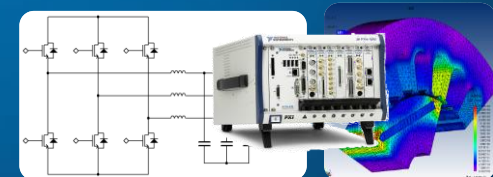
Industrial Internet of Things
(InsightCM SDK)



Full Power
Digital Dyno Test Rigs



Real-Time HIL Simulation
(Veristand, OpalRT, StarSim, El. Motor Sim)



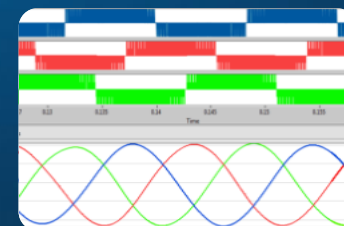
Utility Networking Toolkits
(DDS, IEC-61850, DNP3, ...)



Commercial Deployment
(General Purpose Inverter Controller)



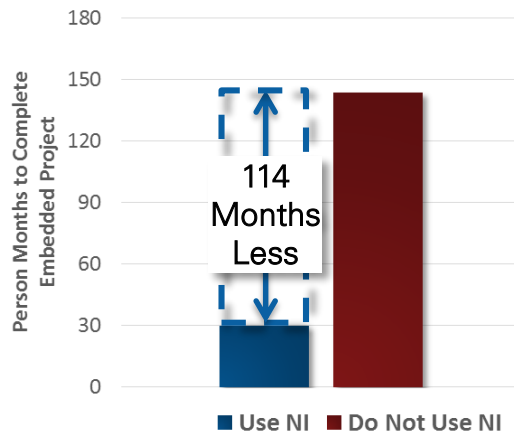
Power Measurement Suite
(IEC EN 61000, 50160, ...)



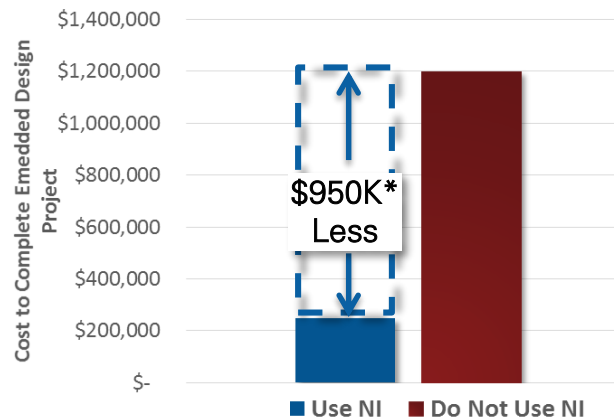
The results are in:

Improved approach to embedded design delivers a 4X advantage

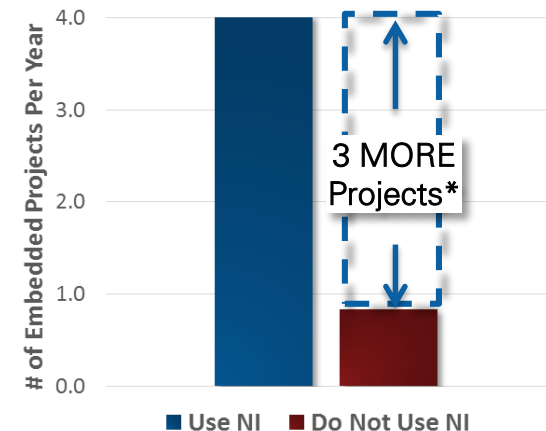
What More Could Your Business
do with an Additional
114 Months?



What Could You Change in
Your Products to Win More
Business?



What More Could You do with
3 Additional Embedded
Projects /Year with the Same
Development Budget?



Based on data from Wilson Research Group, 2012 National Instruments/UBM Survey of Embedded Markets, January – April 2012

*Assumes \$100K per engineer fully burdened cost/year.

Does not include additional cost such as high-end EDA tools required for custom design – if included your advantage using NI increases.

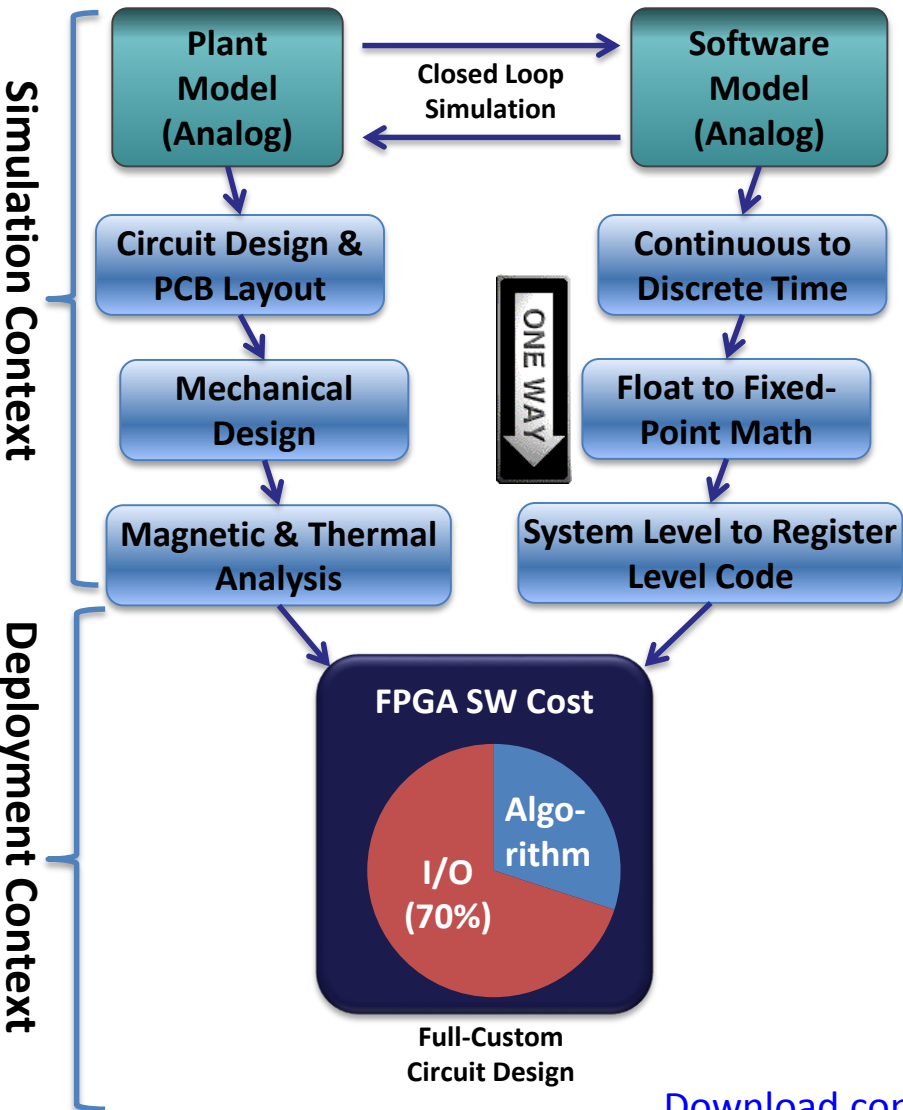
[View Survey Results](#)

The UBM/EETimes study included 1,648 responses from embedded engineers from Americas, Europe and Asia (margin of error +/- 2.0%). The Wilson Research study included 443 responses NI embedded design customers from Americas, Europe and Asia (margin of error +/- 3.9%).

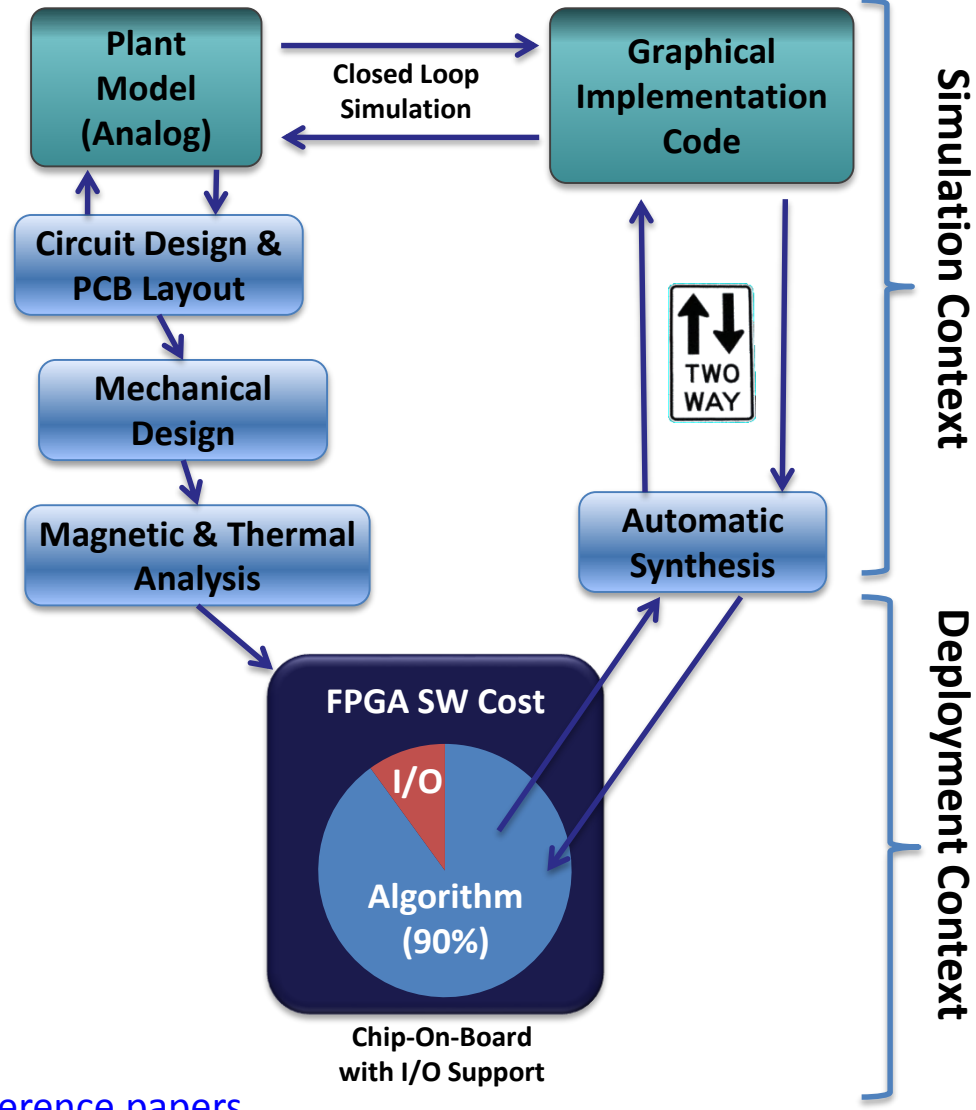


Reducing the Simulation to Deployment Cycle from Weeks to Hours

Traditional Methodology



NI LabVIEW RIO Toolchain

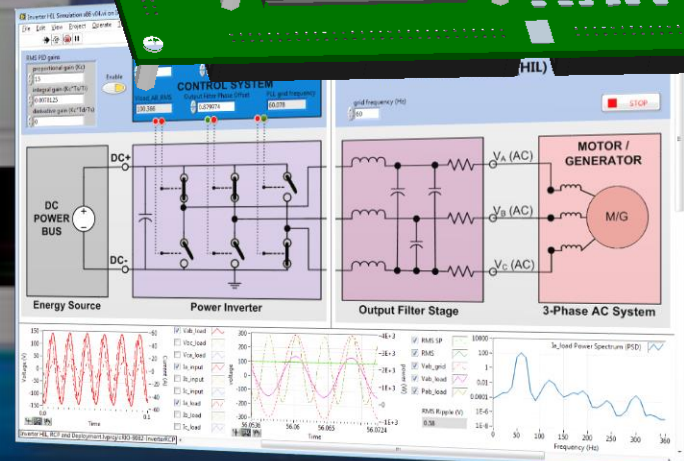
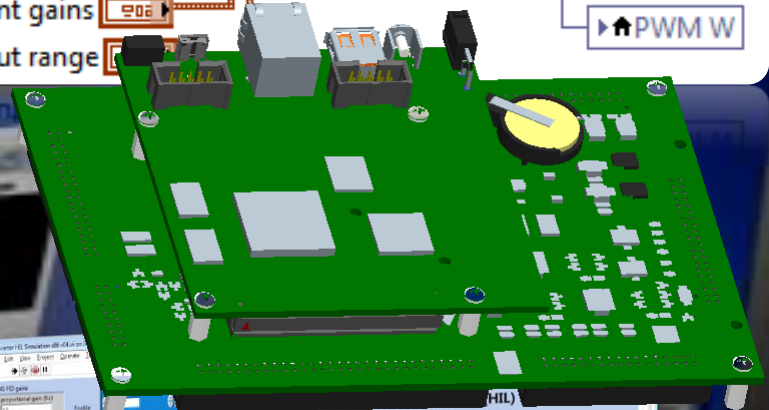
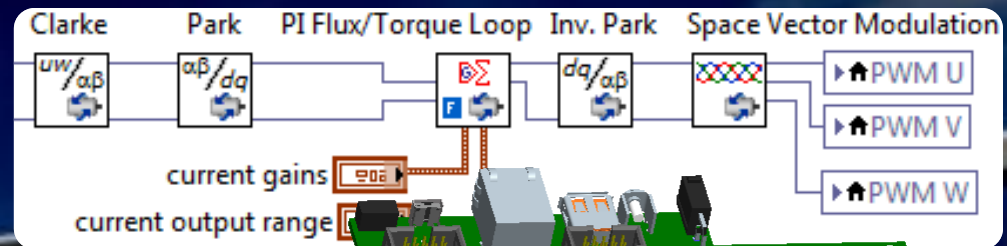


[Download conference papers](#)

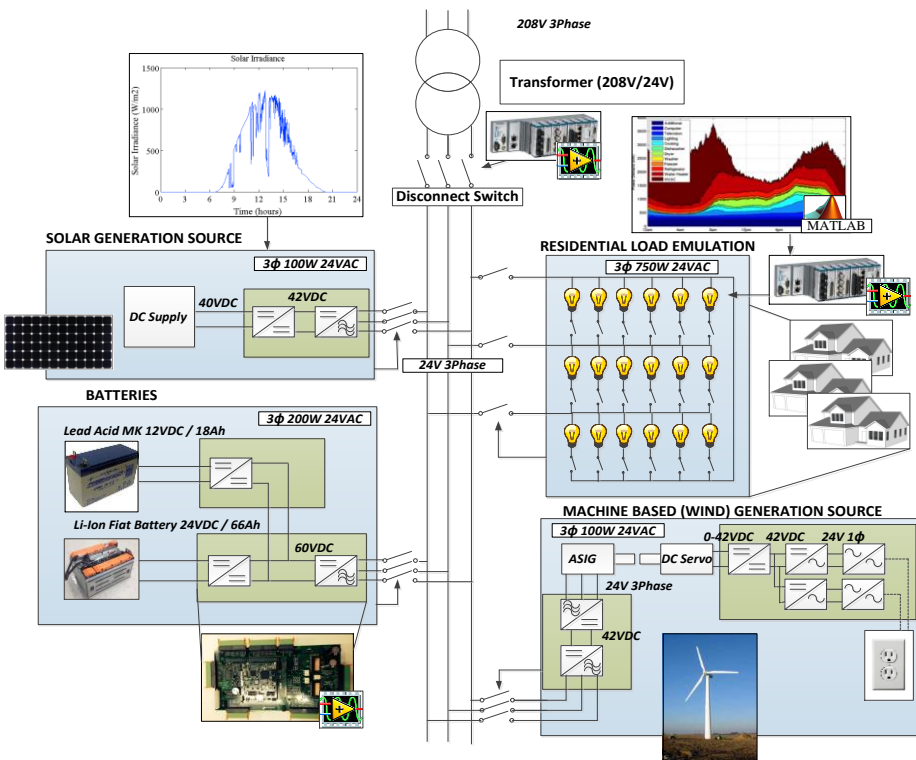
The Digital Energy Revolution

- Digitized and digitally controlled
- Networked
- Field reconfigurable
- Modeled and simulated
- Improving at exponential rates

“Today, approximately 30 percent of all power generation utilizes power electronics between the point of generation and consumption. By 2030, it is expected that up to 80 percent of all generated electricity will utilize power electronics.” –US Dept. of Energy



Oak Ridge National Labs (ORNL): Software-defined Intelligent Grid Research Integration and Development platform (SI-GRID)



**PHYSICAL MICROGRID:
NI RIO FPGA BASED CONTROL SYSTEMS
WITH LOCAL DIGITAL TWINS**



**CONTROL
VALUES**



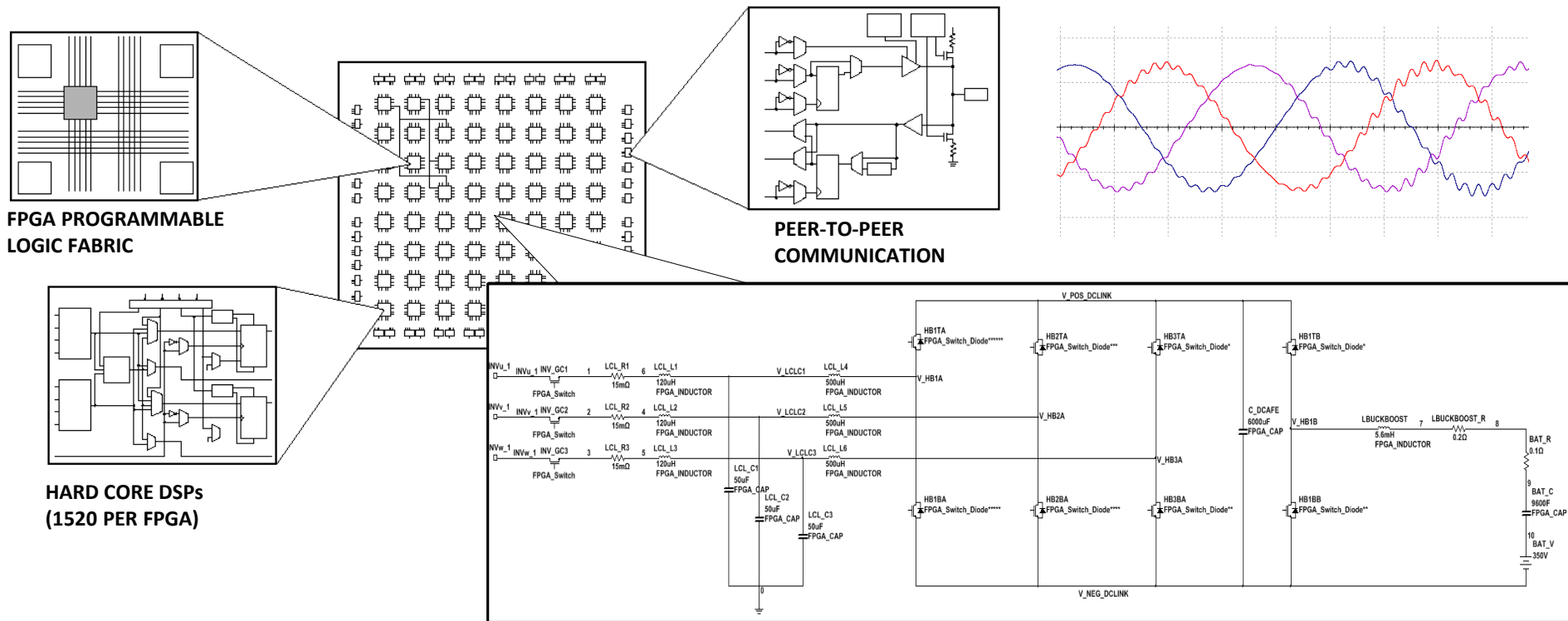
**PREDICTED
VOLTAGE,
CURRENT**



**REAL-TIME GRID SIMULATION:
FPGA BASED LOW-LATENCY
RECONFIGURABLE SUPERCOMPUTER**

Automatic Model Conversion to Reconfigurable FPGA Hardware

Models for power system including power electronics and electrodynamic models are automatically converted to ultra-high speed hardware accelerated implementation using graphical floating point high level synthesis.



ORNL Real-Time Power Grid Simulator – Benchmark Circuit

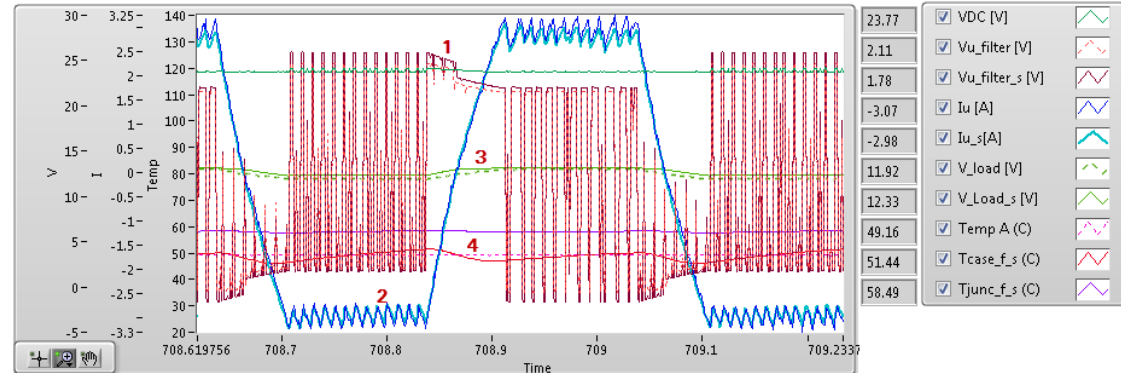
Power Grid Simulation System:

- 80 FPGAs
- 450 Peer-To-Peer Streams Between FPGAs
- 1 Microsecond Simulation Timestep
- 32 GB/s Data Computed

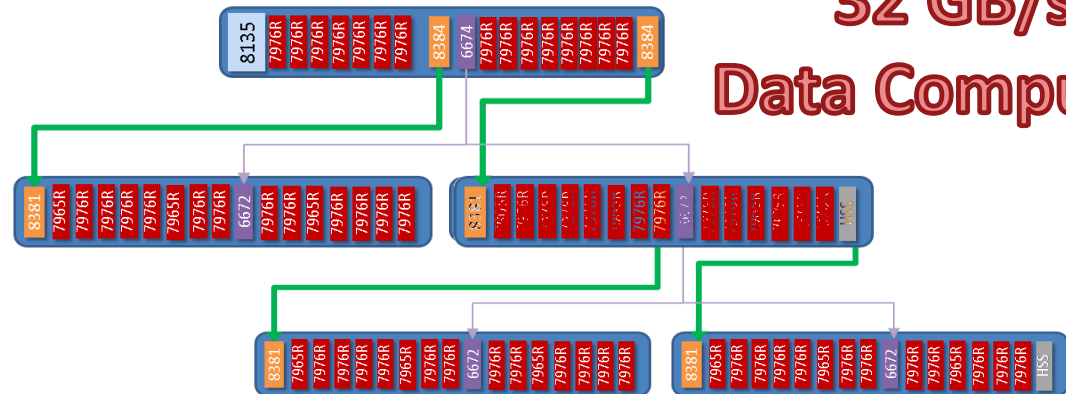
1 MHz Real-Time Grid Simulation:

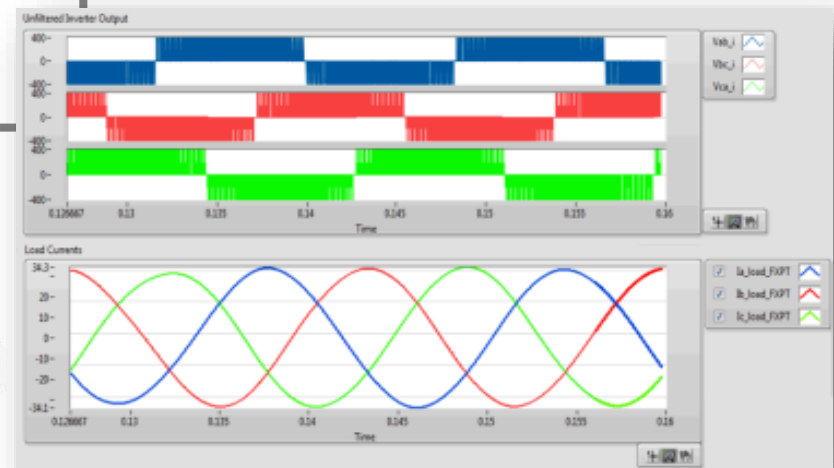
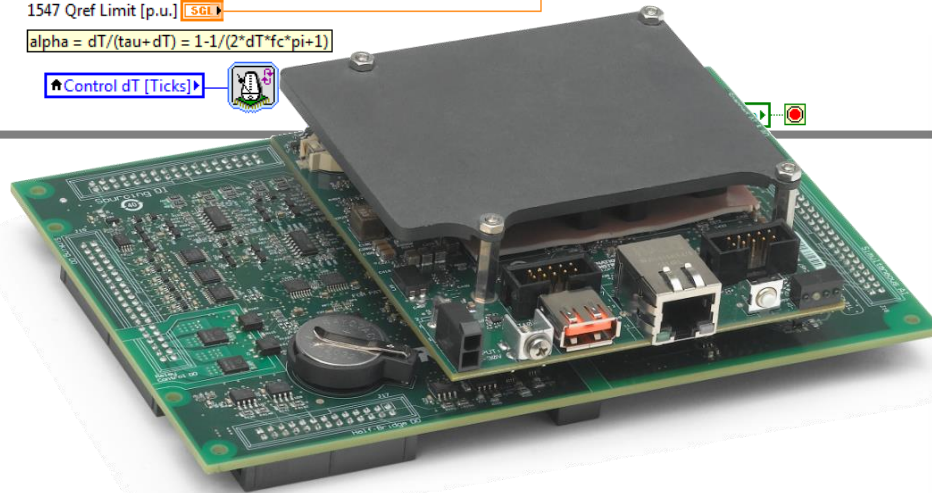
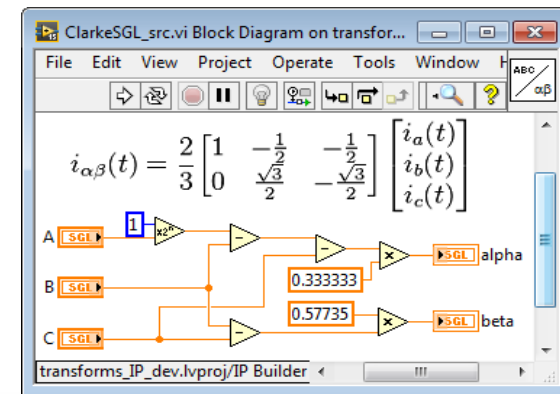
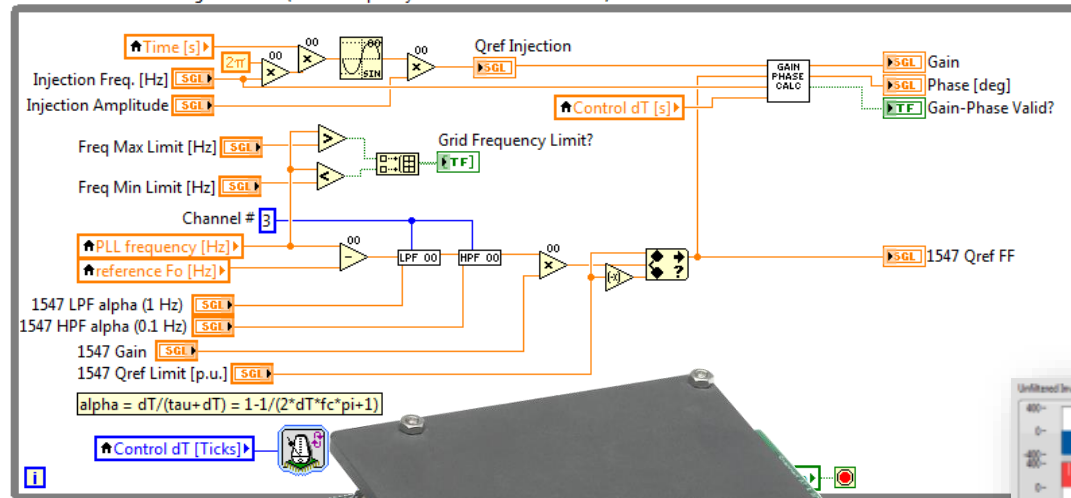
- 2 Main Power Grids
- 80 Microgrids
- 80 Distribution Lines
- 160 3-Phase Inverters
- 160 Energy Storage Converters
- 1280 IGBT/Diode Switches

SINGLE IGBT HALF-BRIDGE DATA (PHYSICAL MEASUREMENT vs. DIGITAL TWIN)



32 GB/s
Data Computed





NEXT STEP

JOIN THE DEVELOPER COMMUNITY AT
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