WBG Opportunities in PV Inverters Enabled by Superior Dynamic Performance

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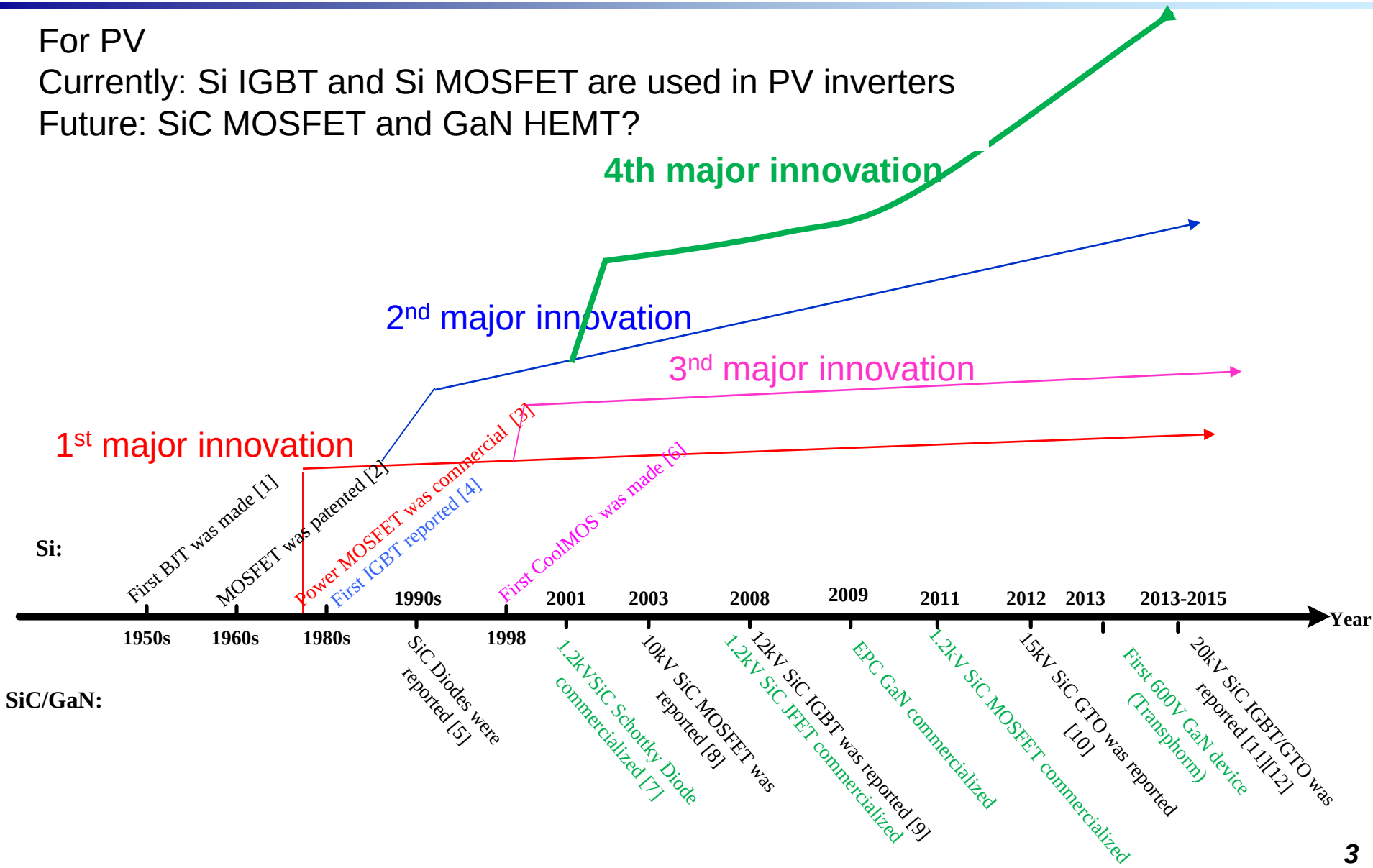
Presentation Outline

- WBG Device Performance: Possibility vs. Reality

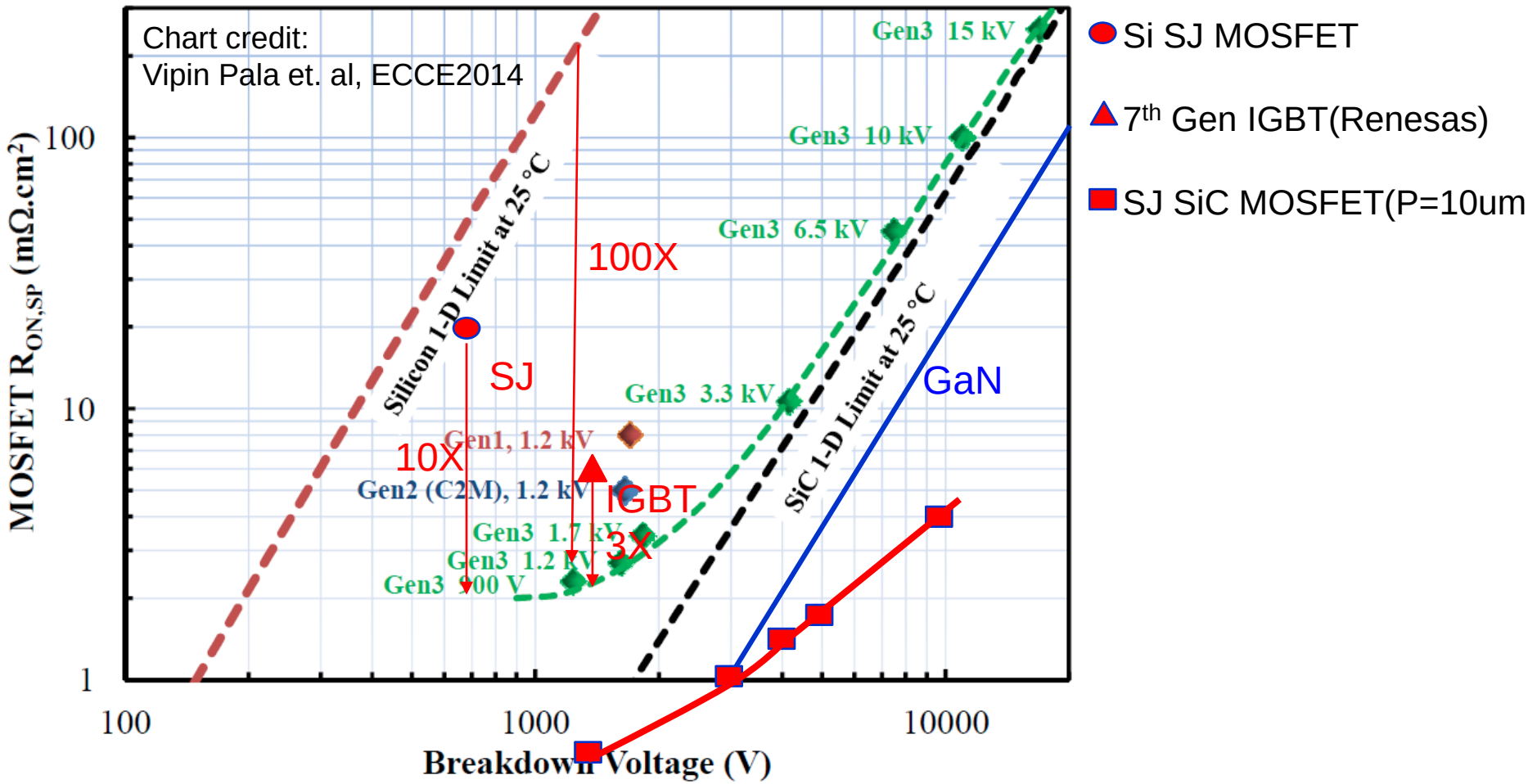
- WBG PV Inverter Adoption Strategies & Opportunities

Power Semiconductor Innovations

For PV
Currently: Si IGBT and Si MOSFET are used in PV inverters
Future: SiC MOSFET and GaN HEMT?

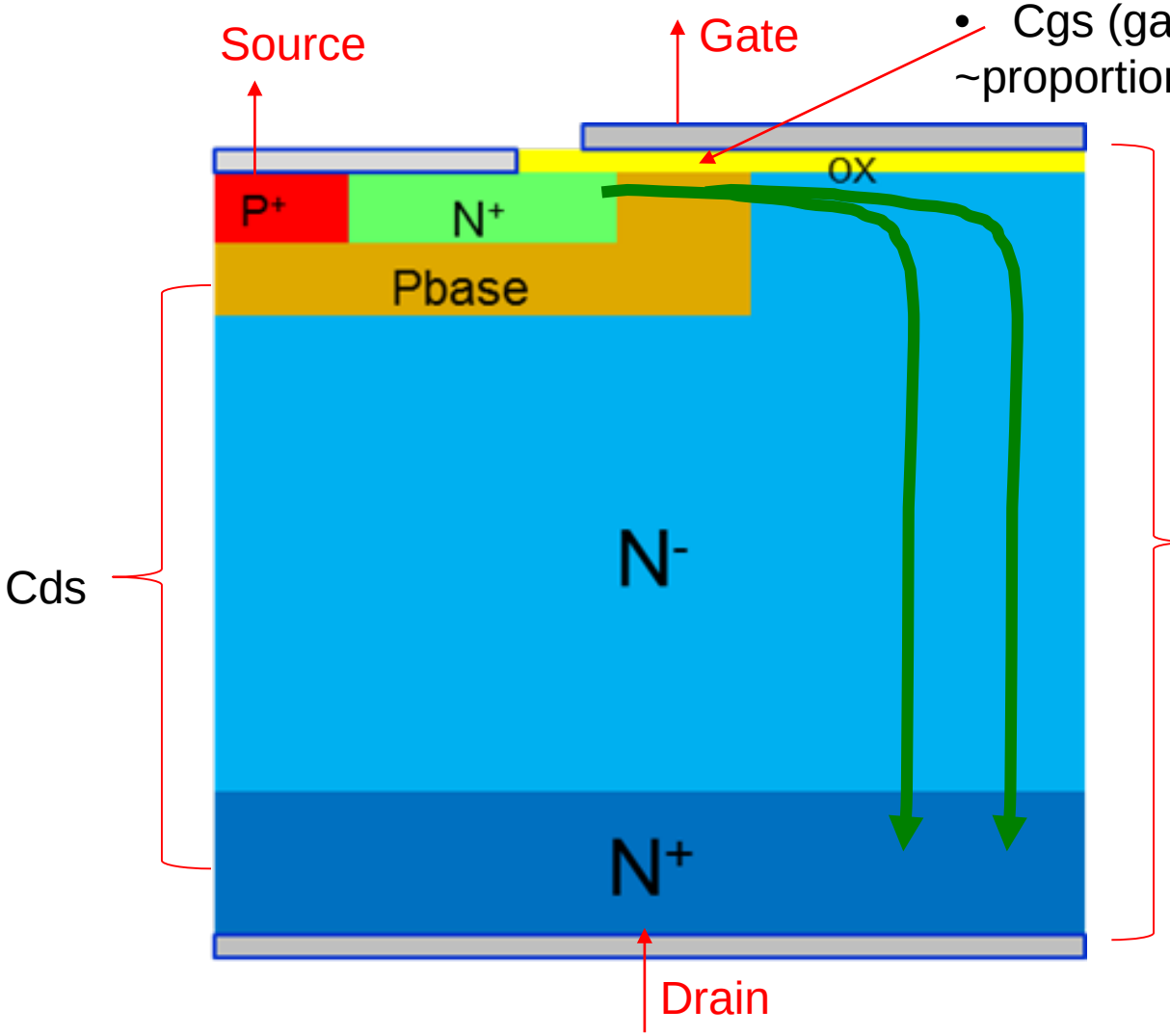


Conduction Loss: Current Status



- **Theoretically about 1000X reduction over Si MOS. Currently 100X reduction achieved @1200V. So another 10 time possible**
- **The improvement is only about 10X over SJ devices @600V! Only about 3X over advanced IGBT**
- **SiC roadmap: 1) Channel mobility improvement, 2) channel density (trench) 3) wafer thinning; 4) SJ SiC MOSFET, 5) large wafer size (e.g. 6 inch to 8 inch)**

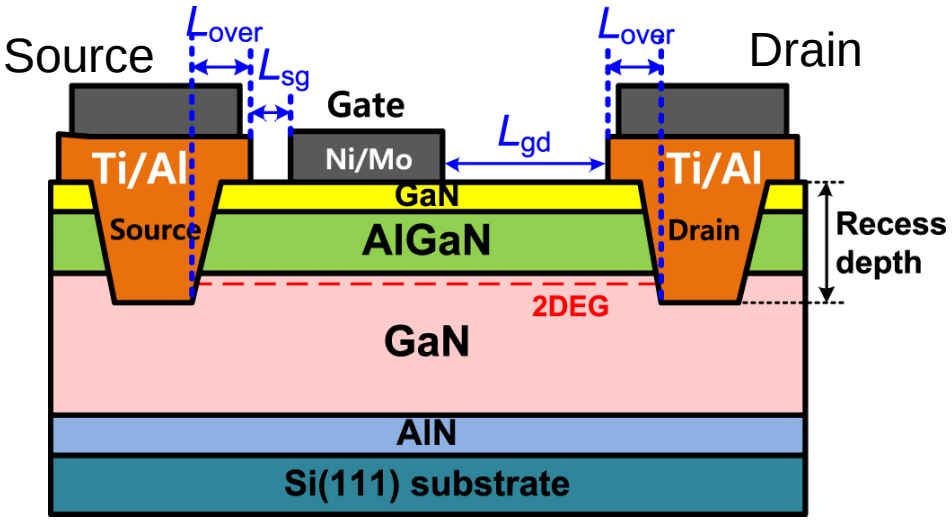
How about Device Capacitance?



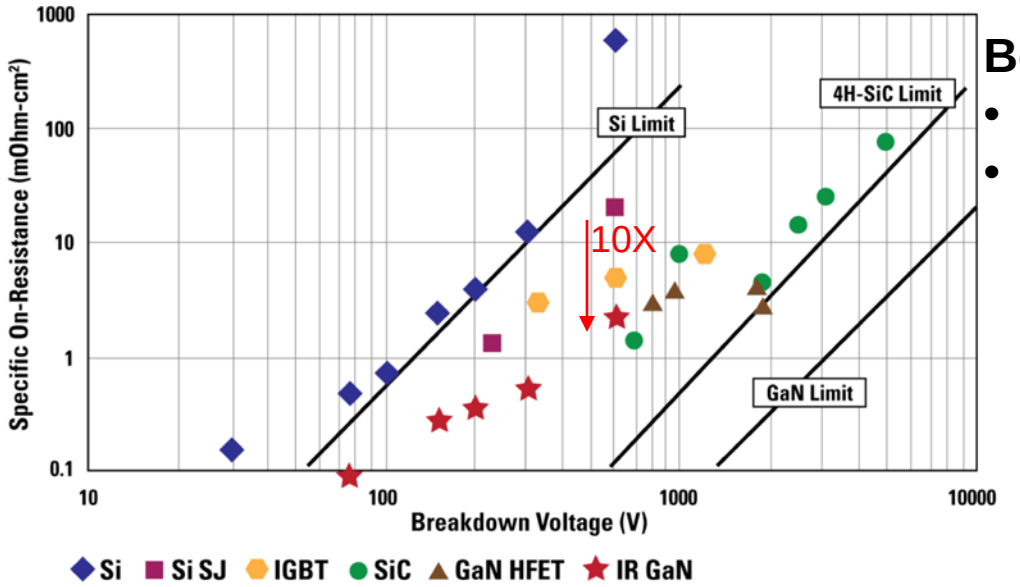
- Coss=Cds+Cgd
(Drain-Source & Drain-Gate)
Capacitance/per area
~ episilon*Ec
So ~10X increase in output capacitance

GaN: Lateral Device Construction

Smaller capacitance than vertical Device!!!



Comparison of R_{on} for Si, SiC, and GaN



Credit: International Rectifier

Bottomline:

- On Ron, not as good as vertical SiC
- But much lower capacitance!

A Closer Look at Ron, Capacitance

*Si SJ: Infineon IPW65R037C6
*SiC MOSFET: SCT2120AF from Rohm
*GaN HFET: GS66516T from GaNSystem

} 600V devices

	Ron (mohm)	Ciss (nF)	FOM 1 (Ron*Ciss)	Coss (nF)@400V	FOM2 (Ron*Coss)
Si SJ	37	7.24	267	0.38	14
SiC MOS	120	1.2	144	0.09	10.8
GaN HFET	25	.52	13	0.13	3.25

- Gate loop is getting faster
- Linearly proportional to die size

SiC has another 10X reduction potential/currently too low channel mobility

- Lateral device has further advantage

Drain loop
dV/dt etc will increase?

Turn-off dV/dt ~ I/C=J/C_{sp}

Turn-on dV/dt~Ig*Vdc/Qgd

Third Quadrant Operation & Diode Reverse Recovery: Cost & Performance

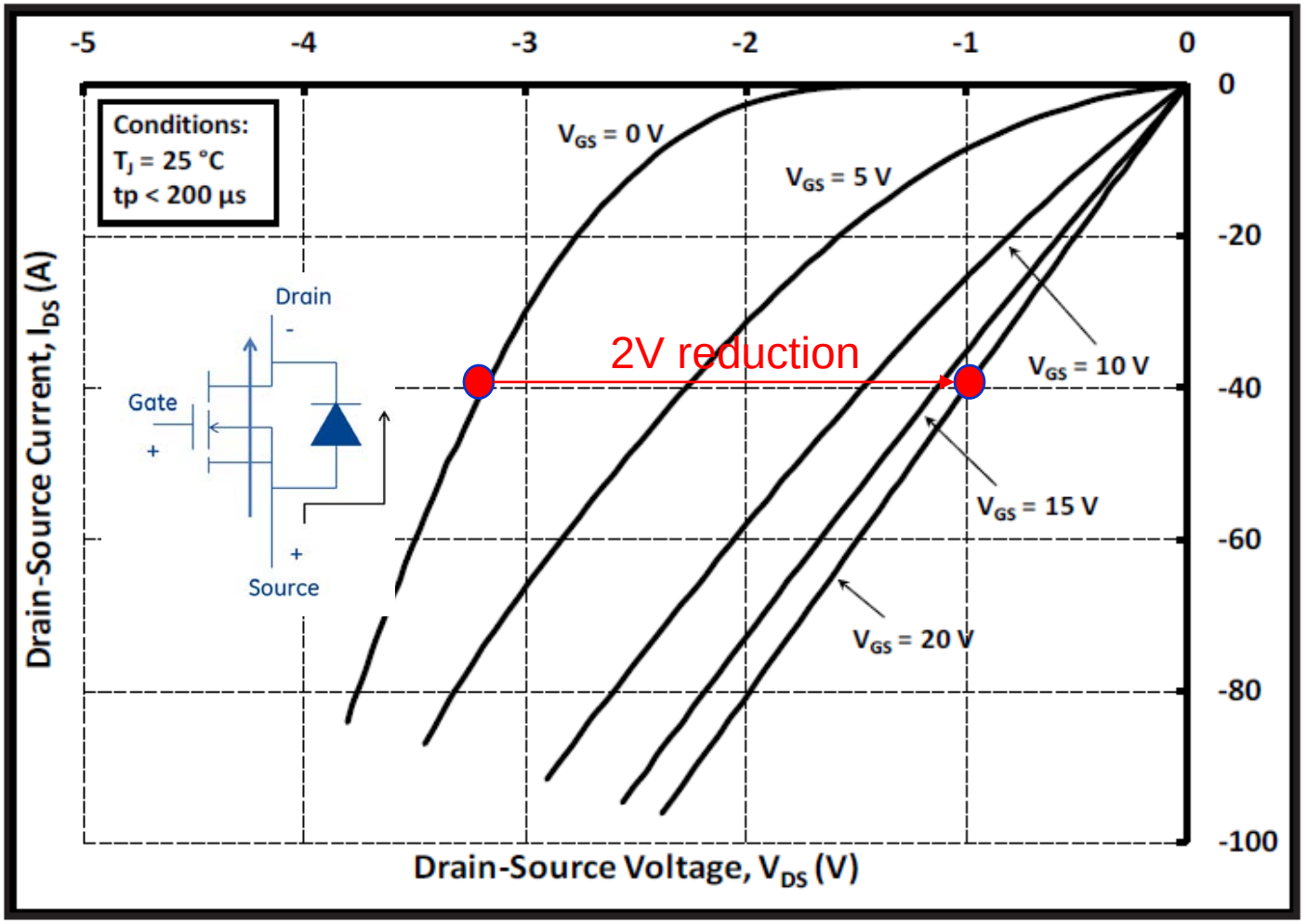
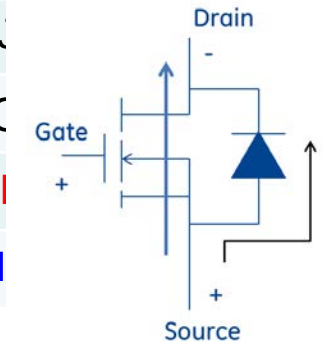


Figure 14. 3rd Quadrant Characteristic at 25 °C

Third Quadrant Operation & Diode Reverse Recovery: Cost & Performance

*Si SJ: Infineon IPW65R037C6
*Si 1200V FS-IGBT: Infineon IkW40N120T2
*SiC MOSFET: 1200V/25mohm Cree MOSFET
*GaN HFET: GS66516T from GaNSystem: 600V

	Ron (mohm)	Qrr (uC)	FOM (Ron*Qrr)
Si SJ		36	1332
Si IGBT		6.6	288
SiC MOSFET		0.406	10
GaN HFET		0.113	2.8



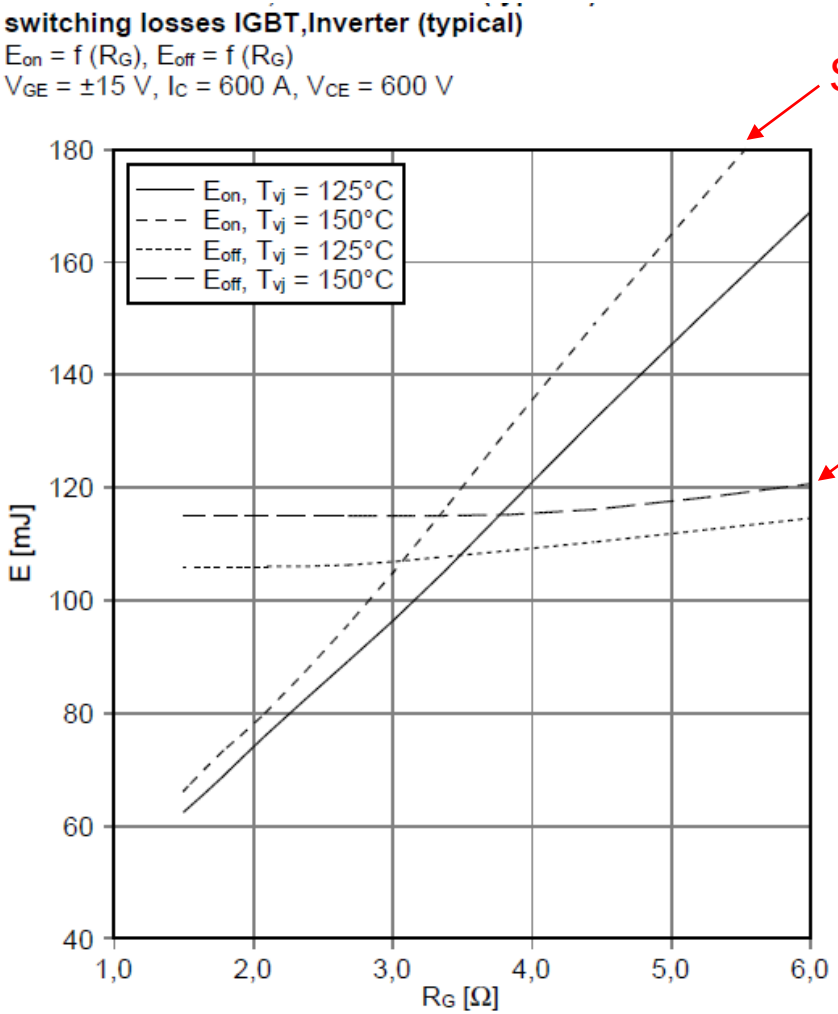
Entering an era where diode reverse recovery loss no longer a major concern

- Losses are dominantly capacitive loss Eoss dissipated on the switch!
- Stored energy in the diode is typically recovered during the next diode turn-on event
- SiC MOSFET operates as a synchronous rectifier further reduces diode conduction losses (smaller than JBS diode)

IGBT Dynamic Losses: Bipolar Current Conduction Physics

1200V/600A Infineon IGBT Module

Total US solar: 32 GW (2016), roughly 38 Mega-A if equivalent to 480VAC



Substantial Eon ~ 300 uJ/A

Substantial reduction to
8 uJ+2Eoss in Hard SW
0 in ZVS

Substantial Eoff ~ 200uJ/A

Substantial reduction to 0

Incremental reduction of this losses are possible as we move to 8th, 9th generation etc

WBG chip size reduction & gate loop

Gate loop quality factor: $$Qg = \frac{1}{R_{g,int}+R_{g,ext}+R_{driver}}\sqrt{\frac{L_g+L_s}{C_{isss}}}$$

Gate loop intrinsic speed: $$Sg = \frac{1}{\left(R_{g,int}+R_{g,ext}+R_{driver}\right)*Ciss}$$

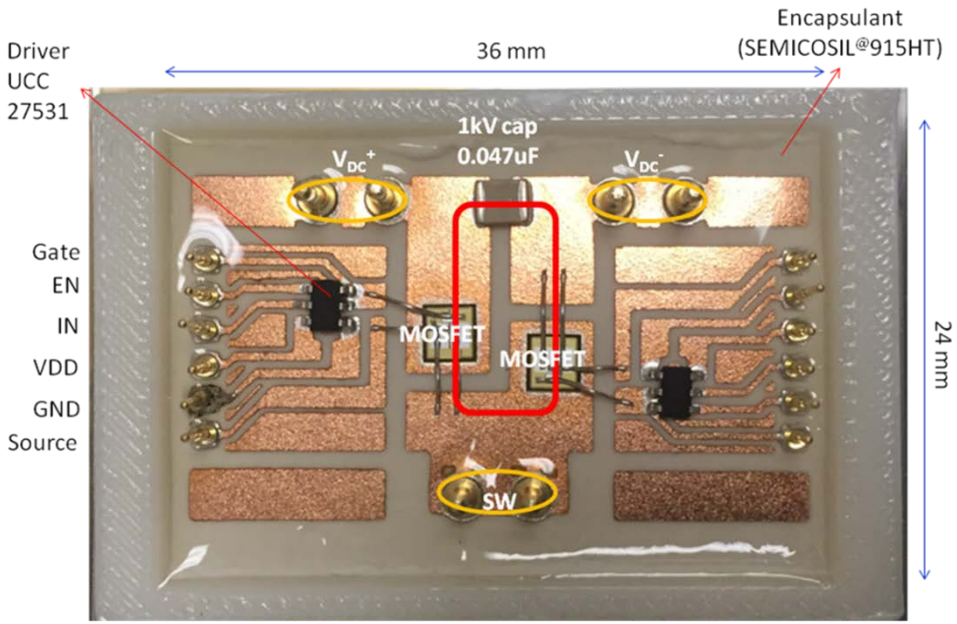
Gate loop figure of merit (GFOM): $$GFOM = \frac{Sg}{Qg} = \sqrt{\frac{1}{(Lg+Ls)*Ciss}} = \omega_g$$

Conclusion: Lg+Ls must be proportionally reduced for WBG devices to take advantage of the intrinsic speed of WBG devices.

Monolithic integration

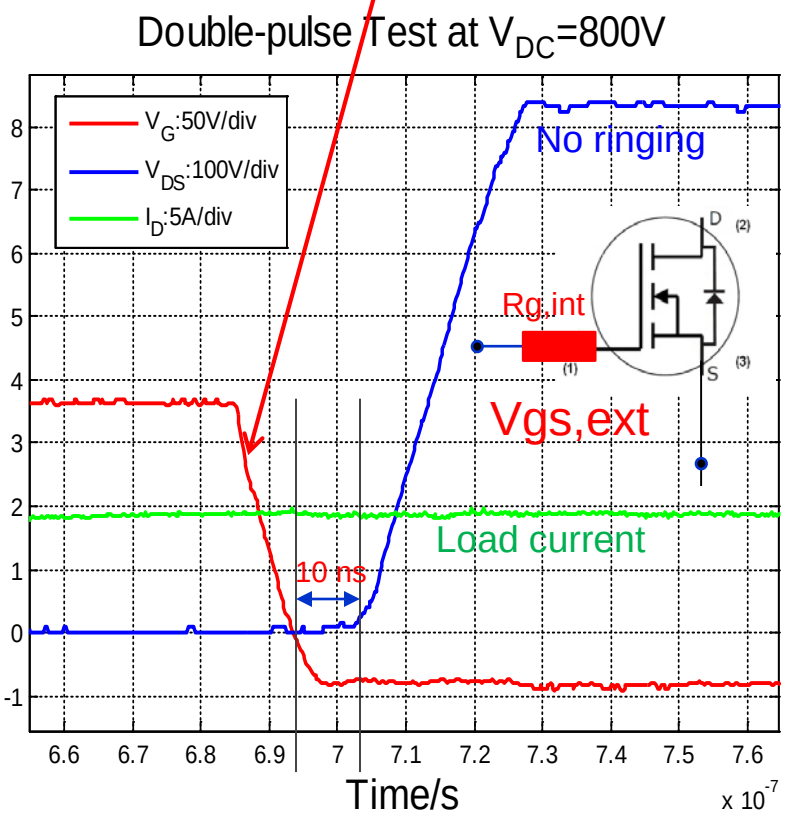
Multichip integration and packaging innovation

Hard-Driven MOSFET: Small Rg/Lg



SiC half-bridge module with ultra low parasitic inductance (Lg+Ls~1.5 nH, Rg,ext=0)

Measured external Vgs,ext
No current measurement possible

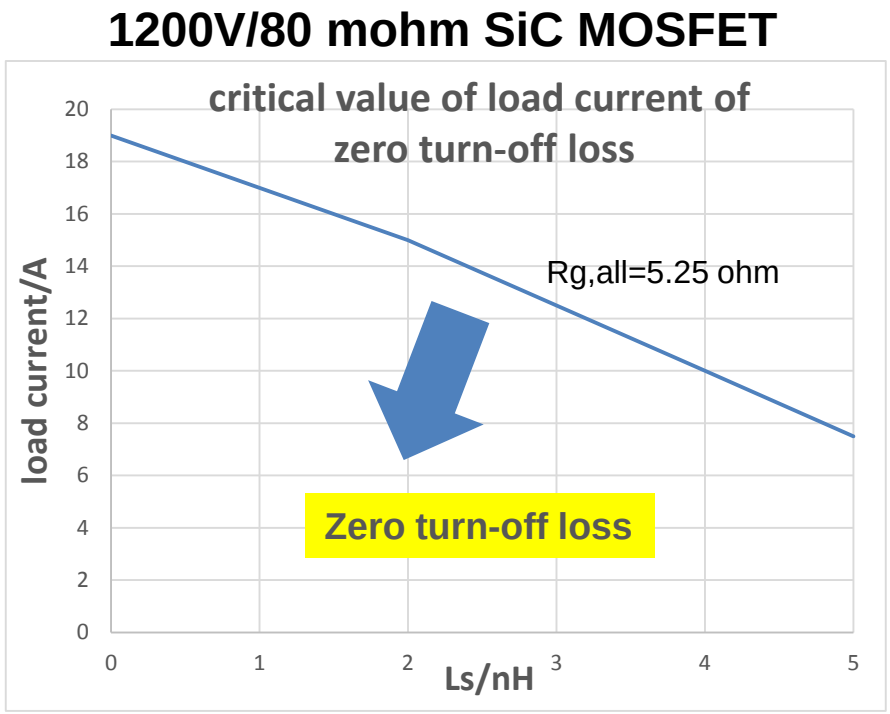


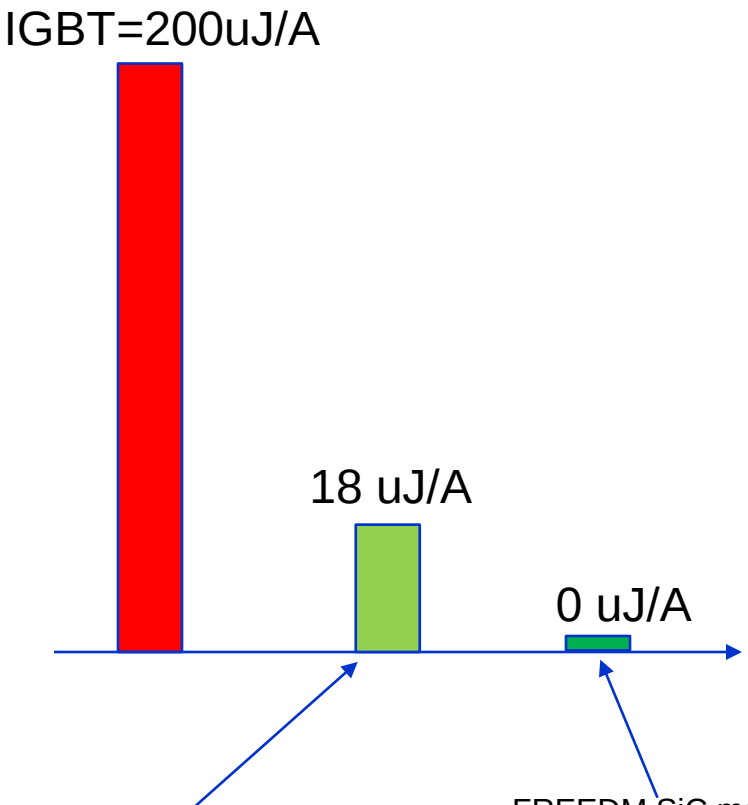
Zero turn-off loss (ZTL) can be achieved

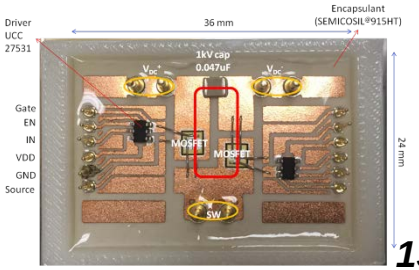
1200V/80mohm SiC Power MOSFET chips used

Ron	Rg, int	Qg	Qgp	Qgd	Qoss(equiv)
80 mohm	4.6 ohm	50 nC	10nC	20nC	80 nC@1kV

Zero Turn-off Loss (ZTL) Range

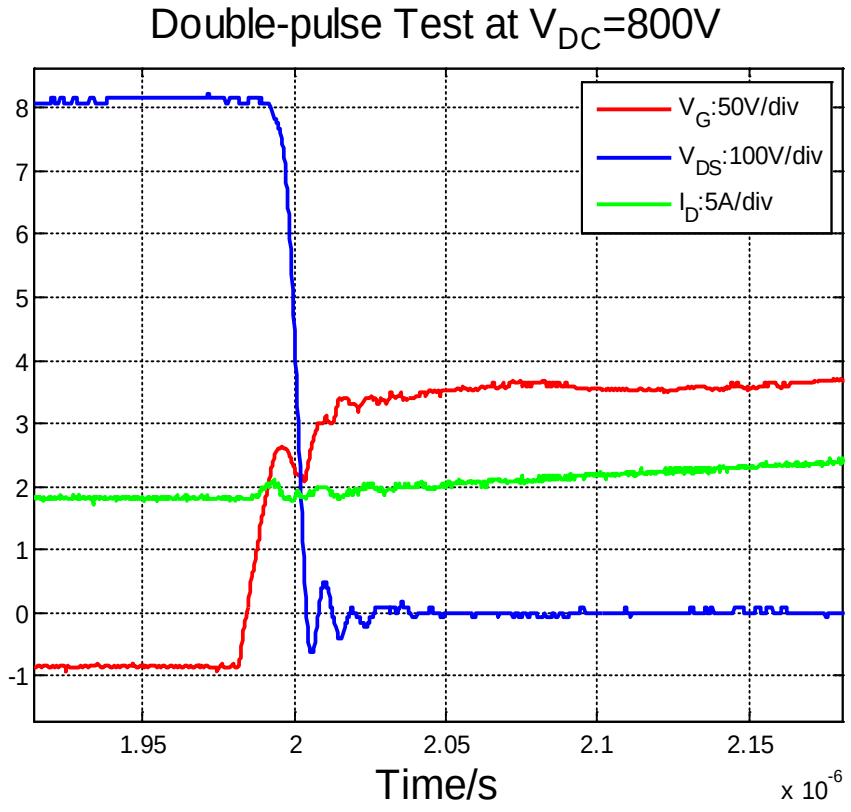


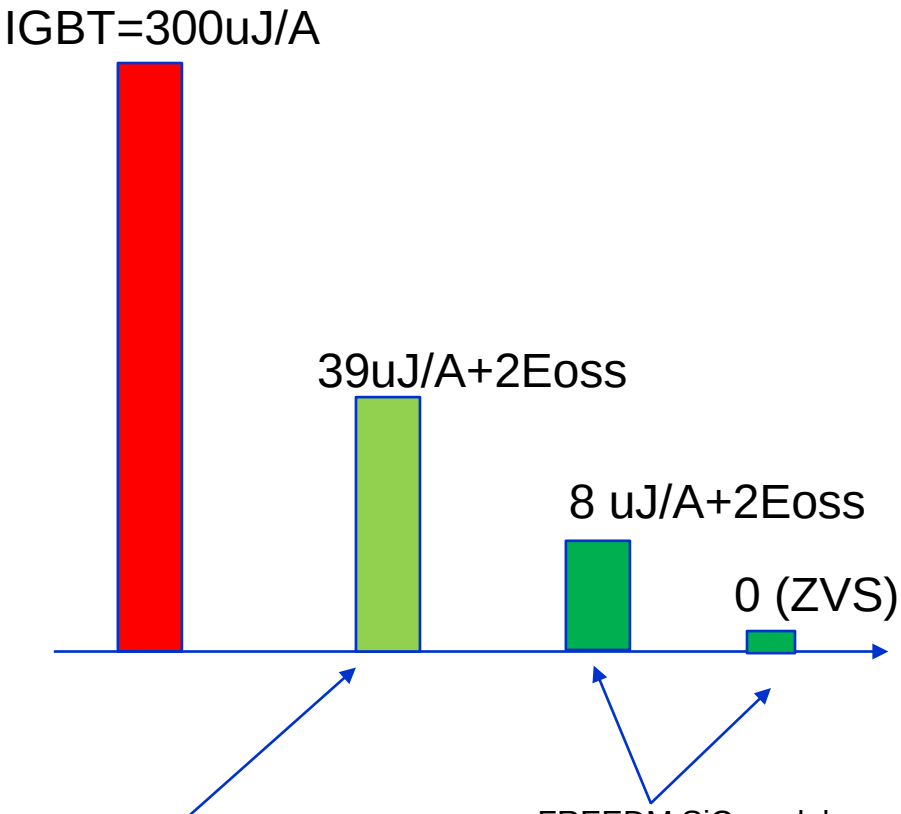




*Li and Huang at WIPDA 2015

Turn-on Process: Approaching Minimum Eon

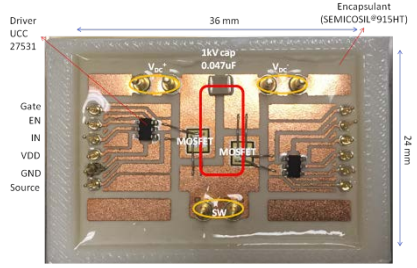




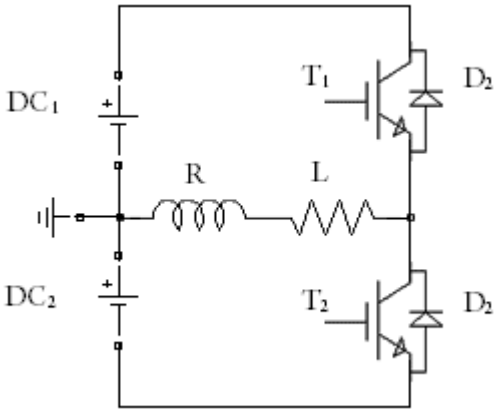
$$Eon = (2 + \frac{3 * I * Qgd}{2 * Igd * Qoss})Eoss$$

Cree SiC module

FREEDM SiC module

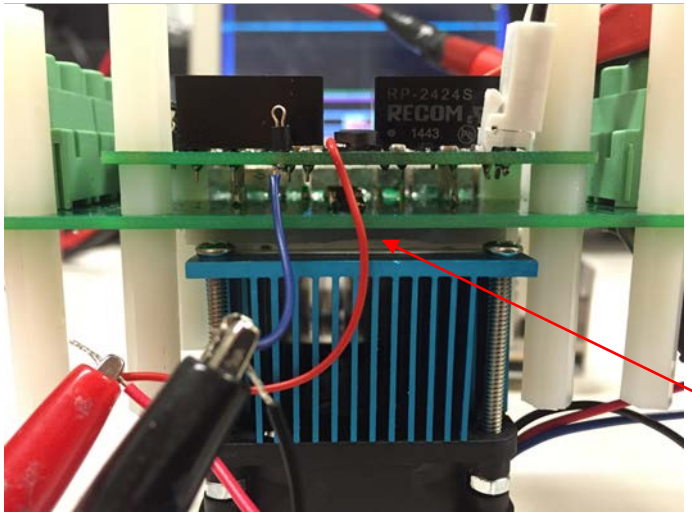


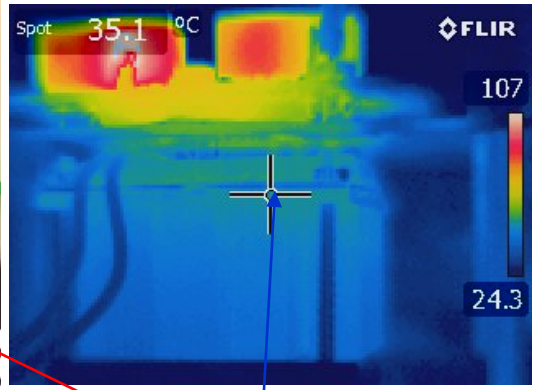
3.38 MHz operation of 1.2 kV SiC MOSFET (ZVS turn-on, ZTL turn-off)



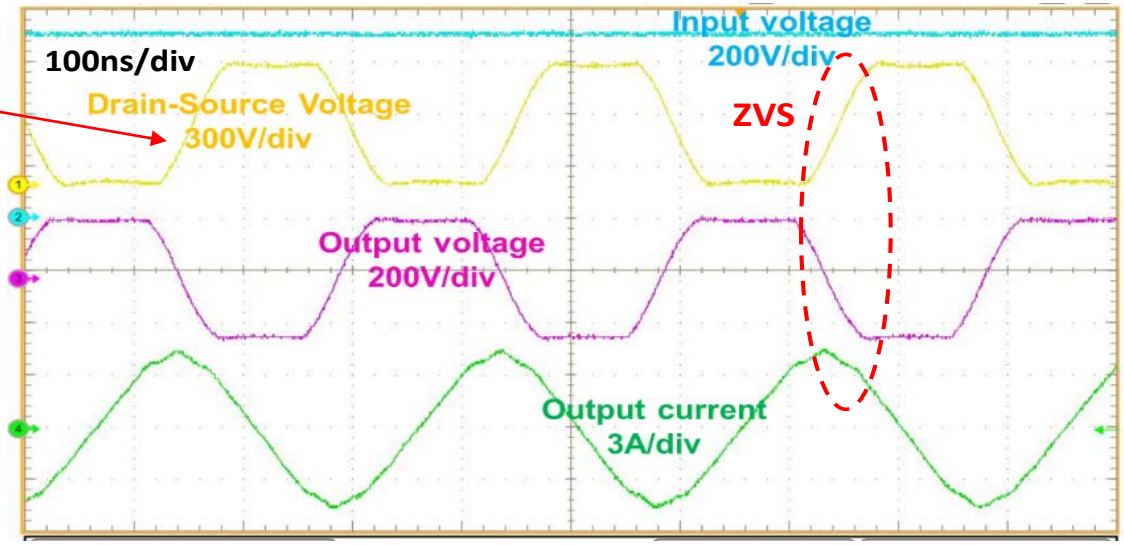
Vdc=700V, Ipeak=9.2A

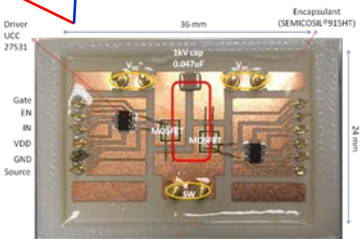
Side view of converter





Slower dV/dt





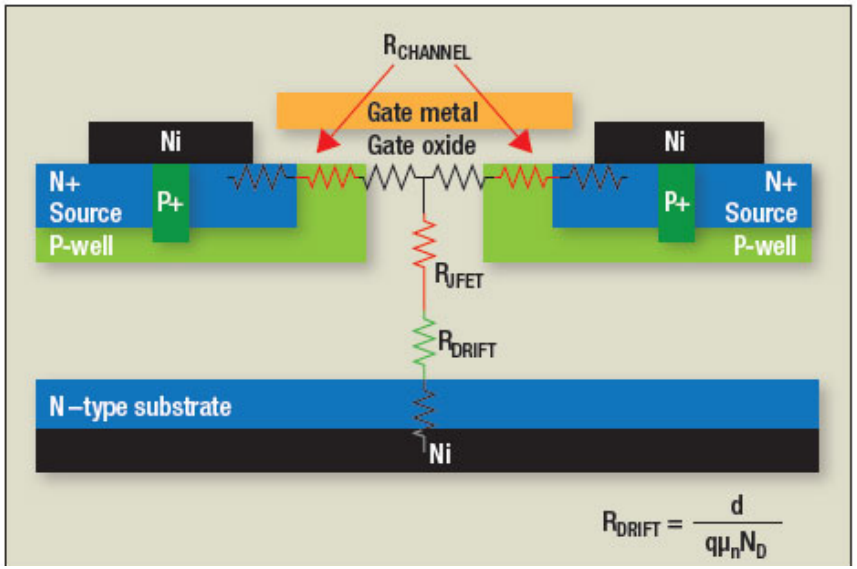
Estimated Tj=43°C

*Guo and Huang at WIPDA 2015

Demonstrated almost zero dynamic loss

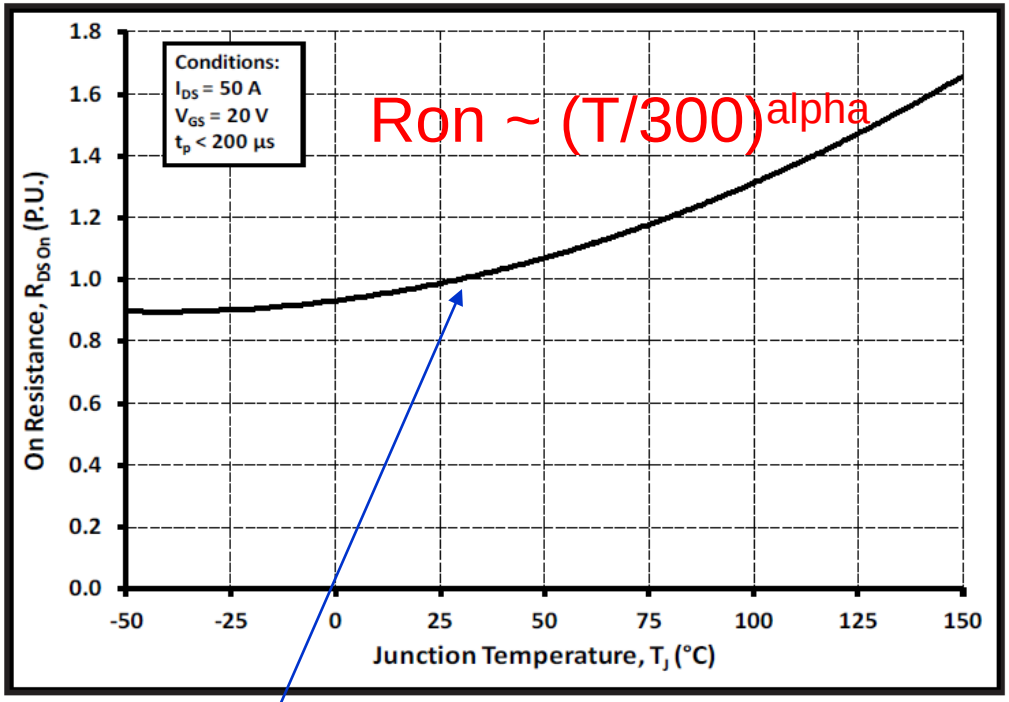
How about high Tjmax?

SiC MOSFET Cross Section



$$R_{ds(on)} = R_{CH} + R_{JFET} + R_D$$

NTC PTC



- **1200 SiC MOSFET: alpha=1.54 (this will go higher in the future when Rch is improved**
- **10 kV MOSFET: alpha =3.5**

SiC MOSFET: High Temperature?

$$P\max = \frac{Tj\max - Ta}{Rja} = I^2 R(T) = J^2 A^2 R(T)$$

$$R(T) = \frac{R_{sp0}}{A}\left(\frac{T}{T0}\right)^{\alpha}$$

Package determined

Heatsink determined

$$Rja = Rjc + Rca = \frac{K1}{A} + \frac{K2}{A}$$

$$J = \sqrt{\frac{Tj\max - Ta}{(K1+K2)}\frac{Ta^{\alpha}}{R_{sp0}Tj\max^{\alpha}}}$$

- Device reliability?
- Packaging Reliability?

Optimal Maximum Tjmax should be around ()

$$Tj\max, opt = \frac{\alpha}{\alpha - 1}Ta$$

>500C if alpha=1.54
191C if alpha=2.8
120C if alpha=3.5

WBG Adoption Strategies

- Residential:
  - SiC SBD/JBD in microinverter has been a reality for a number of years (**dynamic loss reduction**)
  - Next step might be the use of GaN in Mhz flyback/microinverters (**dynamic loss reduction, variable frequency CRM)**
  - Panel power increasing from 200W to >300W, need to increase power density

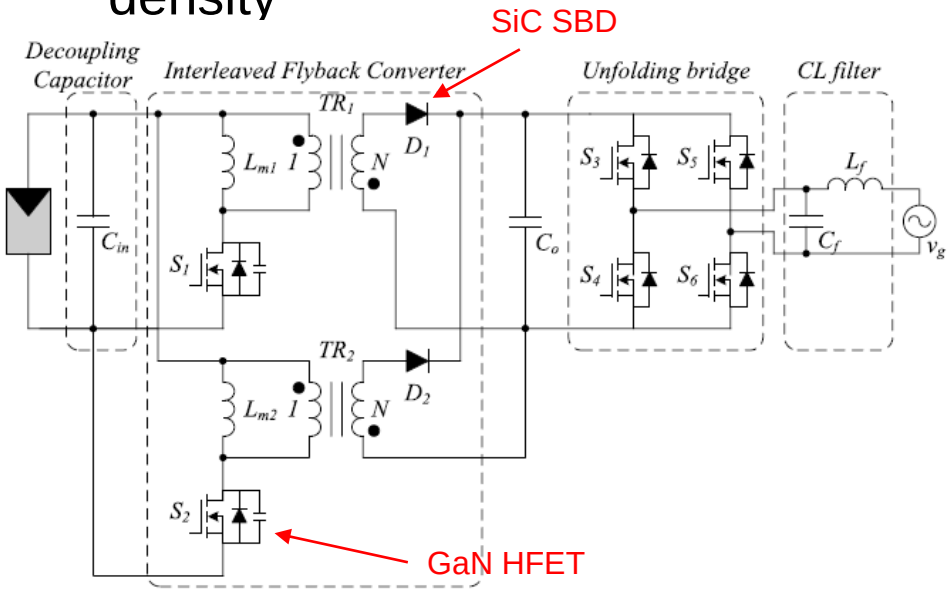


Fig. 1. Flyback micro-inverter for the PV application.

Fig 13: Prototype with thermal management employed during testing.

McLamara, Huang , APEC 2015

SunShot U.S. Department of Energy

Device Level Hybrid (I) for high power PV inverter

Fuji 1700V/400A hybrid module

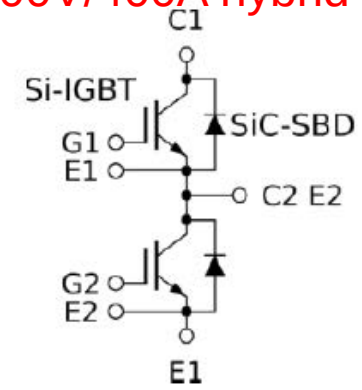
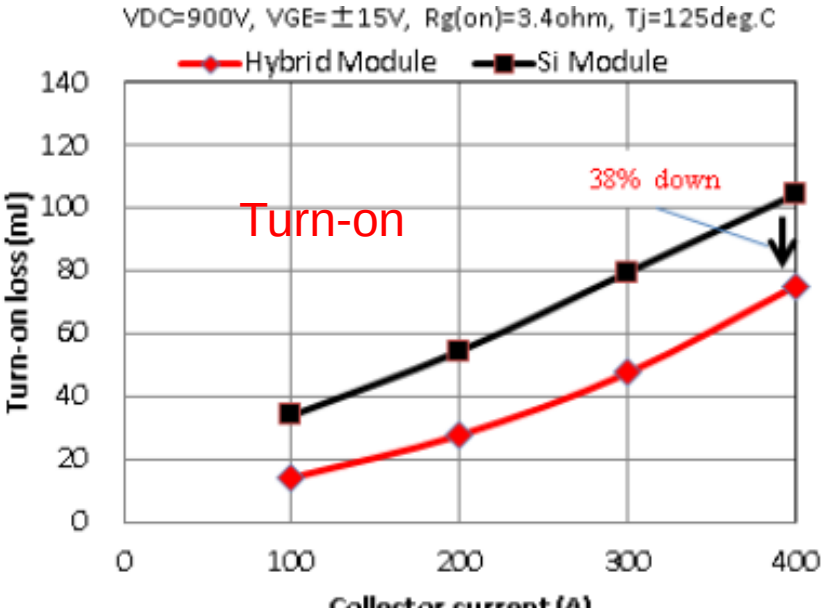
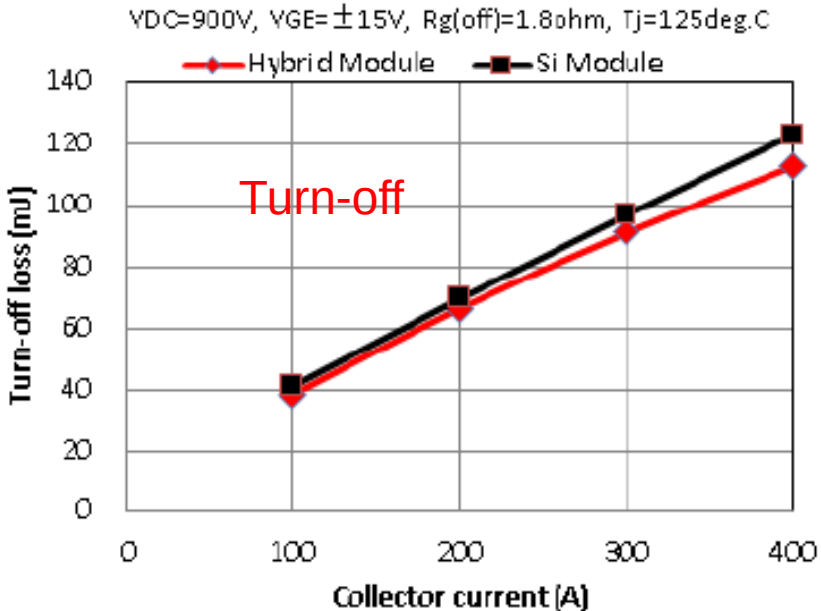


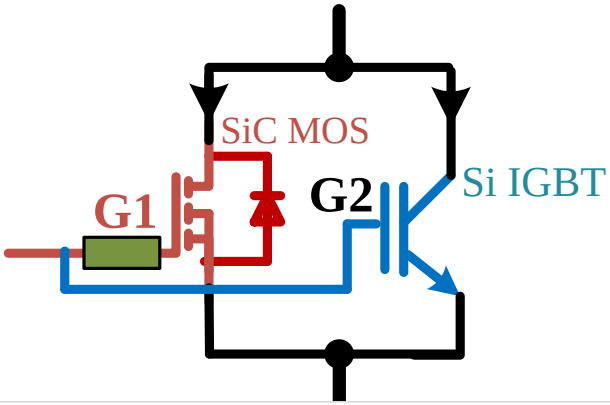
Fig. 1. 1700V/400A 2in1 hybrid module (W80mm x D110mm x H30mm)

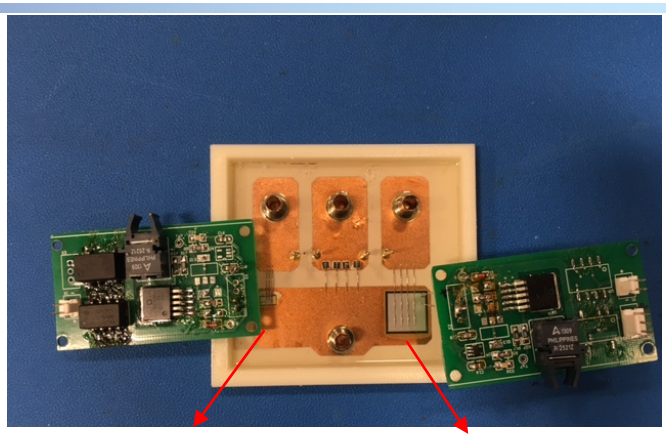




T. Takaku *et al*., "Development of 1700V hybrid module with Si-IGBT and SiC-SBD for high efficiency AC690V application,"
ECCE Asia (ICPE-ECCE Asia), Seoul, 2015, pp. 844-849.

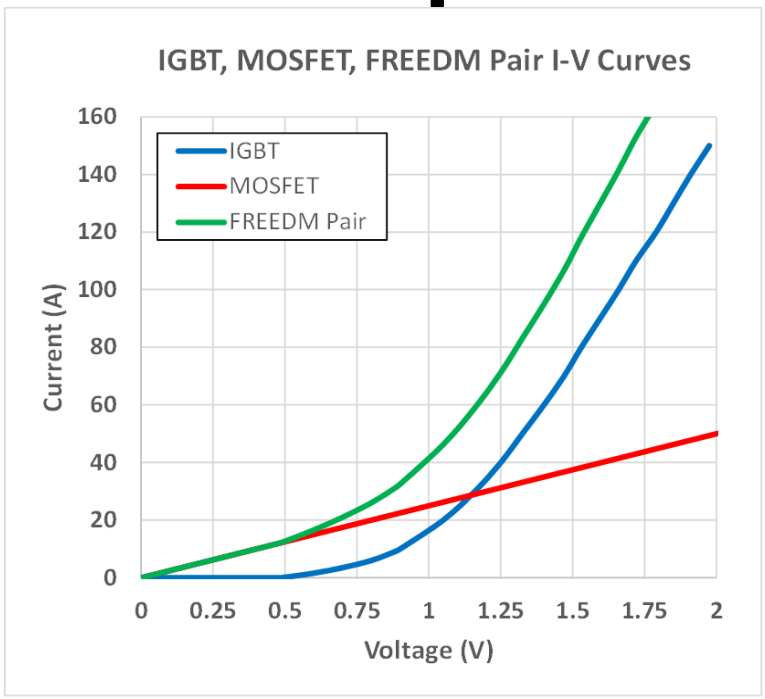
Device Level Hybrid (II)
1200V/200A FREEDM-Pair



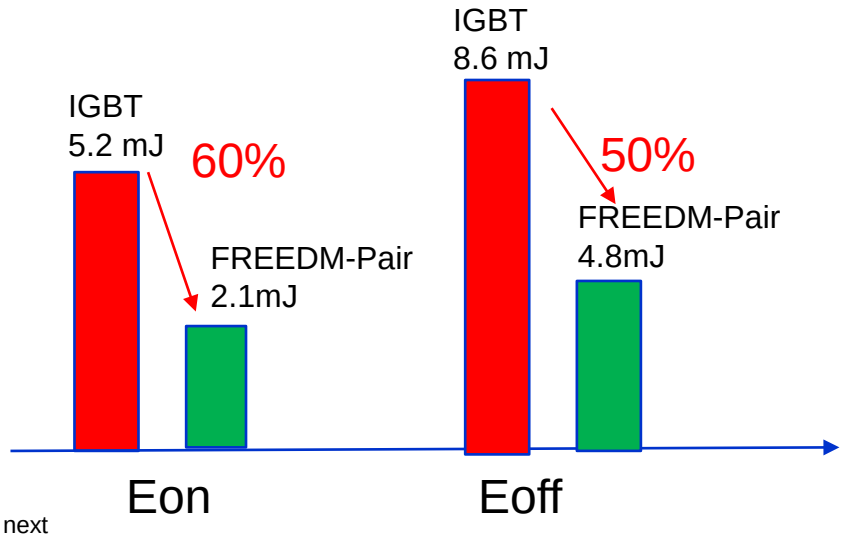


Wolfspeed 1.2kV/40mΩ
SiC MOSFET

ABB 1.2kV/150A
Si IGBT

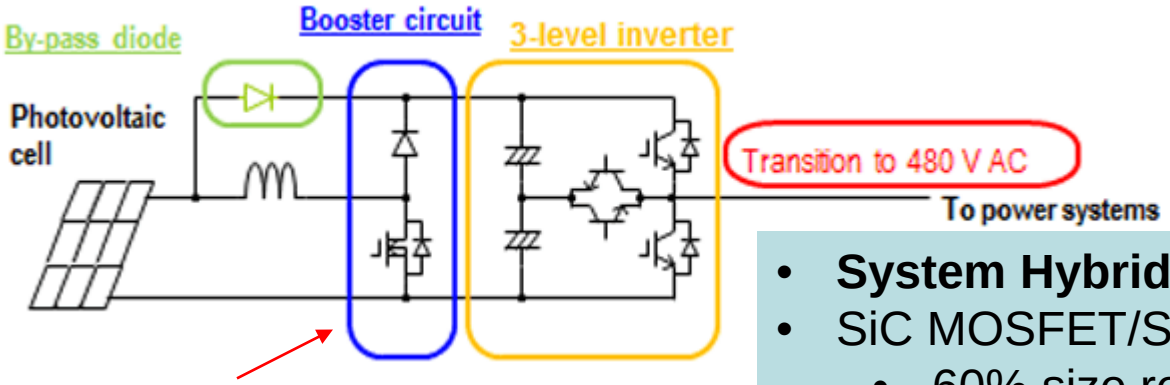


@600V/100A
Both tested with SiC SBD freewheeling diode



Huang, Alex Q.; Song, Xiaoqing; Zhang, Liqi, "6.5 kV Si/SiC hybrid power module: An ideal next step?," IWIPP, 2015 IEEE International Workshop on , vol., no., pp.64-67, 3-6 May 2015

System Level Hybrid

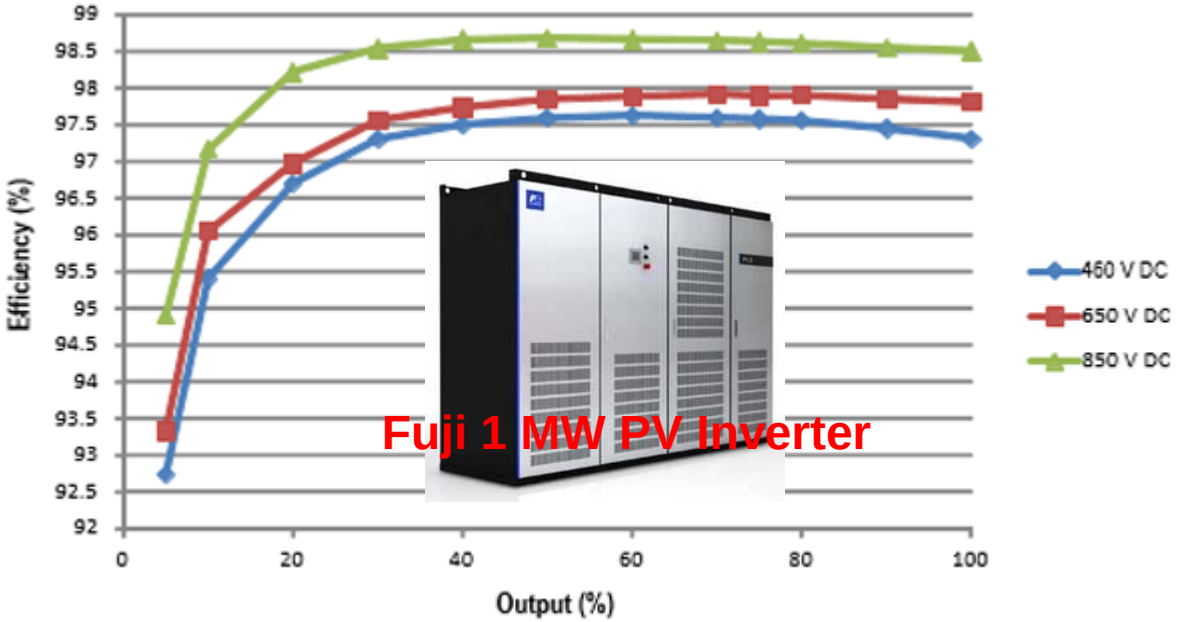


Fuji Electric

- **System Hybrid solution**
- SiC MOSFET/SBD used
  - 60% size reduction in boost converter
  - Utilizes MOSFET's SW loss
- 98.8% efficient

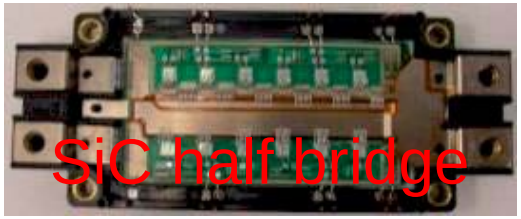
SiC MOSFET/SBD **IGBT**

83 kW boost

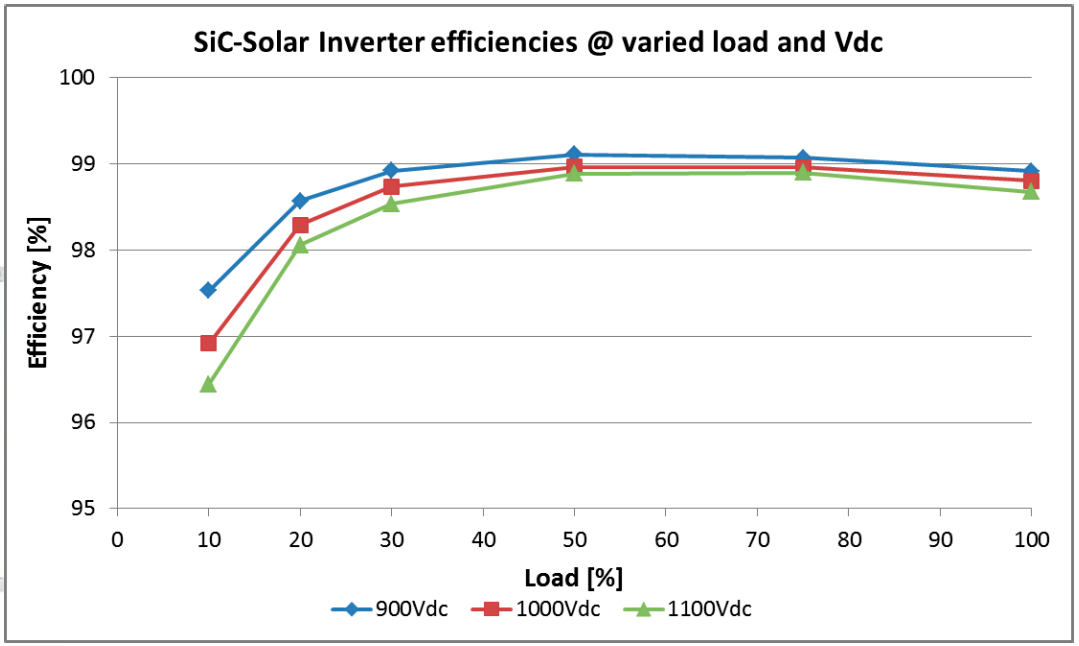


https://www.fujielectric.com/company/research_development/theme/sic_pcs.html

GE Pure SiC PV Inverter



- **1500 VDC PV Inverter**
- **1700V Full SiC MOSFET solution**
- Air cool system (cost and reliability)
- System cost ?
- **Annual energy production UP**

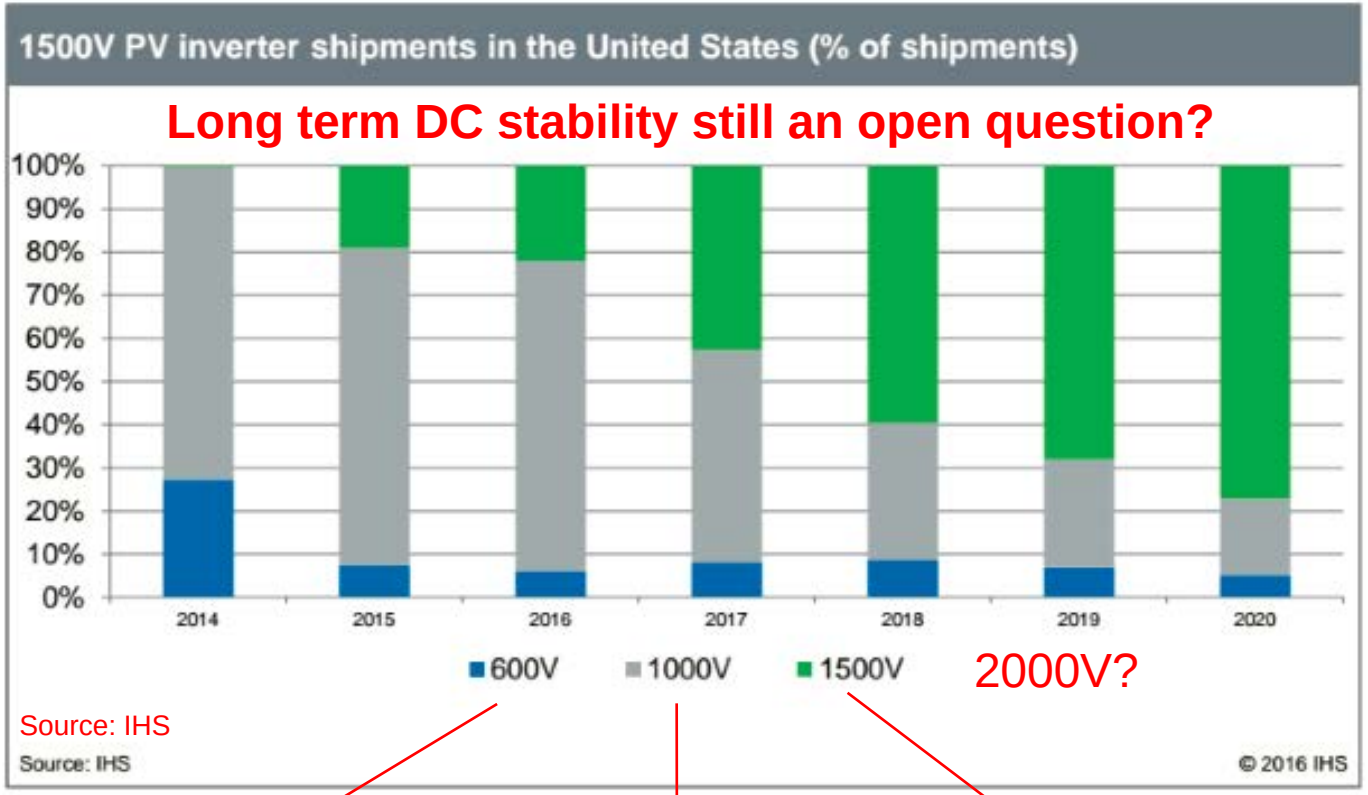


http://www.pv-tech.org/products/ges-advanced-silicon-carbide-technology-at-core-of-next-gen-1500-volt-centr

PV Inverter Opportunity: Customization of the voltage class

Three trends in the global PV inverter market that are impacting the United States in 2016

Drive to reduce PV system costs will accelerate demand for 1500V technology



MPPT voltage<600V

900V SiC Devices

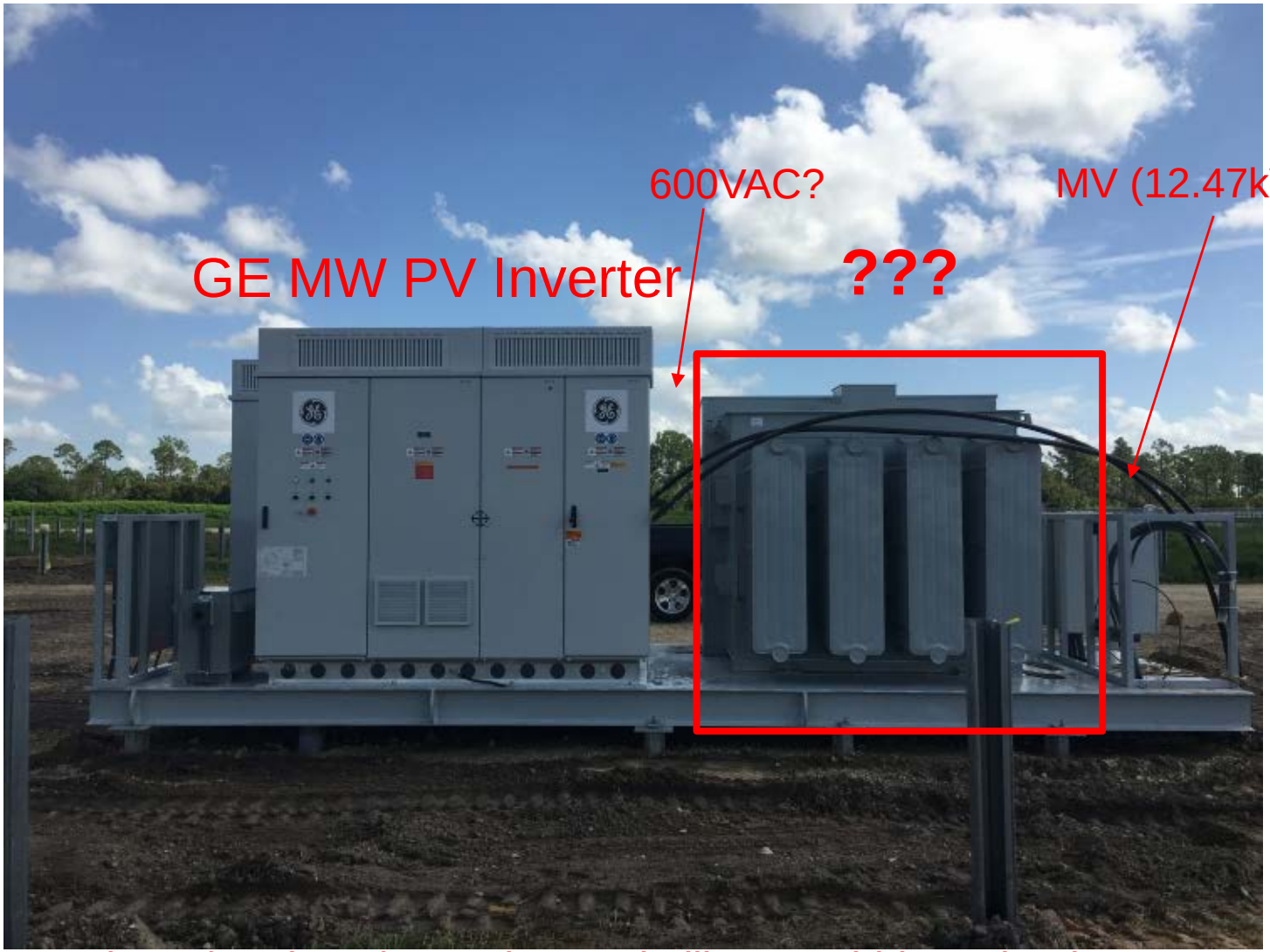
MPPT voltage=850

1200V SiC devices

MPPT voltage~1300

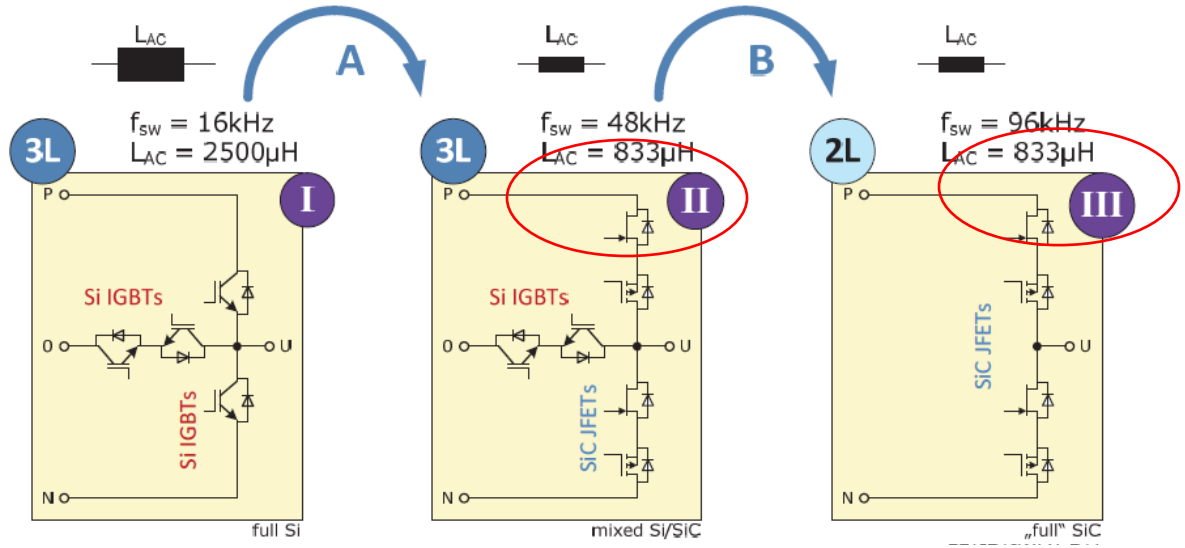
1700V SiC devices?

MV PV Inverter ?



http://www.pv-tech.org/products/ges-advanced-silicon-carbide-technology-at-core-of-next-gen-1500-volt-centr

Topology Simplification and System Cost Reduction



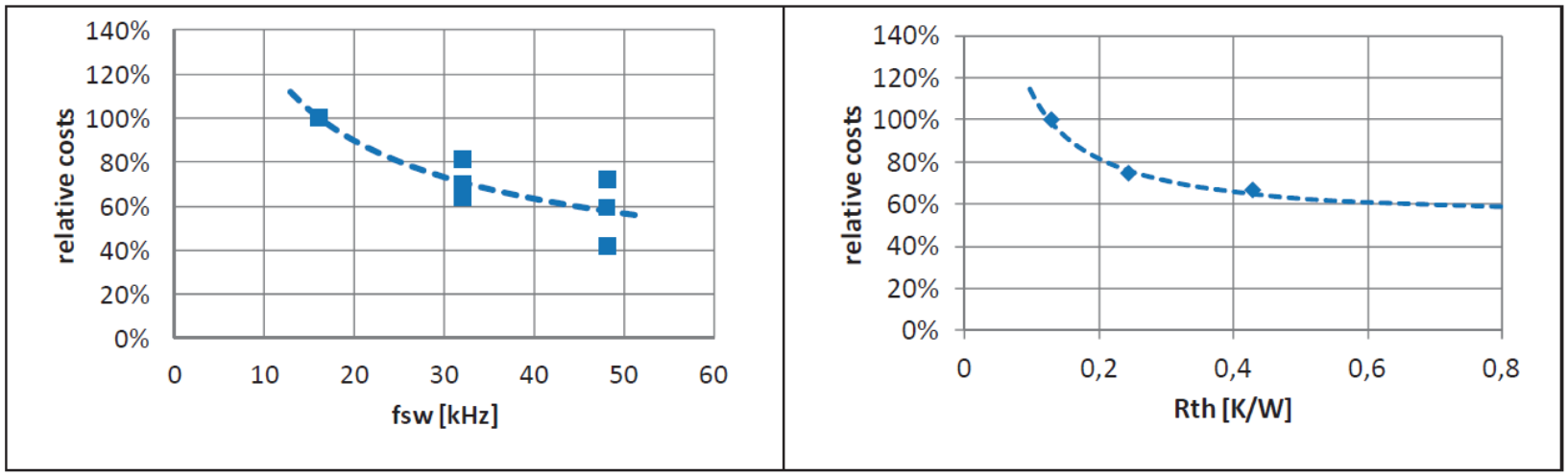
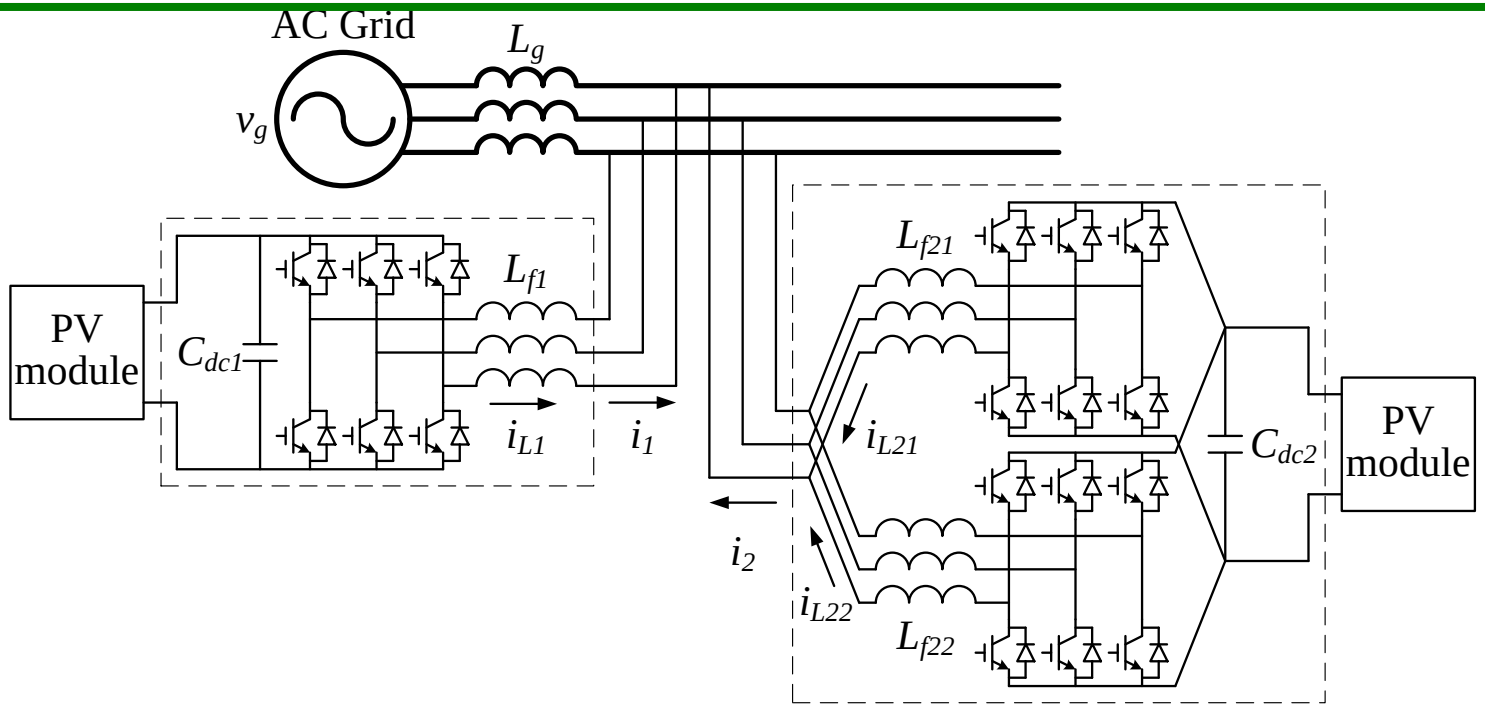
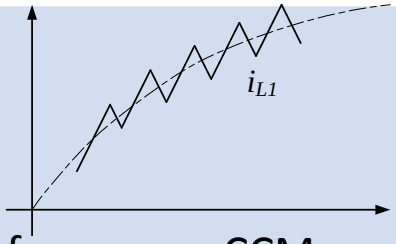
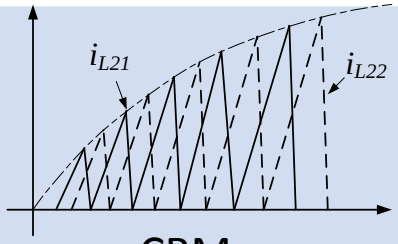


Fig. 4: System costs of magnetic components (left) and heat sink (right) as functions of technical performance.

*Ulrich Schwarzer et. al, "System Benefits fopr Solar Inverter using SiC Semiconductor Modules", in PCIM 2014

Mhz PV Inverter Opportunity: Filter Reduction



Single inverter	Interleaved inverter
 constant frequency, CCM	 variable frequency, CRM
hard switching	**ZVS/lower EMI**
large filter inductor: (10kW/240Vac/10kHz) 0.8mH/50A; e.g. 5.2 inches Kool Mμ toroid	small filter inductors: substantial reduction by increasing f and operate in CRM!

WBG Adoption Strategies

- Long term: Die size shrinking/wafer scaling (**device cost reduction**) potential is huge for GaN and SiC
  - SiC:
    - 6 inch to 8 inch
    - Channel mobility improvement
    - Wafer thinning
  - GaN:
    - 8 inch to ?? Inch
    - Optimal drift length design
- Moving from bipolar device (IGBT) to unipolar device (SiC MOSFET, SJ SiC MOSFET, GaN HEMT) with smaller die size
  - Significantly better dynamic performance than Si, hence is the most important factor in driving PE applications **for system cost reduction**
  - In ZVS circuits, f is a variable that can change from 10 kHz to 10 Mhz
- Adoption focuses on performance improvement at acceptable cost
  - **Hybrid device/system**

FREEDM systems center

Thank You