Additively Manufactured Photovoltaic Inverter (AMPVI)

Prime: National Renewable Energy Laboratory

Principal Investigator: Dr. Sudipta Chakraborty

Contributors:
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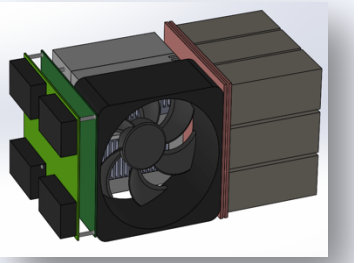

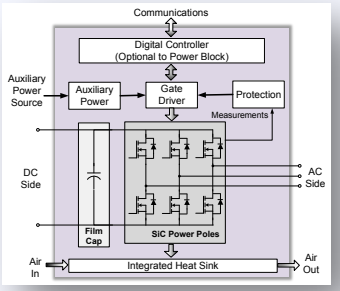

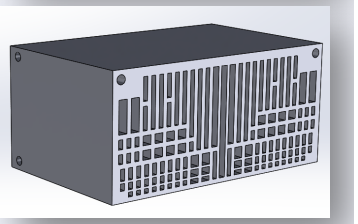

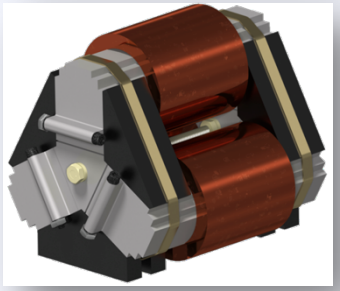

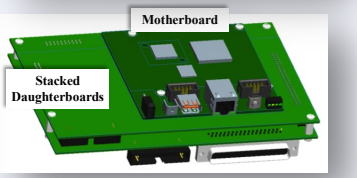

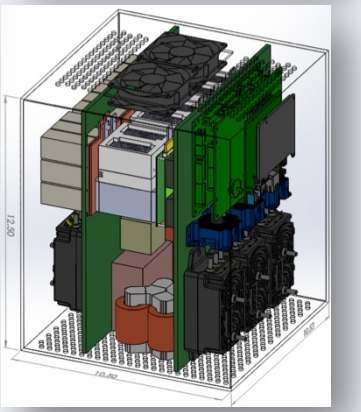

Presented at ***DOE workshop on Enabling High-Penetration Solar PV through Next-Generation Power Electronic Technologies***
Golden, CO
October 11, 2016

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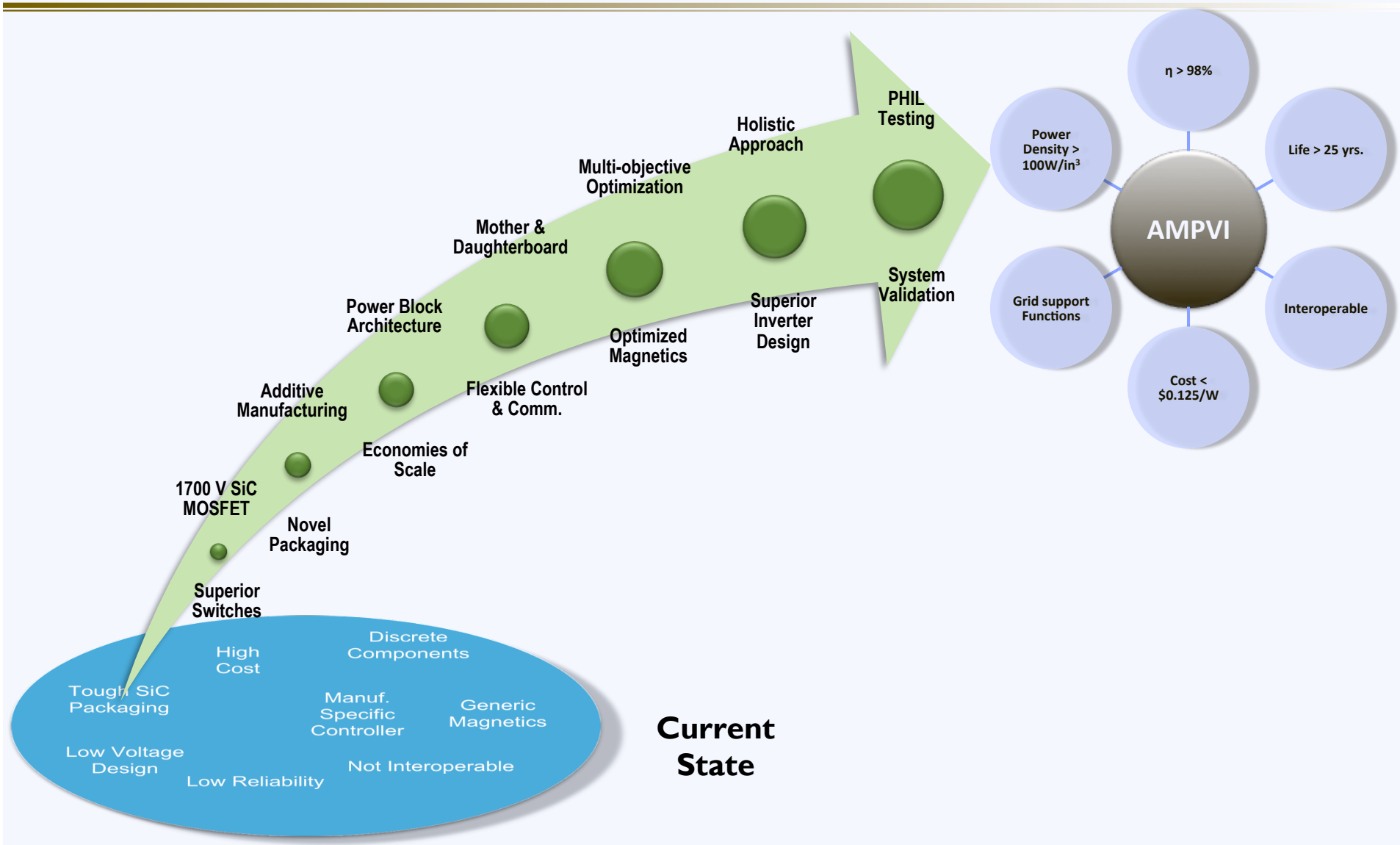
Project Objective

- To enable integration of hundreds of GWs of solar generation to the U.S. electric power system, this project will develop a unique PV inverter design that combines high-voltage Silicon Carbide (SiC) with revolutionary concepts such as additive manufacturing and multi-objective magnetic design optimization
- The final deliverables from the project will include:
  a) High power density (>100W/in^3), high efficiency (>98%) power block and 50 kW prototype inverter
  b) Additive manufacturing techniques for power block and heat sink
  c) Magnetic design optimization tool
  d) A versatile controller
  e) Standard HIL inverter testing techniques
  f) Cost and reliability analysis of SiC based PV inverter

SunShot PE Target Metrics

Power Electronics Target Metrics	
Attribute	**Target Metric[18]**
Conversion Efficiency: Defined as the ratio of the usable output power (AC or DC) versus available input power from the PV panels. Typically, the PV inverters in the U.S. are tested to the CEC (California Energy Commission) efficiency using a weighted formula[19]	> 98%
Service Life and Reliability: Defined as the useful life of the power electronic subsystems to support the required plant availability under normal operation and maintenance	> 25 years[20]
Power Density: Defined as the ratio of rated output power versus device volume and weight.	> 100 W/in^3 for residential and small commercial systems
System Cost: Defined as the lifetime cost of the power electronic device, including initial capital cost and the operation and maintenance (O&M) cost over the service life.	< $0.10/W, utility scale < $0.125/W, commercial scale < $0.15/W, residential scale
Grid-Support Functions: **These include a host of smart inverter functions such as volt/var, volt/watt, frequency/watt, voltage ride-through, power factor control, reactive power support, ramp rate control, and so on. These functions can be activated either autonomously through default settings or remotely through utility SCADA commands.**	Compliance with ANSI, IEEE, and NERC standards[21,22,23]
Interoperability: Defined as the capability of the power electronic devices to exchange and readily use information—securely, effectively with other system components.	Compliance with Open Standards which include SunSpec Modbus, Smart Energy Profile (SEP 2), IEC 61850, MultiSpeak, and DNP3

Project Technical Approach



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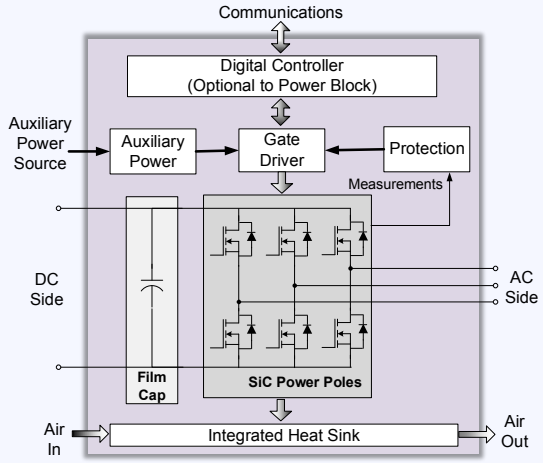
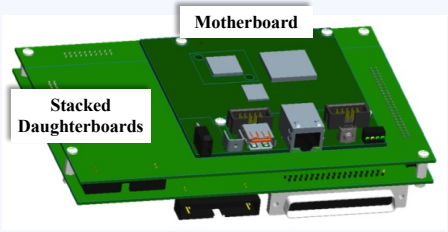
Project Technical Approach

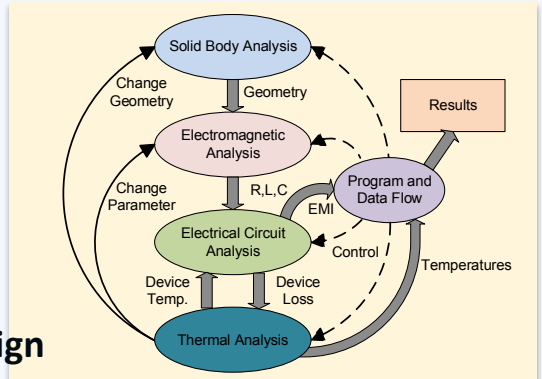
Topology



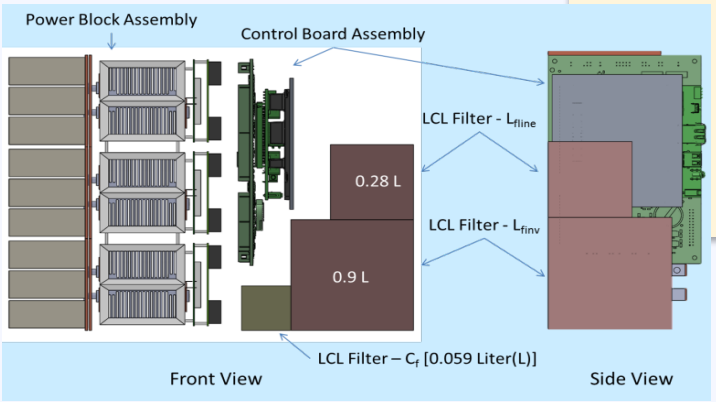
Controller

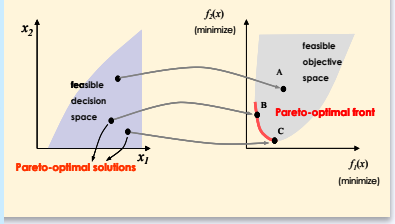


Magnetic Design

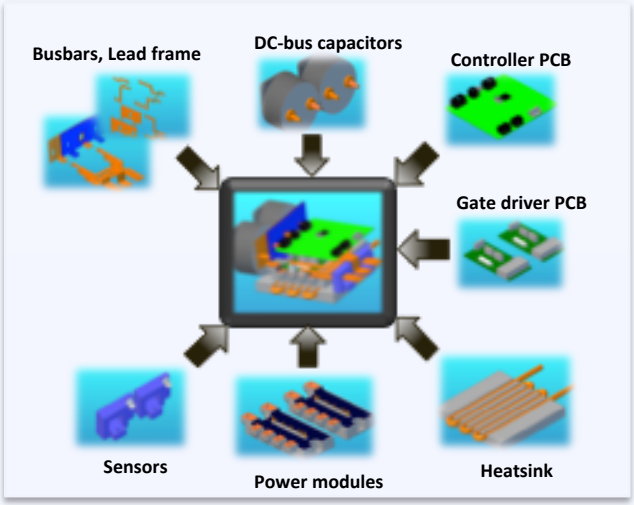


Thermal and Mechanical Design

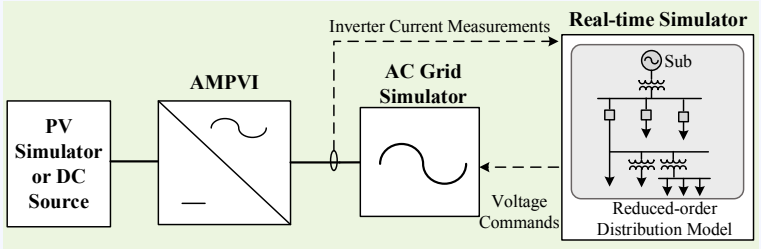




AM-based Power Block



System-level Validation



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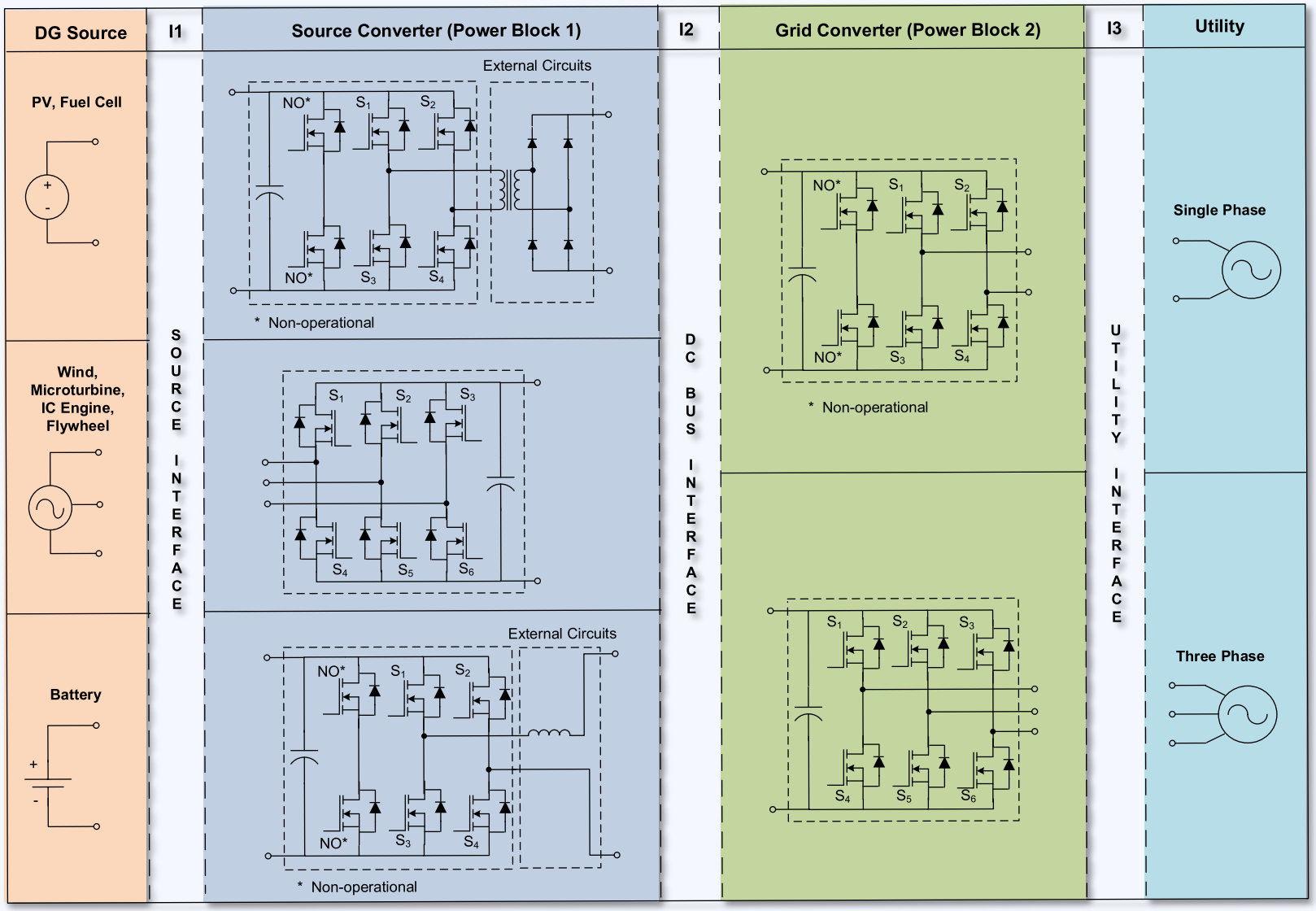
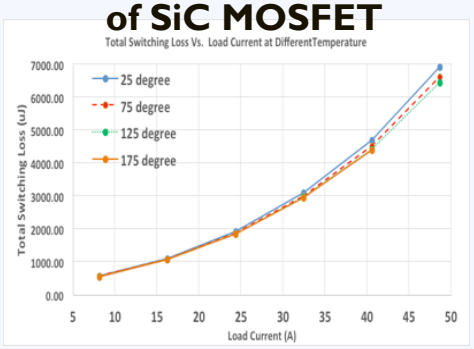
Economies of Scale

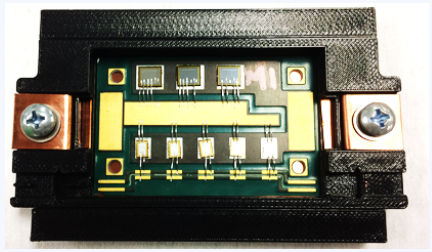


AM-based Power Block with 1700V SiC MOSFETs and Diodes

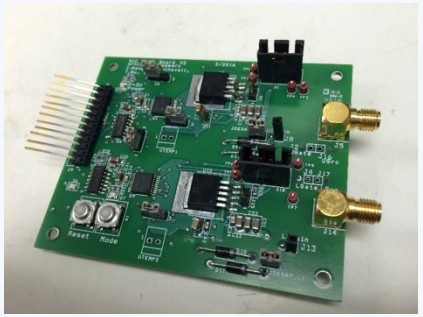
Dynamic Characterization of SiC MOSFET



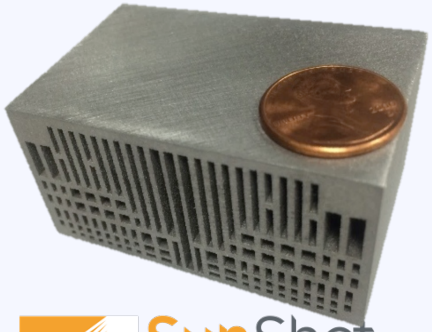
Fabricated All-SiC Module



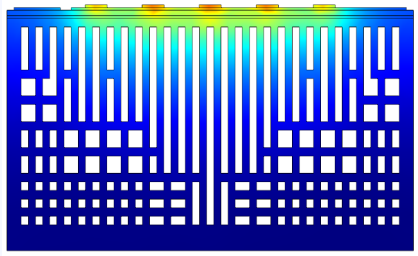
Gate Driver Board



3D Printed Heatsink

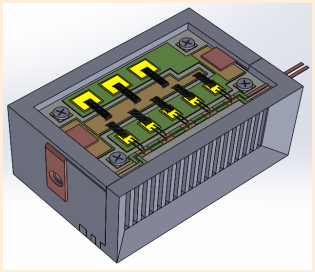


Thermal Analysis

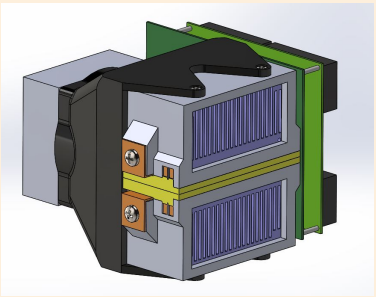


Power Block Assembly

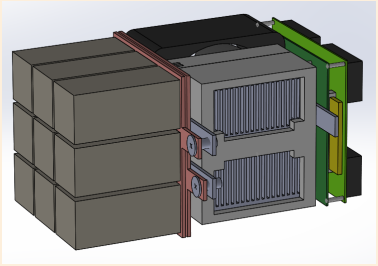
Switch Package



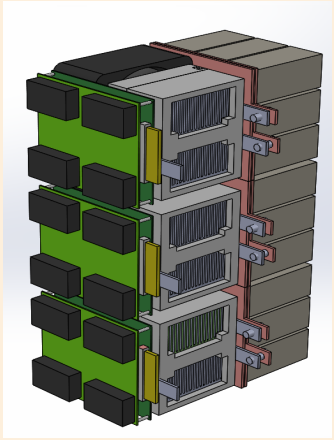
Phase-leg Module with Cooling System



Phase-leg Module with Cooling System and DC Capacitors



Three-phase Power Block



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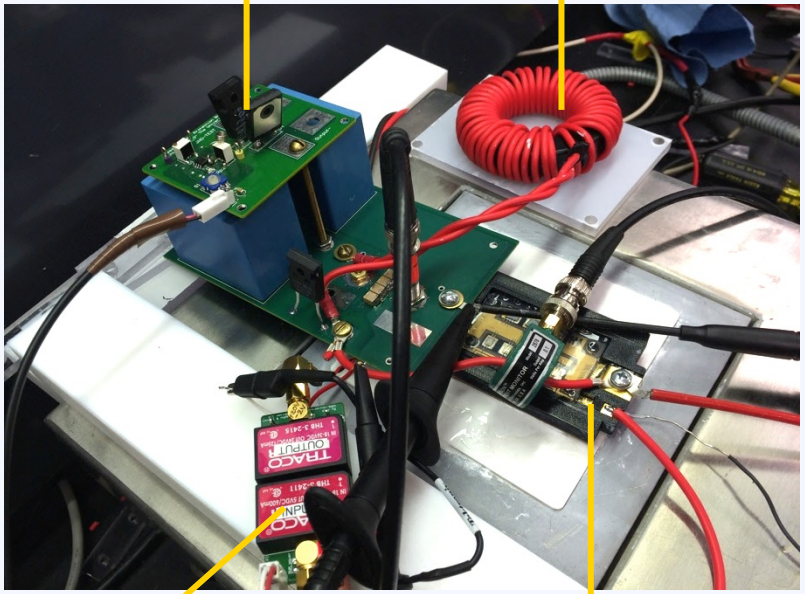
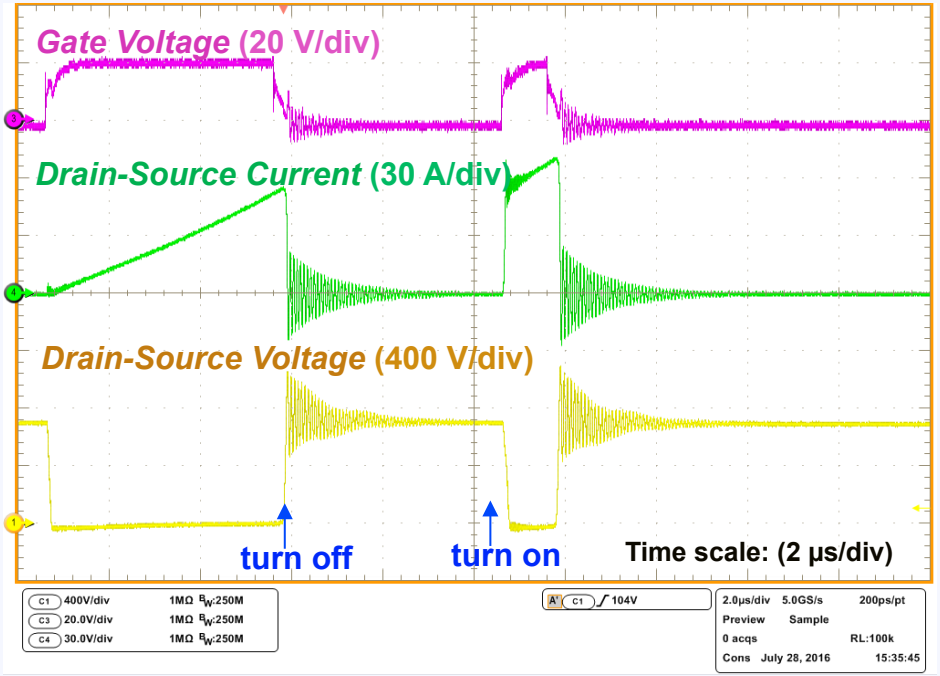
Power Block – Testing

- The switching performance of the SiC module is evaluated through a high voltage double pulse test setup



Initial Test Results for SiC Module



- Power stage with high voltage (>2000V DC) and current capability (>20A RMS)
- Embedded solid-state circuit breaker for fast and reliable overcurrent protection
- Preliminary test: 700V dc bus voltage and 55A load current
- Excellent turn-on switching behavior; moderate turn-off ringing due to non-optimized external power loop connection

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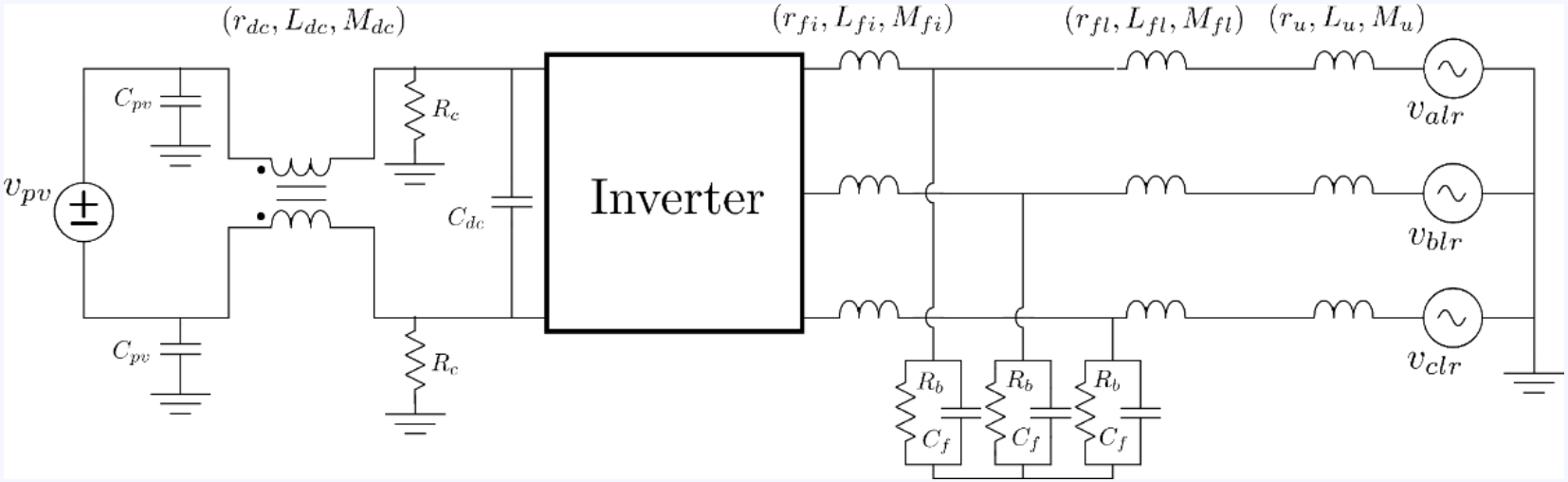
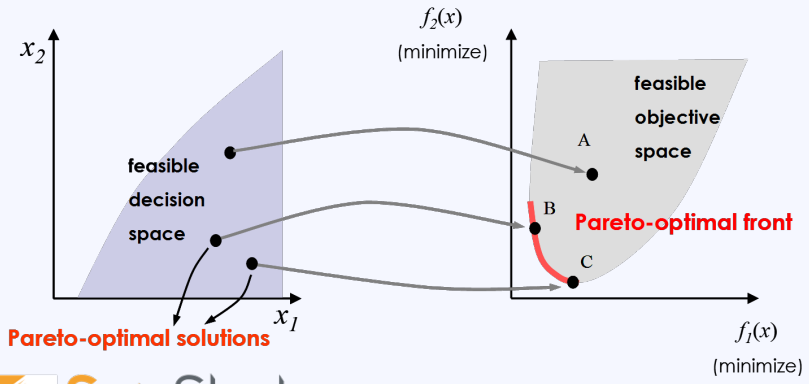
Inductor Design Using Multi-Objective Optimization

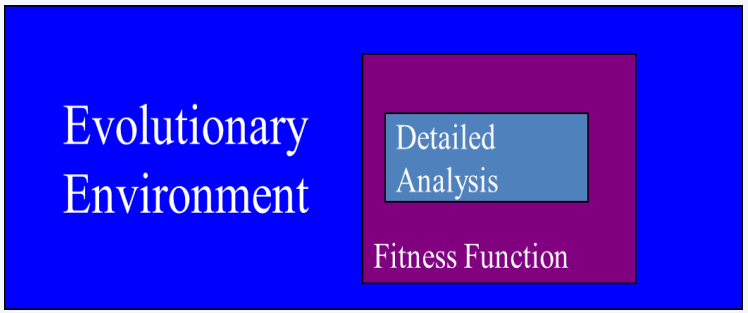
AMPVI Circuit Topology



Multi-Objective Design Methodology



Evolutionary Computing for MO Design



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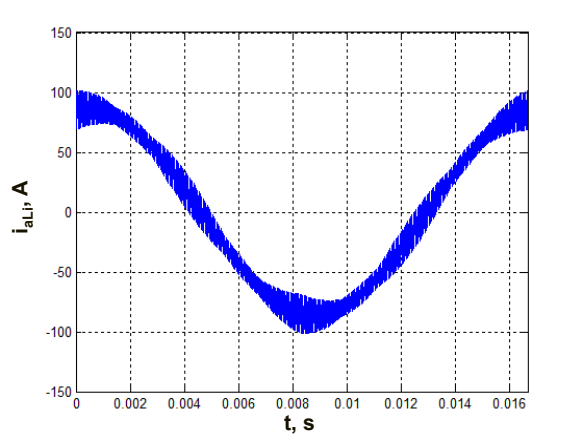
Example: AC Inductor Design

Inverter Side Current



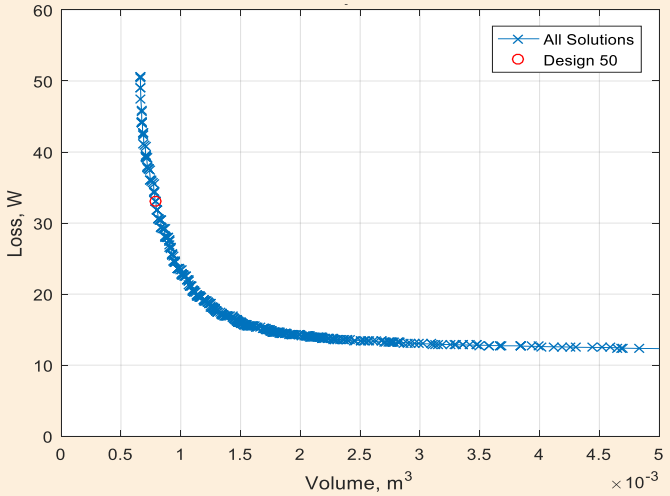
<u>Integrated Analysis</u>
Magnetic – MEC
Thermal – TEC

<u>Losses</u>
AC resistive losses (skin effect)
Proximity effect loss
Core loss (hysteresis + eddy)

<u>Constraints</u>
Geometry/bending radius
Aspect ratio
Mass/Loss
Current density
Inductance (and variation)
Cross-inductance
Peak wind. temperature

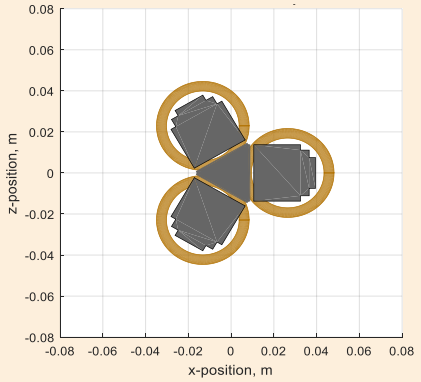
<u>Objectives (minimize)</u>
Volume
Loss

Pareto-Optimal Front

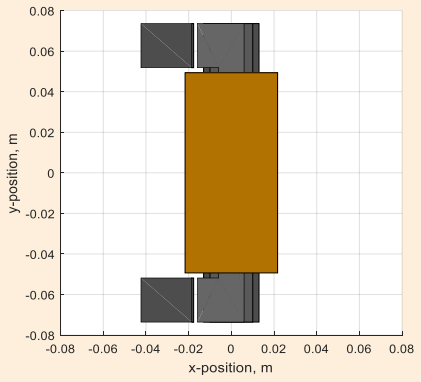


Y-Core AC Inductor

Top View



Profile View



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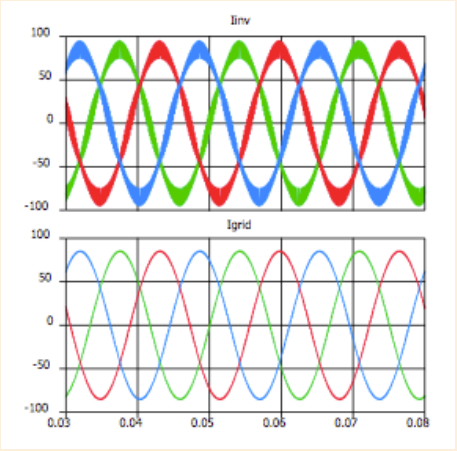
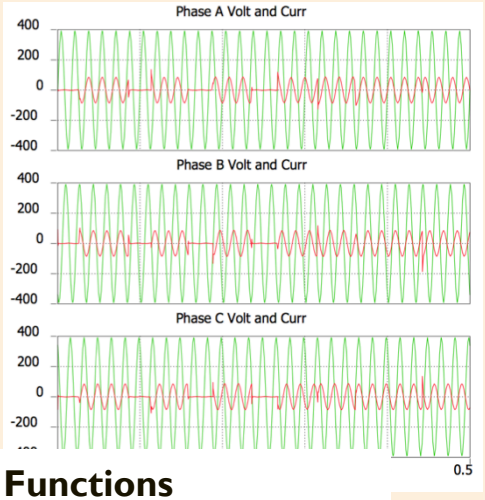
Controller

Control Algorithms and Simulation Validation

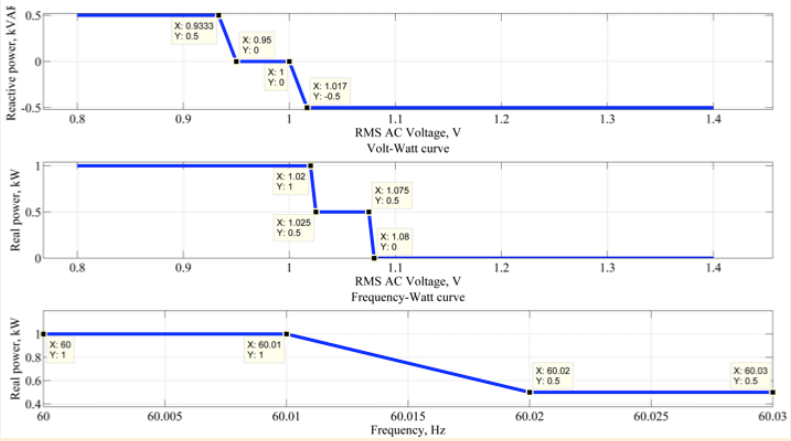
Grid-tied Current Control



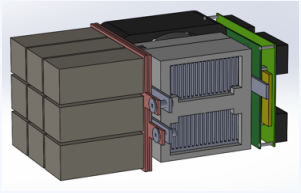
4-Quadrant Operation



Advanced Functions (VVAR, FWATT, Ride through, AI etc.)

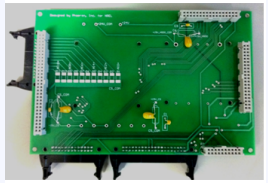


Controller Hardware and Interface



Power Module

ORNL Gate Driver Board



Interface Board

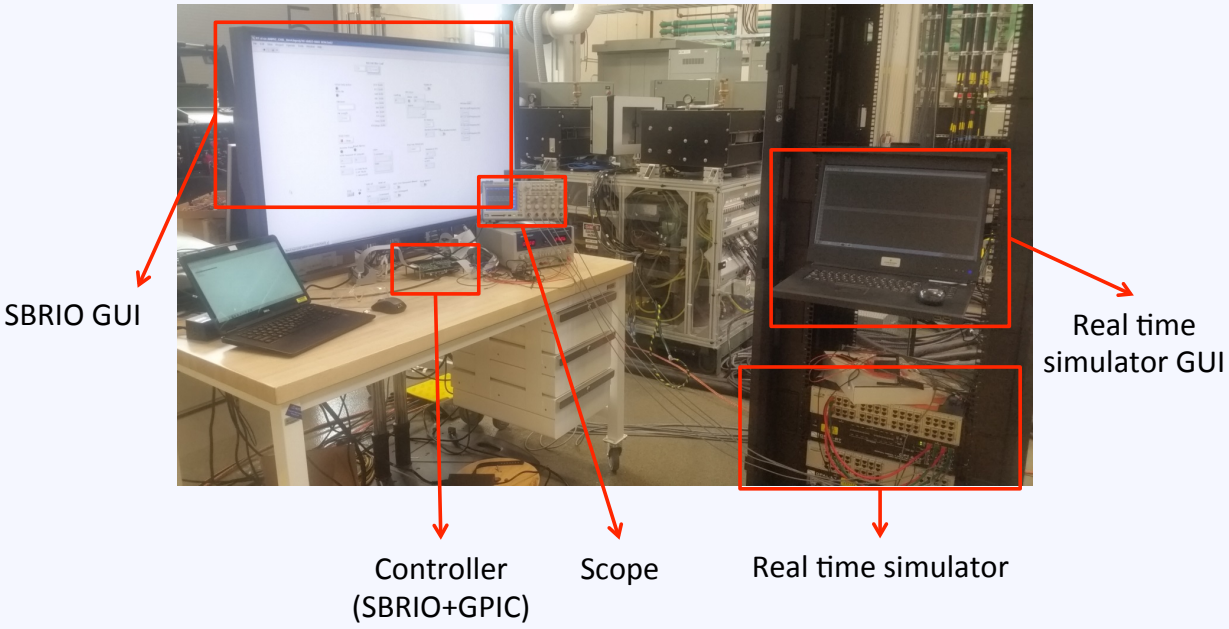
NI 9607

NI 9683 Controller

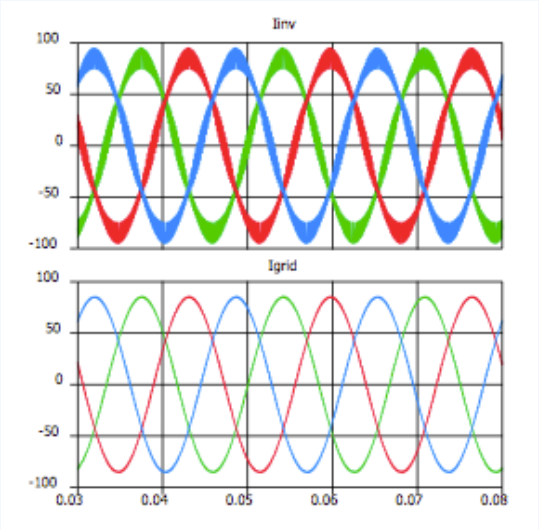
SBRIO: Xilinx Zynq-7000, 667 MHz dual-core ARM Cortex-A9 processor, an Artix-7 FPGA, and a mezzanine card connector

Controller Hardware-in-the-Loop (CHIL)

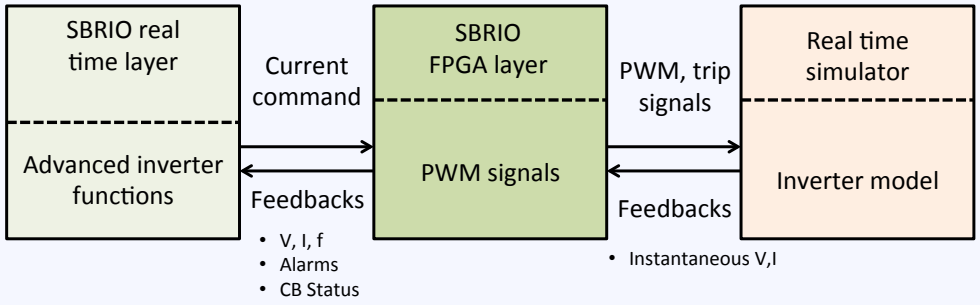
CHIL Experimental Setup



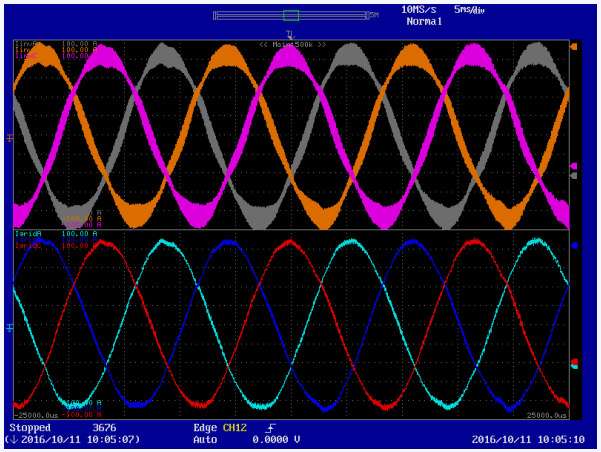
Pure Simulation



CHIL System Architecture



CHIL Results



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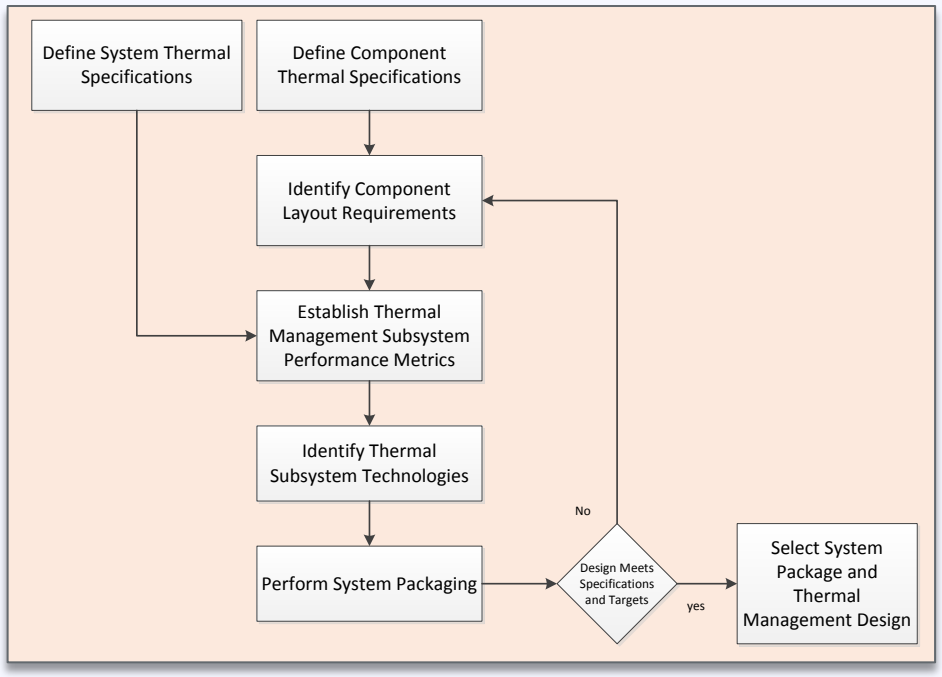
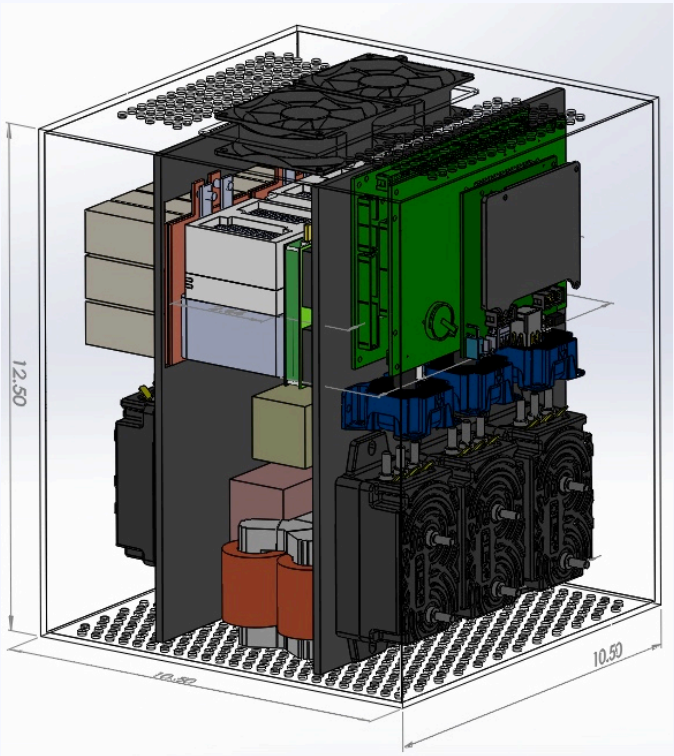
Component Layout (Alpha-prototype)

Thermal Design Process



Packaging

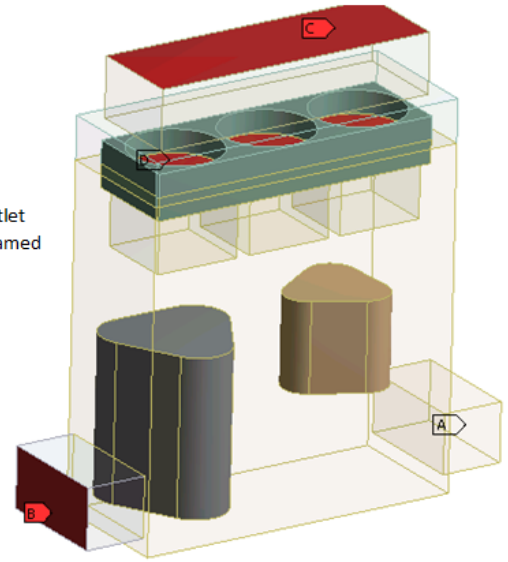


- Components are grouped into three thermal subsystems :
  - I: DC capacitors, DC current and voltage sensors
  - II: power block, LCL filters
  - III: Control board, AC current and voltage sensors
- Subsystem II has largest heat loads and therefore becomes the main focus in thermal design
- The inverter designed volume is 1378 in^3, yielding a power density of approximately 36 W/in^3

Evaluation of Thermal Design

Air Temperature Distribution

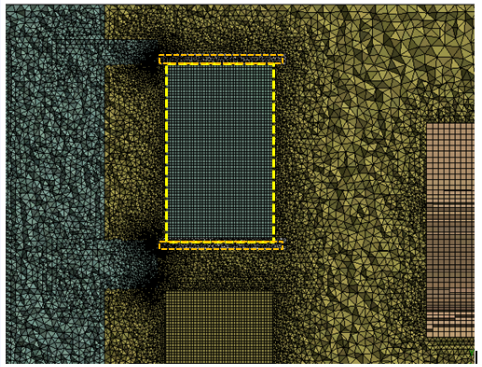
A. Inlet vent
B. Inlet vent
C. Pressure outlet
D. Fans (one named selection)



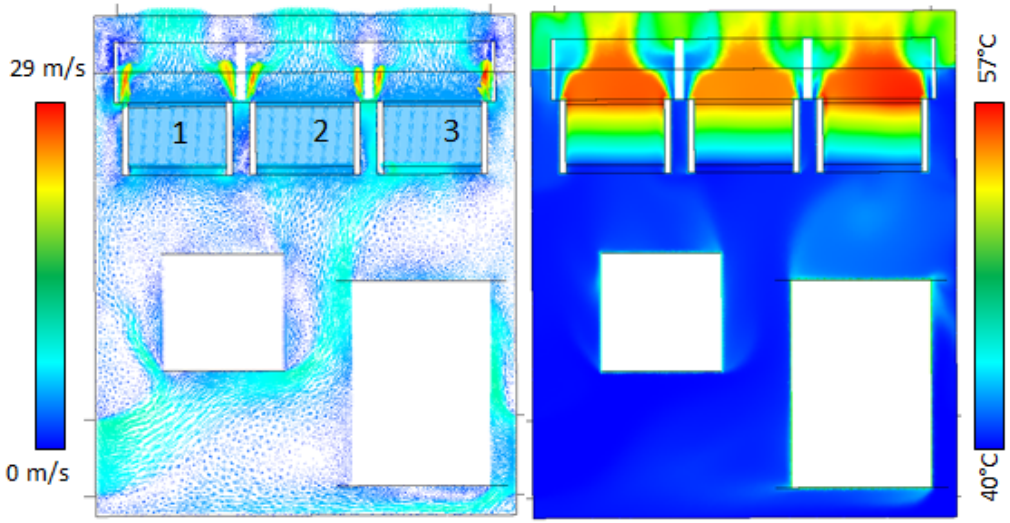
Boundary Conditions

- Heat exchanger is modeled as a porous media within ANSYS
- Parameters are defined to match the desired pressure drop versus flow of the specified heat exchanger

Sample Mesh



Preliminary CFD Simulations



Velocity Vectors

Center Plane Temperature

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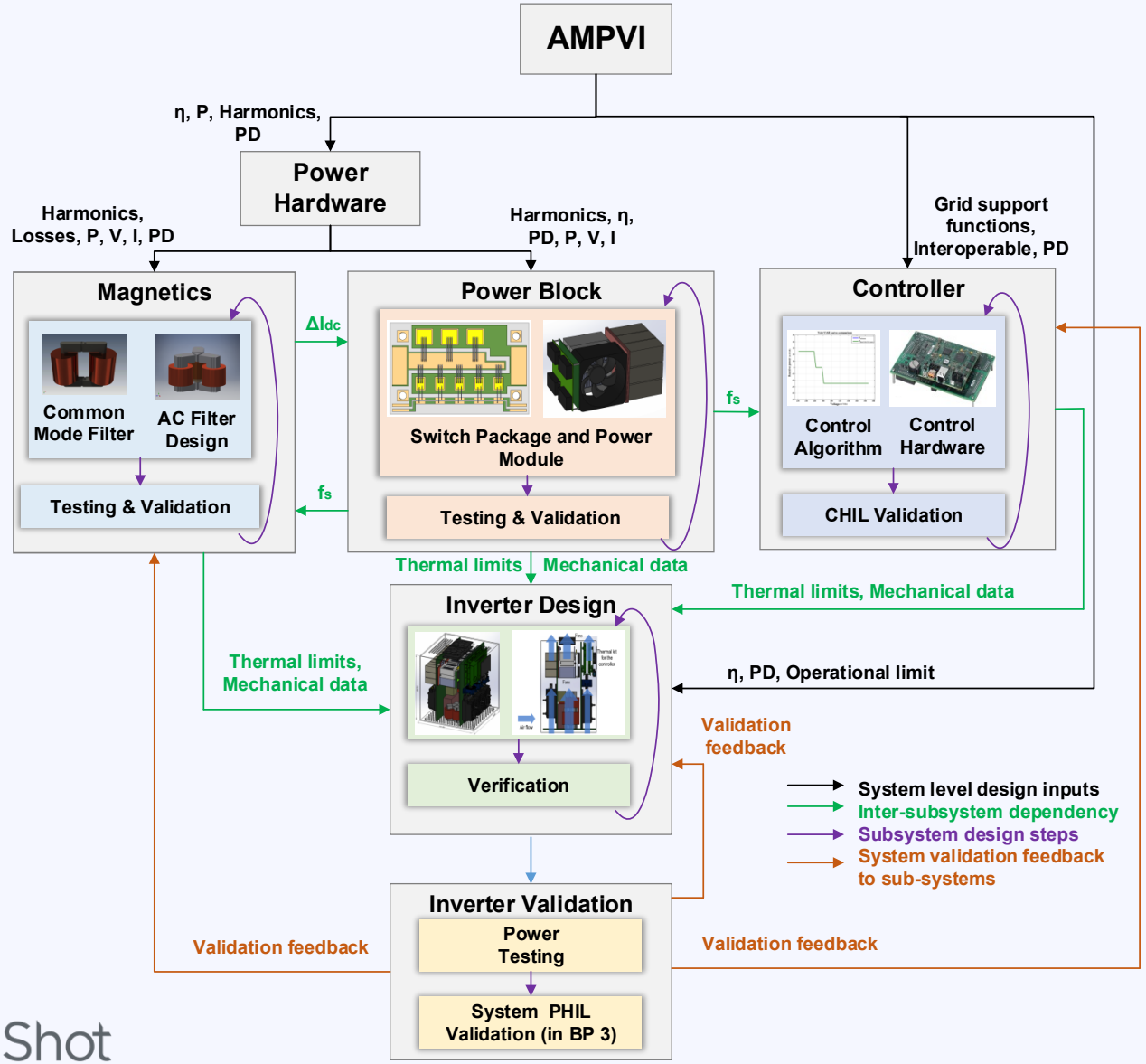
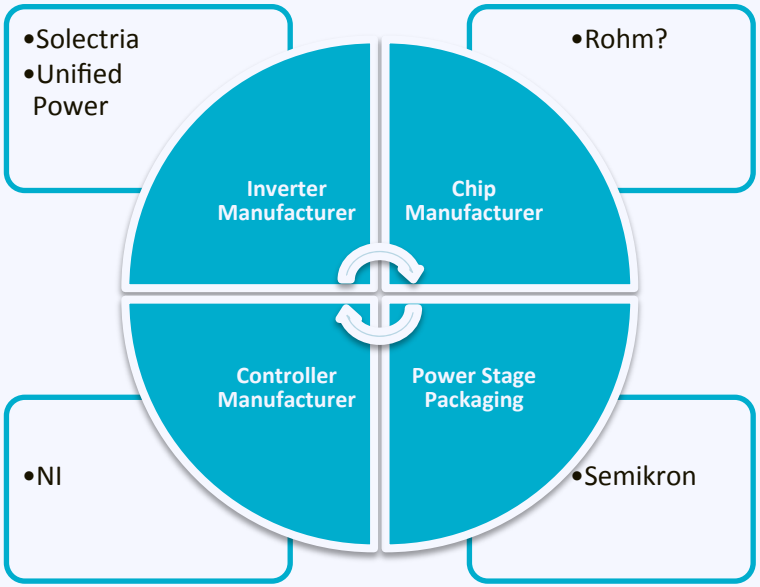
AMPVI Design Process Flow



Stakeholder Engagement

- Technology advisory panel (TAP)
  - Getting industry feedback and building industry interest in developed technologies for future commercialization
  - TAP was formed and currently have four members Solectria, Unified Power, National Instruments, Semikron USA
    - 1-hour call in every 3 months
    - No travel requirement
    - Typically be at high level without discussing any detailed technology or IPs
    - May need to sign a multi-party NDA if detailed technologies discussed



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Thank You!!