Enhanced High Temperature/High Speed Data Link for Logging Cables

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EGS: High Temp Tools, Drilling Systems

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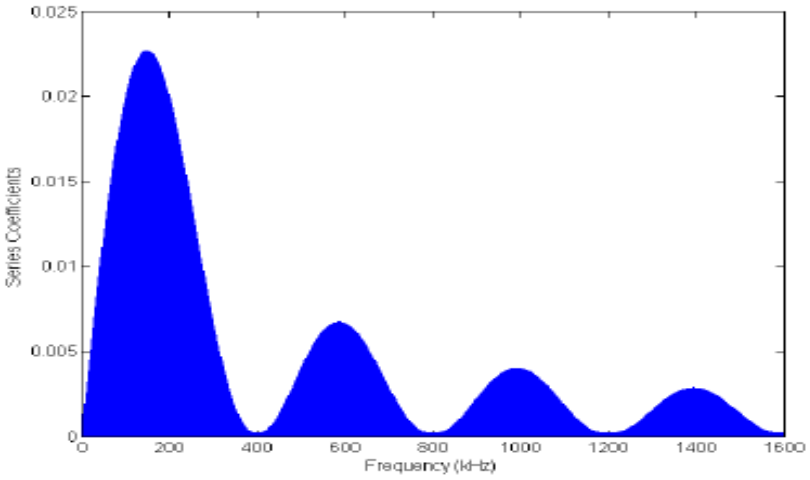
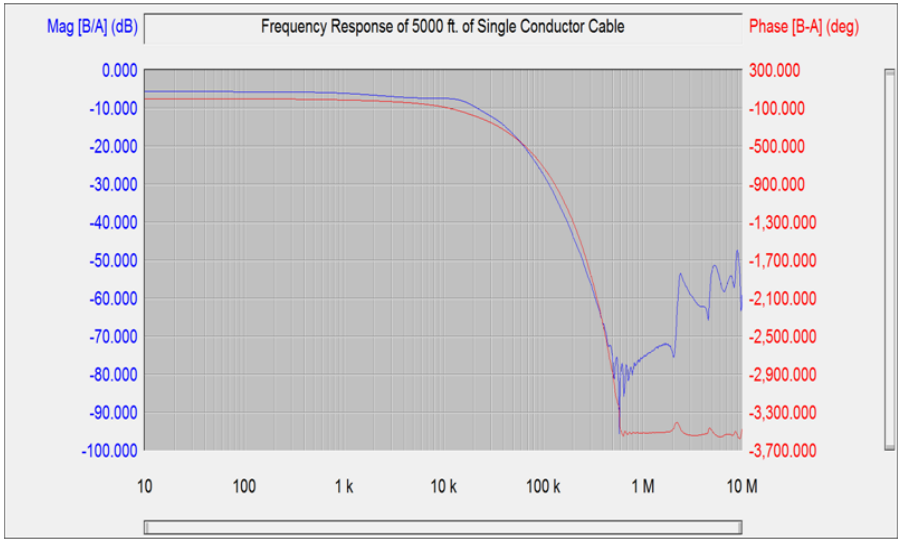
Relevance/Impact of Research

- Background
  - Increased need for high bandwidth data transition
    - New generation of sensor
    - Increased speed and accuracy
  - Uplink bottleneck
    - Poor signal characteristics of high-temperature (HT) wirelines
  - Currently data rates are limited to ~200 kbps
- Goals
  - Enable high transmission rate of raw data from downhole tools
    - Acoustic logging, seismic measurements
  - Develop an asymmetric HT high-speed (HS) data link system
    - Uplink data rates >1Mbps over 5000 ft of single-conductor wireline
    - Downlink data rates sufficient for command and control
    - Temperatures up to 210ºC

Scientific/Technical Approach

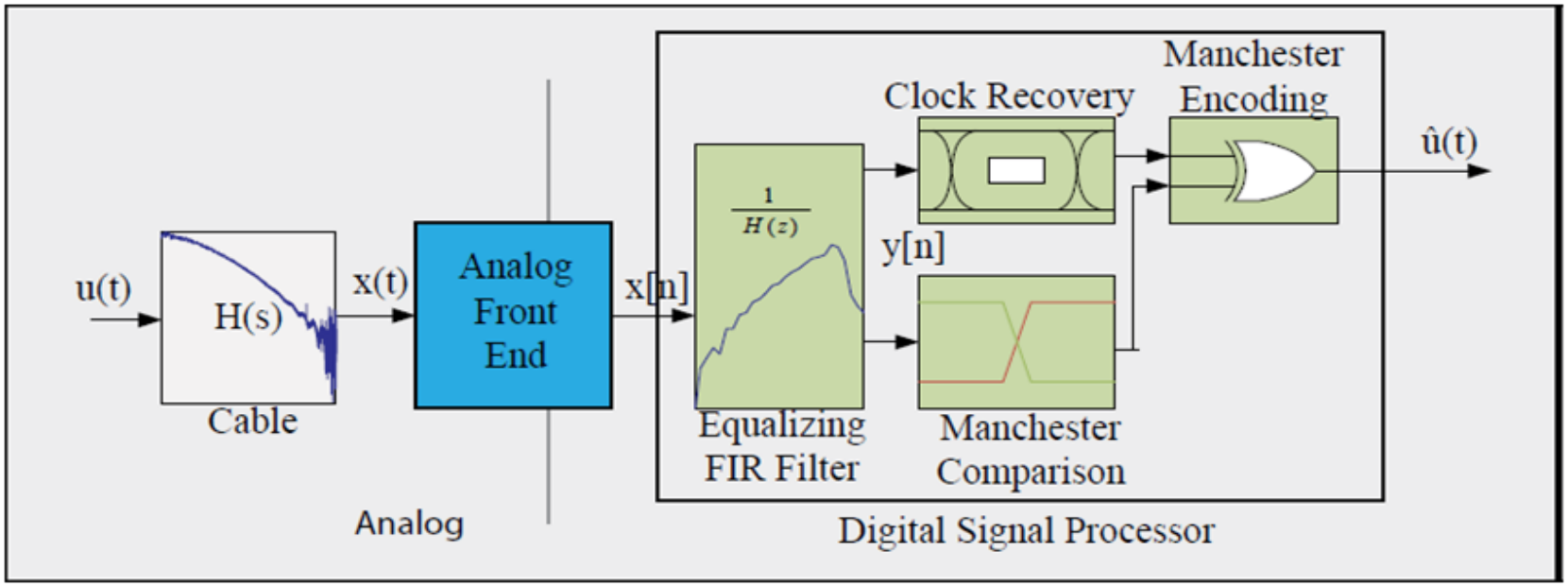
- Challenges
  - Limitations of HT single conductor wirelines
    - Designed for tension, temperature, corrosive environment, power transmission
    - Not designed for data transmission
  - Limitations of HT electronics
    - Lack of necessary components
    - Few components available
    - Low processing speed
    - Variability in temperature ratings
  - Appropriate use of bandwidth
    - Must maximize available bandwidth to maximize performance
    - Some protocols are more efficient than others





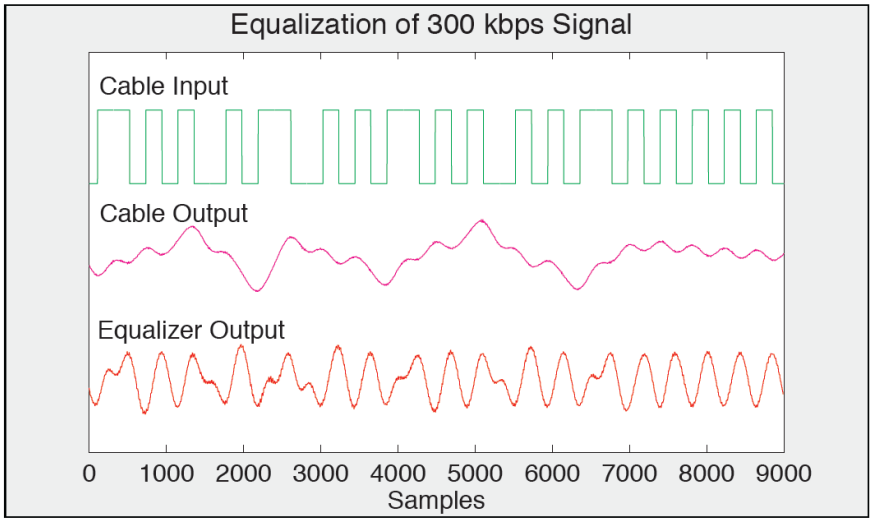
Scientific/Technical Approach

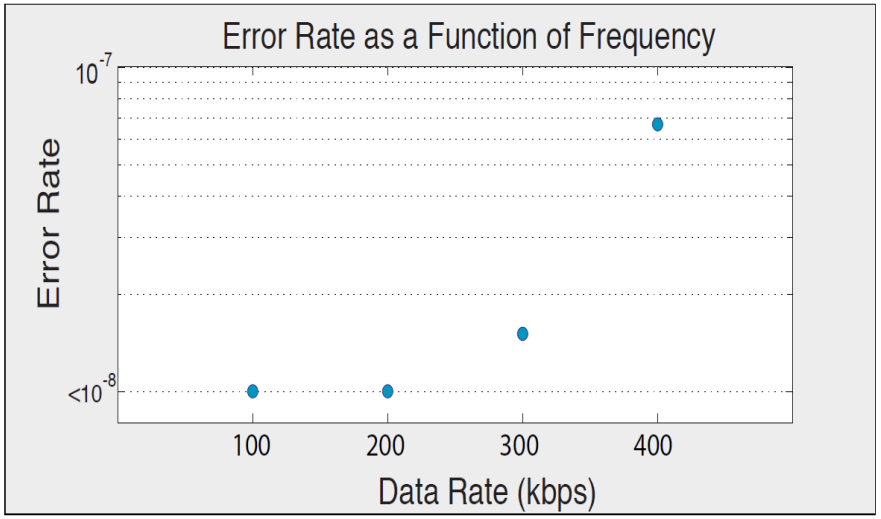
- Phase 1
  - Use Manchester encoding (special case of BPSK) in combination with equalizing filter uphole to mitigate wireline distortion
  - Does not require complicated downhole electronics
    - Data is xor-ed with clock
  - Equalizing filter is difficult to design and computationally intensive



Phase 1 Results

- The equalizer was implemented on a Altera Cyclone III Field Programmable Gate Array (FPGA) using a 720 tap finite impulse response (FIR) filter
  - 25MHz sampling rate
- The clock and data recovery block, which is also implemented in the Cyclone III FPGA, works to take the equalizer output and convert it back into digital clock and data signals
- The system uses a correlator to recovery the data signal and a first order PLL to recover the clock
- Maximum data rate achieved is 400kbps with very low error rate
- Fulfilled the objectives of phase 1



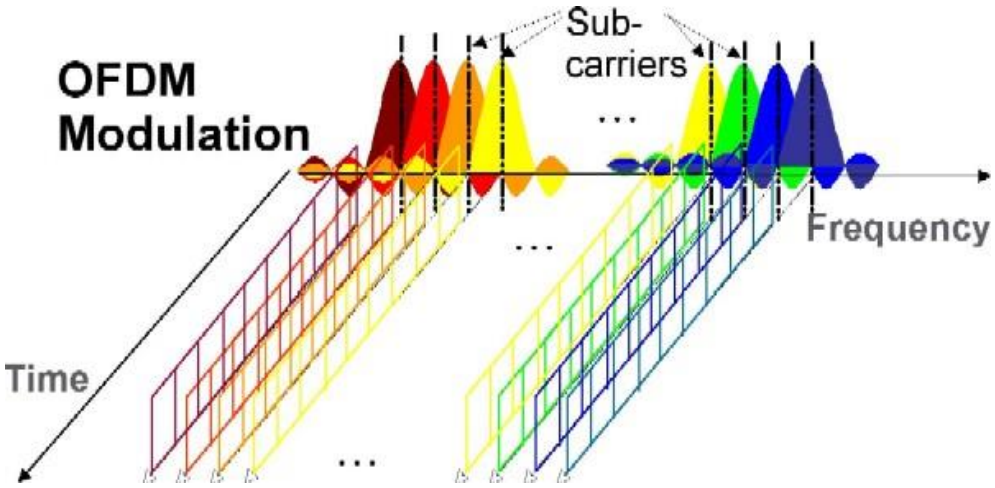


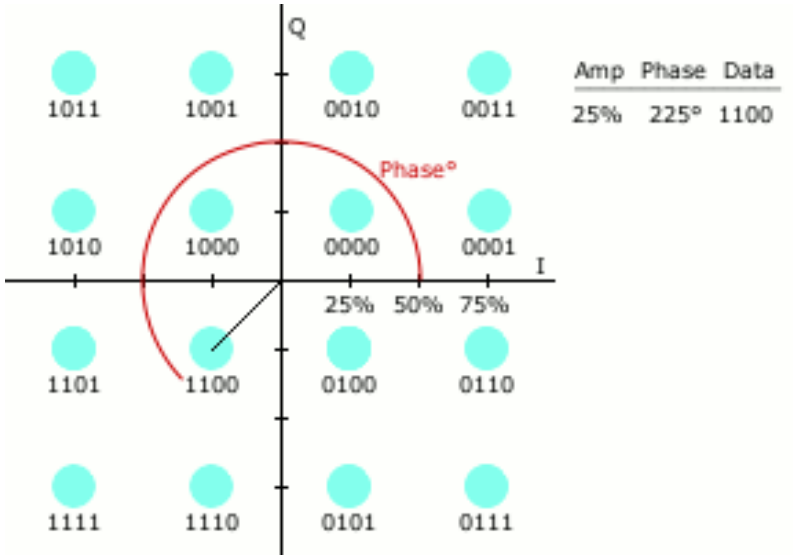
Scientific/Technical Approach

- Phase 2 lessons
  - The phase 1 approach did not allow to increase speed much beyond 400kbps
    - Increased error rate and difficulty with PLL locking on for clock recovery
  - Inefficient use of bandwidth by Manchester code
- Phase 2 approach
  - New approach leverages methods developed by telecom industry
    - DSL, LTE..
    - OFDM – Orthogonal frequency division multiplexing
  - Increased requirements for downhole electronics
  - Simplified uphole electronics
  - Goal to reach speeds >1Mbps

Scientific/Technical Approach

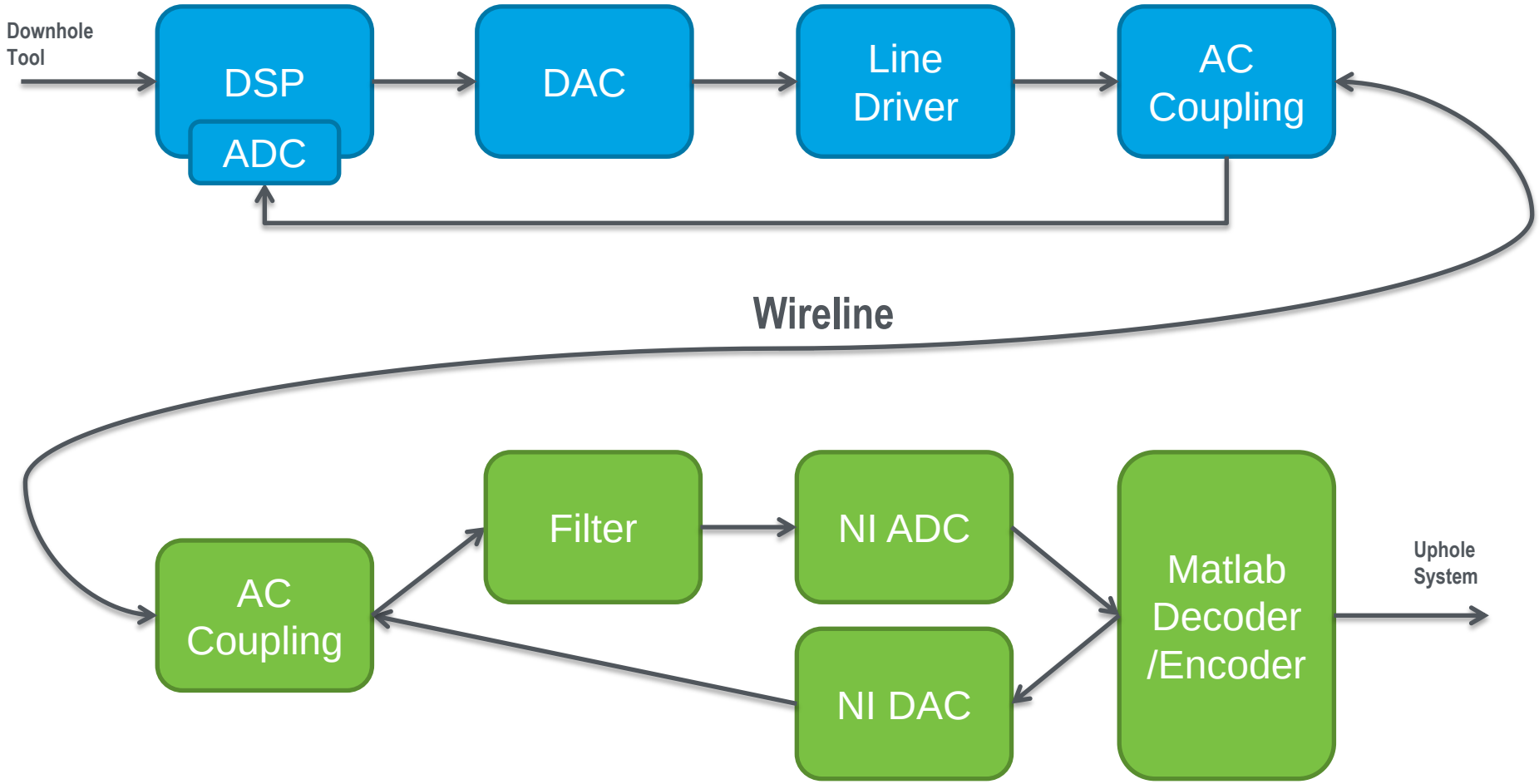
- OFDM – Orthogonal frequency division multiplexing
  - Divides the available bandwidth in to multiple narrow band channels
  - Computationally intensive – FFT
  - Efficient use of bandwidth
- QAM – Quadrature Amplitude Modulation
  - Each channel uses QAM to encode the data
  - The data is encoded by changing the amplitude and phase of a sinusoid
- Compensates for channel distortions
- Sensitive to clock mismatch





Scientific/Technical Approach

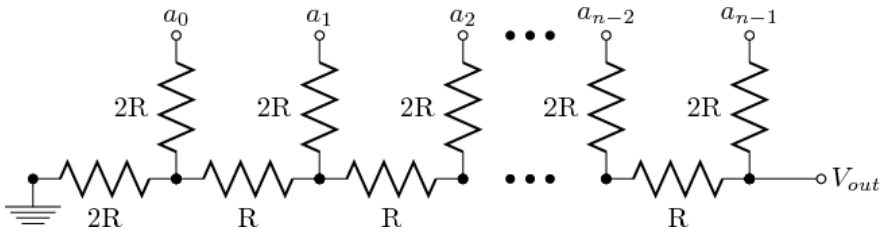
- System Components

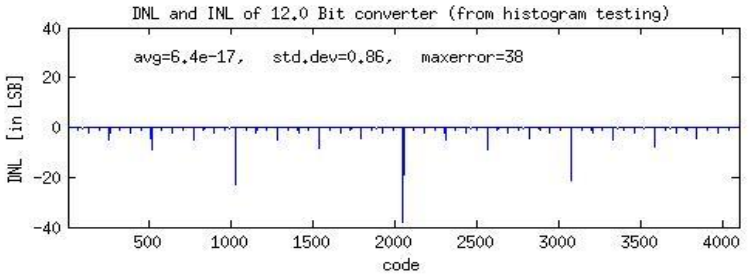


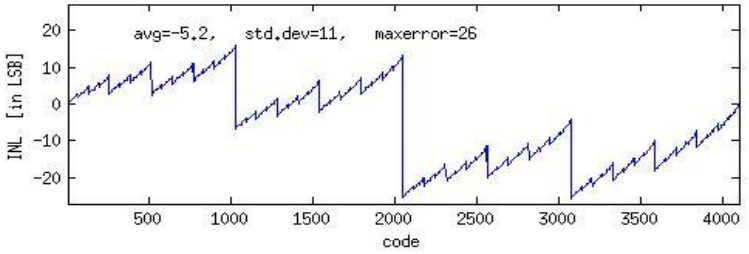
Accomplishments, Results and Progress

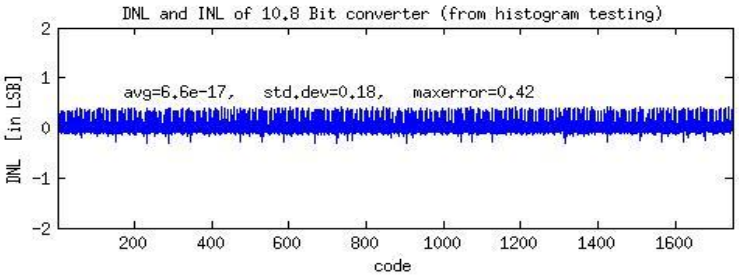
HT digital to analog converter

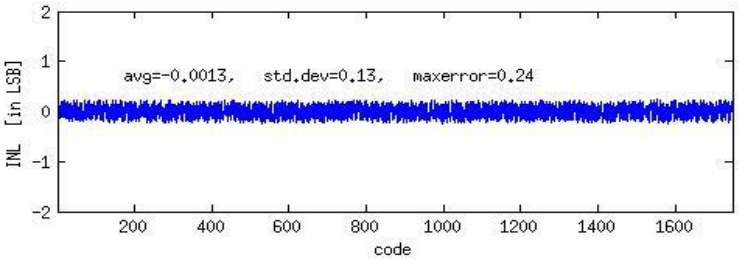
- No commercial part available
- Adopted classical R2R ladder approach
- Required precision of ~10 bits initial size 12 bits
- Linearity problems
  - Resistor mismatches
  - Resistor values
  - Achievable rate
- Developed a linearizing algorithm
  - Sacrifices some bits to linearize output
- 10.8 bit DAC with max DNL of 0.42 LSB and max INL of 0.23 LSB
- Precision can be increased further by increasing initial size of the DAC





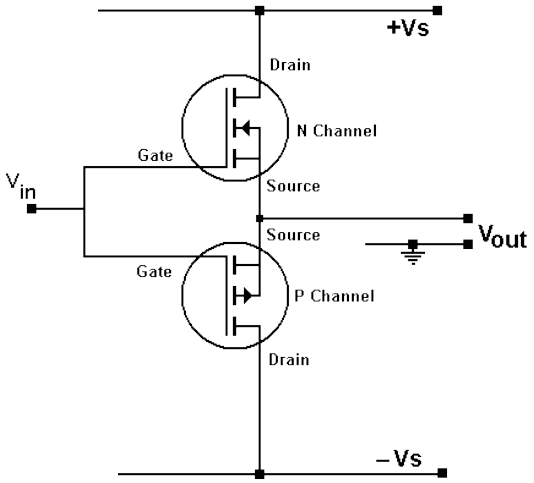


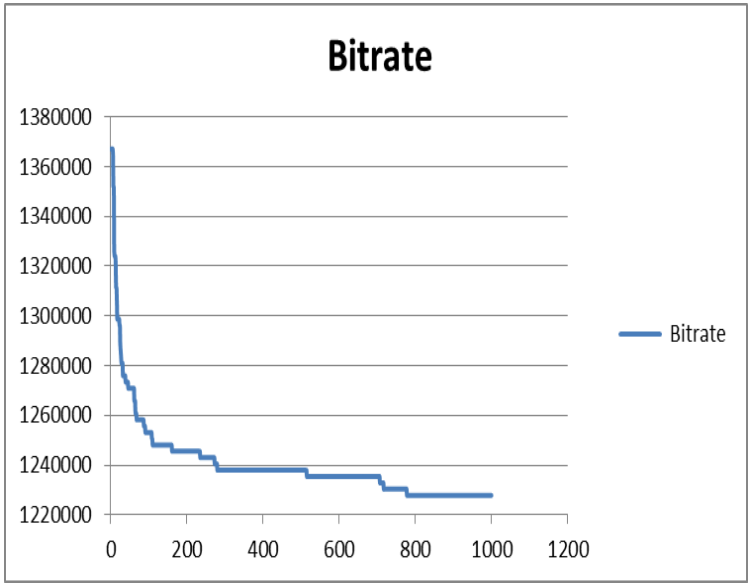




Scientific/Technical Approach

- Developed prototype system
  - Downhole: TI DSP, custom DAC and custom line driver
  - Uphole: programmable analog filter, NI hardware and a laptop with Matlab
- Preliminary Results
  - Observed speeds up to 1.5Mbps over 5000ft of wireline
    - Higher speeds possible but will require link protocol
    - Protocol automatically decreases speed to decrease error rate
  - Observed speed up to 600kbps over 12000ft of wireline





Accomplishments, Results and Progress

Original Planned Milestone/ Technical Accomplishment	Actual Milestone/Technical Accomplishment	Date Completed
FY(14) Select HT components (FPGA/processor, precisely matched resistors for DAC, op-amps and transistors for analog line driver) for construction of the downhole transceiver. Develop a robust link protocol capable of adjusting link parameters to changes in cable conditions and mitigating occasional transmission errors	Selected appropriate components as well as developed suitable DAC and line driver	Partially Completed – the work on the link protocol is ongoing
FY(14) Develop and test uphole and HT downhole transceivers capable of transmitting data at 1 Mbps over 5,000 feet of single conductor wireline using spread spectrum techniques	Constructed benchtop uphole and HT downhole prototype capable of transmitting data at >1Mbps	09/2014
FY(14) Evaluate the system in a laboratory environment at temperatures up to 210°C and various wireline lengths by measuring the data rates and corresponding error rates.		Ongoing – finalizing the details for all the components.

Future Directions

- Finalize details of the link protocol
  - Error correction
  - Retransmission
  - downlink
- Test updated version of line driver
  - More suitable components just became available
- Fabricate whole downhole system on HT PCB for testing
- Test the whole system up to 210C
  - 5000ft and 12000ft wireline
  - DAC and line driver performance
  - Error rates

Mandatory Summary Slide

- Enable high transmission rate of raw data from downhole tools
  - Acoustic logging, seismic measurements
- Phase 1
  - Employed Manchester encoding and uphole equalizing filter to achieve rates up to 400kbps.
  - Not scalable to higher bitrates
- Phase 2
  - Developed prototype HT HS data link system employing OFDM
    - Developed custom DAC
    - Developed custom line driver
  - Observed data rates >1Mbps over 5000 ft of single-conductor wireline
  - Temperatures up to 210ºC