Development & Industrialization of InGaN/GaN LEDs on Patterned Sapphire Substrates for Low Cost Emitter Architecture

2015 Building Technologies Office Peer Review

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

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Project Summary

Timeline:

Start date: August 1, 2013

Planned end date: July 31, 2015

Key Partners: None

Key Milestones:

1. Repeatable demonstration of PSS emitter performance within 1.5% of the TFFC counterpart;
   - met January 2014
2. Demonstration of PSS emitter performance exceeding TFFC counterpart by 2%:
   - met January 2015
3. Industrialization of PSS flip-chip process with light output equal to or better than TFFC devices in a low-cost package: target: July 31, 2015

Budget:

Total DOE $ to date: $1,299,711 (Feb 2015)

Total future DOE $: $591,179

Project Goal:

Develop Patterned Sapphire Substrate (PSS) – based LEDs with performance matching the best thin-film flip-chip devices to enable next-generation, low-cost LED products.

Target Market/Audience:

Commercial products are targeted for the high-brightness illumination markets.

Purpose and Objectives

Problem Statement:

- In Lumileds' traditional products, the highest Lm/W performance has been from thin-film flip-chip (TFFC) LED architectures.
- Production of TFFC emitters requires a number of complex processing steps and necessitates mounting the LED to an intermediate (Level 1) package.
- This DOE-assisted project is developing next-generation LED emitters using patterned sapphire substrates as an alternative to TFFC to enable size and cost reduction while maintaining state-of-the-art performance.

Target Market and Audience:

The LED components pursued in this program are targeting indoor and outdoor illumination markets which demand the most competitive Lm/W and Lm/$ characteristics in small footprint components.

Impact of Project

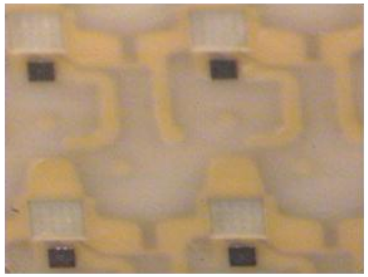
1. The endpoint of this project is commercialization targeted in 2015 of PSS-based components with best-in-class Lm/W performance at a 20% cost reduction over last year's TFFC product counterparts targeted for high-output, small-footprint illumination products.
2. The achievements of this project are measured by:
   a. Near-term (performance improvements in PSS products)
   b. Intermediate-term (commercialization of low-cost LEDs based on PSS die)
   c. Long-term (utilization of PSS architectures in extended applications and higher levels of integration)

Problem Statement

- In Lumileds' traditional products, the best Lm/W performance has been from thin-film, flip-chip (TFFC) LEDs.
- In TFFC texturing the surface of the GaN enables 40% greater light out-put relative to a smooth surface.
- Production of TFFC devices requires removing the sapphire substrate and additional complex processing.
- The use of patterned sapphire substrates allows the sapphire substrate to remain in place and enables chip-scale packaging.

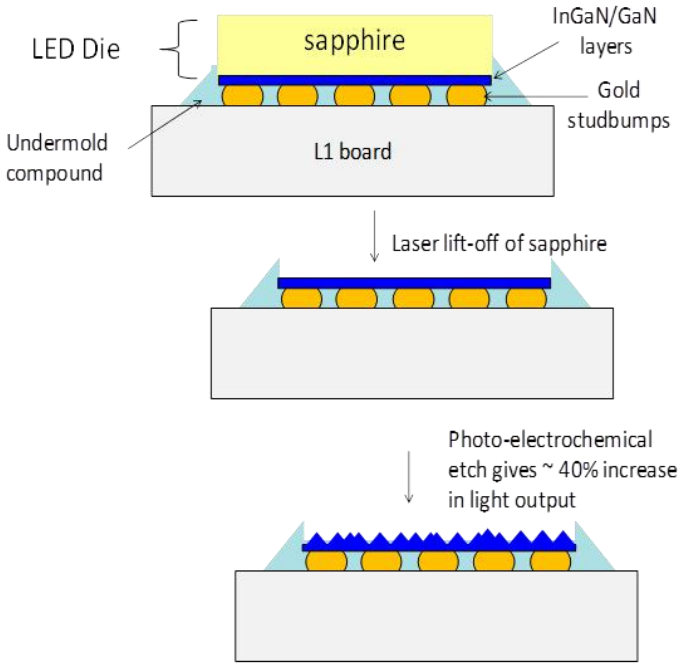
Epitaxy & Wafer Fabrication

LED layers are grown and processed on sapphire substrates.



LED Die Fabrication

Singulated die are "flip-chip" attached to a metallized ceramic carrier.



TFFC Process steps

LED layers are separated from their substrate and roughened.

TFFC process adds complexity and cost to the LED product!

Approach

Approach: Design and establish optimized patterned sapphire substrate geometries and improved LED epitaxial growth processes to enable a chip-scale package LED with state of the art performance with a >20% reduction in cost.

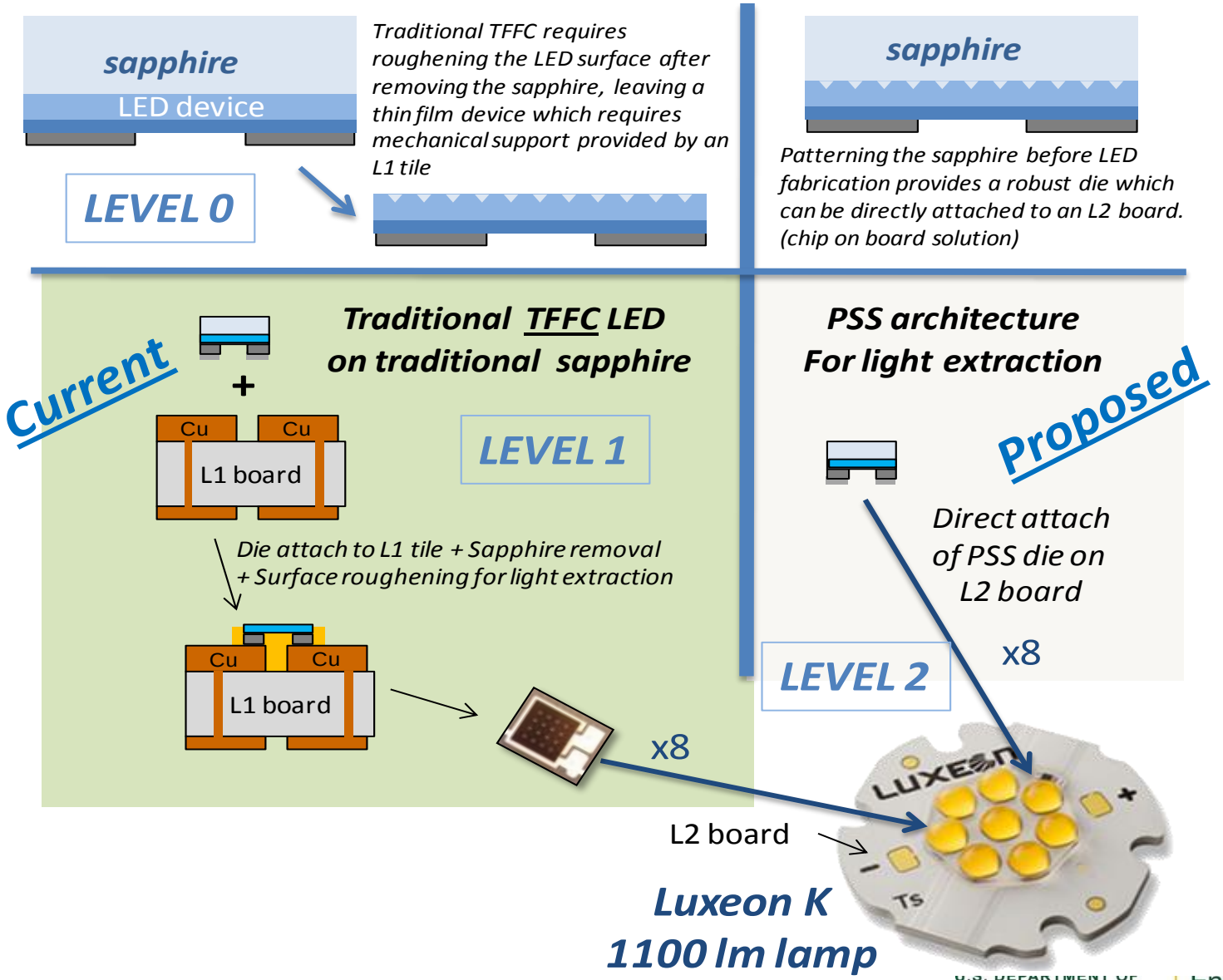
Key Issues: Our second generation PSS structure and process has resulted in an 8% improvement in Lm/W over our first generation PSS, thus demonstrating the potential of performance on par with the best TFFC products. This achievement is enabling Lumileds to develop the Next-Generation LED architectures for smaller and less expensive components for illumination productions in the second phase of this project.

Distinctive Characteristics: Two Next-Generation Emitter product applications are under development:

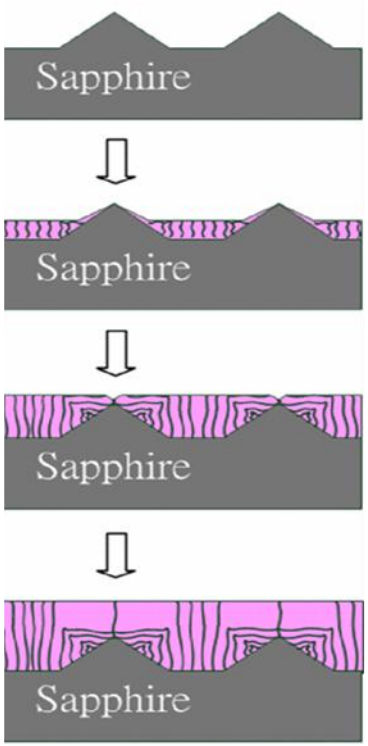
(1) a low-cost, direct-attach, chip-scale packaged part

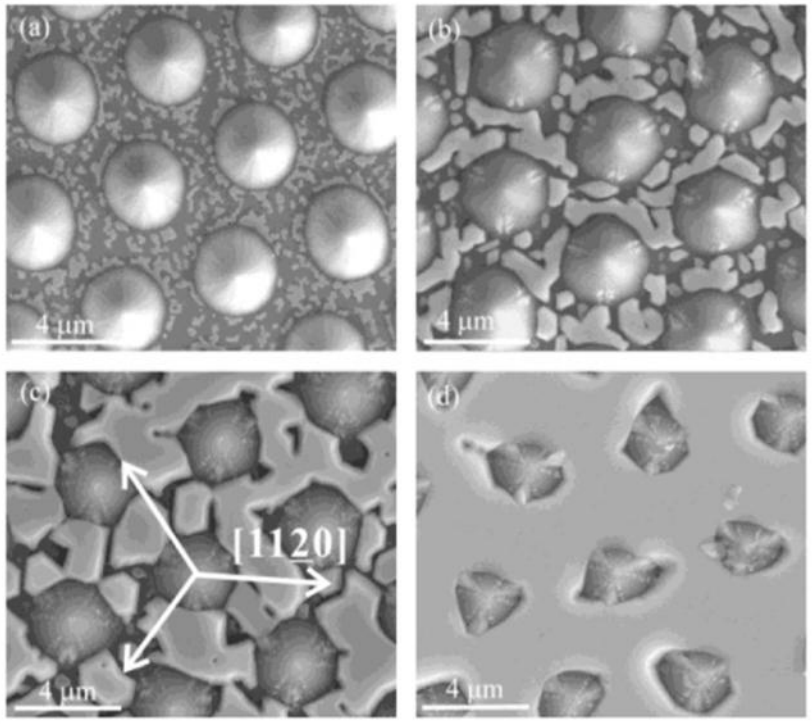
(2) a small foot-print, high-drive packaged part for high directionality and high Lm/$.

LEDs on Patterned Sapphire Substrates Enables Simplification



Growth of LED Layers on PSS Wafers – Project Challenges

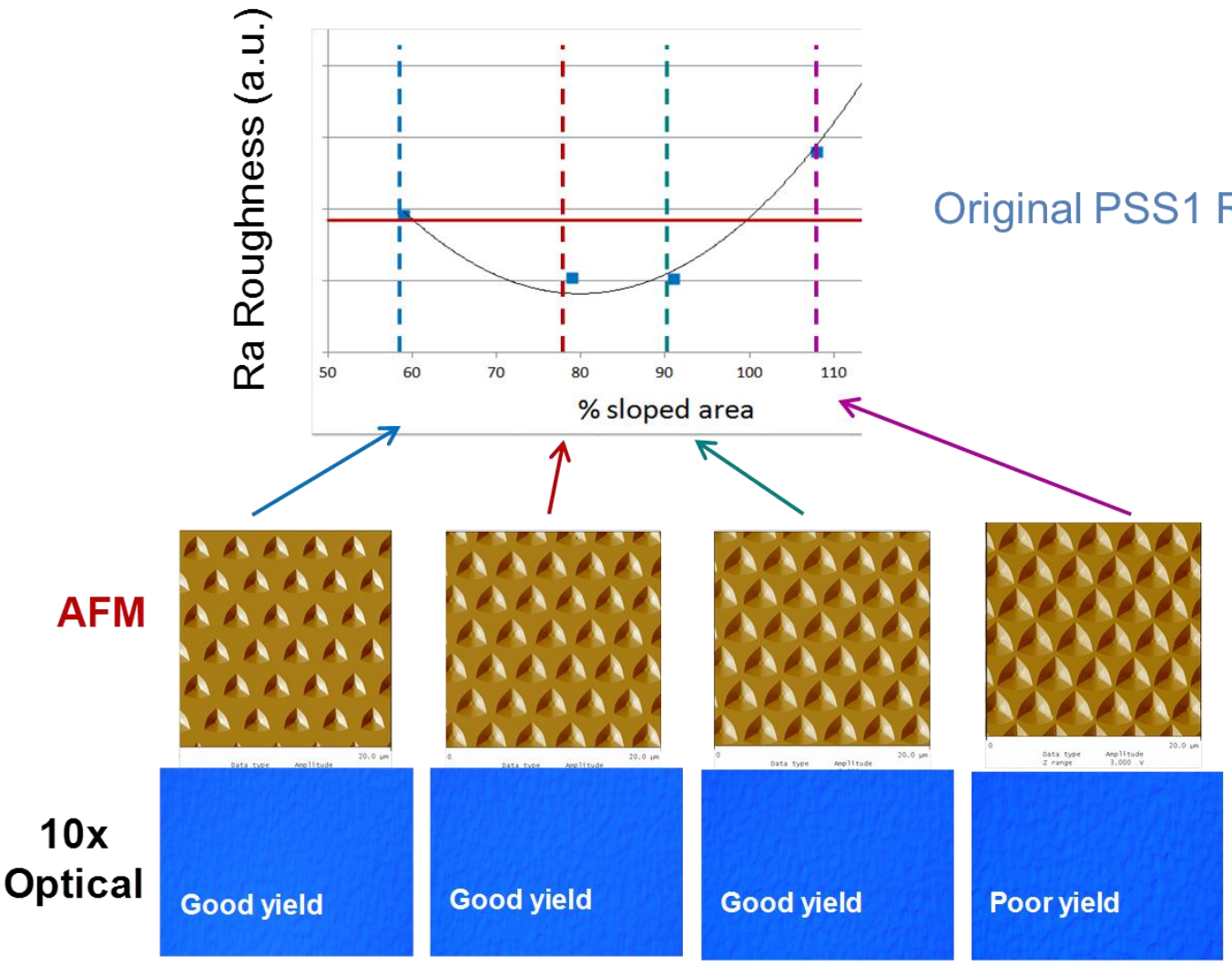




Images taken from Xiao-Hui Huang, et al. Optics Express, Vol. 19, Issue S4, pp. A949-A955 (2011)

- Design and fabrication of optimal PSS features for high light extraction and LED yield.
- Growing smooth, high-quality epitaxial layers on highly patterned PSS wafers.
- Engineering high-performance, low-cost package architectures which best exploit the features of the PSS LED die.
- Implementing high-volume manufacturing capabilities for the above.

Tradeoff of Patterned Area vs Epitaxial Layer Quality



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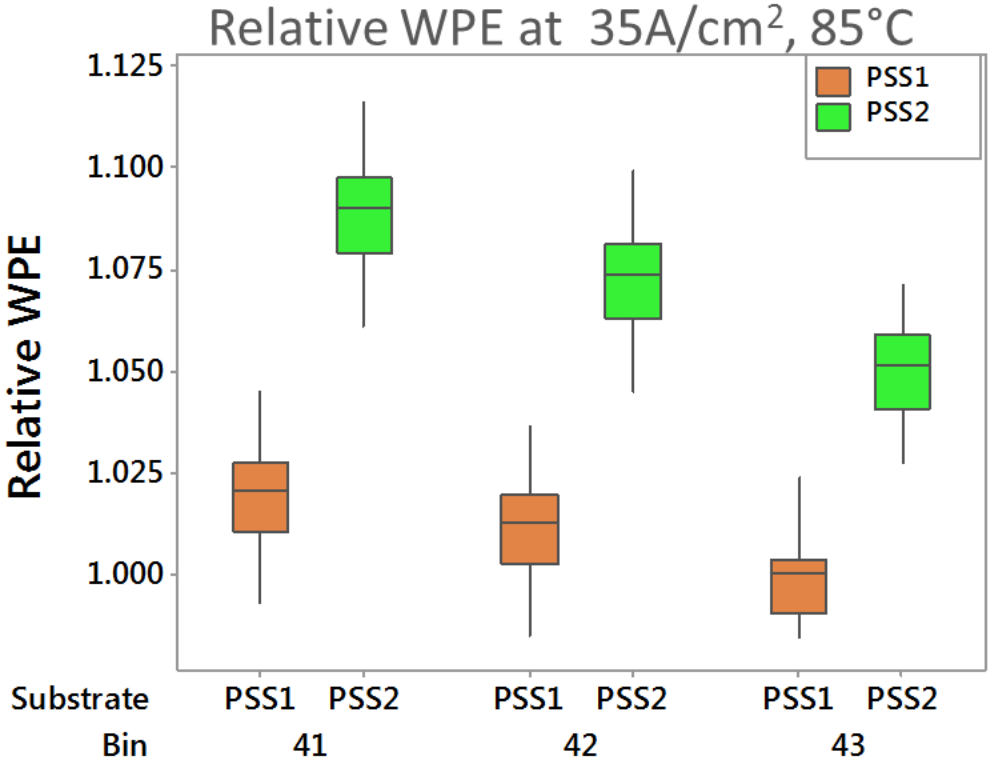
Progress and Accomplishments

- Down-selection and industrialized manufacturing of new “PSS2” patterns.
- Established methods for automated visual inspection during PSS substrate manufacturing.
- Established LED epitaxial growth methods on all major reactor platforms.
- Wafer-level LED fabrication yield-data showing comparable performance to “process of record” epitaxial wafers.
- Demonstrated initial data showing PSS2 emitter performance in 1mm^2 LUXEON Q package exceeding its LUXEON Rebel TFFC counterpart in multiple epitaxial growth and wafer fabrication runs.
- ~4-5% gain in light output attributed to PSS2 added to ~4% gain in LUXEON Q through Gen2 die design.
- ***Commercial release of the PSS2 pattern and epitaxial growth process into LUXEON Q products, with the official product data sheet updated for higher flux specifications (>12% gain in flux for 3000K 80 CRI at 35A/cm2).***
- Down-selection of candidate packaging concepts for next-generation emitter architecture.

Market Impact of Project

- 5- 8% higher Wall Plug Efficiency by optimizing the PSS substrate and epitaxy.
- Largest improvements are seen at highest drive current.
- These improvements have been released in Luxeon Q products and are enabling our “Next-Generation Emitters”



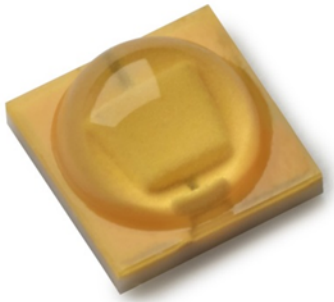
PSS2 % WPE gains over PSS1 at 25C			
λ bin	**350mA**	**700mA**	**1000mA**
41	5.9	7.4	8.7
42	5.4	6.9	7.9
43	4.9	6.1	6.8
Avg	5.4	6.8	7.8

Market Impact of Project

Advancements in PSS pattern design and LED die architecture have improved the light output performance of Lumileds LUXEON Q product by more than 8% allowing future expansion of this technology to more applications.

PSS Comparison to TFFC State of the Art

- LUXEON Q is the first generation PSS product from Lumileds – introduced in 2013
- Product is a PSS flip-chip die attached to reflective submount (not a CSP product)
- At introduction the initial efficacy lagged behind the TFFC product leader LUXEON
- Product Spec sheet revised in 2014 for LUXEON Q based on improved flux!



LUXEON Q

LUXEON Q *Increase in flux from 2014 to 2015 (data sheet values)*

Luxeon Q Product		May 2014	Jan 2015				PSS2-G2 effect
Lumileds Part Number	Nominal CCT (K)	Typical Luminous Flux (lm) 350 mA	Typical Luminous Flux (lm) 350 mA	Typical Efficacy (lm/W) 350 mA	700 mA	1000 mA	% increase
L1Q0-278000000zzz0	2700K	100	113	115	97	87	13.0%
L1Q0-308000000zzz0	3000K	102	115	117	99	88	12.7%
L1Q0-358000000zzz0	3500K	106	117	119	102	92	10.4%
L1Q0-407000000zzz0	4000K	123	132	134	115	104	7.3%
L1Q0-577000000zzz0	5700K	127	134	136	118	106	5.5%

Market Impact: Looking Forward

The PSS2 die in a LUXEON Q package offers performance on par with best TFFC products.

- 1mm^2 die in a 3.5x3.5 mm ceramic package,
- non-Lambertian radiation profile.

We are presently working toward achieving the same PSS performance in smaller packages to meet targeted market applications in the illumination markets.

- 2.5x2.5mm and smaller packages
- Option for direct-attached and unpackaged devices
- Lambertian radiation profiles.
- >130Lm/W for warm white (3000K/80 CRI) at 350mA/mm

Project Integration and Collaboration

Project Integration:

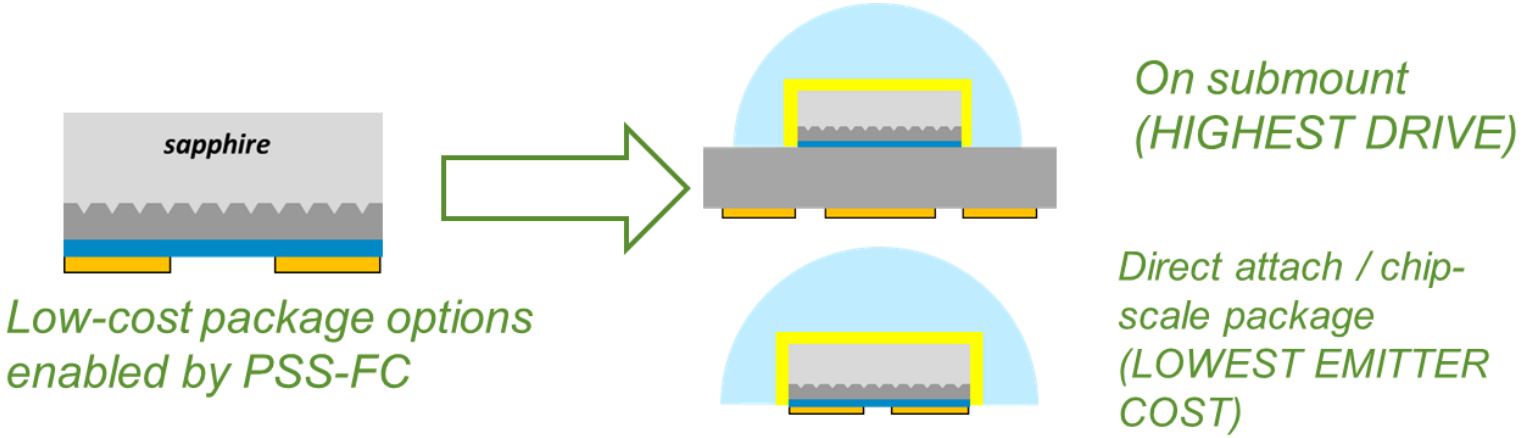
- This project is a collaboration of Lumiled's staff in (1) Technology Development (2) Manufacturing Operations and (3) Product Development and (3) Sales and Marketing.
- The demands of our customers and emerging applications are identified by the Marketing and Product Development teams and drive the future requirements for size, performance and cost.
- Lumileds Technology Development and Manufacturing teams have collaborated closely to ensure timely industrialization of new processes and methods developed in this program.
- All funded work has been performed internally at our San Jose, CA facility without subcontracts.

Communications:

Results have been communicated in regular reports to DoE SSL division, annual peer review meetings and SSL's R&D workshops.

Next Steps and Future Plans

- Establish low-cost next generation emitter architectures for illumination products.
- *Applications are demanding smaller footprints, lower profiles, higher performance and lower cost!*



Current Tasks and Challenges of PSS architectures

- Maintaining high Lm/W in smaller package sizes
- Obtaining high-efficacy with directional illumination (managing side-emission).
- High ESD robustness in direct attach products

REFERENCE SLIDES

Project Budget

Project Budget: Total allocated budget for 2 years is $3,781,783 with 50% cost share

Variances: As of February 2015 there is a variance of $402,026.

Cost to Date: $2,599,424 out of $3,781,783 has been spent through Feb 2015 (DOE portion is 50%).

Additional Funding: None

Budget History					
August 1, 2013 – FY2014 (past)		FY2015 - July 31, 2015 (current – end date)		FY2016	
DOE	Cost-share	DOE	Cost-share	DOE	Cost-share
$1,048,732	$1,048,732	$842,160	$842,160	NA	NA

Project Plan and Schedule

Project start: August 1, 2013

Project finish: July 31, 2015