Print-based Manufacturing of Integrated, Low Cost, High Performance SSL Luminaires

2015 Building Technologies Office Peer Review

Screen printer & Dryer

Furnace

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

Sridhar R. Nimma,
sridharrnimma@eaton.com
EATON Corporation

Project Summary

Timeline:

Start date: 9/15/2013

Planned end date: 12/31/2015

Key Milestones

1. Increase LED Fixture Lifetime; 6/15/2014
2. Decrease cost of LED Fixture; 12/15/2015

Budget:

- Budget: $4,937,345 / 50% Cost Share
- Budget Period 1 complete

Budget period	DOE	Eaton
1	$ 1,072,691	$ 1,072,690
2	$ 1,395,981	$ 1,395,983

Target Market/Audience:

General Illumination Applications.

Key Partners:

Cooper Lighting by EATON — S. Nimma, Dr. C. Bohler, R. Modi, J. Trublowski, C. Shane

Heraeus — R. Persons, D. Malanga, M. Challingsworth

HaikuTech Multilayer Ceramics — R. Höppener, R. Vanolmen, A. Karbasi

Project Goal:

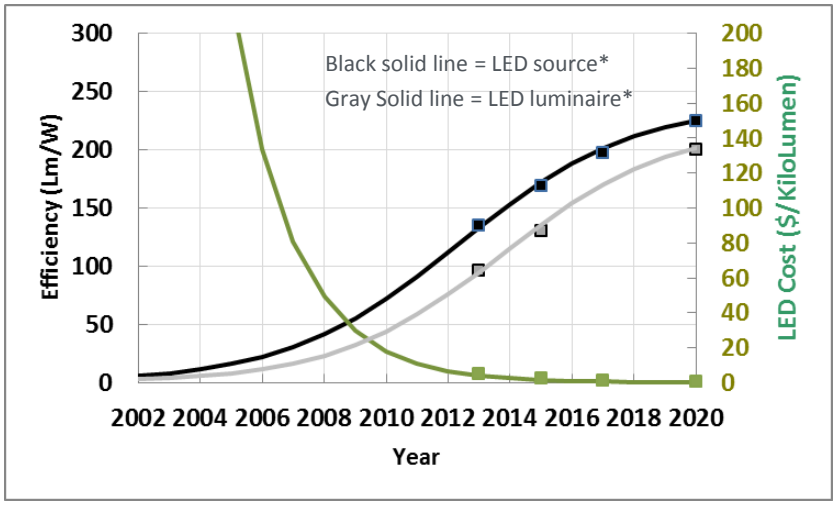
The objective of the project is to increase adoption of solid-state lighting through an integrated manufacturing process to produce high quality products at reduced cost with increased production throughput to meet rapidly rising demand.

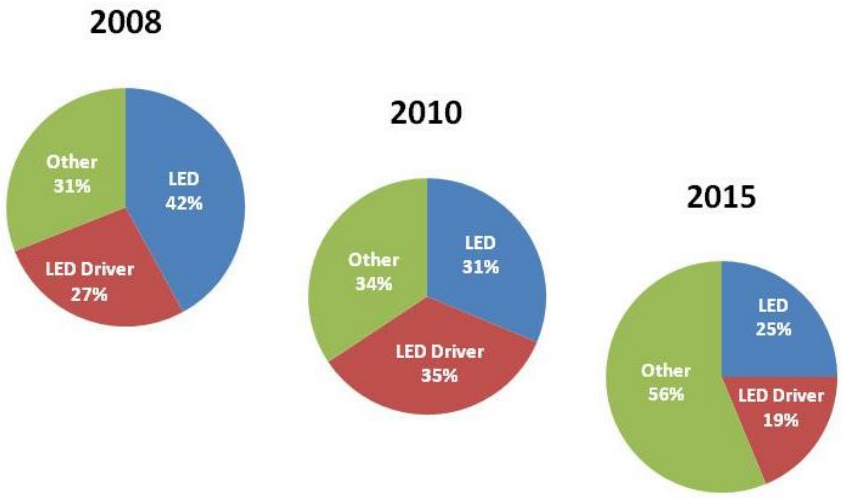
Project Purpose

DOE Areas of Interest (AOI) Projections

AOI Metric (s)	Status at Start of Program	2015 Target(s)	Program Target
Manufacturing Throughput	N/A	x2 Increase	3.07x
OEM Lamp Price	$50/klm	$10/klm	0.94/klm-3.13/klm
Assembly Cost ($)	N/A	50% reduction every 2 -3 years	-75%
Color Control (SDCM)	7	4	4

LED/Luminaire Efficiency and Cost Roadmaps





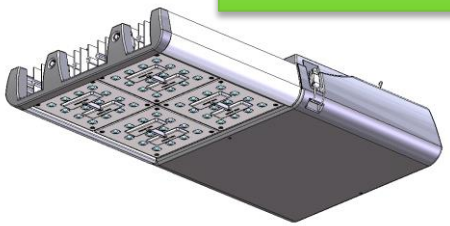
DOE Solid-State Lighting Research and Development Multi-Year Program Plan, April 2014.
**Fit lines added*

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

Program Objectives / Technology Description (L1-L4)

Standard Design:

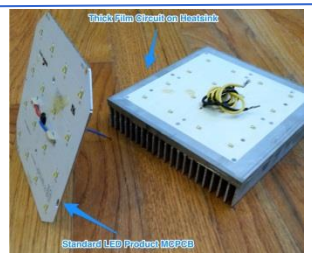
L1



Baseline

- Traditional LED Fixture
- High Manual Assembly Costs
- HighThermal Resistance
- Separate Driver Assembly
- High Material Costs (Heatsink, Wires, Gaskets, Housings, TIM)

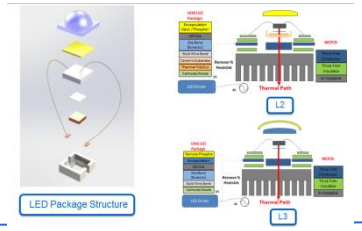
L2



15% Cost Improvement

- Replaces MCPCB and TIM with Printed Circuit on Heatsink
- Improved Thermal Resistance
- Lower Manual Assembly Costs

L3



28% Cost Improvement

- Replaces MCPCB and TIM with Printed Circuit on Heatsink
- Improved Thermal Resistance
- Lower Manual Assembly Costs

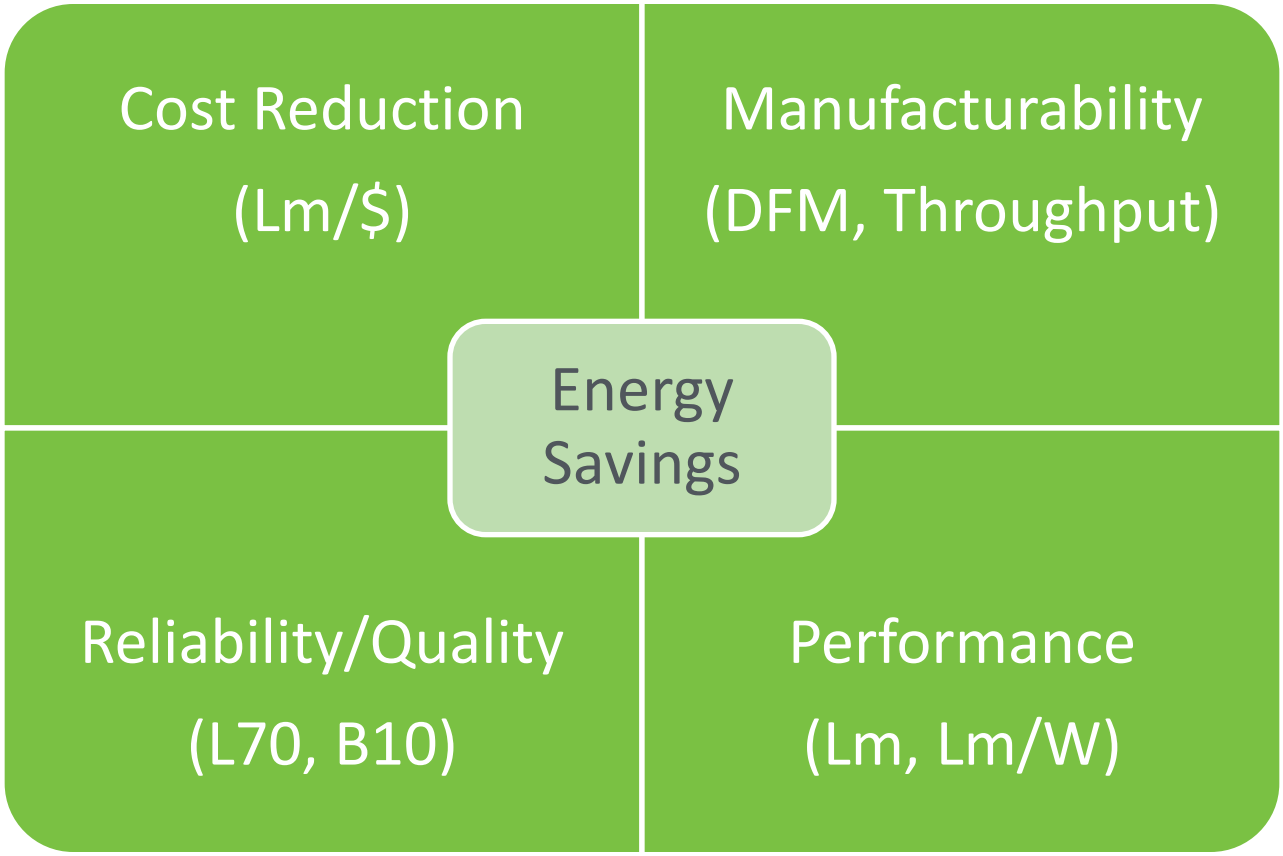
L4

45% Cost Improvement

- Integrated Driver Circuit
- Full/Optimal Level of Integration
- Full Automation of Electronics Component Assembly (SMT)
- Additional Material Savings
- Less Sealing Required
- Additional Labor Savings

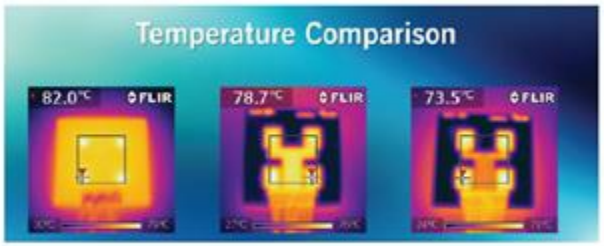
END GOAL

SSL Market Drivers



Project End Goal

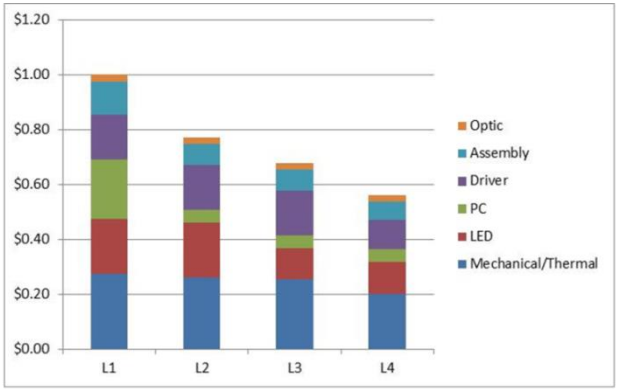
- Increase LED Fixture Lifetime



8.5 ° C Decrease

Thermal Improvement Options:
- 1.8 – 2X Lifetime increase
- Up to 5% LED count reduction

- Decrease Cost of LED fixture



L1: Traditional PC approach
L2: LED Pkg on Heatsink
L3: LED Chip Scale Package on Fixture
L4: L3 + Integrated Electronics

Project Goals in line with DOE Energy savings Goal and Luminare FY20 Milestone targets

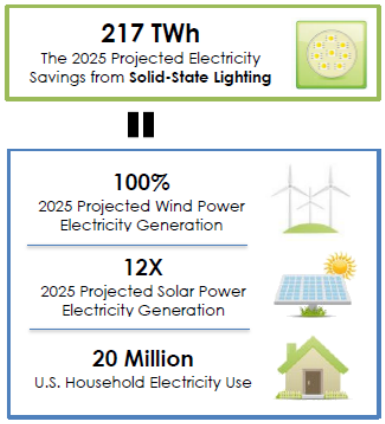


FIGURE 1.1 2025 PROJECTED ELECTRICITY SAVINGS FROM SSL [3]

TABLE 4.4 LED PACKAGE AND LUMINAIRE MILESTONES

Year	Milestones
FY10	Package: >140 lm/W (cool-white); >90 lm/W (warm-white); <$13/klm (cool-white)
FY12	Luminaire: 100 lm/W; ~1,000 lumens; 3500K; 80 CRI; 50,000 hours
FY15	Package: ~$2/klm (cool-white); ~$2.2/klm (warm-white)
FY17	Luminaire: >3,500 lumens (neutral-white); <$100; >150 lm/W
FY20	Luminaire: 200 lm/W Smart troffer with integrated controls: <$85

Note: Packaged devices measured at 25°C and 35 A/cm^2.

DOE Solid-State Lighting Research and Development Multi-Year Program Plan, April 2014

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

Approach : Thick Film Process

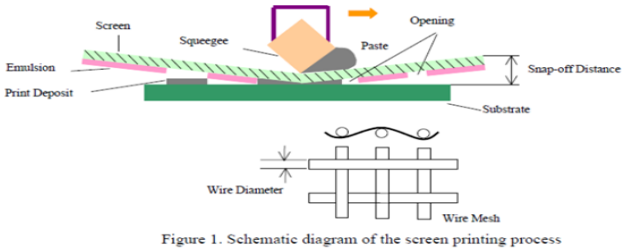
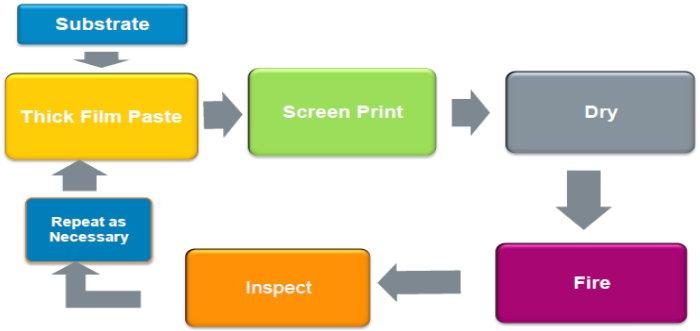


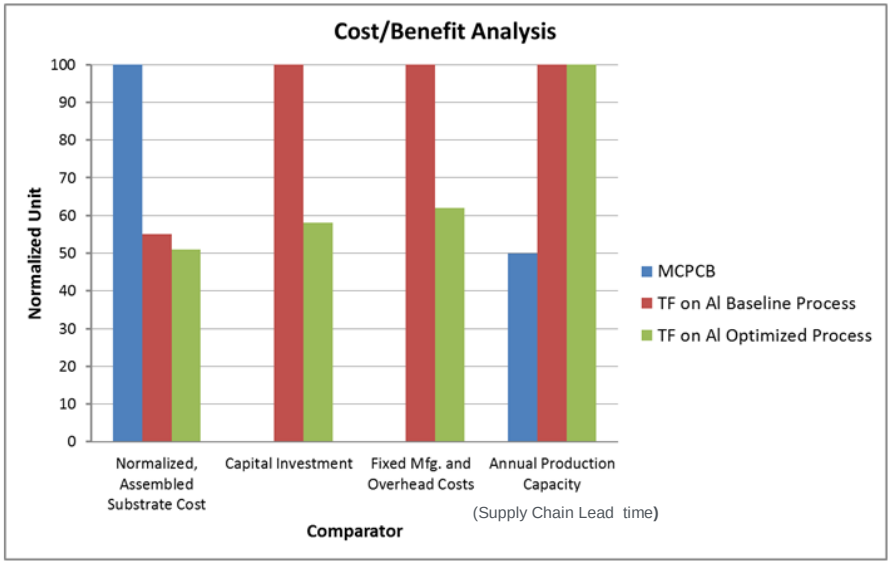
Figure 1. Schematic diagram of the screen printing process

* Screen Printing Method



Cycle Is Repeated Multiple Times for Each Circuit Layer

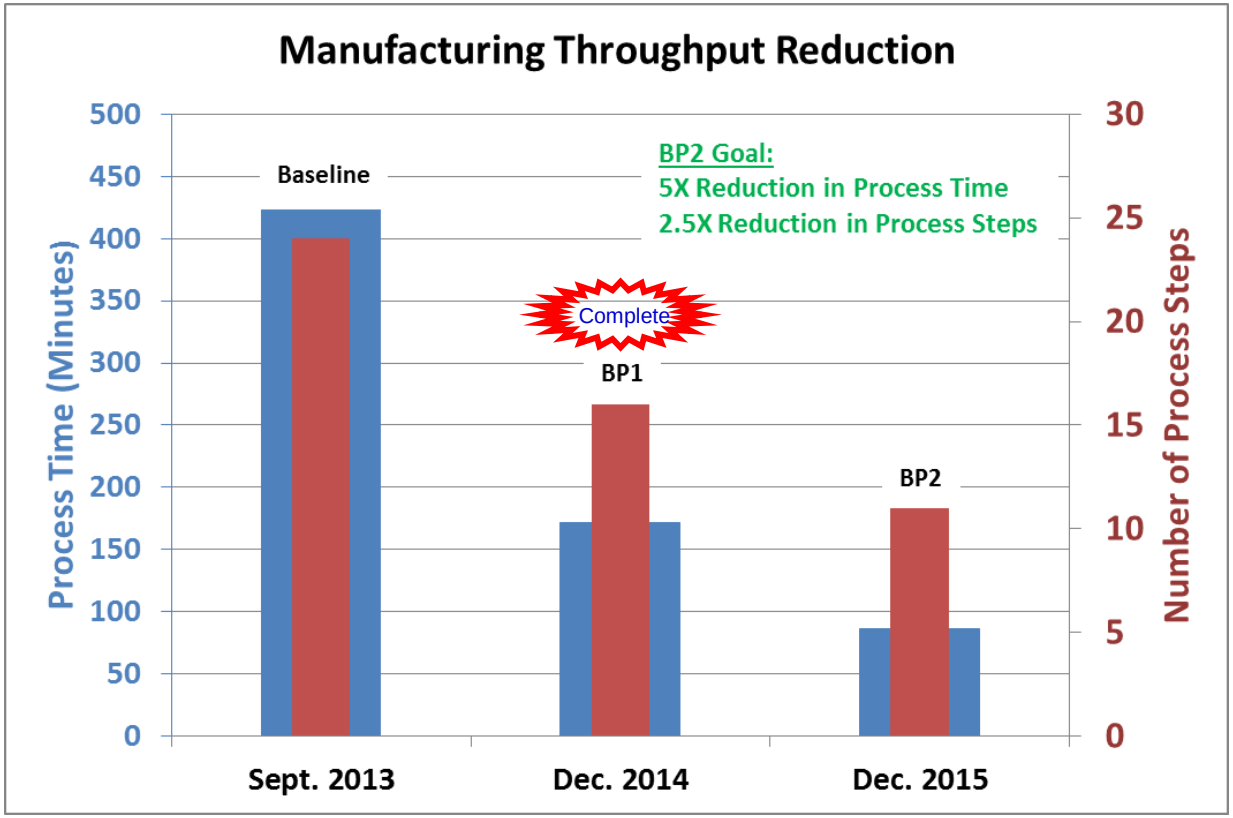
Benefits of this Project



1. Increased Automation
2. Manufacturing Flexibility.
3. Reduced Lead time.
4. Less Inventory of complex parts.

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

Key Focus Area: Process Improvement

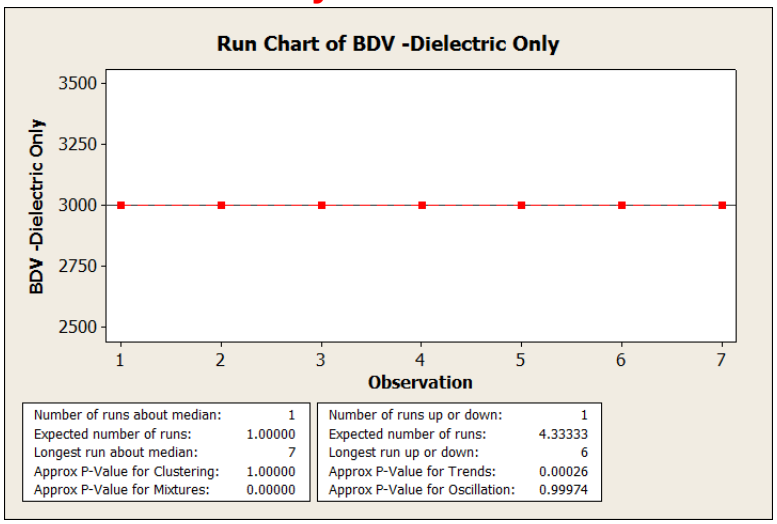


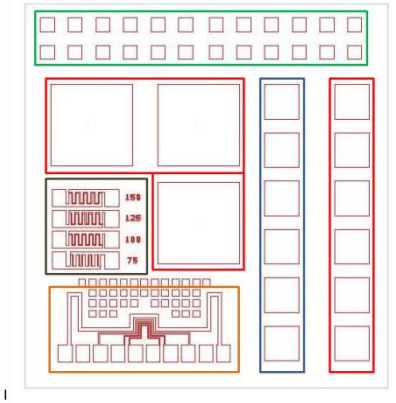
BP1 Results:

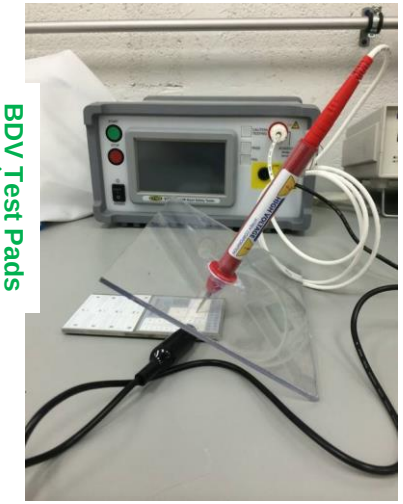
- **Process Step-count reduced by 8**
- **Process Time reduced by 251 minutes**
- **Projected AOI Metric met for Systemic Throughput, $/klm and Assembly Costs**

Key Focus Area: AC Breakdown Voltage (BDV) Variability

Dielectric Only: Excellent Results

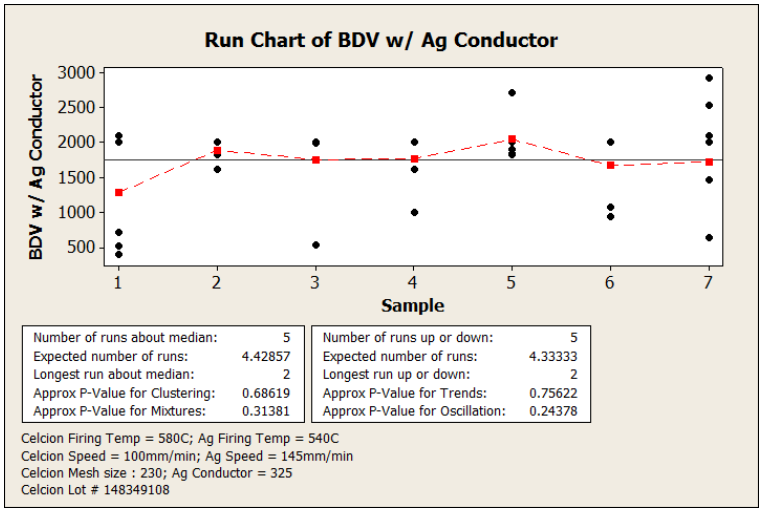


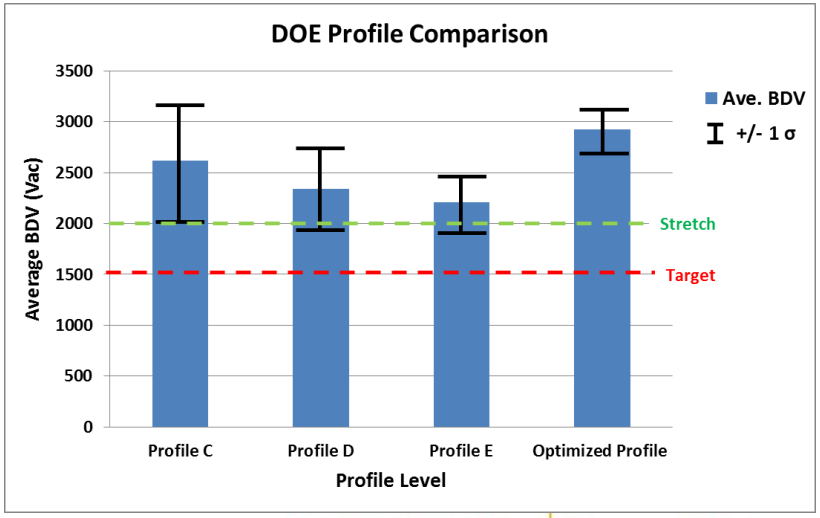




Test Method

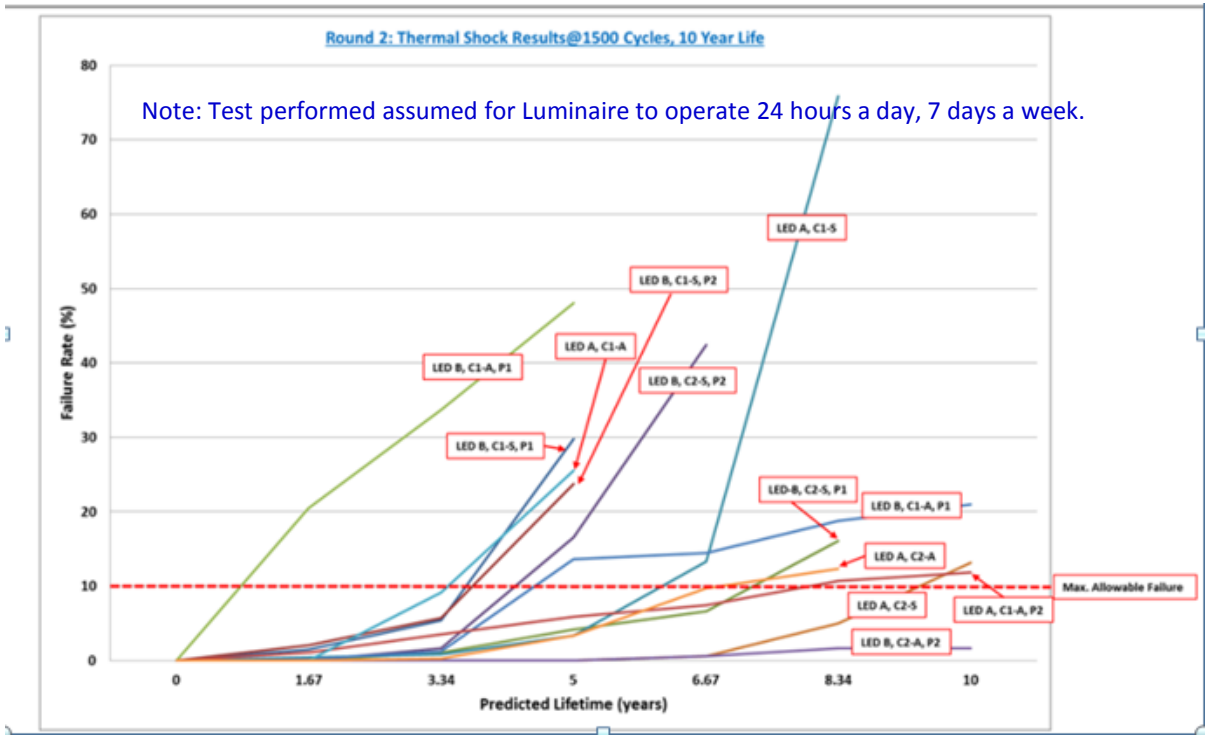
Conductor Interactions



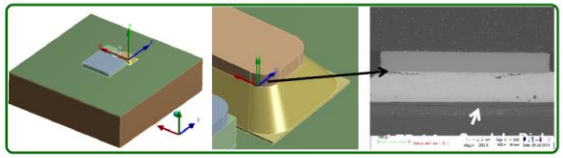


U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

Key Focus Area: CTE Mismatch Reliability Validation



Life Summary for -40C-85C-Luxeon- New Solder Profile							
Solder	Location	Mean Case		Best Case		Worst Case	
		Small Pad	Medium Pad	Small Pad	Medium Pad	Small Pad	Medium Pad
Small Solder	Top	5.04E+02	6.35E+02	1.42E+03	1.83E+03	2.11E+02	2.61E+02
Small Solder	Bottom	4.96E+03	1.93E+04	1.80E+04	8.14E+04	1.69E+03	5.82E+03
Large Solder	Top	1.83E+04	1.84E+04	7.69E+04	7.74E+04	5.55E+03	5.58E+03
Large Solder	Bottom	3.33E+04	2.18E+04	1.49E+05	9.30E+04	9.56E+03	6.49E+03
Life required is 1500 Cycles							



- Failure locations match with actual failure (211 in Analysis vs. 196 in Test)
- Medium pad has more life than small pad (265 in MP vs. 211 in SP)

Take Away

- Many parameters need to be considered (conductor material, LED construction, substrate and pad geometry, etc.) to optimize both the model and substrate design for lifetime and reliability
- Several configurations successfully achieved the thermal shock goal in test
- Good correlation was achieved between the model and test, however, further model refinements are needed to fully exploit the applicability for all designs

Progress and Accomplishments

Thermal Stress simulation output matches experimental data on single LED and stacked construction.

Thermal Shock Reliability analysis indicates that the design parameters have a significant effect on the lifetime.

The Optimized Process based on Lab scale equipment has reduced the number of Process Steps by 8 while reducing the total Process Time by 251 minutes.

Proof of Concept designs initiated to demonstrate L2/L3/L4 on Outdoor, Recessed and Ambient Platforms. Initial designs completed and IP filed.

Progress and Accomplishments

Lessons Learned

- Ability to control material interactions through process control is key in fabrication of consistent, high quality substrates
- Targeting the applications early in the development phase will appropriately limit the experimental scope (i.e. don't try to boil the ocean)
- The SSL market changes very quickly and the ability to recognize and implement new technology quickly (i.e. CSP vs chip and wire for L3) is key to making sure that the concepts demonstrated are relevant

Chip Scale Package (L3)

Market Impact:

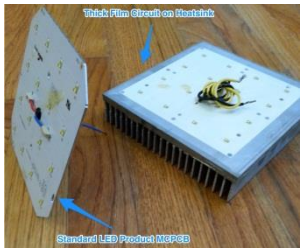
Project planning & activities defined to meet Project Goals

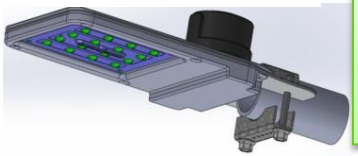
~ 4000 – 5000 Lumens

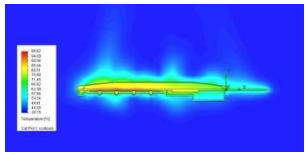
OVH HID 2010
100W; 2234 in³

XNV LED 2013
50W; 695 in³

TF LED 2015
42W; 232 in³

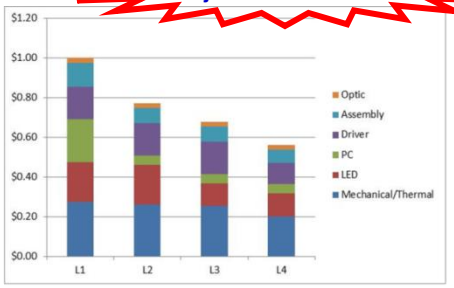






Integrated / Optimized
- Electronics (PCB, Driver, LED's)
- Heatsink
- Housing
- Optics

On Track to meet Project End Goal



L1: Traditional PC approach
L2: LED Pkg on Heatsink
L3: LED Chip Scale Package on Fixture
L4: L3 + Integrated Electronics

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

Next Steps

Equipment readiness , Process validation, Throughput Analysis and Cost Validation for pilot production at Peachtree City Facility.

Reliability validation of Chip Scale Packages .

Demonstrate and perform system level Reliability Validation of driver components directly onto a fixture (Level 4 or L4).

Demonstrate flexible manufacturing for non-planar and recessed product designs.

Build Proof of concepts and perform validation study on Recessed, Ambient and Roadway Products.

Project Integration and Collaboration

Partners, Subcontractors, and Collaborators

EATON/Cooper Lighting:
- Full design and manufacturing of LED lamps and fixtures
- Full, in-house testing capability
- Extensive component supply base

EATON Corporate Research and Technology (CRT):
- 25 Years experience in Thick Film Technology
- Extensive materials analysis capability
- Expertise in running government programs

Heraeus:
- Manufacturing of thick film materials
- Internal R&D staff for new material and process development
- Fully facilitized for development of new thick film processes

HaikuTech:
- Production level design and manufacture of Thick Film equipment
- Pilot Thick Film line in Miami, FL
- Internal processing expertise

Communications:
- DOE Manufacturing Workshop: May,2014
- Peer Review Event: June,2014
- DOE Workshop 2015: January,2015

Project Budget

Project Budget: $4,937,345.

Variances: In July 2014, budget period 1 was extended by 3 months. The budget was modified reducing budget period 1 by approx. $793k and increasing budget period 2 by the same. The cost of the manufacturing process equipment and facility improvements were removed from the DOE program in order to perform additional effort including: full scale reliability testing, expanded electronic design beyond reference level, expanded fixture prototyping and to improve manufacturing capacity and throughput.

Cost to Date: Budget Period 1 complete; Total cost incurred (2/28/2015): $2.16M

Additional Funding: None

Budget History

9/15/2013 – 12/31/2014 BP 1 (complete)		1/1/2015-12/31/2015 BP 2 (In Process)		FY2016 (planned)	
DOE	Cost-share	DOE	Cost-share	DOE	Cost-share
$1,469,116	$1, 469,116	$ 999,556	$ 999,557	$ 0	$ 0
(396,425)	(396,426)	396,425	396,426	$ 0	$ 0
$1,072,691	$1,072,690	$1,395,981	$1,395,983	$ 0	$ 0

Project Plan and Schedule

Budget Period	Budget	Start Date	End Date
1	$2,145,381	09/15/2013	12/31/2014
2	$2,791,964	01/01/2015	12/31/2015

Deliverables and Major Milestones *(Equipment / Management)*	Due Date	Status R/Y/G
No-Cost extension Approval	7/14	
EATON's Capital Approval & Equipment PO release	6/14	
Lab Approval / initialization	7/14	
Lab Construction complete	9/14	
PTC Laboratory Operational	6/15	

Deliverables and Major Milestones *(Technical)*	Due Date	Status R/Y/G
CTE Mismatch Modeling / Reliability qualification.	9/14	
Equipment Specification and ordering	6/14	
L3 Demonstration – CSP route definition	7/15	
Equipment readiness at PTC Lab	6/15	
Throughput Analysis	9/15	
Proof of Concepts - Demonstration	11/15	

Current Activities

- Demonstration of reduced mfg process steps (27 to 11) on Larger Substrates.
- Design guides for Chip Scale Packages.
- Reliability Samples build for CSP LED's.
- Evaluation of the equipment build to meet project guidelines.
- Proof of concepts design initiation.

Future Work

- Integrated DRIVER design prototypes and reliability study.
- Equipment installation at PTC facility.
- Throughput Analysis of process at PTC Facility.
- Demonstration of proof of concepts with Thick Film line at PTC lab.