FREEDM SYSTEMS CENTER

# Flexible Large Power Solid State Transformer (FLP-SST)

FREEDM Systems Center
North Carolina State University

Dr. Subhashish Bhattacharya

Aug 2019

NC STATE UNIVERSITY
ASU Arizona State University
Florida State University
Florida A&M University
Missouri S&T
RWTH Aachen University
ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich
The University of Auckland Maidment Theatre

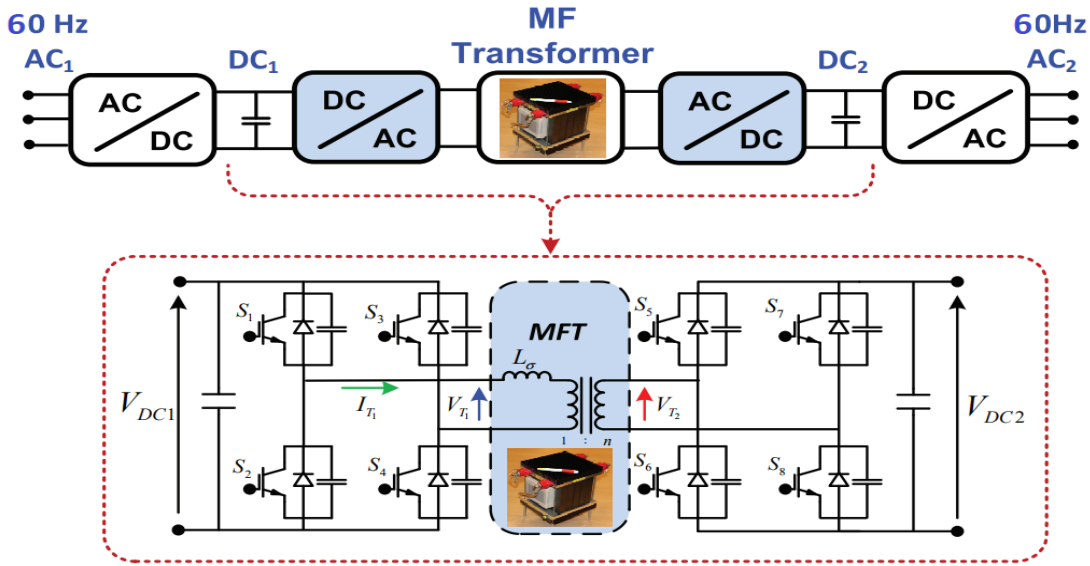
# Large power transformer in US electric grid

- Large power transformers (LPTs) – most critical component of the electric grid
- Due to their large physical dimension and custom design are neither interchangeable nor stored as a spare inventory
- Failure of such LPTs is concern to maintain grid resiliency and reliability since replacement of such LPTs involve longer lead times, special transportation arrangement, man – power and capital expenditure.
- To mitigate some of these concern a **modular, scalable, efficient** and **rapid recovery** solution is proposed.


Transportation of a large power transformer.

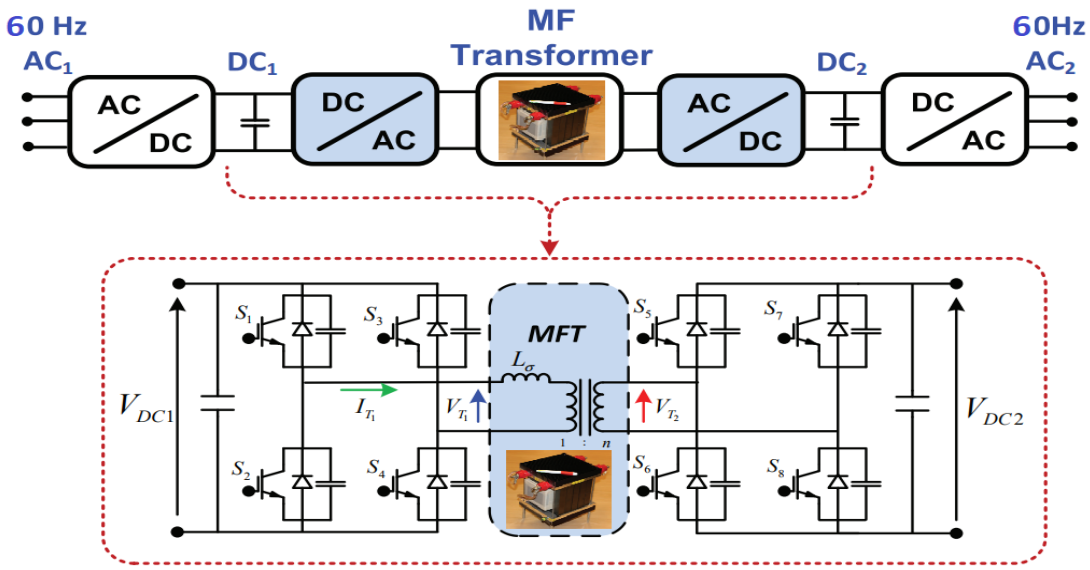
# Project Objectives

- A modular solution, where flexible voltage ratings will be achieved by series/parallel connection of a basic building block (a power electronics based medium frequency transformer to achieve required voltage isolation and variable step-up and step-down voltage ratios)



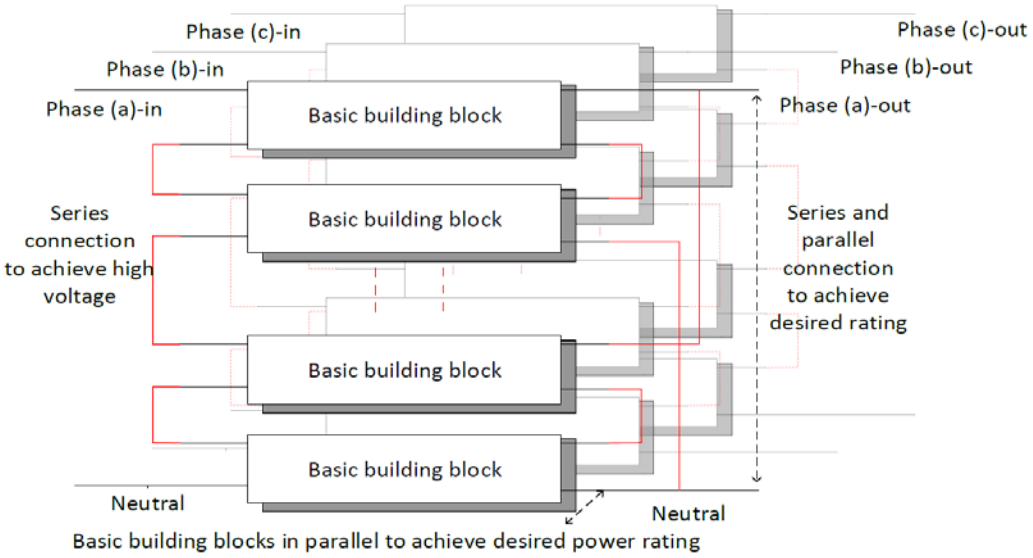
# Technical Approach

- A basic building block of consisting of the following stages to form Flexible Large Power Solid State Transformers.
  1. AC-DC Rectifier Stage
  2. Isolated DC-DC transformer converter stage, with medium-frequency transformer with variable buck-boost voltage step-up and step down ratios.
  3. DC-AC inverter stage



# Technical Approach

FLPSST realization using series and parallel connection of the basic building blocks.

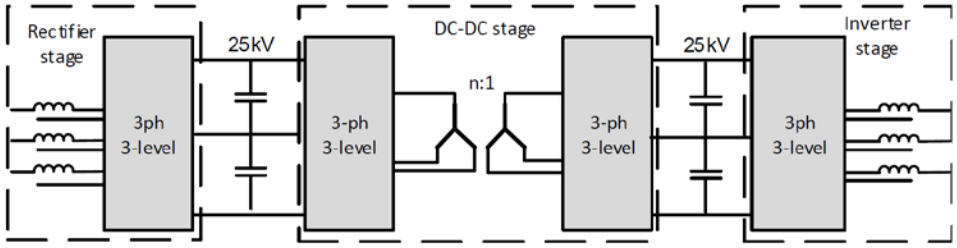



10kV and 15kV MOSFETs/IGBTs open up possibility of using simple circuitry. Also they reduce size and enable air cooled thermal management.

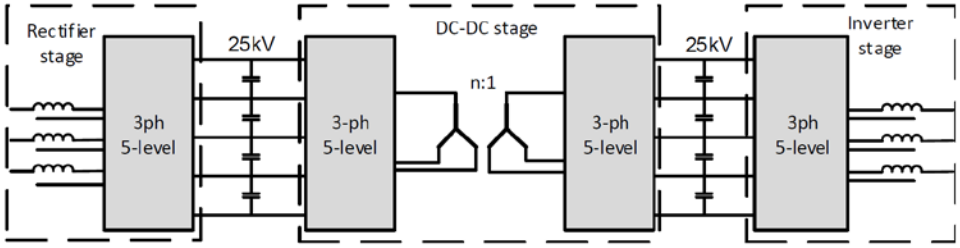
# Possible Topologies for the Building Blocks

preliminary assessment of 1, 2 and 5 MVA basic building blocks were carried out using the latest medium voltage SiC devices.

1. 10 kV SiC-MOSFET and 15 kV JBS Diode.
2. 15 kV SiC-IGBT and 15 kV JBS Diode.




3-level FLPT-BB topology using 10kV SiC-MOSFET devices.

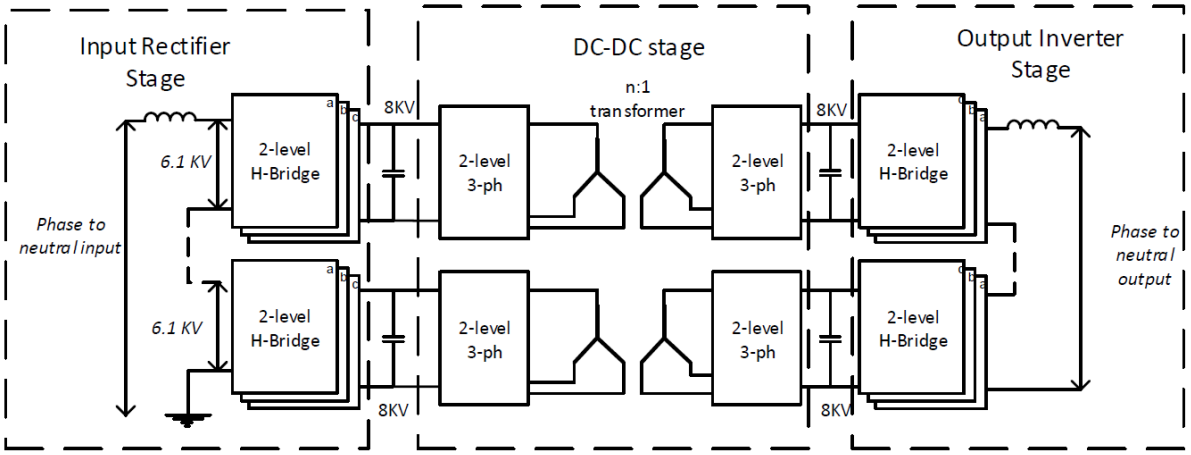



5-level FLPT-BB topology using 10kV SiC-MOSFET devices.

# Possible Topologies for the Building Blocks

preliminary assessment of 1, 2 and 5 MVA basic building blocks were carried out using the latest medium voltage SiC devices.

1. 10 kV SiC-MOSFET and 15 kV JBS Diode.
2. 15 kV SiC-IGBT and 15 kV JBS Diode.

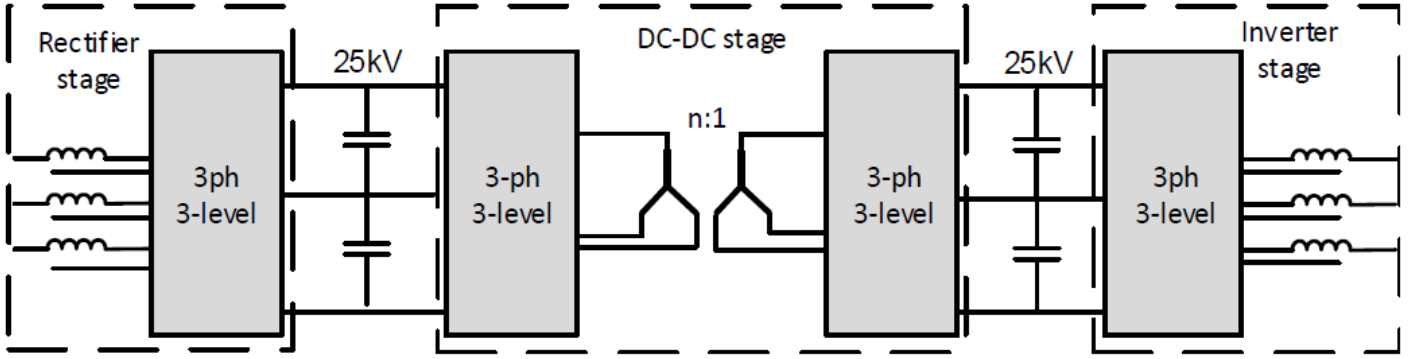



2-level Cascade H-Bridge (2L-CHB) FLPT-BB using 10kV SiC-MOSFETs.

# Possible Topologies for the Building Blocks

preliminary assessment of 1, 2 and 5 MVA basic building blocks were carried out using the latest medium voltage SiC devices.

1. 10 kV SiC-MOSFET and 15 kV JBS Diode.
2. 15 kV SiC-IGBT and 15 kV JBS Diode.




3-level FLPT-BB topology using 15kV SiC-MOSFET devices.

# Possible Topologies for the Building Blocks

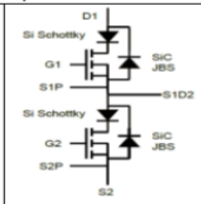
## Summary

1. 10 kV SiC-MOSFET and 15 kV JBS Diode.
2. 15 kV SiC-IGBT and 15 kV JBS Diode.

**10kV SiC-MOSFET three-phase FLPT Transformer building blocks (3ph-FLPTBBs)**

Power rating: 1 – 2 – 5 MVA
Input voltage: 13.8kV
Output voltages: 4.16
Technology: 10kV SiC MOSFET and JBS Diode
Device: CREE Inc. 10kV SiC DMOSFET/JBS Diode Half H-Bridge Module
Device current rating: 240A

10kV Half H-Bridge Module Capable of 240A When Fully Populated



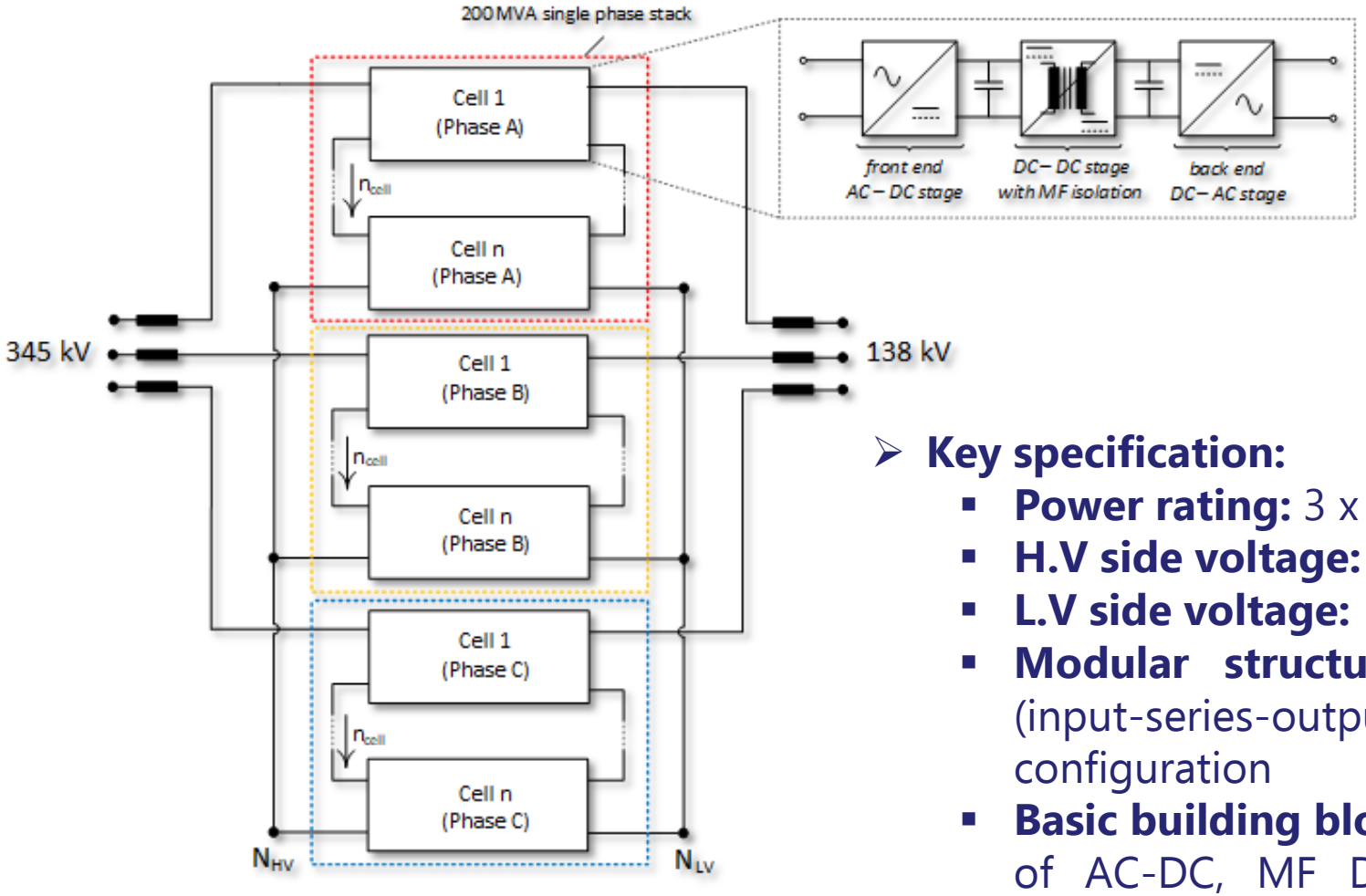

| Topology | Power Rating (MVA) | DC-link | | Output AC rms current @ 4.16kV | # of devices | AC-DC stage @ 10kHz | DC-DC stage @ 20kHz | DC-AC stage @ 10kHz | Total | DC-DC Transformer @ 20kHz | | Weight (lb) (1.3x factor included)[1] | Volume ($m^3$) (2.5x factor included)[2] | Losses (kW) | Efficiency (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Voltage (kV) | Current (A) | | | | | | | Weight (lb) | Volume ($m^3$) | | | | |
| 5-level | 1 | 25 | 40 | 139 | switch | 48 | 72 | 24 | 144 | 120 | 0.5 | 757 | 1.54 | 13 | 98.7 |
| | | | | | diode | 18 | 36 | 18 | 72 | | | | | | |
| | 2 | | 80 | 278 | switch | 48 | 96 | 48 | 192 | 240 | 1 | 1085 | 2.33 | 31.4 | 98.4 |
| | | | | | diode | 18 | 54 | 36 | 108 | | | | | | |
| | 5 | | 200 | 695 | switch | 48 | 144 | 96 | 288 | 600 | 2.5 | 2496 | 5.45 | 144.3 | 97.1 |
| | | | | | diode | 18 | 90 | 72 | 180 | | | | | | |
| 3-level | 1 | 25 | 40 | 139 | switch | 24 | 36 | 12 | 72 | 120 | 0.5 | 397 | 0.92 | 8 | 99.2 |
| | | | | | diode | 6 | 12 | 6 | 24 | | | | | | |
| | 2 | | 80 | 278 | switch | 24 | 48 | 24 | 96 | 240 | 1 | 724 | 1.71 | 18.8 | 99.06 |
| | | | | | diode | 6 | 18 | 12 | 36 | | | | | | |
| | 5 | | 200 | 695 | switch | 24 | 72 | 48 | 144 | 600 | 2.5 | 1570 | 3.86 | 86.4 | 98.2 |
| | | | | | diode | 6 | 30 | 24 | 60 | | | | | | |
| 2-level CHB | 1 | 8 | 62.5 | 139 | switch | 24 | 24 | 96 | 168 | 120 | 0.5 | 397 | 0.92 | 19.2 | 98 |
| | | | | | diode | 0 | 0 | 0 | 0 | | | | | | |
| | 2 | | 130 | 278 | switch | 24 | 48 | 144 | 288 | 240 | 1 | 724 | 1.71 | 77.6 | 96 |
| | | | | | diode | 0 | 0 | 0 | 0 | | | | | | |
| | 5 | | 312.5 | 695 | switch | 24 | 72 | 336 | 552 | 600 | 2.5 | 1570 | 3.86 | 355.7 | 94.8 |

Selected topology

10kV SiC-IGBT/JBS Diode three-phase FLPSST possible building blocks.

# Flexible Large Power Solid State Transformer (FLPSST)

## ➢ System overview and key specifications




➢ **Key specification:**

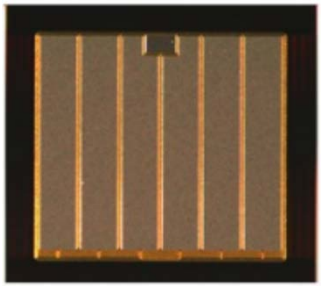
- **Power rating:** 3 x 200 MVA
- **H.V side voltage:** 345 kV
- **L.V side voltage:** 138 kV
- **Modular structure** with ISOS (input-series-output-series) configuration
- **Basic building block** comprising of AC-DC, MF DC-DC, DC-AC stage

FREEDM SYSTEMS CENTER

## ➢ Power semiconductor devices

### ➢ 6.5 kV SiC MOSFET

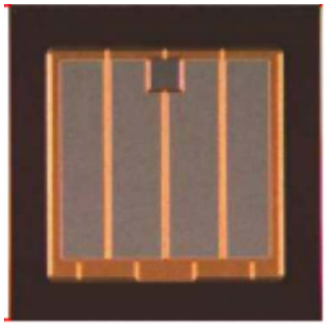
- **$V_{DS}$:** 6.5 kV
- **$I_D$:** 30 A
- **specific $R_{DS(on)}$ :** 80 mΩ



8.4 mm x 8.4 mm
6.5 kV SiC MOSFET bare die

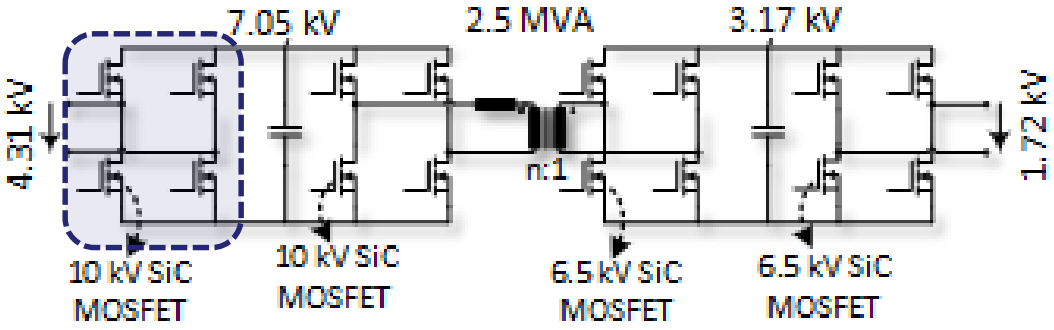
### ➢ 10 kV SiC MOSFET

- **$V_{DS}$:** 10 kV
- **$I_D$:** 20 A
- **Specific $R_{DS(on)}$:** 350 mΩ



8.1 mm x 8.1 mm
10 kV SiC MOSFET bare die

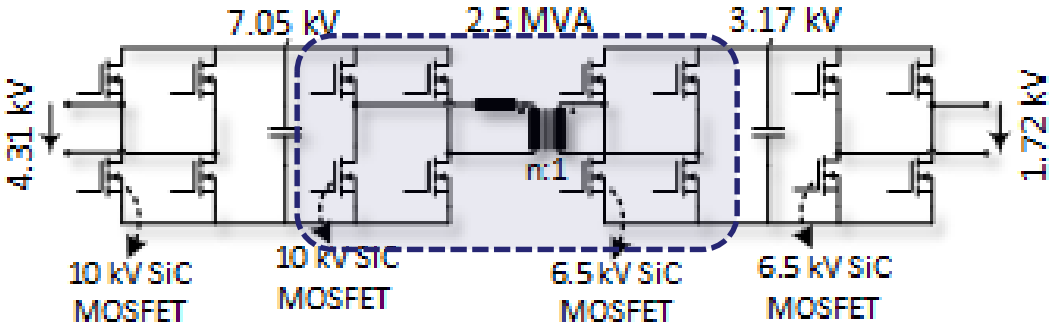
# 2.5 MVA basic building block topology: Type - A




- **Power rating:** 2.5 MVA
- **$n_{cell}$:** 80

| Parameter | Value |
|---|---|
| Cell input side DC link voltage | 7.05 kV |
| Cell input side AC rms voltage and current | 4.31 kV, 579.12 A |
| Cell input side peak current | 818.99 A |
| Cell AC-DC stage switching frequency | 10 kHz |
| Cell AC-DC stage devices<br>Number of devices per switch position | 10 kV SiC MOSFETs<br>55 x 10 kV/20 A SiC MOSFETs |

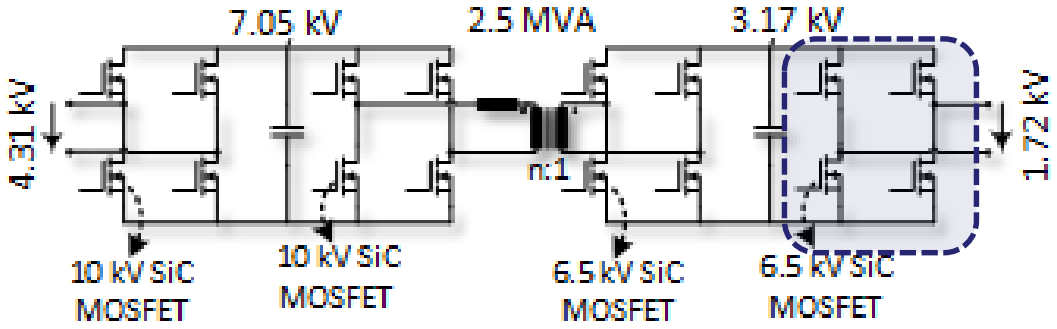
# 2.5 MVA basic building block topology: Type - A




- **Power rating:** 2.5 MVA
- **$n_{cell}$:** 80

| Parameter | Value |
|---|---|
| Cell DC-DC stage transformer specification | n:1 = 2.22, $L_{lkg} \approx$ 183 µH, VA = 2.5 MVA |
| Cell AC-DC stage switching frequency | 10 kHz |
| Cell DC-DC stage primary side devices<br>Number of devices per switch position | 10 kV SiC MOSFETs<br>55 x 10 kV/20 A SiC MOSFETs |
| Cell DC-DC stage secondary side devices<br>Number of devices per switch position | 6.5 kV SiC MOSFETs<br>55 x 6.5 kV/30 A SiC MOSFETs |

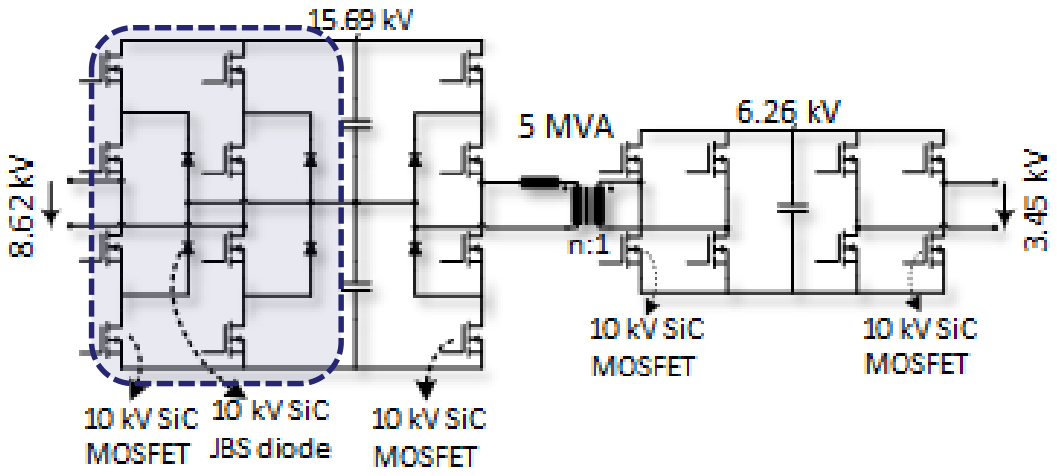
# 2.5 MVA basic building block topology: Type - A




- **Power rating:** 2.5 MVA
- **$n_{cell}$:** 80

| Parameter | Value |
|---|---|
| Cell input side DC link voltage | 3.17 kV |
| Cell input side AC rms voltage and current | 1.72 kV, 1449.27 A |
| Cell input side peak current | 2049.58 A |
| Cell DC-AC stage switching frequency | 10 kHz |
| Cell DC-AC stage devices<br>Number of devices per switch position | 6.5 kV SiC MOSFETs<br>91 x 10 kV/20 A SiC MOSFETs |

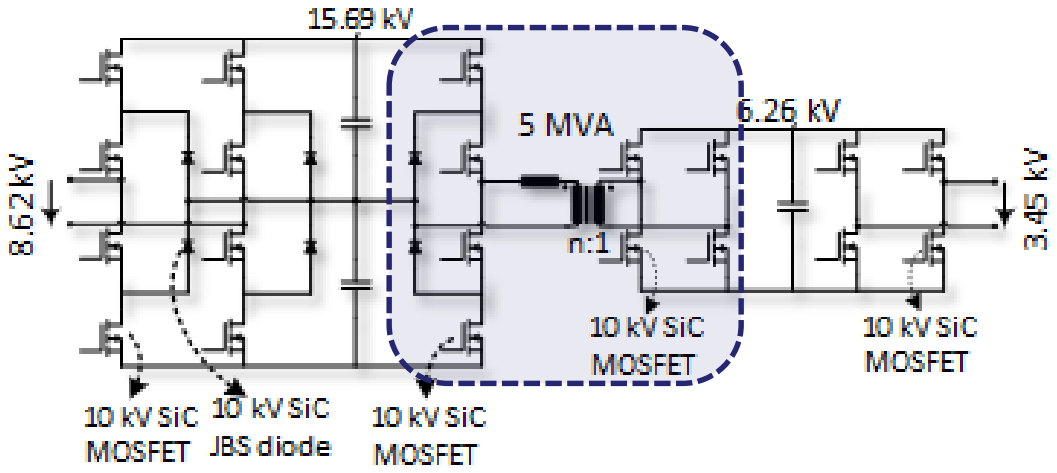
# 5 MVA basic building block topology: Type - B




- **Power rating:** 5 MVA
- **$n_{cell}$:** 40

| Parameter | Value |
|---|---|
| Cell input side DC link voltage | 15.69 kV |
| Cell input side AC rms voltage and current | 8.62 kV, 579.12 A |
| Cell input side peak current | 818.99 A |
| Cell AC-DC stage switching frequency | 10 kHz |
| Cell AC-DC stage devices<br>Number of devices per switch position | 10 kV SiC MOSFETs & JBS diode<br>55 x 10 kV/20 A SiC MOSFETs & JBS diode |

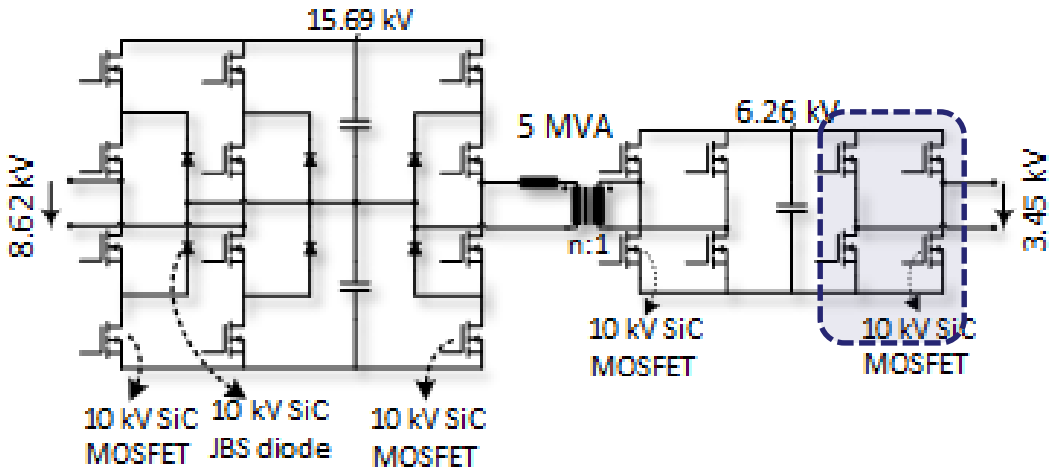
# 5 MVA basic building block topology: Type - B




- **Power rating:** 5 MVA
- **$n_{cell}$:** 40

| Parameter | Value |
|---|---|
| Cell DC-DC stage transformer specification | n:1 = 1.25, $L_{lkg} \approx 115$ µH, VA = 5 MVA |
| Cell AC-DC stage switching frequency | 10 kHz |
| Cell DC-DC stage primary side devices<br>Number of devices per switch position | 10 kV SiC MOSFETs & JBS diodes<br>57 x 10 kV/20 A SiC MOSFETs |
| Cell DC-DC stage secondary side devices<br>Number of devices per switch position | 10 kV SiC MOSFETs<br>71 x 10 kV/20 A SiC MOSFETs |

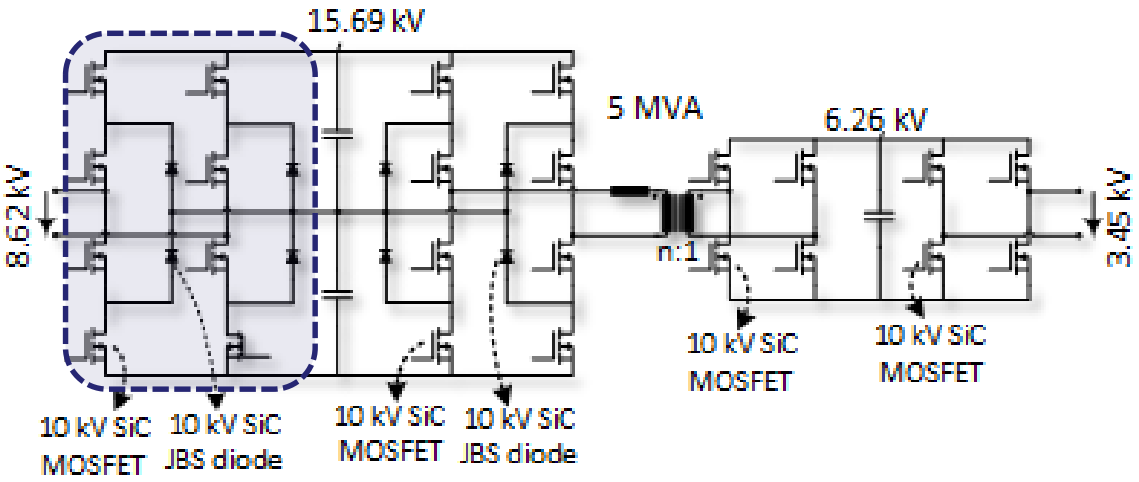
# 5 MVA basic building block topology: Type - B




- **Power rating:** 5 MVA
- **$n_{cell}$:** 40

| Parameter | Value |
|---|---|
| Cell input side DC link voltage | 6.26 kV |
| Cell input side AC rms voltage and current | 3.45 kV, 1449.27 A |
| Cell input side peak current | 2049.58 A |
| Cell DC-AC stage switching frequency | 10 kHz |
| Cell DC-AC stage devices<br>Number of devices per switch position | 10 kV SiC MOSFETs<br>137 x 10 kV/20 A SiC MOSFETs |

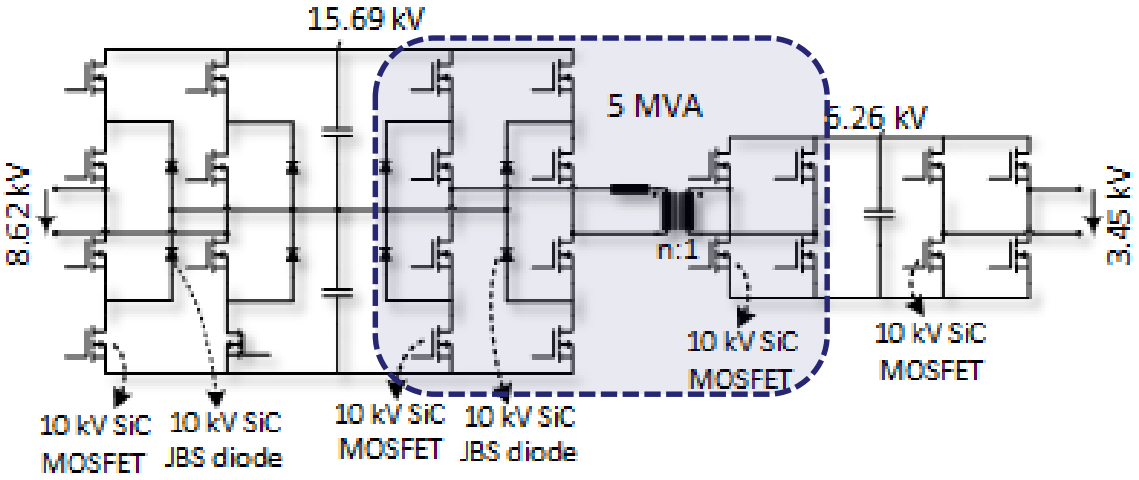
# 5 MVA Basic building block topology: Type - C




- **Power rating:** 5 MVA
- **$n_{cell}$:** 40

| Parameter | Value |
|---|---|
| Cell input side DC link voltage | 15.69 kV |
| Cell input side AC rms voltage and current | 8.62 kV, 579.12 A |
| Cell input side peak current | 818.99 A |
| Cell AC-DC stage switching frequency | 10 kHz |
| Cell AC-DC stage devices<br>Number of devices per switch position | 10 kV SiC MOSFETs & JBS diode<br>55 x 10 kV/20 A SiC MOSFETs & JBS diode |

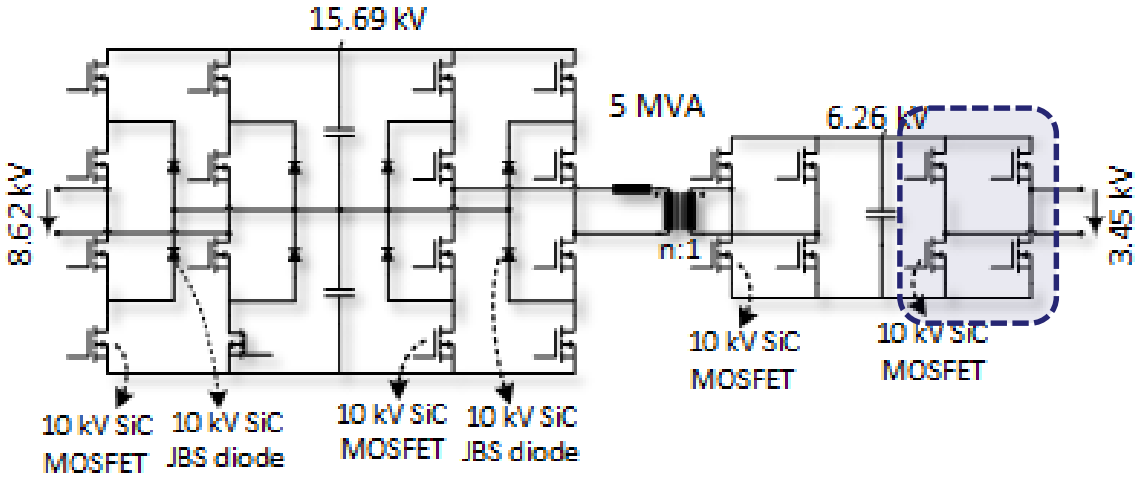
# 5 MVA basic building block topology: Type - C




- **Power rating:** 5 MVA
- **$n_{cell}$:** 40

| Parameter | Value |
|---|---|
| Cell DC-DC stage transformer specification | n:1 = 2.5, , $L_{lkg} \approx 437$ µH, VA = 5 MVA |
| Cell AC-DC stage switching frequency | 10 kHz |
| Cell DC-DC stage primary side devices<br>Number of devices per switch position | 10 kV SiC MOSFETs & JBS diodes<br>30 x 10 kV/20 A SiC MOSFETs |
| Cell DC-DC stage secondary side devices<br>Number of devices per switch position | 10 kV SiC MOSFETs<br>75 x 10 kV/20 A SiC MOSFETs |

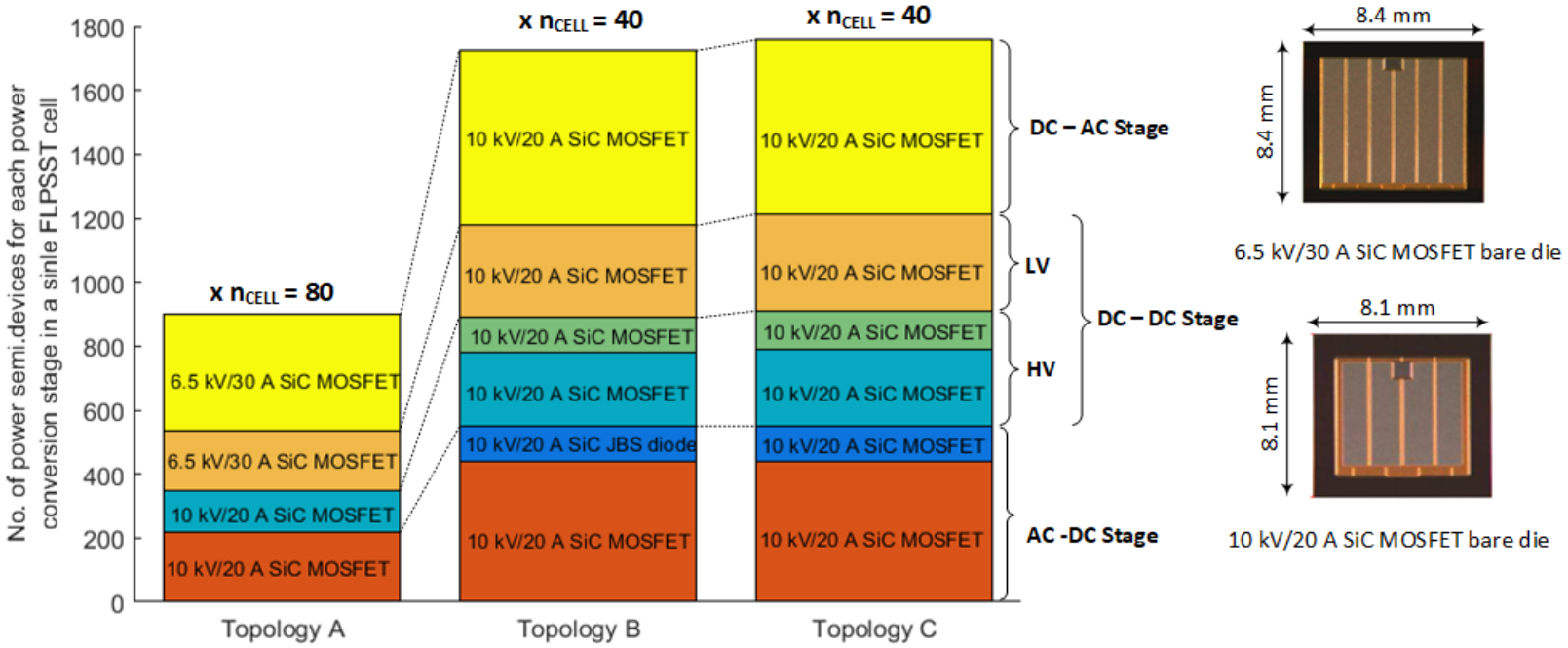
# 5 MVA basic building block topology: Type - C




- **Power rating:** 5 MVA
- **$n_{cell}$:** 40

| Parameter | Value |
|---|---|
| Cell input side DC link voltage | 6.26 kV |
| Cell input side AC rms voltage and current | 3.45 kV, 1449.27 A |
| Cell input side peak current | 2049.58 A |
| Cell DC-AC stage switching frequency | 10 kHz |
| Cell DC-AC stage devices<br>Number of devices per switch position | 10 kV SiC MOSFETs<br>137 x 10 kV/20 A SiC MOSFETs |

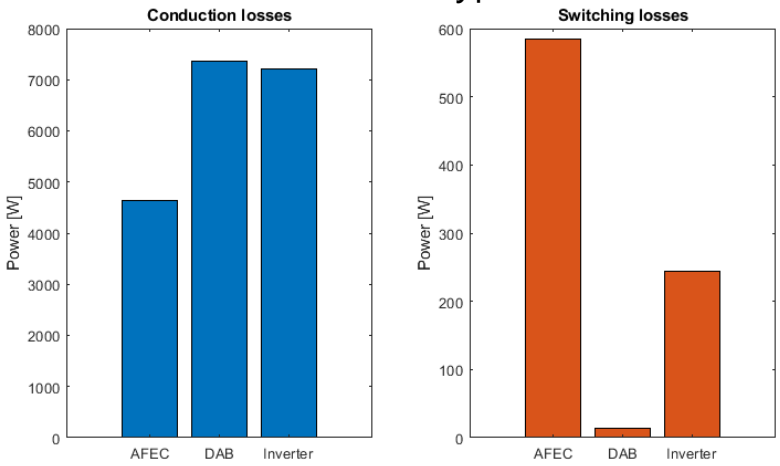
# Comparison of basic building block topologies in terms of power semiconductor device requirements



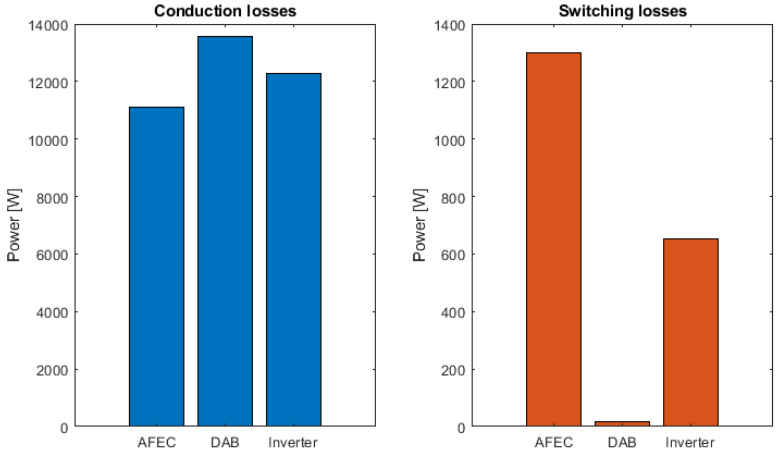

- Amongst three topologies Type – B configuration utilizes lowest number of power semiconductor devices and number of series connected modules per phase stack.

# Comparison of basic building block topologies in terms of power semiconductor losses

- 2.5 MVA Type - A



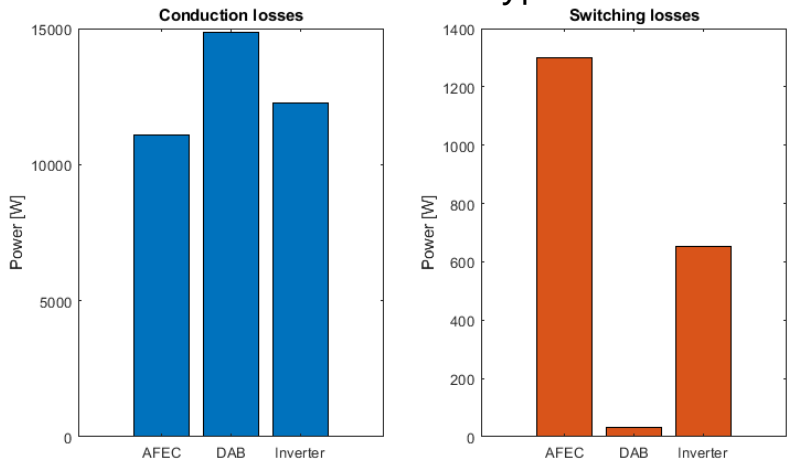

- 5 MVA Type - B



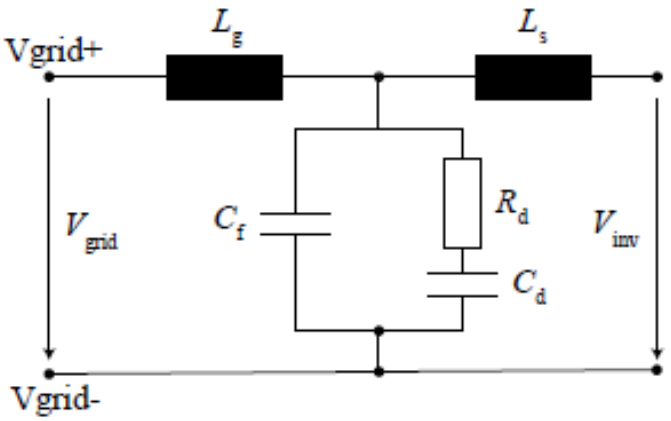

- Power semiconductor losses expressed as a percentage of rated power.

| FLPSST building block | Semiconductor losses (% of rated power) |
|---|---|
| Type - A | ≈ 0.8 % |
| Type – B | ≈ 0.77 % |
| Type – C | ≈ 0.8 % |

- 5 MVA Type - C



# 13.8 KV Grid Side Converter Design LCL Filter




- Filter specifications
  - Total impedance is 0.1 p.u. ($X_{L_c} + X_{L_i}$ = 0.1 p.u.)
  - Maximum reactive power of filter capacitor ($C_f$) is 10%
  - Resonance frequency ($f_{res}$): $7f_{grid} < f_{res} < \frac{1}{5} f_{sw}$
  - Q is choosen to be 3 and the damping resistor is designed.

**Based on the specifications, the calculated parameters for 13.8 KV LCL filter is summarized as follow,**

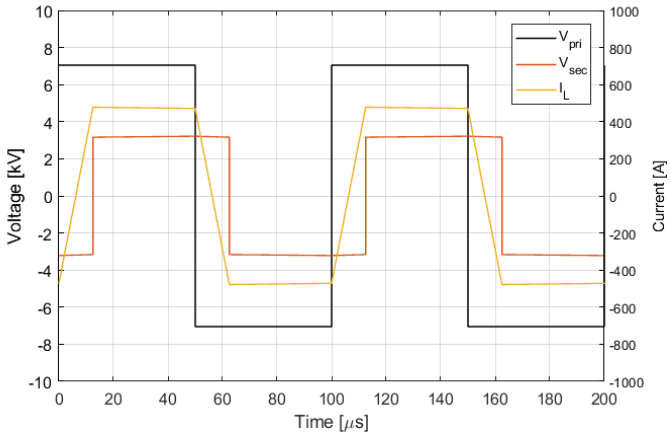
| Parameters | Designed Value |
|---|---|
| **Converter side Inductance ($L_s$)** | 8.8 mH |
| **Grid side Inductance ($L_g$)** | 1.3 mH |
| **Capacitances ($C_f$, $C_d$)** | 7 μF |
| **Damping Resistance ($R_d$)** | 4.17 Ω |

# MV MF isolation transformer for FLPSST basic building blocks

**Key challenges:**

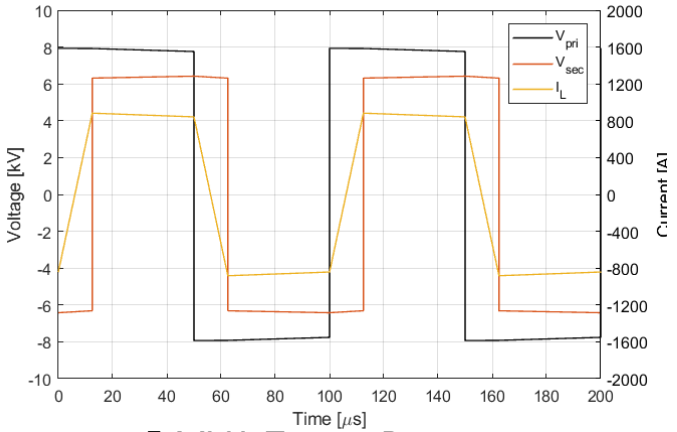
- High isolation voltage requirements
- Isolation coordination – set by top most cell in a phase stack.
- Mixed frequency medium voltage electric field stresses
- Low isolation capacitance requirements
- Thermal management
- Magnetic core material

MV MF isolation transformer primary, secondary winding voltages and currents for basic building block topologies.



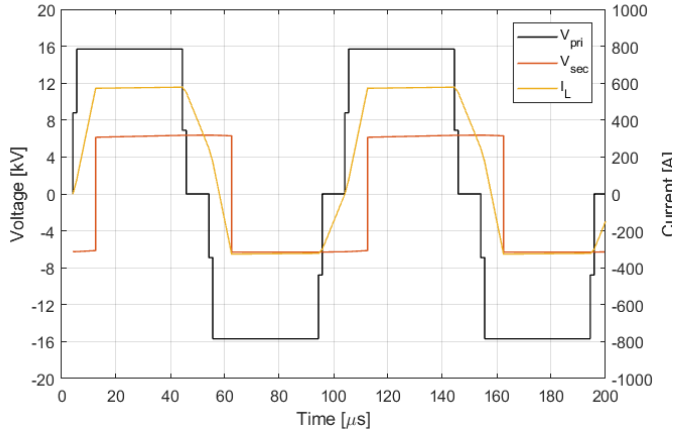

2.5 MVA Type - A

**Power rating:** 2.5 MVA
**Max. diff. voltage stress:** 7.05 kV
**Max. rms and peak winding currents:** ≈ 1040 A, 944 A
(Two level voltage waveform)




5 MVA Type - B

**Power rating:** 5 MVA
**Max. diff. voltage stress:** ≈ 7.89 kV
**Max. rms and peak winding currents:** ≈ 1105 A, 986 A
(Two level voltage waveform)




5 MVA Type - C

**Power rating:** 5 MVA
**Max. diff. voltage stress:** ≈ 15.69 kV
**Max. rms and peak winding currents:** ≈ 1445 A, 1041 A
(Two level voltage waveform)

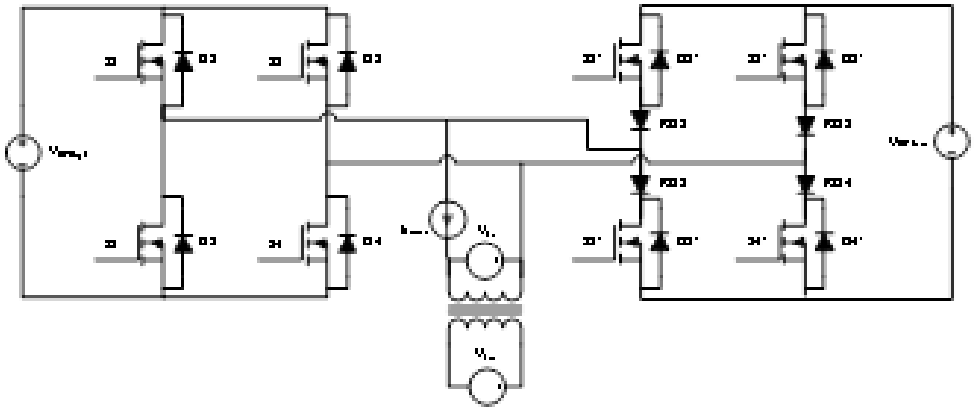
FREEDM SYSTEMS CENTER

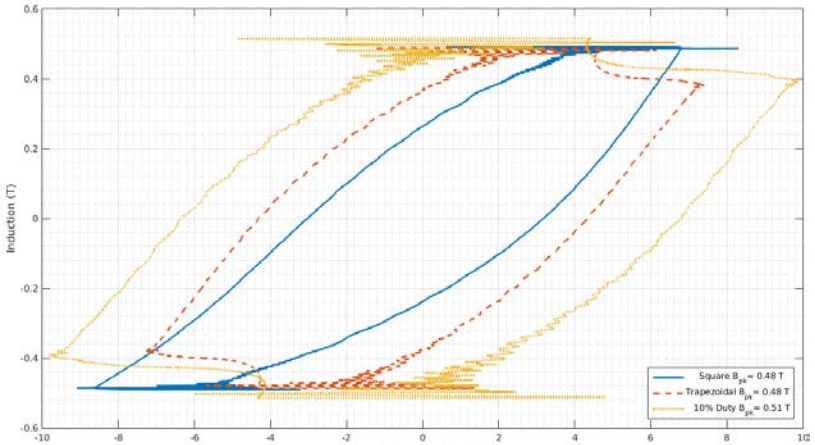
## ➢ MV MF isolation transformer for FLPSST basic building blocks

**Key challenges:**

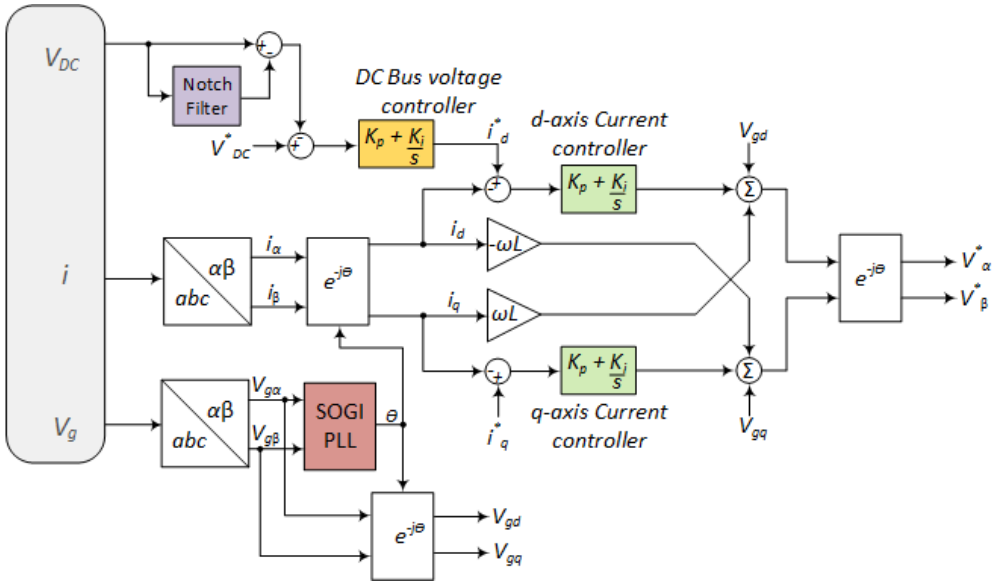
- High isolation voltage requirements
- Isolation coordination – set by top most cell in a phase stack.
- Mixed frequency medium voltage electric field stresses
- Low isolation capacitance requirements
- Thermal management
- Magnetic core material

Test set up for characterizing the magnetic core materials under trapezoidal excitation.



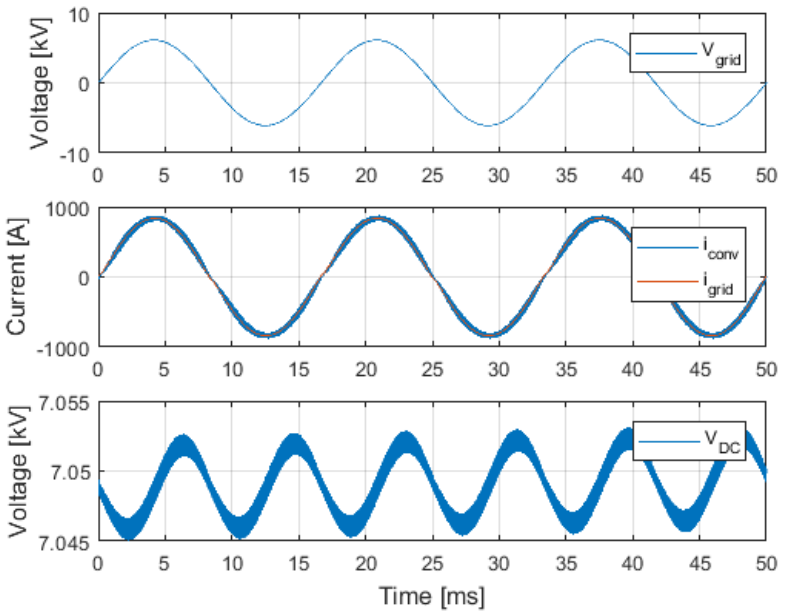


## ➢ Control loop structure of the basic building block



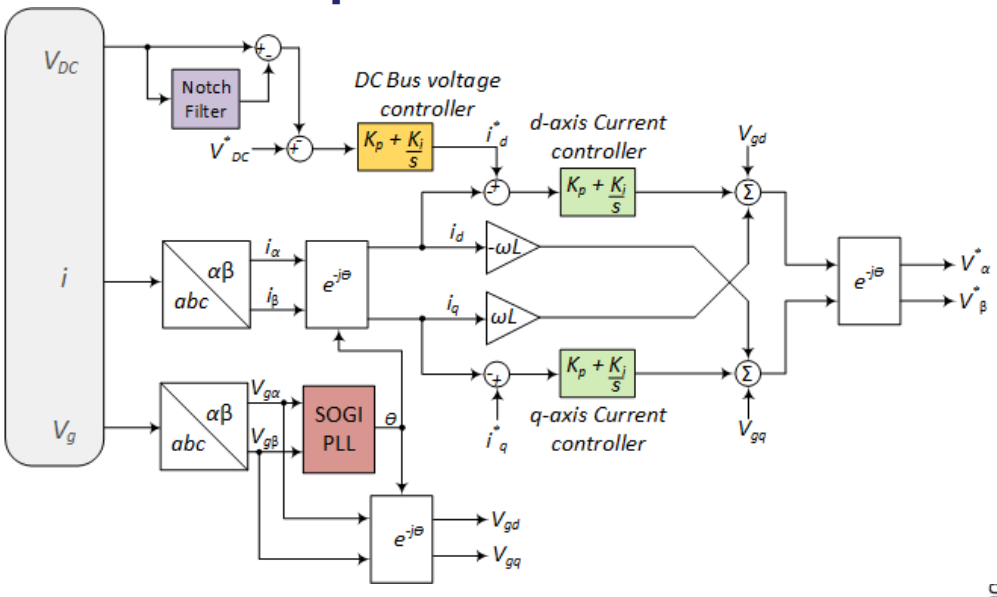

- Schematic of an AFEC control loop implementation

- Simulation results for 2.5 MVA AFEC



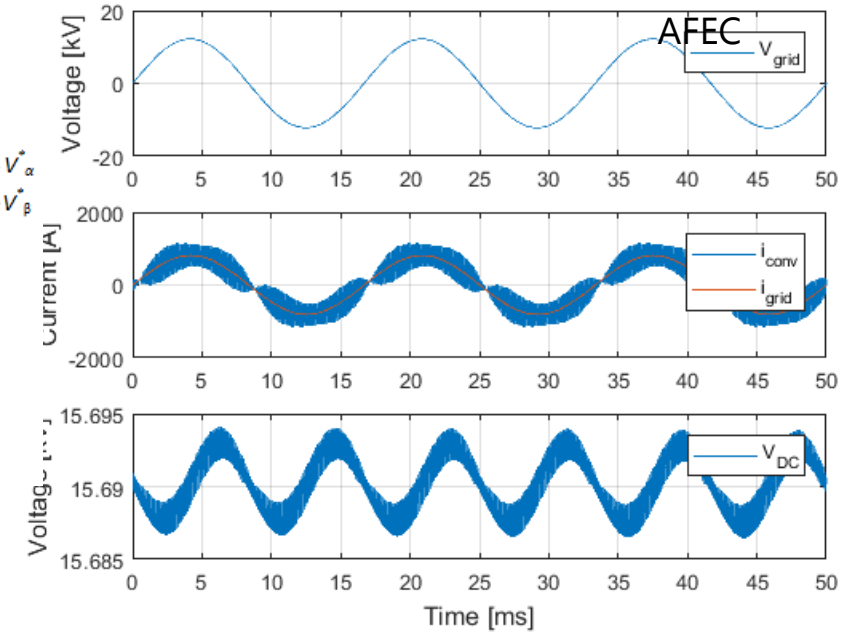

- DC bus voltage controller
- Notch filter for 120 Hz voltage ripple filtering (inherent power pulsation at twice the grid frequency in single phase system)
- Active and reactive power control with synchronous reference frame dq current control
- Controller bandwidth and tuning is performed following method presented in [1].

# ➢ Control loop structure of the basic building block



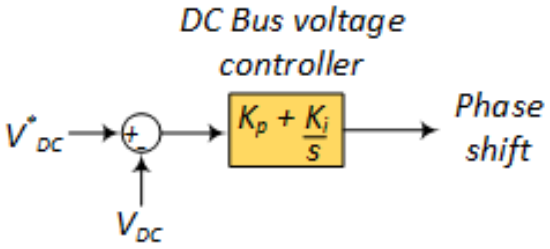

Schematic of an AFEC control loop implementation

- Simulation results for 5 MVA AFEC

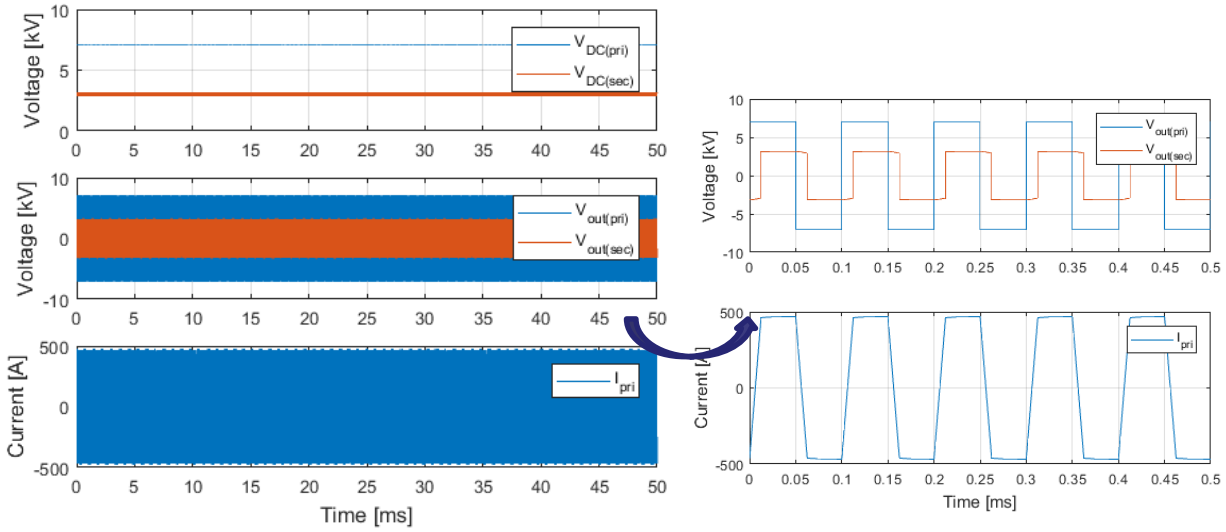



- DC bus voltage controller
- Notch filter for 120 Hz voltage ripple filtering (inherent power pulsation at twice the grid frequency in single phase system)
- Active and reactive power control with synchronous reference frame dq current control
- Controller bandwidth and tuning is performed following method presented in [1]

## ➢ Control loop structure of the basic building block



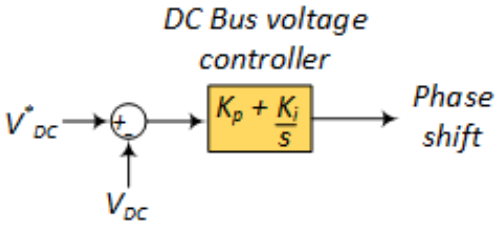

Schematic of an DAB control loop implementation



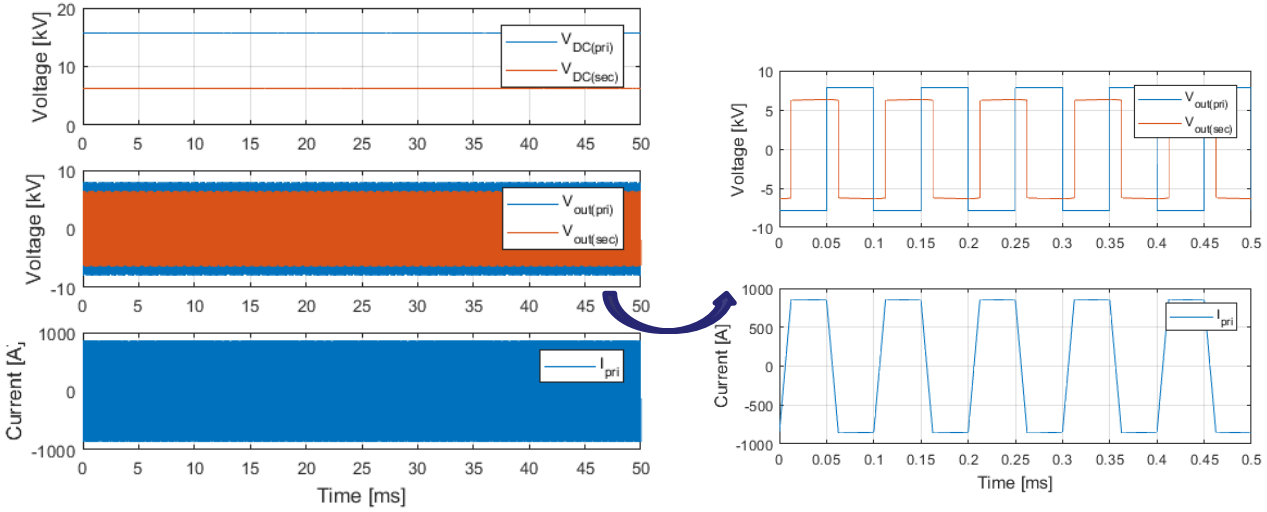

Simulation results for 2.5 MVA DAB (Type - C)

- DC bus voltage controller controls the DC bus voltage at the secondary side of the DAB.
- Loading of the LV side inverter generates power pulsation at twice the grid fundamental frequency,
- The DAB LV capacitance size requirement is relatively higher to maintain the voltage ripple within the acceptable limit and for proper functioning of the PI controller.

## ➢ Control loop structure of the basic building block




- Schematic of an DAB control loop implementation

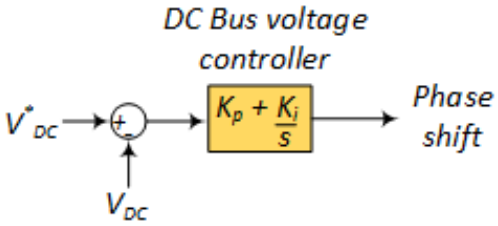


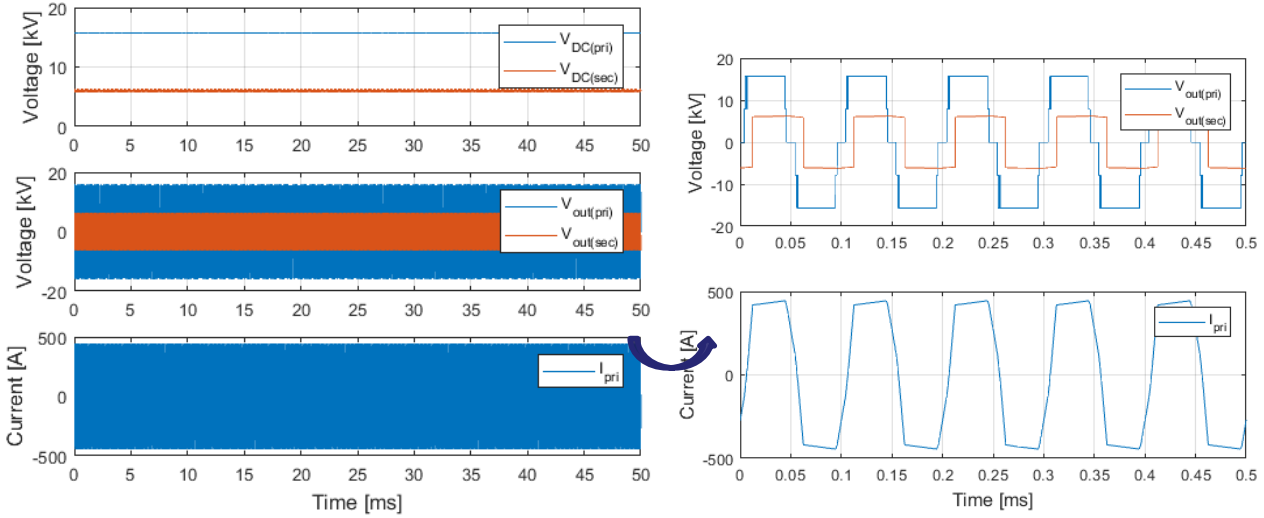

Simulation results for 5MVA DAB (Type B)

- DC bus voltage controller controls the DC bus voltage at the secondary side of the DAB.
- Loading of the LV side inverter generates power pulsation at twice the grid fundamental frequency,
- The DAB LV capacitance size requirement is relatively higher to maintain the voltage ripple within the acceptable limit and for proper functioning of the PI controller.

# ➢ Control loop structure of the basic building block

- Schematic of an DAB control loop implementation



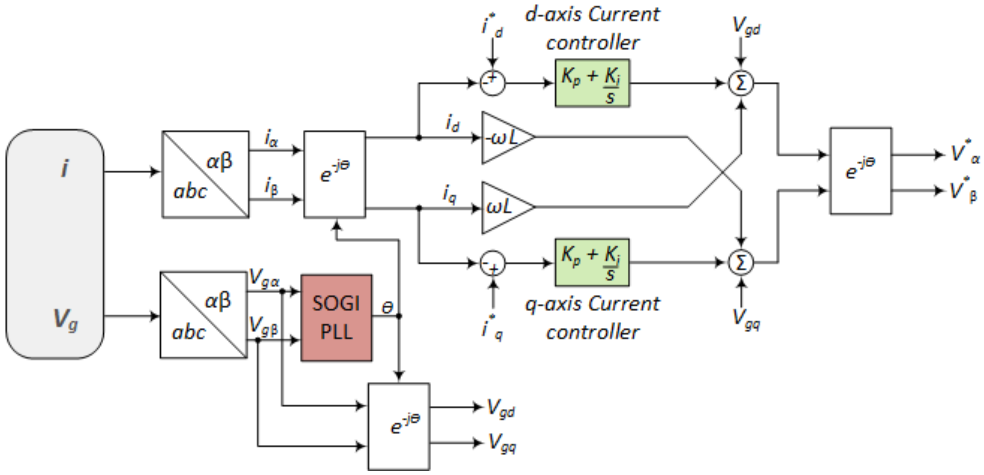

Simulation results for 5 MVA DAB

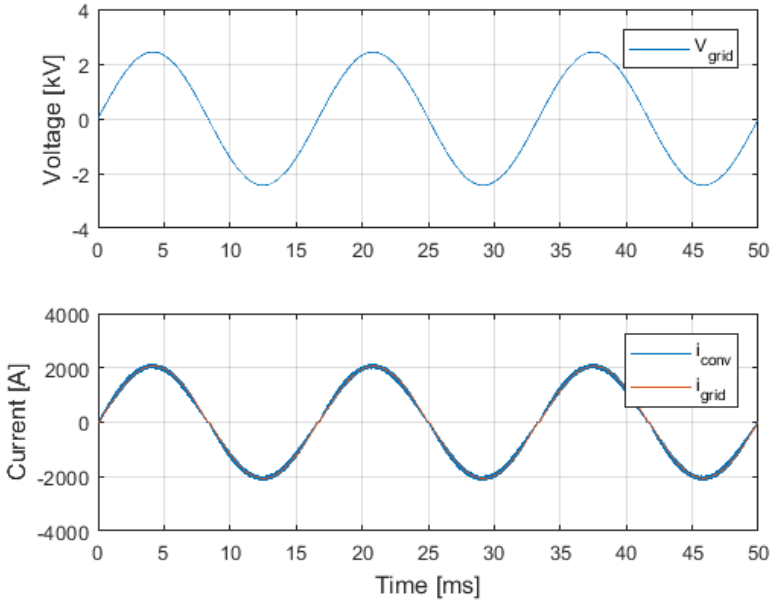
- DC bus voltage controller controls the DC bus voltage at the secondary side of the DAB.
- Loading of the LV side inverter generates power pulsation at twice the grid fundamental frequency,
- The DAB LV capacitance size requirement is relatively higher to maintain the voltage ripple within the acceptable limit and for proper functioning of the PI controller.

FREEDM SYSTEMS CENTER

## ➢ Control loop structure of the basic building block

- Schematic of an inverter control loop implementation



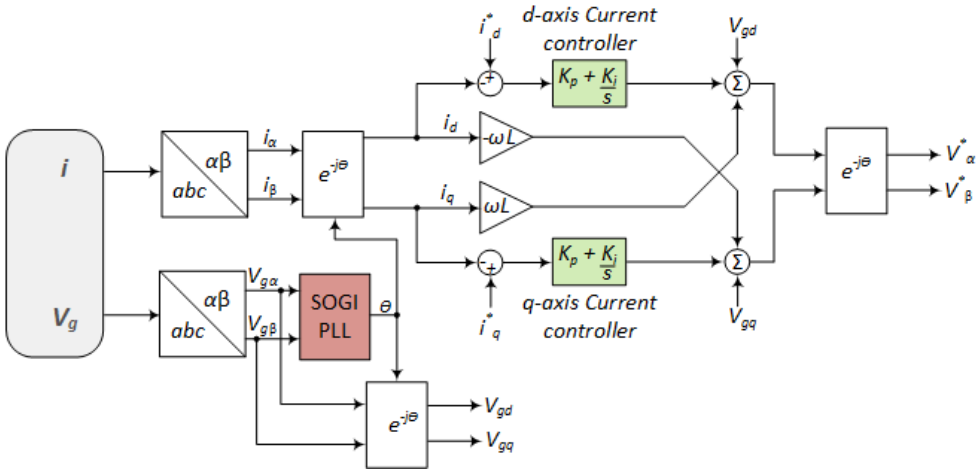



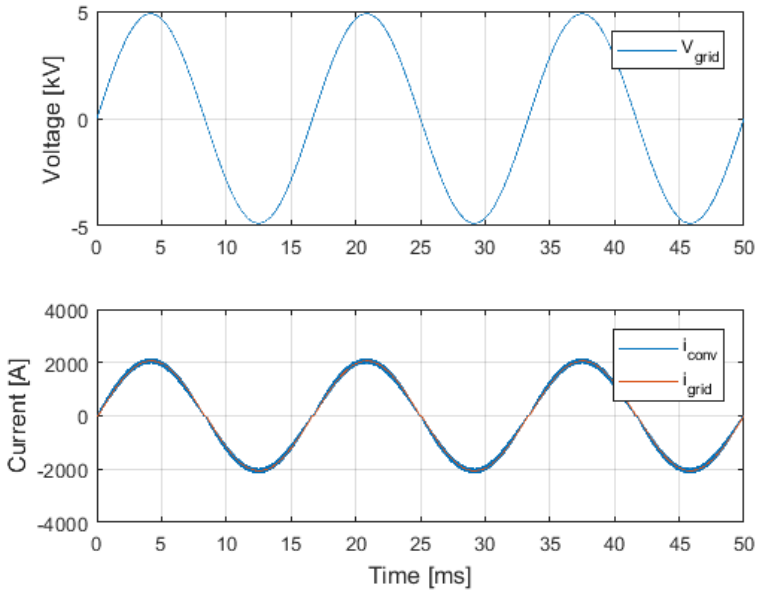

Simulation results for 2.5 MVA Inverter

- Active and reactive power control with synchronous reference frame dq current control
- Controller bandwidth and tuning is performed following method presented in [].

# ➢ Control loop structure of the basic building block

- Schematic of an inverter control loop implementation




Simulation results for 5 MVA Inverter

- Active and reactive power control with synchronous reference frame dq current control
- Controller bandwidth and tuning is performed following method presented in [].

FREEDM SYSTEMS CENTER

# Power Sharing in Low Frequency Transformers

## Goal

To assess the feasibility of modular low frequency transformers and investigate impact of transformer parameter mismatch on current and voltage sharing in low-frequency, modular, large-power-transformers

## Problem

- **Current sharing** – important to prevent transformers from caring too much current causing them to overheat and degrade
- **Voltage sharing** – important to prevent transformers from exceeding rated insulation. Also important to avoid **magnetic core saturation**, which causes output voltage distortion and high magnetizing current

# Power Sharing in Low Frequency Transformers

## Example transformer specs:

**Example transformer specs:**

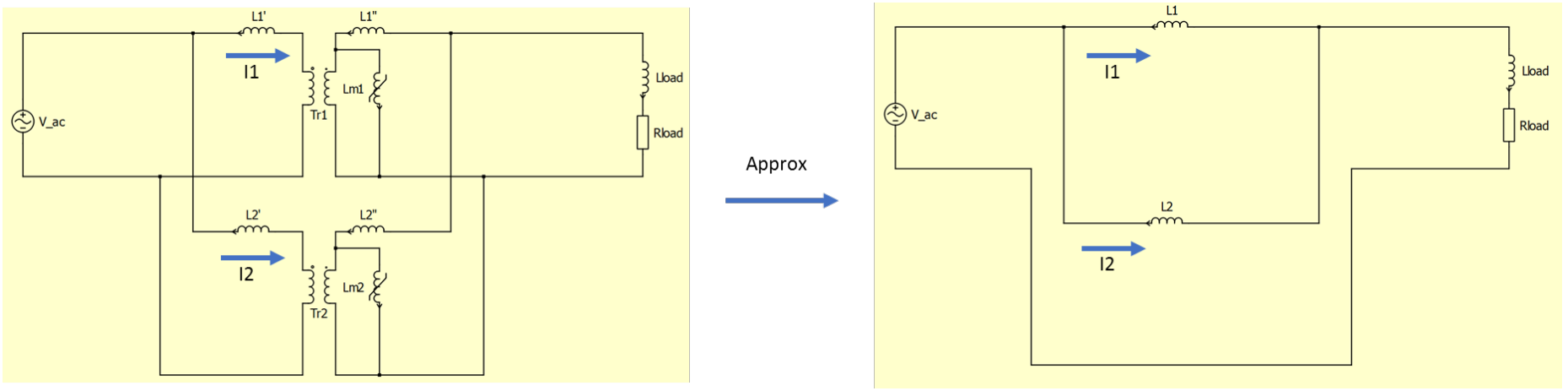
- 5 MVA, 100 kV:10 kV
- Leakage inductance: 10% (5% primary, 5% secondary)
- Magnetizing current: 1%
- Load: 5 MVA, PF 0.5
- Transformer losses: none
- Calculated:

| Primary | Secondary |
|---|---|
| **$Z_{base}$: 2 kOhm** | $Z_{base}$: 20 Ohm |
| **$L_{leakage}$: j100 Ohm = 265 mH** | $L_{leakage}$: j1 Ohm = 2.65 mH |
| **$I_{base}$: 50 A** | |
| **$I_{magnetizing}$: 500 mA** | |
| **$L_{magnetizing}$: j200 kOhm = 530 H** | |

# Power Sharing in Low Frequency Transformers

## Parallel-Parallel Connection

- Parallel transformers provide redundancy and increase the power capacity
- The two transformers must have the same voltage ratings and turns ratios to avoid circulating current.

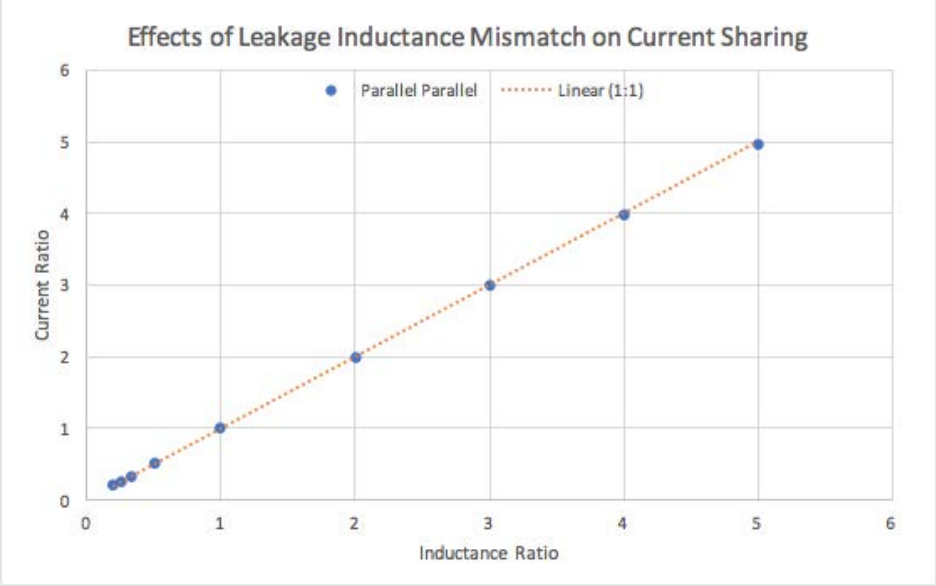


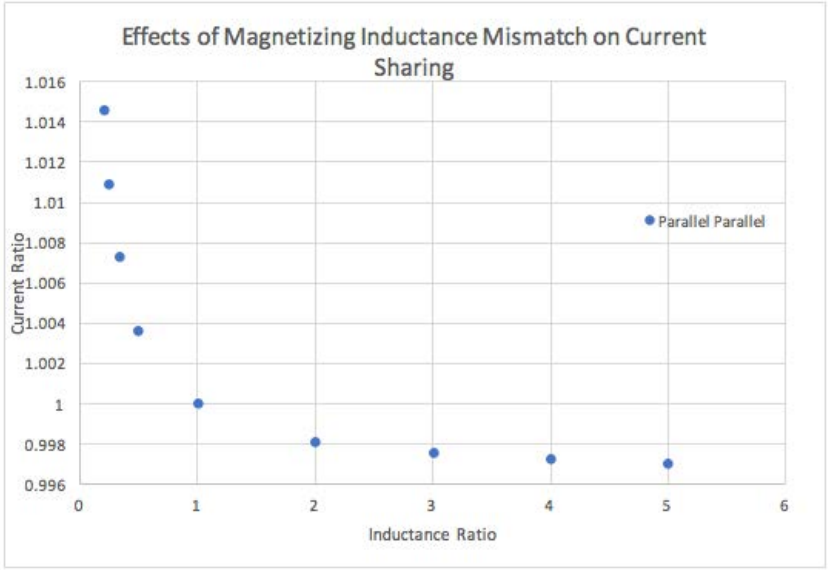

$$I_1 \cong I_{total} \frac{L_{l2}}{L_{l1} + L_{l2}}$$ (if magnetizing inductance is ignored)

# Power Sharing in Low Frequency Transformers

## Parallel-Parallel Connection

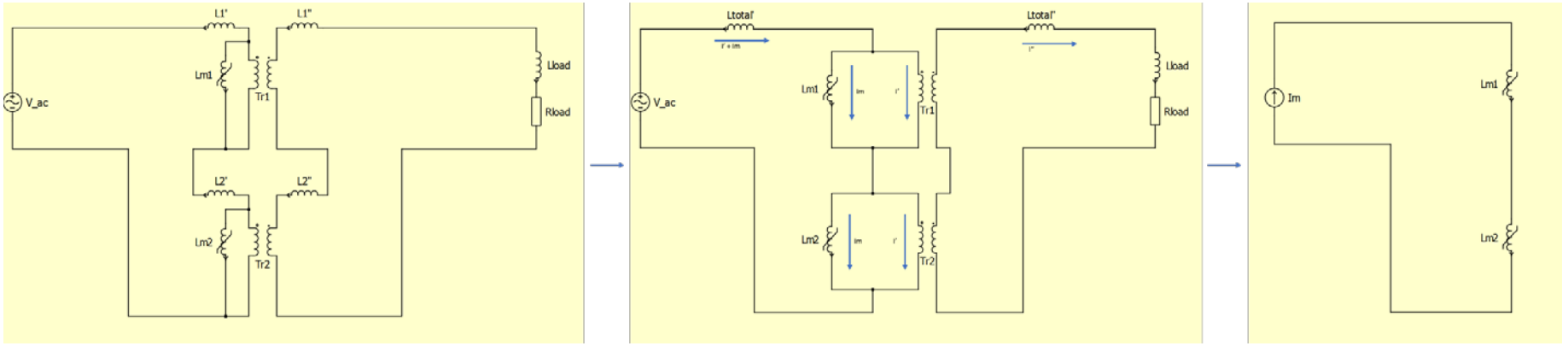
Effect of leakage and magnetizing inductances mismatches on the current sharing



# Power Sharing in Low Frequency Transformers

## Series-Series Connection

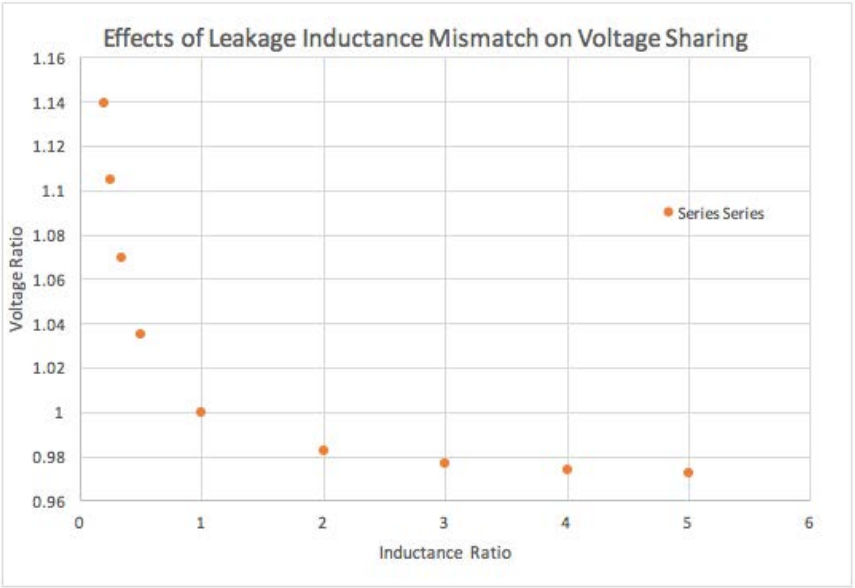


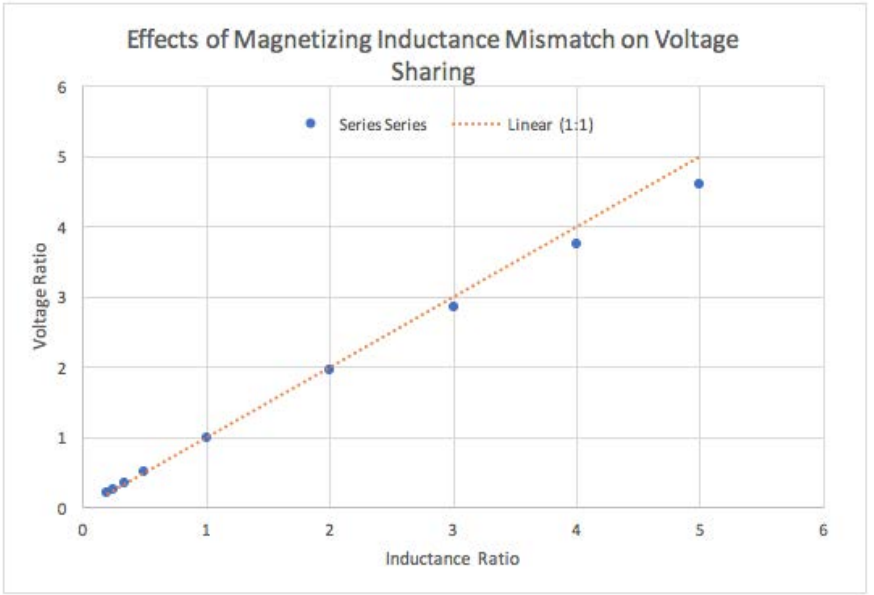

$$V_1 \cong V_{total} \frac{L_{m1}}{L_{m1} + L_{m2}}$$ (leakage inductance << magnetizing inductance)

# Power Sharing in Low Frequency Transformers

## Series-Series Connection

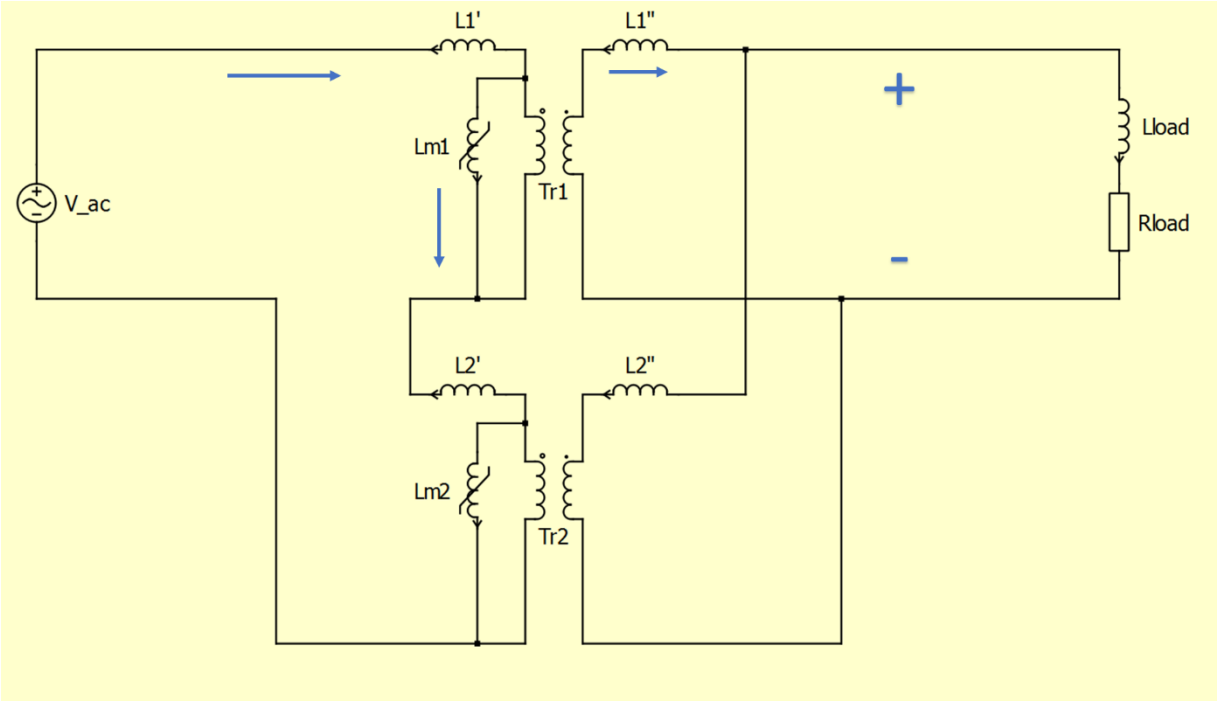
Effect of leakage and magnetizing inductances mismatches on the current sharing



# Power Sharing in Low Frequency Transformers

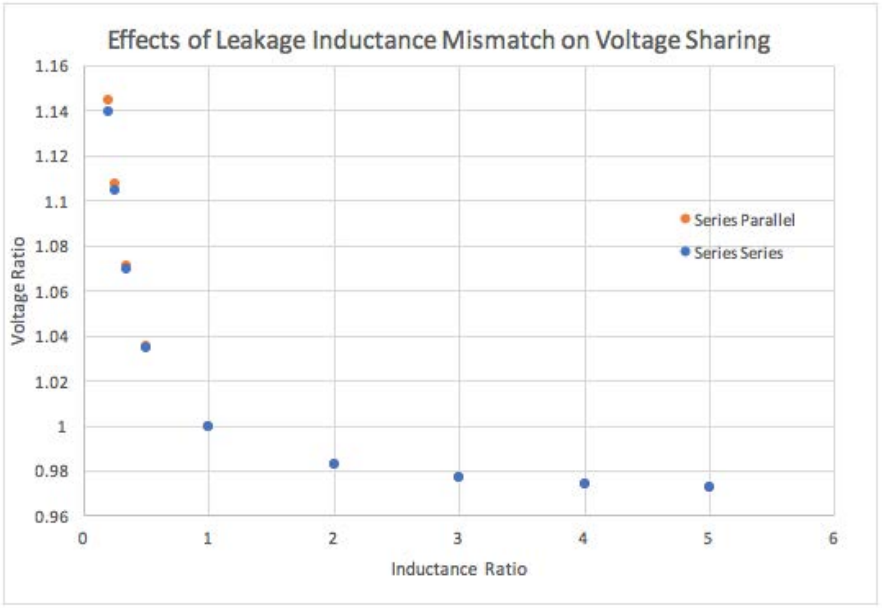
## Series-Parallel Connection

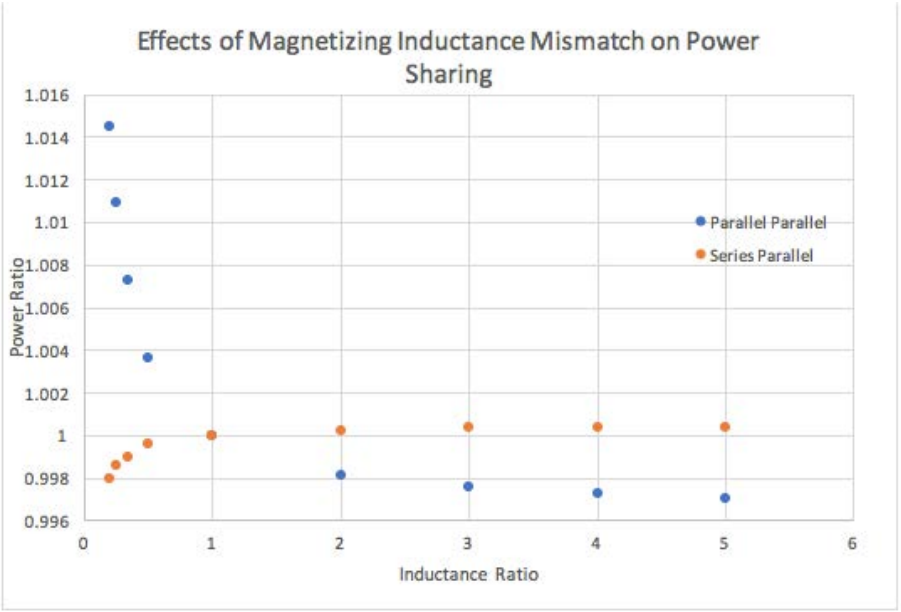


# Power Sharing in Low Frequency Transformers

## Series-Parallel Connection

Effect of leakage and magnetizing inductances mismatches on the current sharing



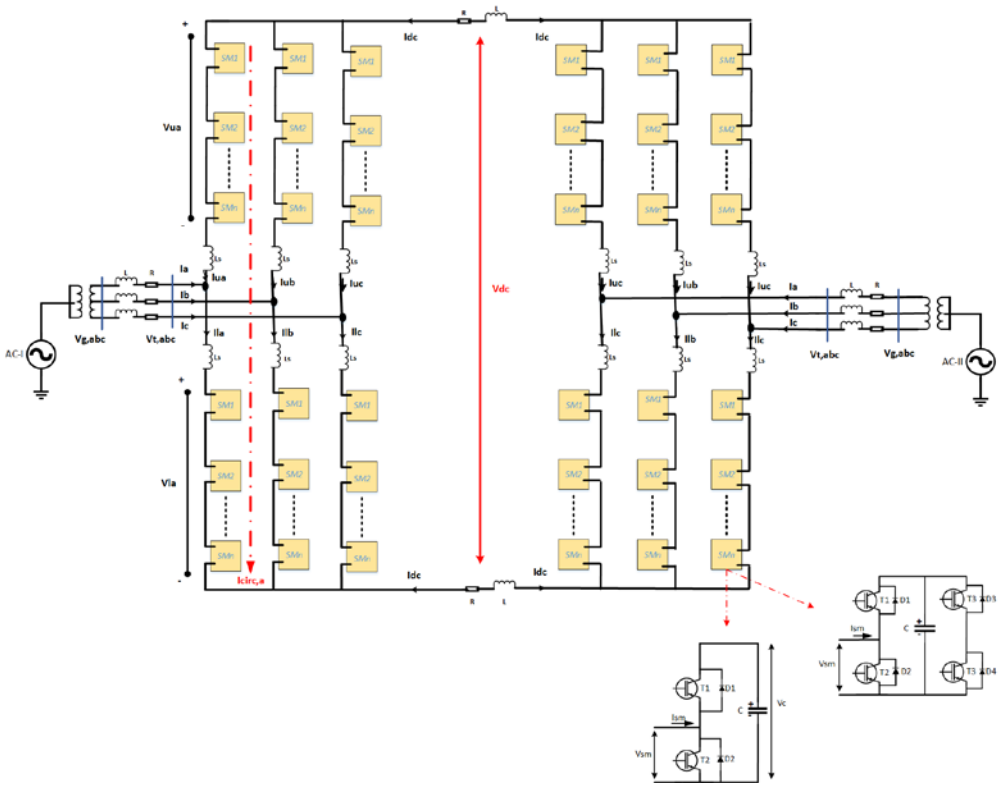
# Power Sharing in Low Frequency Transformers

## Summary

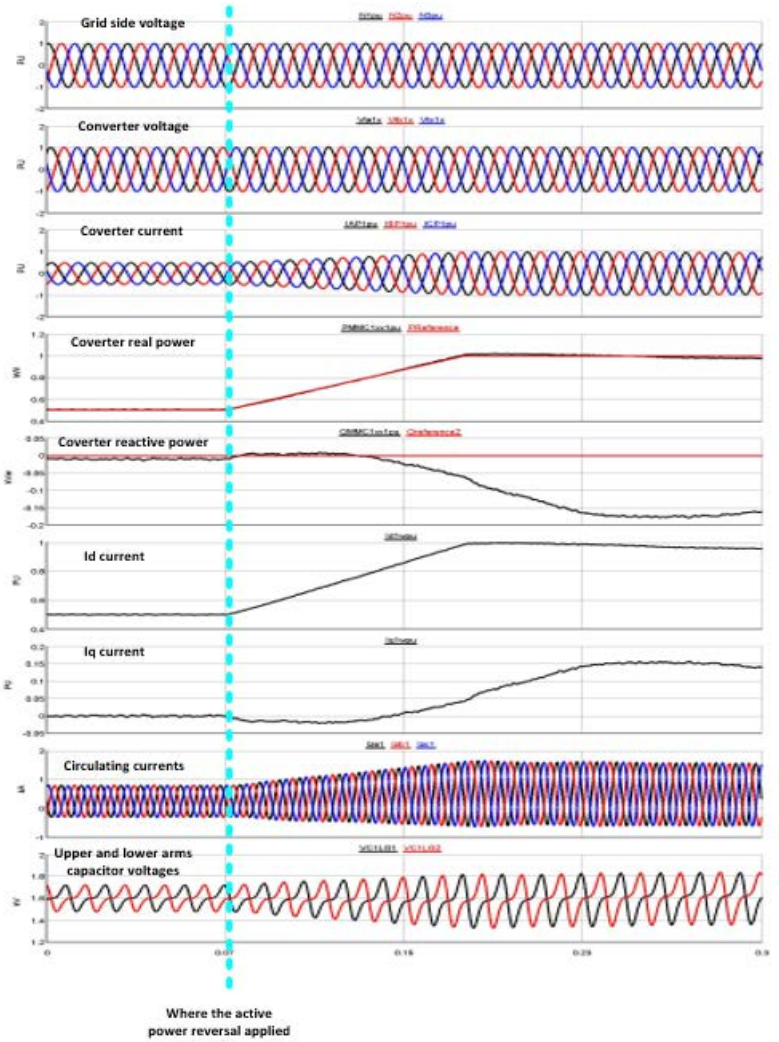
The following table summarizes the level of sensitivity of each type of mismatch on the voltage and current sharing of the different types of transformer connections.

| | | Leakage Inductance Mismatch | Largest Ratio | Magnetizing Inductance Mismatch | Largest Ratio |
|---|---|---|---|---|---|
| Parallel-Parallel | Voltage Sharing | Perfect Sharing | 1 | Perfect Sharing | 1 |
| | Current Sharing | Near Proportional | 4.95 | Near Perfect Sharing | 1.01 |
| Series-Series | Voltage Sharing | Good Sharing | 1.14 | Near Proportional | 4.6 |
| | Current Sharing | Perfect Sharing | 1 | Perfect Sharing | 1 |
| Series-Parallel | Voltage Sharing | Good Sharing | 1.14 | Very Near Perfect Sharing | 1.002 |
| | Current Sharing | Perfect Sharing | 1 | Perfect Sharing | 1 |

# Modular Multi-cell FLPSST based on single phase building blocks

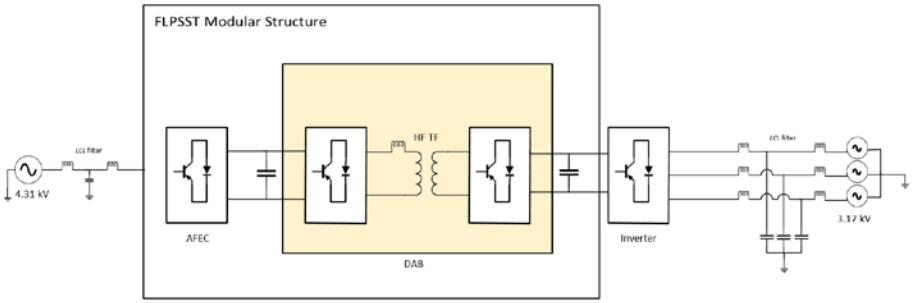



Three-phase Back to Back MMC System.

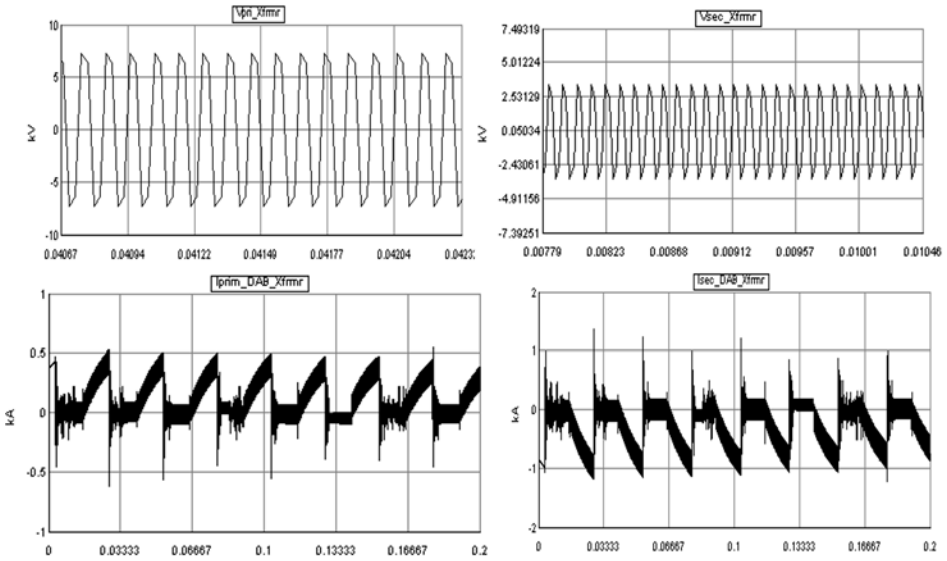



MMC Output Waveform.

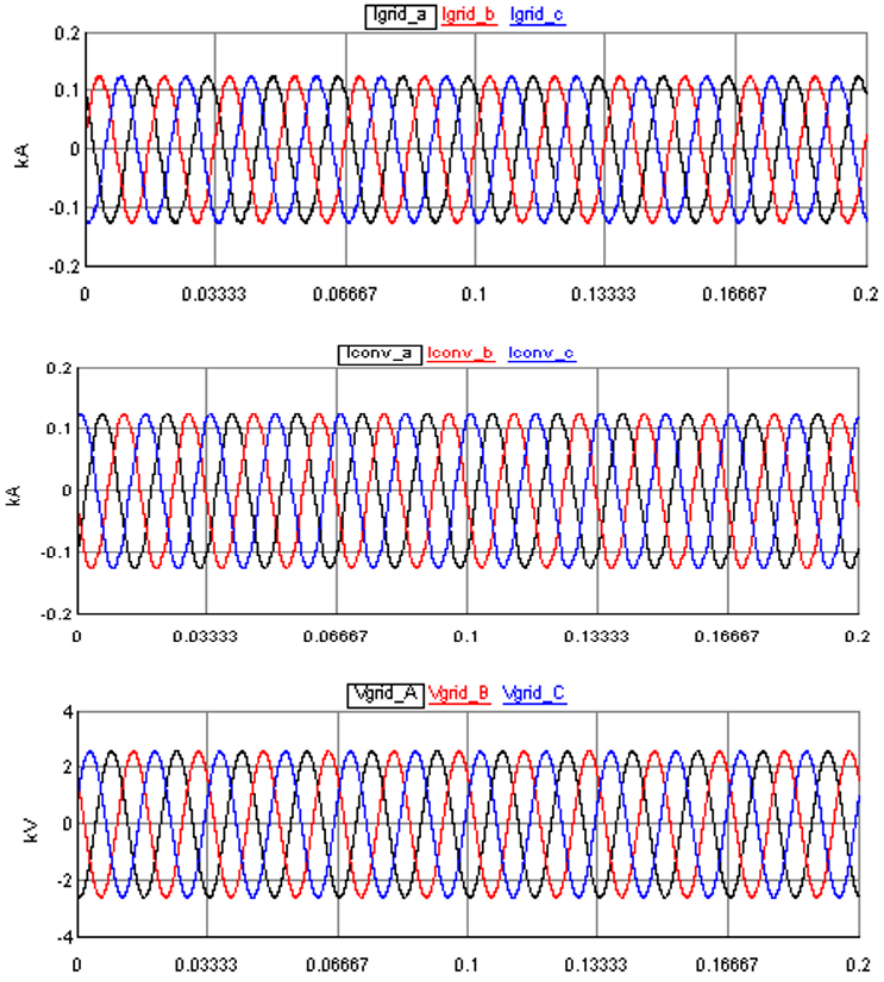
# Real-Time Simulation of Single Phase AC to Three Phase SST




Grid Connected FLPSST Modular Structure.




Primary and Secondary voltages and currents

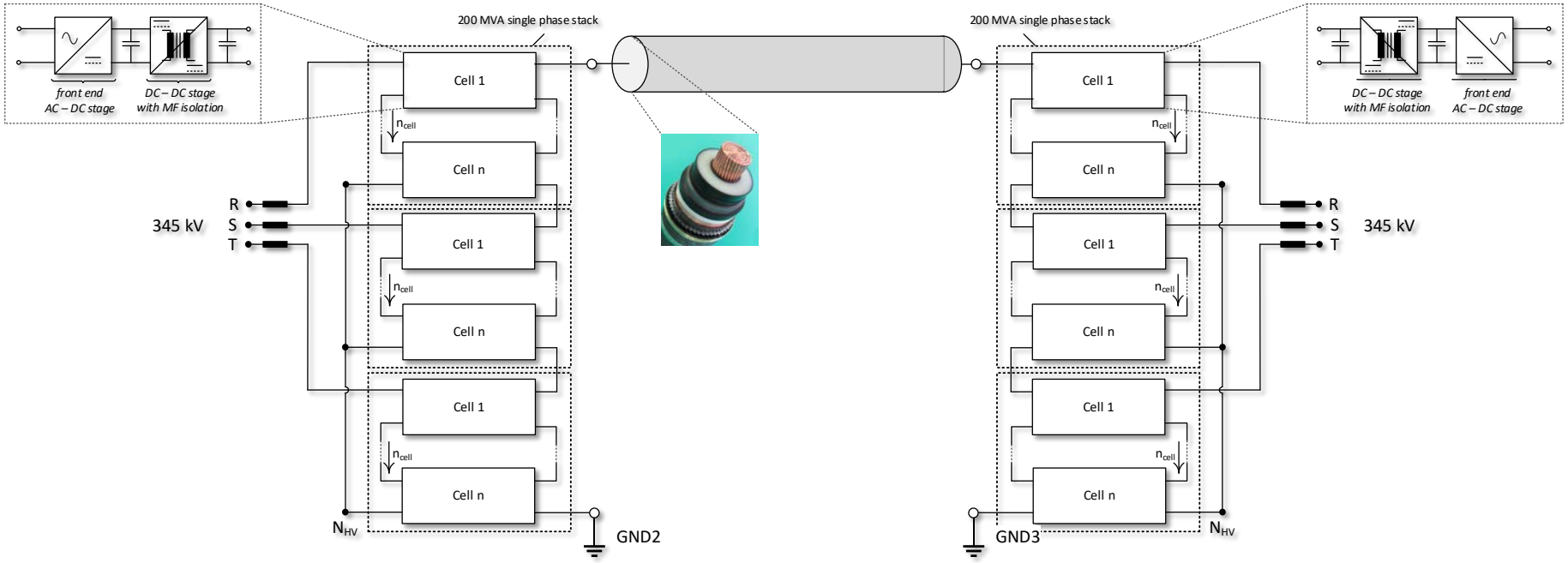



Grid and converter currents and grid side voltage

FREEDM SYSTEMS CENTER

## ➢ Possible applications: Back to back two terminal DC system

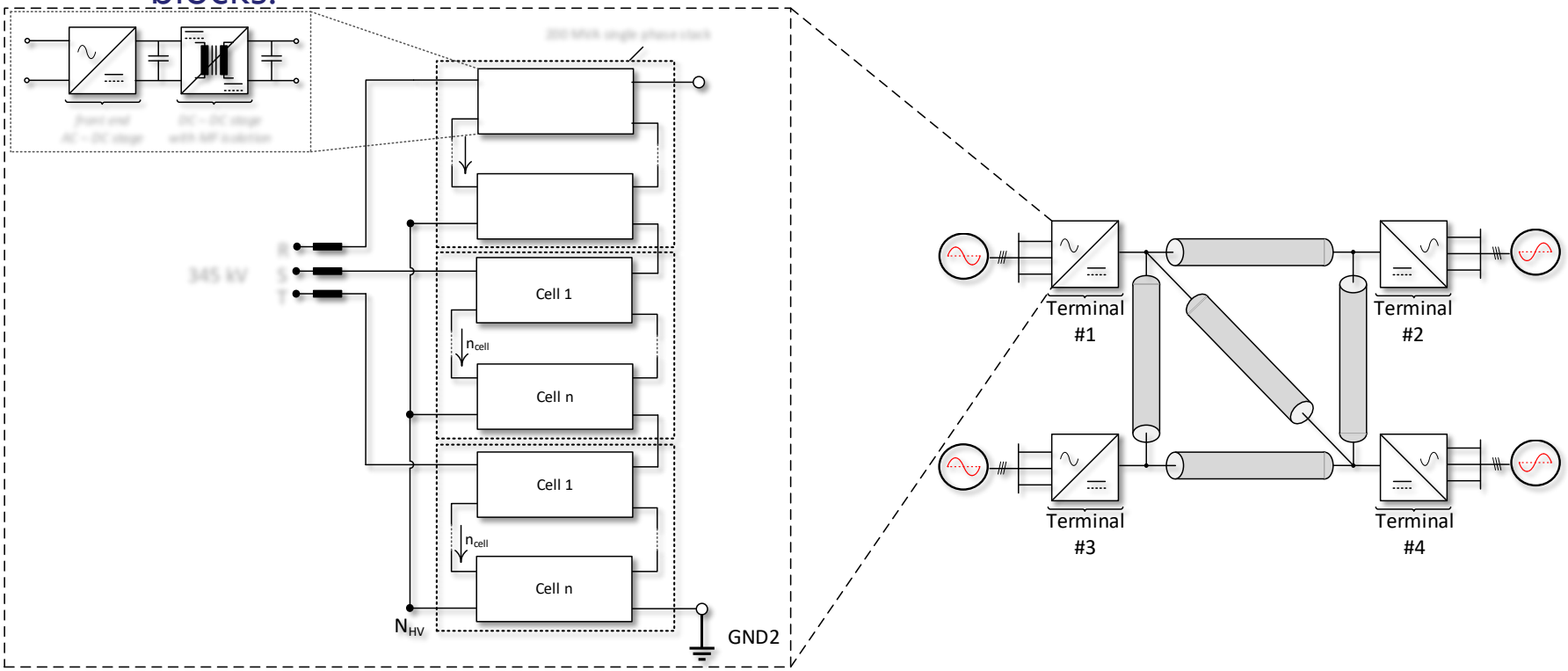
- The FLPSST basic building blocks can be utilized to form the two terminal isolated high voltage DC network.



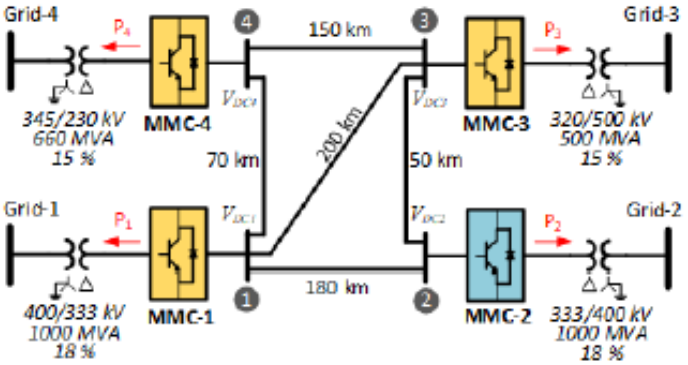
FREEDM SYSTEMS CENTER

## ➢ Possible applications: Back to back two terminal DC system

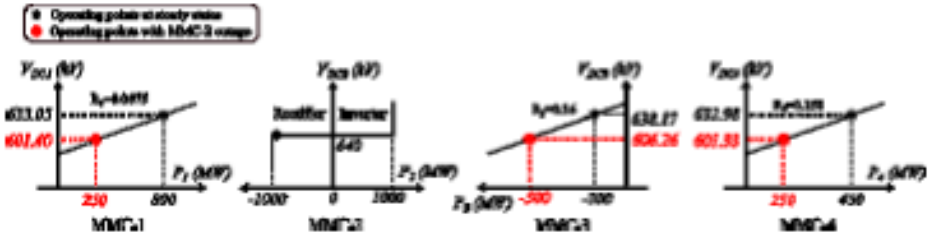
- A muli-terminal HVDC system realization using the FLPSST basic building blocks.



# Performance Evaluation of Four-Terminal MTDC System

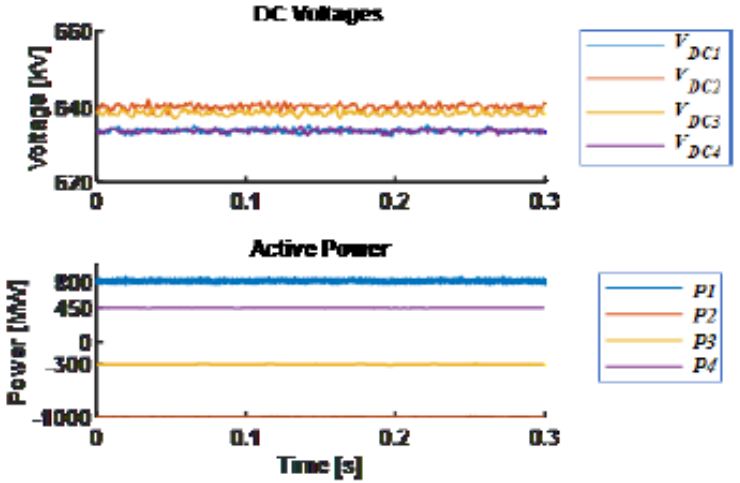



Four-Terminal MMC based-MTDC configuration

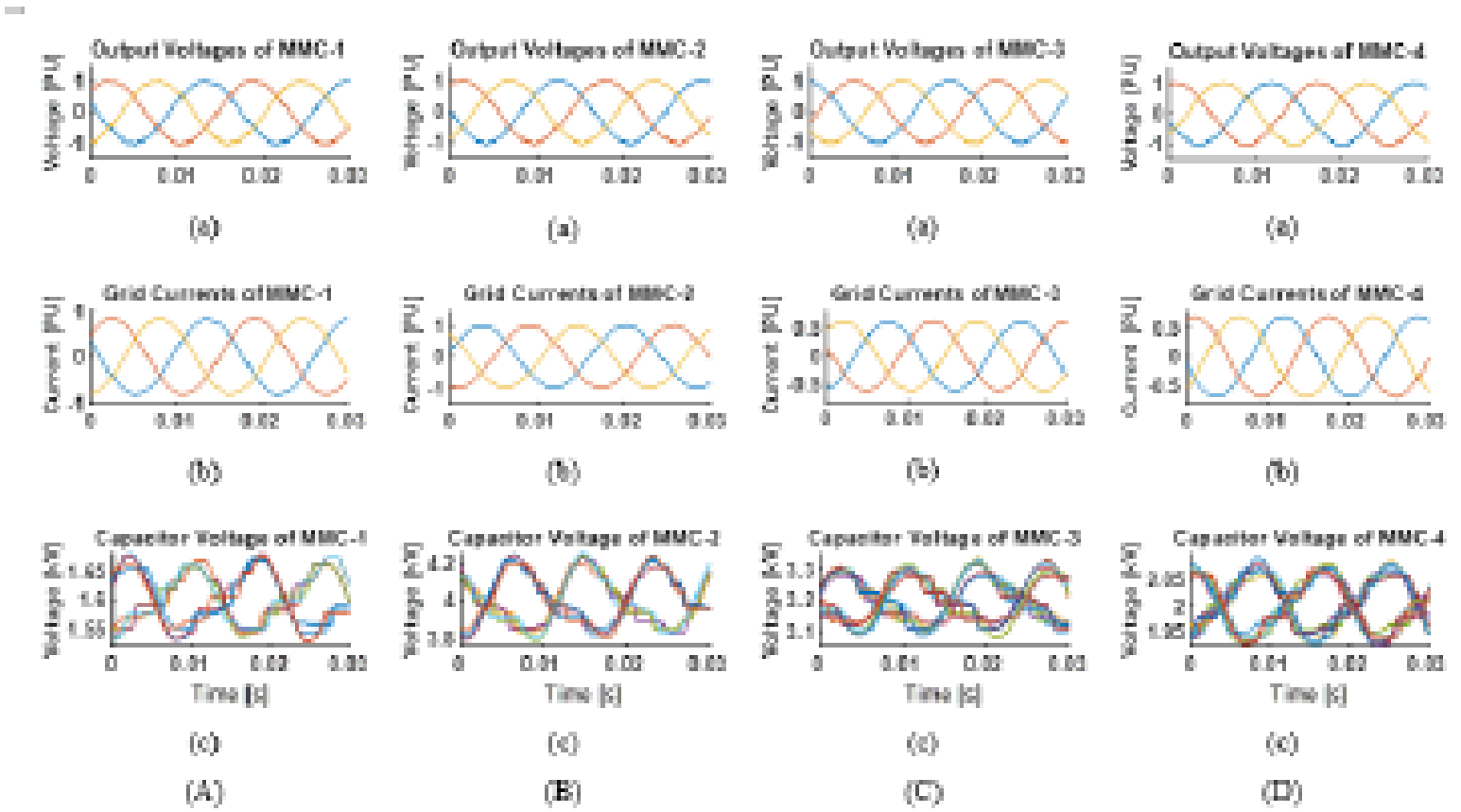


Droop control characteristics of MMCs

RTDS and MMC support unit hardware




Active powers and DC voltages of the MTDC system under steady-state conditions




RTDS results at the steady states, (a) AC output voltages, (b) grid currents, and (c) upper and lower arm SM capacitor voltages: (A) MMC-1, (B) MMC-2, (C) MMC-3, (D) MMC-4

FREEDM SYSTEMS CENTER

## References


[1] CONSIDERATIONS FOR A POWER TRANSFORMER EMERGENCY SPARE STRATEGY FOR THE ELECTRIC UTILITY INDUSTRY, The Electric Power Research Institute for the U.S. Department of Homeland Security Science and Technology Directorate, September, 2014.

[2] LARGE POWER TRANSFORMERS AND THE U.S.ELECTRIC GRID, Infrastructure Security and Energy Restoration Office of Electricity Delivery and Energy Reliability U.S. Department of Energy, June 2012.

[3] Jaffery B. Casady et al., "Medium voltage SiC R & D update, " https://www.nist.gov/sites/default/files/documents/pml/high_megawatt/Wolfspeed-Cree-SiC-Pwr-NIST-wkshp-Apr2016_SHORT.pdf

[4] S. Sabri et al., "New generation 6.5 kV SiC power MOSFET," 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Albuquerque, NM, 2017, pp. 246-250. doi: 10.1109/WiPDA.2017.8170555

[5] D. Johannesson, M. Nawaz and K. Ilves, "Assessment of 10 kV, 100 A Silicon Carbide mosfet Power Modules," in IEEE Transactions on Power Electronics, vol. 33, no. 6, pp. 5215-5225, June 2018.

[6] S. Ji, S. Zheng, Z. Zhang, F. Wang, and L. M. Tolbert. Protection and temperature-dependent switching characterization of latest generation 10 kv sic mosfets. In2017IEEE Applied Power Electronics Conference and Exposition (APEC), pages 783–788,March 2017. doi: 10.1109/APEC.2017.7930784

[7] D. Rothmund, D. Bortis and J. W. Kolar, "Accurate transient calorimetric measurement of soft-switching losses of 10kV SiC MOSFETs," 2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Vancouver, BC, 2016, pp. 1-10.