Qualcomm Atheros, Inc.

HomePlug Green PHY Integrated Circuit Development

Scope of Work

Through this HomePlug Green Physical Layer (PHY) Integrated Circuit Development project ("HomePlug"), Qualcomm Atheros, Inc. (Qualcomm Atheros) developed a compliant power line communications (PLC) solution to support smart grid functionality in a wide range of equipment: advanced metering infrastructure (AMI), smart meters, smart appliances, electric transportation, and home area network peripheral devices.

Objectives

The project aimed to develop a PLC integrated circuit for use in AMI smart meters and customer systems that is fully interoperable with IEEE[1] 1901 and HomePlug equipment, reducing both the circuit's material and manufacturing costs and the device's power consumption. With the development of this new device, Qualcomm Atheros now offers efficient and cost-effective home area networking connectivity options for meters and customer system providers, which reduces implementation costs for both power companies and customers.

At-A-Glance

Recipient: Qualcomm Atheros, Inc.

Company Headquarters: San Jose, California

Total Project Cost: $7,286,202

Total Federal Share: $3,643,101

Project Type: Customer Systems

Equipment

- **Integrated Circuit for Smart Meters and Customer Systems**

Key Benefits

- **Reduced Power Consumption**
- **Reduced Product Costs**

Deployed Smart Grid Technologies

HomePlug Green PHY (HPGP) Integrated Circuit: HomePlug developed a new integrated circuit to provide highly reliable communications for smart meters and other devices, allowing them to interface with customer systems via home area networks. Qualcomm Atheros designed and manufactured this device, which equipment vendors are integrating into electric vehicles, energy management systems, and select smart meters. The device uses existing electrical wiring within the home to communicate data and commands from the smart meter to the customer system. In addition, the device integrates with all internet protocol (IP)-based AMI backhaul and meter communications networks.

This new circuit provides an upgrade to existing Qualcomm Atheros chipsets, which are currently in wide use for smart grid devices. While the existing chipset requires three separate voltages—including 1.05 Volts Direct Current (VDC) for core logic, 3.3 VDC for the analog front end, and 12 VDC for the line driver—the new technology has been designed to be powered from a single 3.3 VDC buss, simplifying power supply design and reducing cost. In addition, a new power save function reduces energy consumption by enabling all HPGP clients within a given network to use a low-power "sleep" state in a coordinated manner, thereby facilitating reductions in power consumption during periods of low network traffic. The HPGP-compliant chipsets (QCA7000 and 7005) are single-chip devices featuring an integrated AFE, digital baseband processor, ARM-based medium access controller, on-board random access memory (RAM), a power management unit, and serial peripheral interface/universal asynchronous receiver/transmitter (SPI and UART) external interfaces.

[1] Institute of Electrical and Electronics Engineers

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This new chipset uses the HPGP and IEEE 1901 data protocols for PLC. This circuit is designed to provide communications for power lines at a frequency range of 2–30 megahertz (MHz), which allows for communications within both home electrical wiring systems and utility distribution systems. This new chipset is designed for high levels of communications reliability and supports data transfer at rates of 4–10 megabits per second (Mbps).

Benefits Realized

- **Reduced power consumption:** QCA7000 and QCA7005 implement advanced power-saving features as defined in the HPGP protocol. These features allow HPGP-compliant devices on a common network to enter/exit low-power operating states (i.e., "sleep mode") in a coordinated manner. When in a low-power state, devices are not capable of communication via the power line. It is therefore important that sleep periods are coordinated.
    - When operating in a low-power state, devices consume 80%–90% less power than when fully powered (<100 milliwatts).
    - For periodic communications (e.g., every 10 seconds), devices can enter a fully powered state to transmit or receive data and rapidly return to a low-power state.
    - Devices can be fully powered for as little as 67 milliseconds to transmit/receive data before returning to a low-power state.
    - Reduced power consumption is essential for a number of applications—particularly for battery-powered equipment.
- **Reduced product costs:** HPGP operates at lower data rates than conventional HomePlug Audio Visual (HPAV) devices. The reduced rates translate into reduced performance requirements for the analog front end (AFE) and a smaller memory requirement (for transmit/receive buffers and tone maps). As a result, implementation using a single-chip architecture was simplified. The single-chip architecture lends itself to a reduced footprint and lower system costs.
- **Electric vehicle applications:** HPGP was adopted for use in providing high-speed communications between electric vehicles and charging infrastructure via the charging cable. HPGP is included in international standards such as ISO/IEC[2] 15118 and SAE[3] J2931.

Lessons Learned

- Meeting demanding environmental and reliability requirements for automotive applications required package modifications and extensive environmental stress tests specified by AEC[4] Q-100.

Future Plans

- Qualcomm's HPGP-compliant chipset QCA7005 is currently in production on six electric vehicles.The chipset has been designed into several electric vehicles and plug-in electric vehicles that will enter production over the next several years.
- The QCA7000 has been adopted for future use in solar panel inverters in Asia.

[2] International Organization for Standardization and the International Electrotechnical Commission
[3] Initially established as the Society of Automotive Engineers
[4] Automotive Electronics Council

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- Plans are to continue to develop product enhancements to the QCA7000 and QCA7005 chipsets to promote use in future smart grid and electric transportation applications.

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