OAK RIDGE National Laboratory

High-Voltage, High-Power Density Traction Drive Inverter

(Keystone Project #1)

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Oak Ridge National Laboratory

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ORNL is managed by UT-Battelle, LLC
for the US Department of Energy

U.S. DEPARTMENT OF ENERGY

Overview

Timeline

- Start Date: FY19
- End Date: FY21
- 25% Complete

Barriers

- Passive components are bulky; Dc bus capacitor takes 20% of inverter volume
- Meeting DOE ELT 2025 High Voltage Power Electronics Targets
  - Power Density: 100kW/L
  - Cost: $2.7/kW
  - Peak Efficiency: > 97%
  - Reliability: 300,000 mile lifetime or 15 years

Budget

- Total project funding
  - DOE share – 100%
- Funding for FY19: $300K

Partners

- **National Renewable Energy Laboratory**
- **ORNL Team Members:** Shajjad Chowdhury, Emre Gurpinar, Randy Wiles

Any proposed future work is subject to change based on funding levels

Relevance – Project Objectives

Overall Objective:

- Develop technologies for next generation traction drive power electronic systems with 8x increase in power density to achieve DOE ELT 2025 target of 100 kW/L.
- Focus on traction drive inverter architecture, optimization of busbar design, minimization of passive components

FY 2019 Objectives:

- Evaluate and select traction drive inverter architecture
  - Impact of increased dc bus voltage
  - Multiphase and segmented inverters
- Produce a design for 100kW high-voltage inverter and validate the design via simulation
  - Evaluate the impact of selected topology on meeting the power density target

Any proposed future work is subject to change based on funding levels

FY19 Milestones and Go/No-Go Decision

Date	Milestones and Go/No-Go Decision	Status
Q1	**Milestone**: Select inverter topology candidates that can provide highest power density by using a higher dc bus voltage and minimizing dc bus capacitor	Completed
Q2	**Milestone**: Evaluate inverter topology candidates and generate component design data	Completed
Q3	**Go/No-Go decision**: Produce a design for 100kW inverter power stage and determine if design can meet DOE ELT 2025 targets. If the selected design can significantly improve power density, then include gate driver circuitry and sensors to complete the design.	On-track
Q4	**Milestone**: Complete a design for 100kW inverter and validate the design via simulation	On-track

Any proposed future work is subject to change based on funding levels

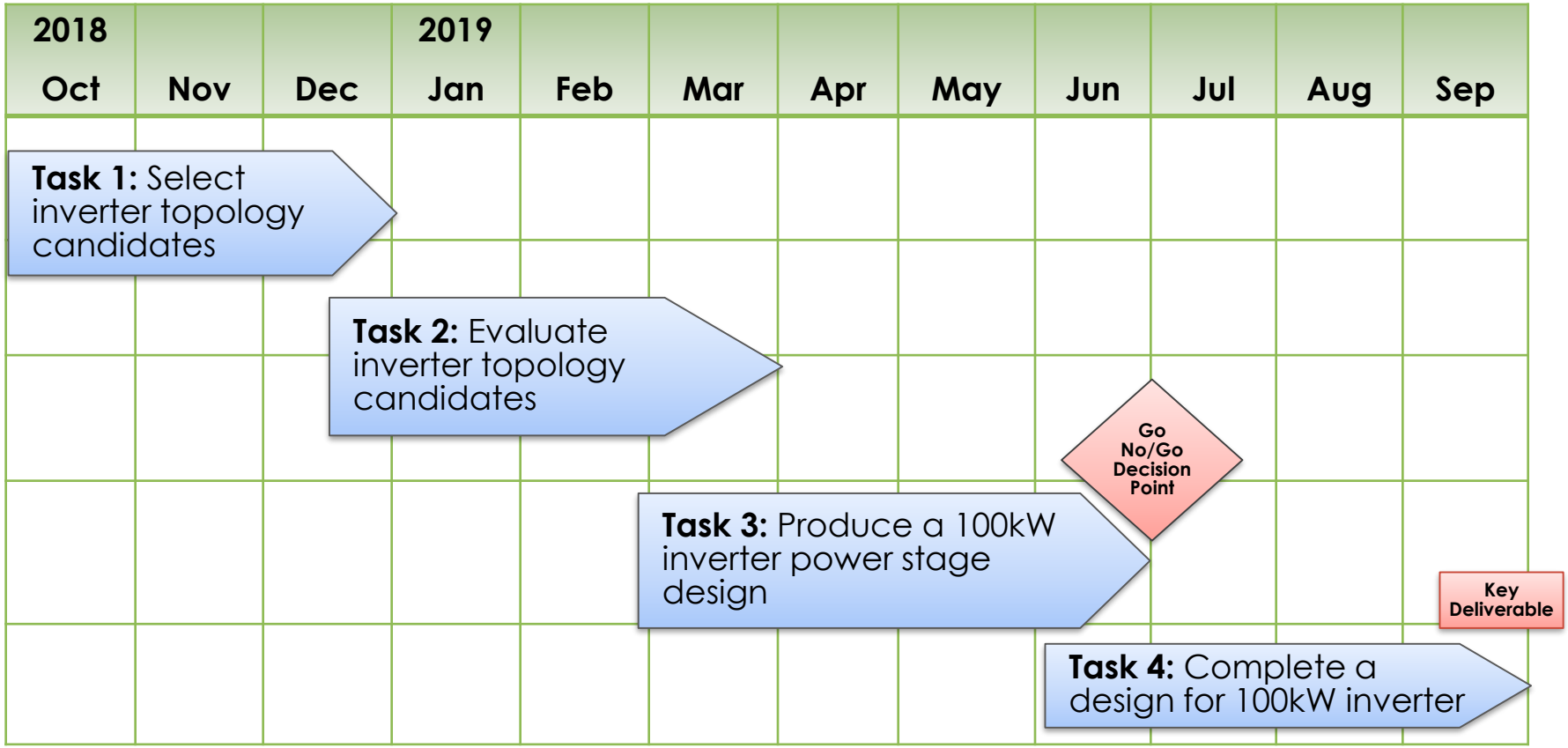
Approach

Goal: Increase traction drive power electronics system power density to meet DOE ELT 2025 targets (100kW/L) by focusing on power inverter architecture research and busbar designs for reduction of passive components

- **Inverter architecture to reduce capacitor requirements:**
  - Multiphase inverter
  - Segmented inverter arrangement
- **Increase dc bus voltage (800V+):**
  - Better utilize SiC switching devices' inherently higher voltage ratings
  - Reduce the size of SiC dies (lower cost)
  - Reduce phase and dc bus current
  - Evaluate impact of insulation requirements
- **Optimize dc bus bar designs:**
  - Embedded and distributed capacitors
  - Direct cooling of dc busbars

Any proposed future work is subject to change based on funding levels

FY19 Timeline



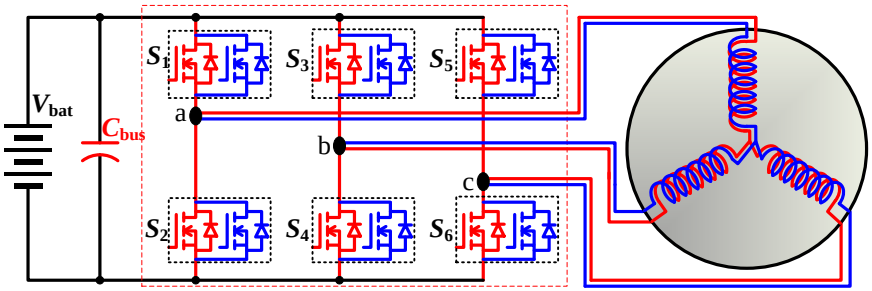
Go No/Go Decision Point: Determine if the inverter power stage design can meet DOE ELT 2025 targets. If the selected design can significantly improve power density, then include gate driver circuitry and sensors to complete the design.

Key Deliverable: A design for 100kW high-voltage, high-power density inverter

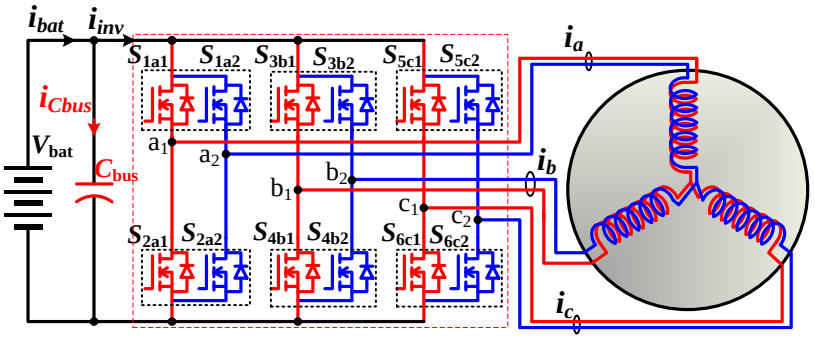
Technical Accomplishments – FY19

Use segmented inverter to reduce the dc bus capacitance

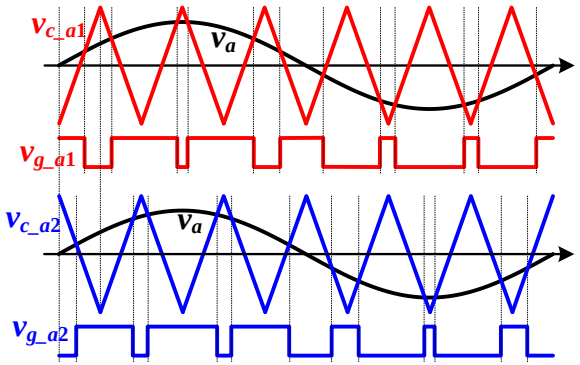
- **Segmented inverter**
  - Separate inverter switch dies and stator windings into two sets of drive unit
  - No changes needed in control of the motor except modifying the pulse width modulation (PWM) scheme
  - Interleaving the switching timings to reduce the dc bus ripple current



Standard 3-phase inverter



Segmented 3-phase inverter

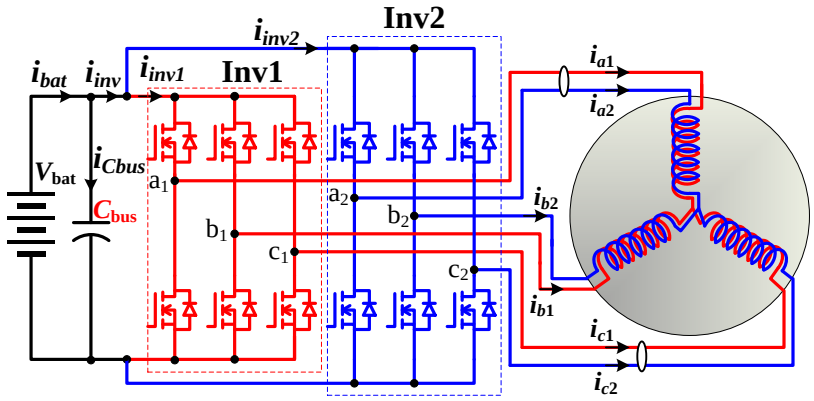


Reduction of capacitor ripple current with interleaved switching

Technical Accomplishments – FY19

Use segmented inverter to reduce the dc bus capacitance

- **Previous PWMs were based on phase-shifted carrier PWMs**
  - Triangle – 90 degrees
  - Sawtooth – 180 degrees



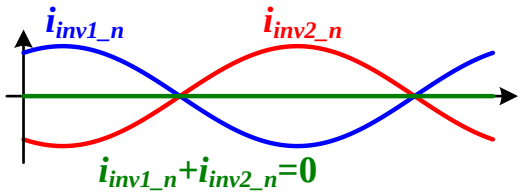
Segmented 3-phase inverter

$$i_{inv1} = 0.5\left\{ I_{dc} + \sum_{k=0}^{\infty}\sum_{n=1}^{\infty} I_{n,k}\,\mathbf{sin}[2\pi(nf_{sw} \pm kf_m)t + \alpha_{n,k}] \right\}$$

$$i_{inv2} = 0.5\left\{ I_{dc} + \sum_{k=0}^{\infty}\sum_{n=1}^{\infty} I_{n,k}\,\mathbf{sin}[2\pi(nf_{sw} \pm kf_m)t + \beta_{n,k}] \right\}$$

$$i_{inv} = I_{dc} + \sum_{k=0}^{\infty}\sum_{n=1}^{\infty} \sqrt{\frac{1+\cos(\beta_{n,k}-\alpha_{n,k})}{2}}\, I_{n,k}\,\mathbf{sin}[2\pi(nf_{sw} \pm kf_m)t + \frac{\alpha_{n,k}+\beta_{n,k}}{2}]$$

0 ~ 1 with $\beta_{n,k} - \alpha_{n,k} := [\pm\pi, 0]$

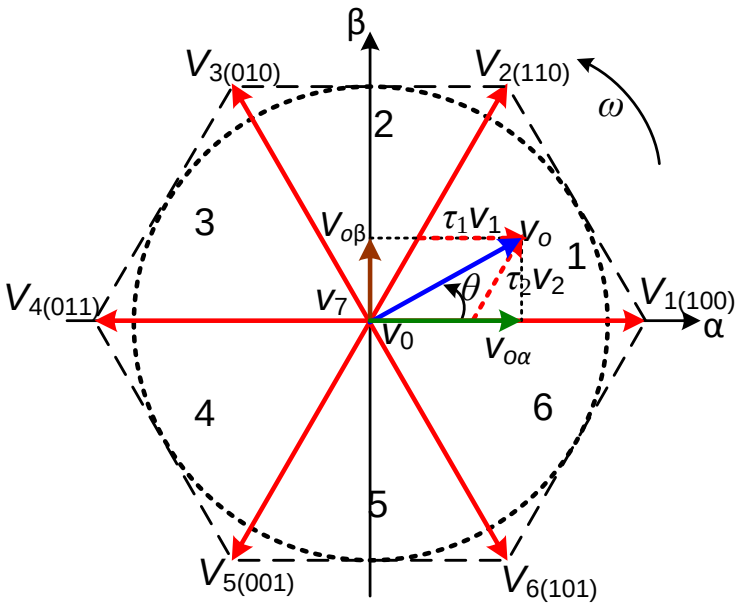


Reduction of capacitor ripple current with interleaved switching

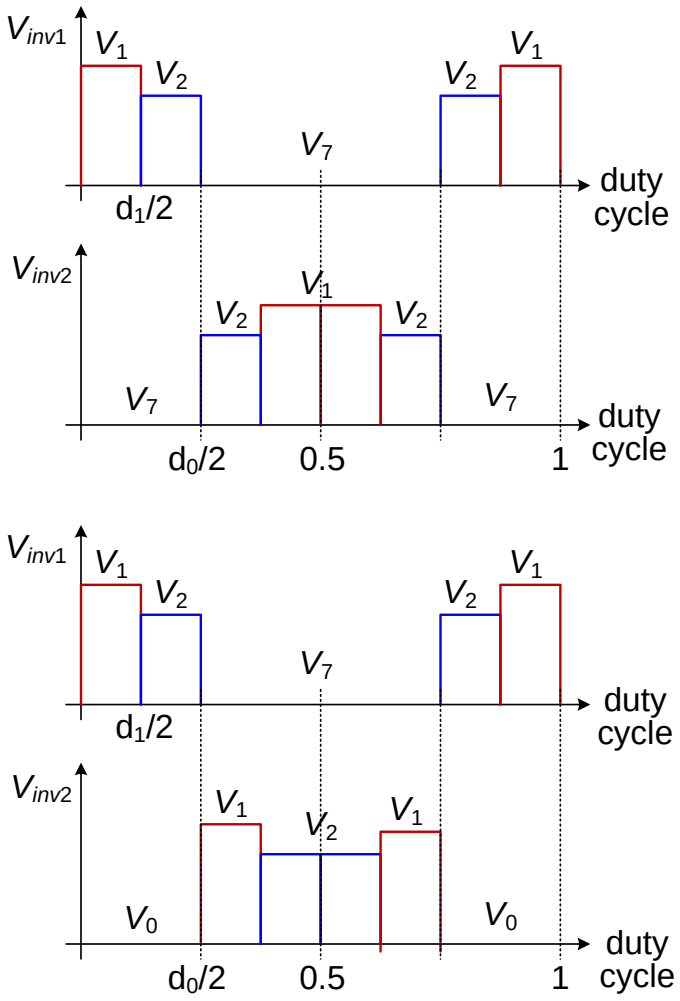
Technical Accomplishments – FY19

Developed New PWM schemes for segmented inverter

- New PWM Schemes
  - Based on space vector (SV) PWMs
  - Optimal zero vector placement
  - Use two-phase modulation to reduce switching losses



Voltage vectors in SV PWMs

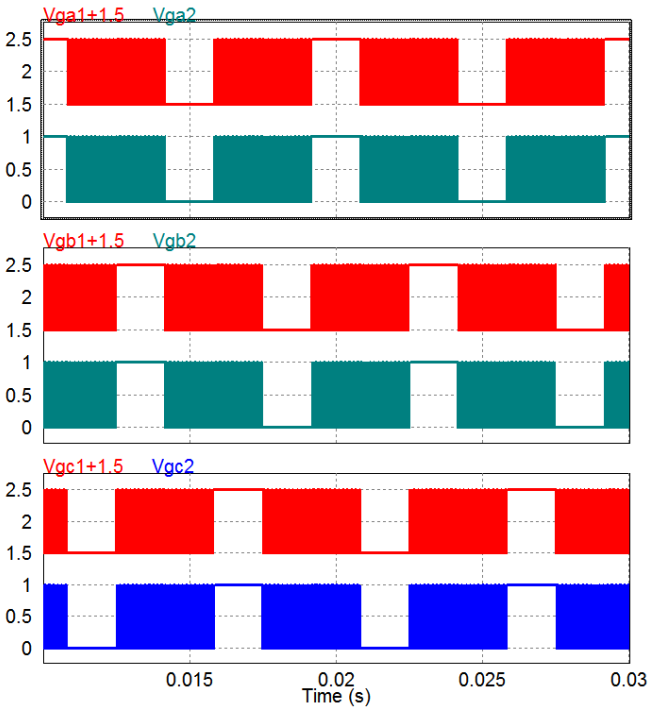


Optimal placement of zero vectors
In SV based 2-phase modulation to reduce dc bus ripple current (for sector 1)

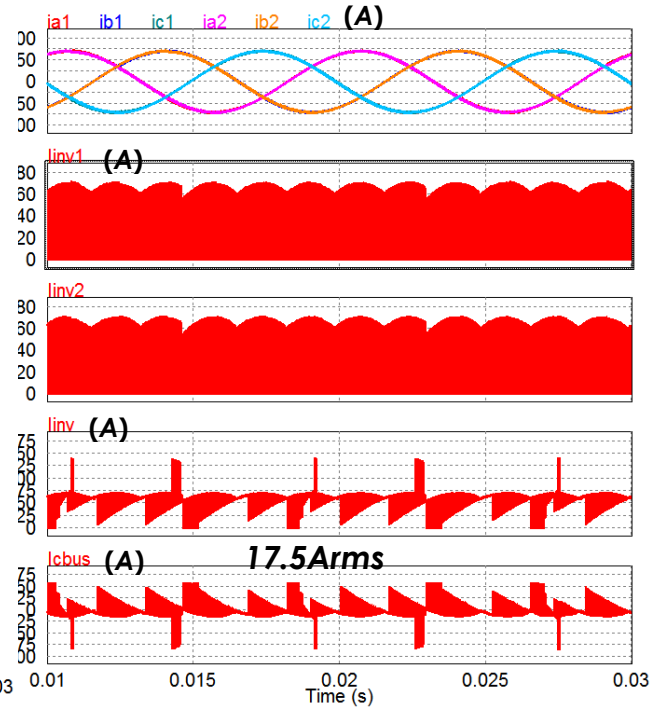
Technical Accomplishments – FY19

Simulation results verified significant reduction in dc bus ripple current with the new PWM schemes for segmented inverter

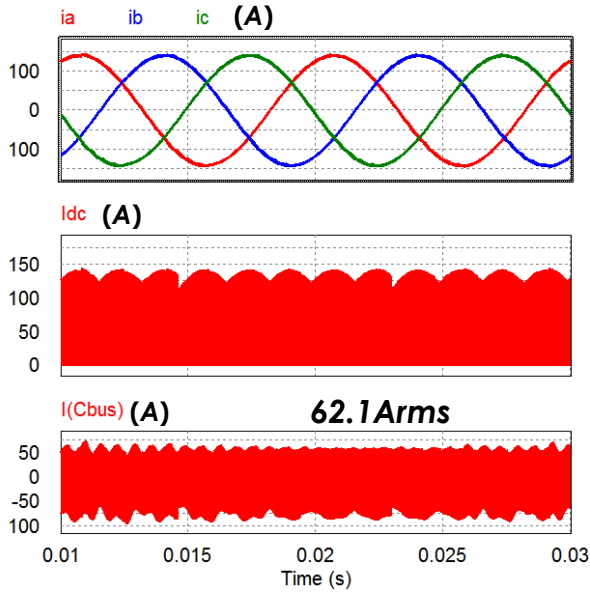
- Conducted simulation study and simulation results show significant reduction (up to 70%) in dc bus ripple current with the new PWM schemes for segmented inverter



Gate signals



Segmented



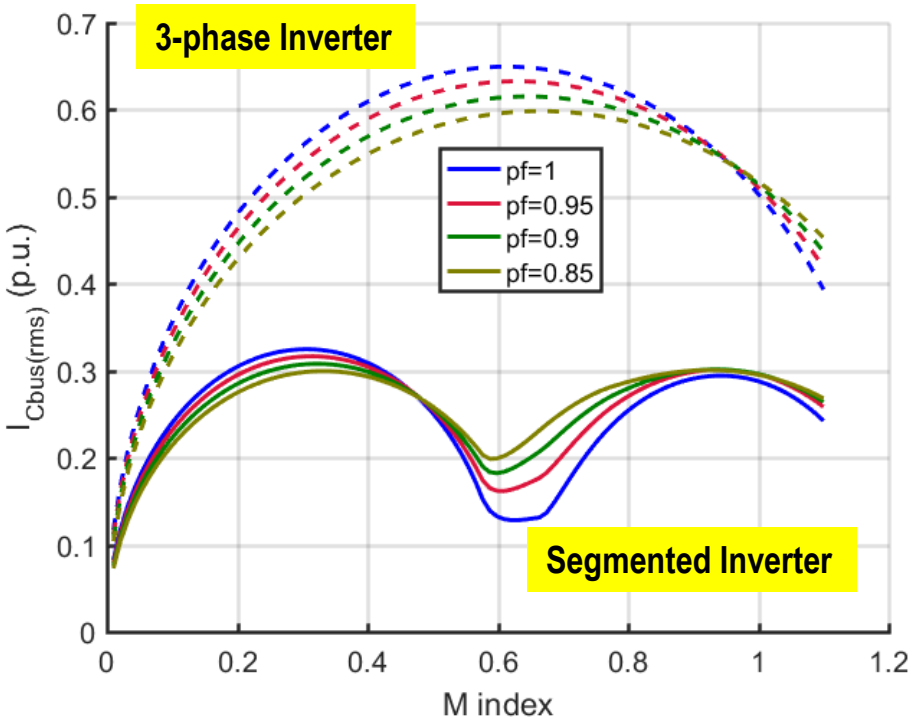
Non-segmented

Simulated operating waveforms (m=0.6, pf=0.9, Iph=100Arms)

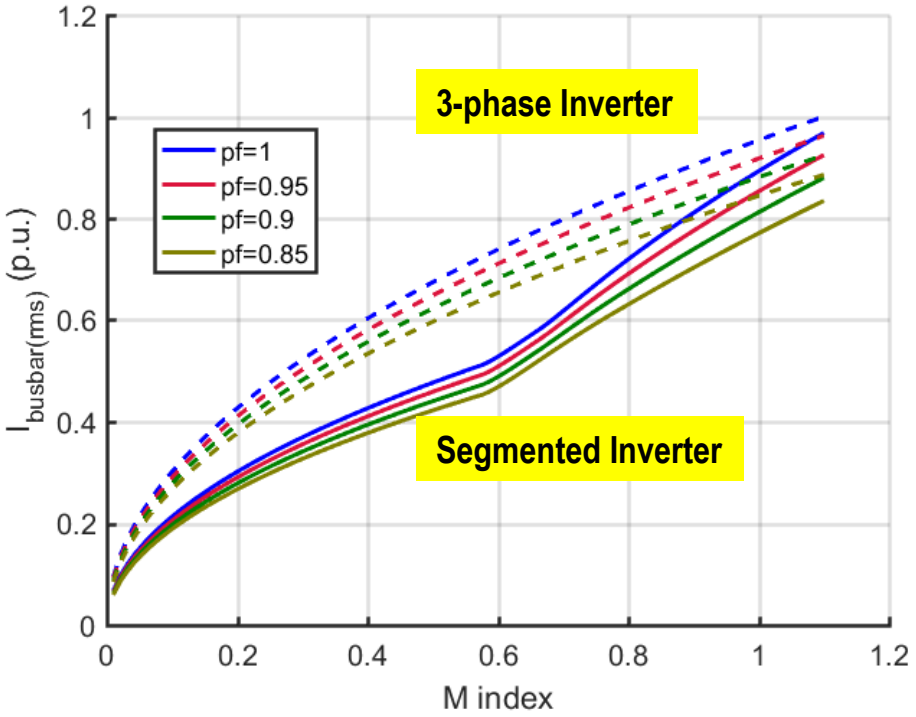
Technical Accomplishments – FY19

Developed Matlab code for switching timing based method for computing the inverter capacitor ripple current and busbar current

- Advantages of the switching timing based method
  - Faster than circuit simulation
  - More accurate and easy to implement various PWMs than analytical formulae
  - Will be used in optimizing inverter designs



Comparison of normalized capacitor ripple current vs modulation index for 3-phase and segmented inverters

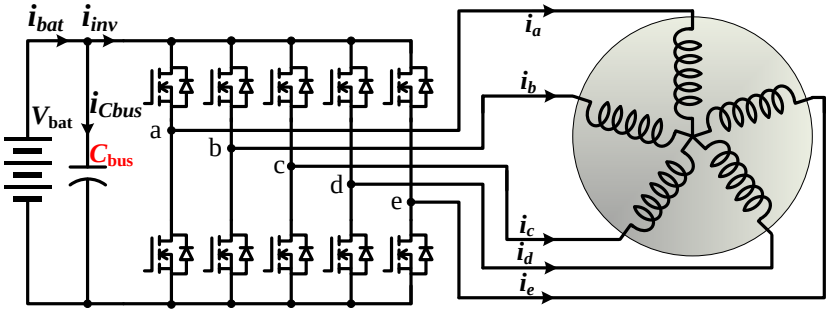


Comparison of normalized busbar current vs modulation index for 3-phase and segmented inverters

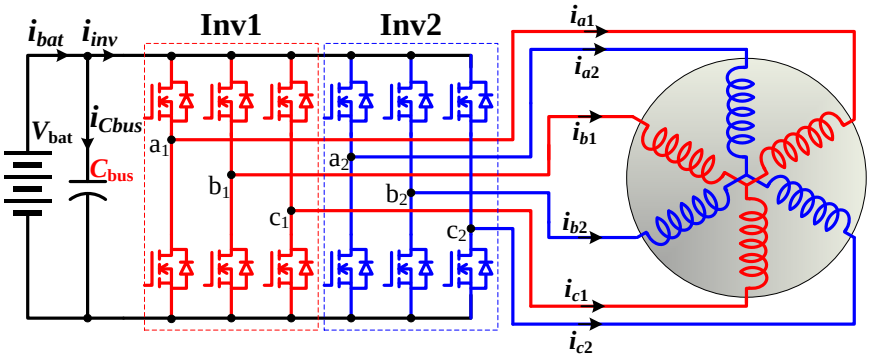
Technical Accomplishments – FY19

Six-phase inverter/motor has favorable features

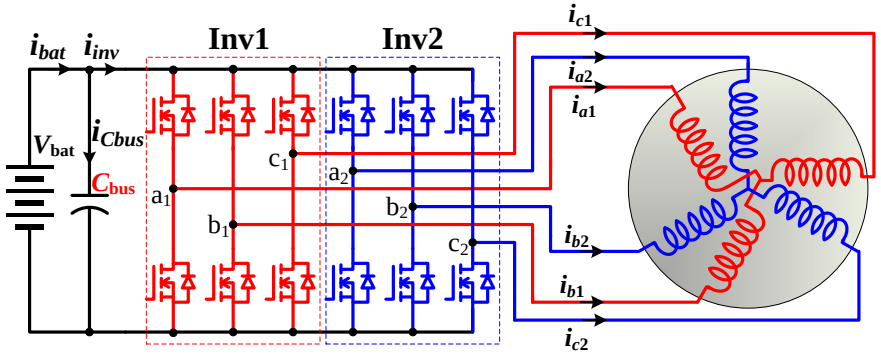
- Conducted feasibility study of multi-phase inverter/motor systems for traction drive applications
  - Lower phase current leads to moderate reduction in dc bus ripple current
  - Fault tolerance
- Five-phase system: complex control
- Six-phase system: operate as a dual three-phase system; simple control; can use segmented PWMs to reduce dc bus ripple current.



Five-phase inverter



Symmetrical six-phase inverter

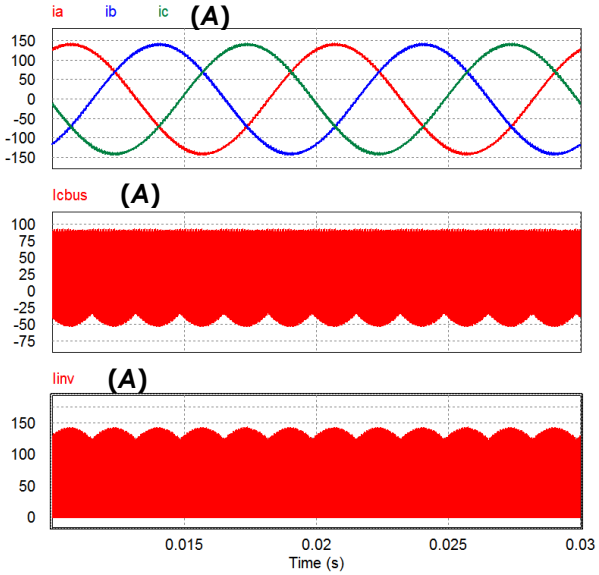


Asymmetrical six-phase inverter (30 degrees phase-shift between phase a_1 and a_2)

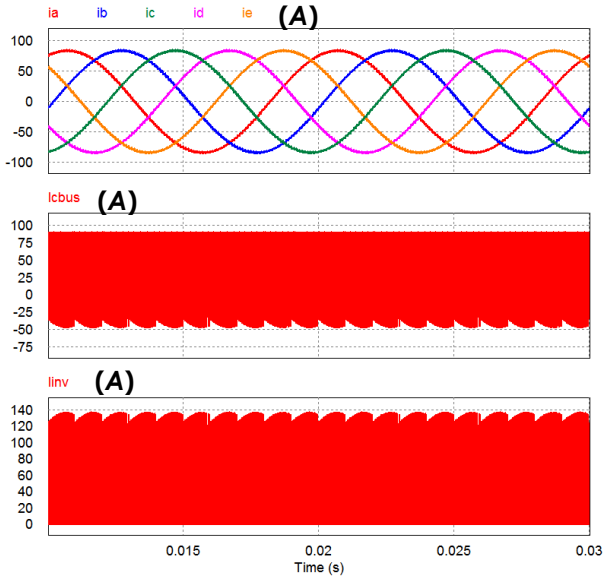
Technical Accomplishments – FY19

Six-phase inverter/motor has favorable features

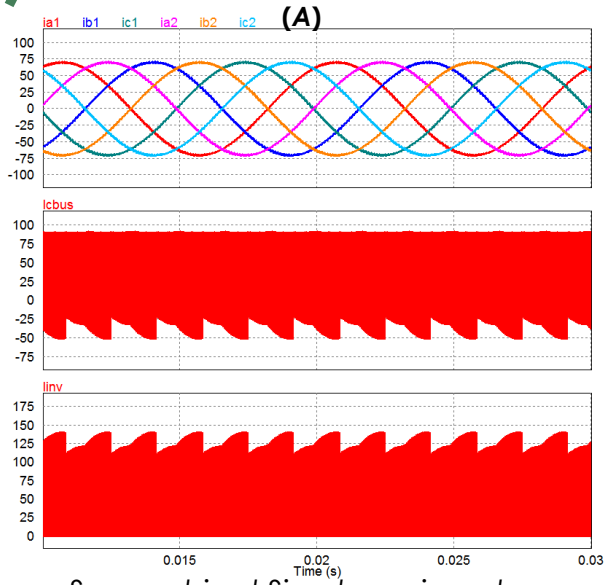
- Simulation results indicate moderate reductions in dc bus ripple current
  - Three-phase inverter, Idc_ripple = 53.8Arms
  - Five-phase inverter, Idc_ripple = 40.4Arms
  - Symmetrical six-phase inverter, Idc_ripple = 38.3Arms
  - Asymmetrical six-phase inverter, Idc_ripple = 43.9Arms (Can use the segmented PWM techniques)



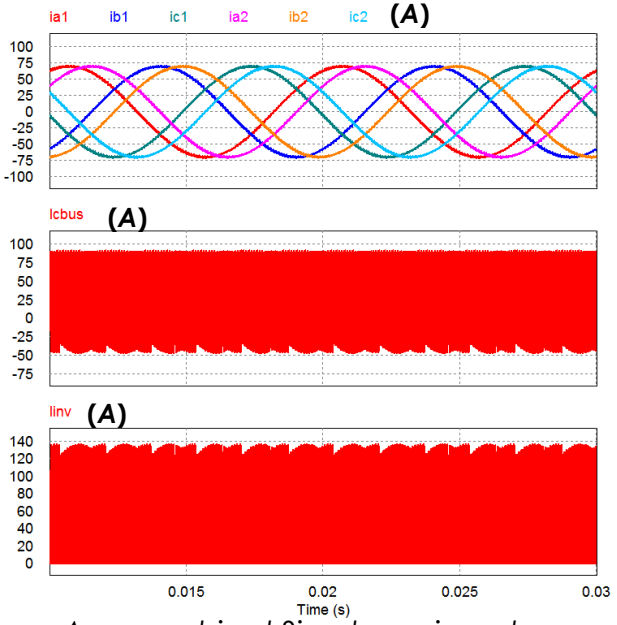
Three-phase inverter



Five-phase inverter



Symmetrical Six-phase inverter



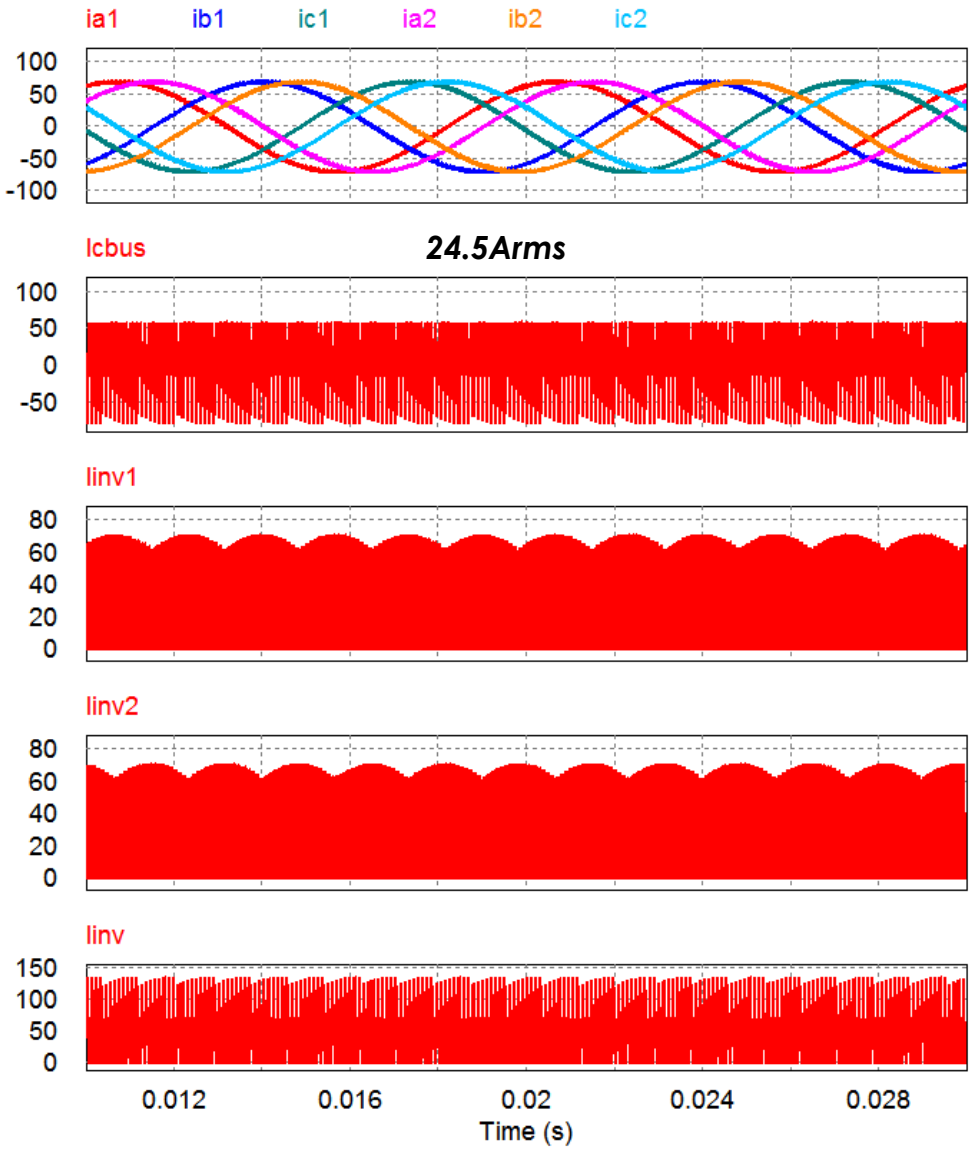
Asymmetrical Six-phase inverter

Simulated operating waveforms (m=0.65, pf=0.9, I3ph=100Arms)

Technical Accomplishments – FY19

Verified the segmented PWM techniques can be used to reduce the dc bus ripple current for the asymmetrical six-phase inverter/motor system

- Use the segmented PWM techniques to reduce the dc bus ripple current for the asymmetrical six-phase inverter/motor system.
- Simulation results show a reduction of 44% compared to when using the non-segmented PWM, 53% compared to the three-phase inverter

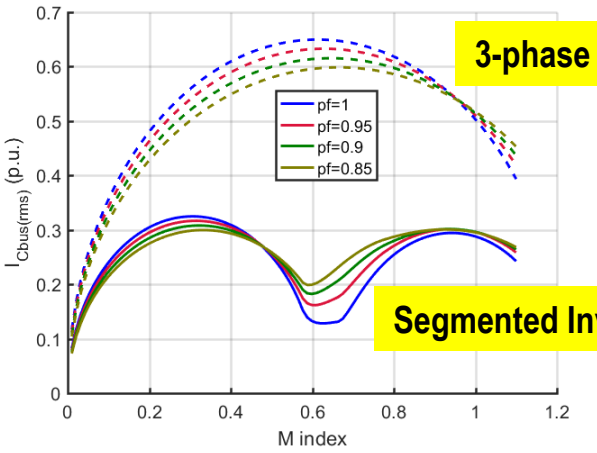


Simulation waveforms for the asymmetrical six-phase inverter using segmented PWM-switching

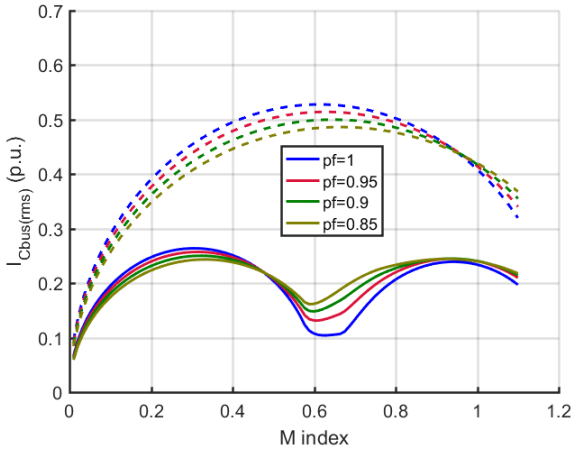
Technical Accomplishments – FY19

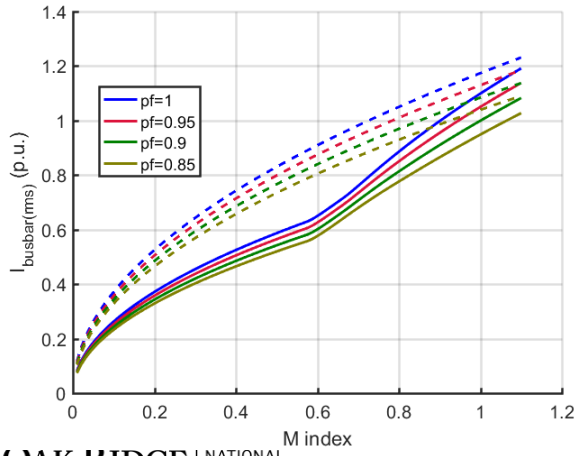
Increasing DC bus voltage can improve inverter power density

- Increasing DC bus voltage
  - Reduces phase current, leading to smaller switch dies and motor connections
  - Reduces dc bus ripple and busbar currents; decreasing the requirements for the dc bus components

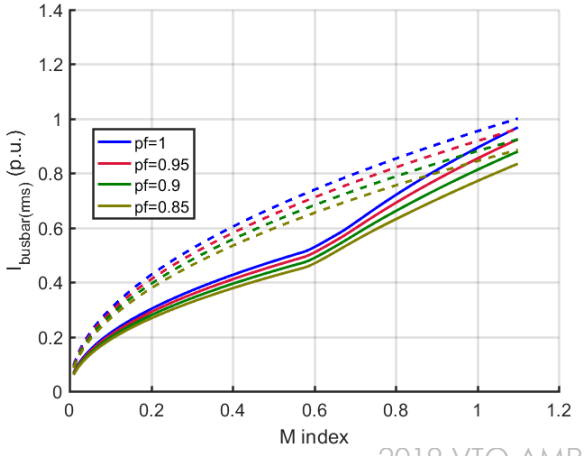


Dc cap. ripple current reduction for Vdc=650V to 800V





Dc busbar rms current reduction for Vdc=650V to 800V



Response to Previous Year Reviewers' Comments

This project is a new start

Collaboration and Coordination with Other Institutions

	**National Renewable Energy Laboratory** • Incorporate thermal management research results into inverter designs • Validate inverter thermal designs

Remaining Challenges and Barriers

- Accurate capacitor lifetime prediction based on driving profiles for optimally sizing the dc bus capacitor.

- Impact of higher dc bus voltage on the system insulation requirements.

Proposed Future Research

- **FY 2019**
  - Develop Matlab code to generate driving cycle inverter dc bus ripple current profiles
  - Develop dc bus capacitor sizing tools based on use cases
  - Design a 100kW high voltage inverter using the segmented topology to identify gaps for achieving the DOE ELT 2025 power density

- **FY 2020**
  - Address the gaps identified in FY 2019
  - Investigate direct dc bus cooling, and busbar designs with embedded and distributed capacitors to further reduce the dc bus capacitor requirements
  - Design and evaluate a 100kW high voltage inverter using WBG power modules developed in this program

Summary

- **Relevance**: Reducing inverter dc bus components will remove some of the barriers in inverter designs to achieve the ELT 2025 targets of 100kW/L and 300,000 mile lifetime
- **Approach**: Develop inverter topologies, increase dc bus voltage, and investigate direct bus cooling to minimize the inverter dc bus design
- **Technical Accomplishments**:
  - Developed space vector based new segmented PWM switching schemes
  - Developed tools in Matlab to accurately and speedily compute inverter dc bus ripple current
  - Evaluated the dc bus ripple currents of multiphase inverter/motor system and identified the asymmetrical six-phase inverter that can use the segmented PWM switching and offer fault tolerance
  - Verified increasing the dc bus voltage proportionally reducing the dc bus ripple current and busbar current
- **Collaborations and Coordination with Other Institutions**:
  - **NREL**: Discussing collaboration on inverter thermal management
- **Future Work**:
  - Develop dc bus capacitor sizing tools
  - Consider busbar designs with embedded and distributed capacitors
  - Design and evaluate a 100kW high voltage inverter using the segmented topology and WBG power modules developed in this program