U.S. DEPARTMENT OF ENERGY | Office of ENERGY EFFICIENCY & RENEWABLE ENERGY

FY 2016 Annual Progress Report for Electric Drive Technologies Program

July 2017

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ACRONYMS AND ABBREVIATIONS

3D	three dimensional
ac	alternating current
A	Ampere
AD	aerosol deposition
Adc	Amps direct current
Ag	silver
AGD	active gate drive
Al	aluminum
AM	additive manufacturing
APT	atom-probe tomography
ASIC	application-specific integrated circuit
ATF	automatic transmission fluid
Au	Gold
BCC	body-centered cubic
BEV	battery electric vehicle
BOPP	biaxially-oriented polypropylene
C	capacitor
CAD	computer-aided design
CAN	controller area network
CE	cluster expansion
CFD	computation fluid dynamics
CI	constant current
CIL	chemical-mechanical planarization
CMP	clamped inductive load
CPSR	constant power speed range
CPT	capacitive power transfer
CTE	coefficient of thermal expansion
CV	constant voltage
CVD	chemical vapor deposition
DAQ	data acquisition
DBC	direct bond copper
dc	direct current
di/dt	instantaneous current change rate
DF	dissipation factor
DFC	density functional theory
DOE	US Department of Energy
dv/dt	instantaneous voltage change rate
DWV	dielectric withstanding voltage
EDT	Electric Drive Technologies
EDV	electric drive vehicle
EM	electric motor
EMI	electromagnetic interference
ESL	equivalent series inductance

ESR	equivalent series resistance
EV	electric vehicle
FCA	Fiat Chrysler Automobiles
FCC	face-centered cubic
Fe	iron
FEA	finite element analysis
FHT	full heat treatment
FIB	focused ion beam
FOA	funding opportunity announcement
FWD	free-wheeling diode
GaN	gallium nitride
GGA	generalized gradient approximation
Gpm	gallon per minute
HAADF	high angle annular dark field
HALT	highly accelerated life test
HEMT	high electron mobility transistor
HEV	hybrid electric vehicle
HREM	high resolution transmission electron microscopy
HTRB	high temperature reverse bias
HTSOI	high temperature silicon-on-insulator
HV	high voltage
HV-WBG	high-voltage wide bandgap
HWFET	Highway Fuel Economy Test
ICD	Interface control document
IGBT	insulated gate bipolar transistor
IM	induction motor
IPMSM	interior permanent magnet synchronous machine
JBS	junction barrier Schottky
K	degrees Kelvin
L	Inductor
LNO	LaNiO3
MA	magnetic annealing
MC	Monte Carlo
MOSFET	metal oxide semiconductor field-effect transistor
MPH	miles per hour
MSR	multiple speed range
NA	North America
NGI	next generation inverter
NREL	National Renewable Energy Laboratory (DOE)
OBC	onboard charger
OEM	original equipment manufacturer
ORNL	Oak Ridge National Laboratory
PAW	projector-augmented wave
PBA	planar bond-all
PCB	printed circuit board
PCBA	printed circuit board assembly

PE	power electronics
PEI	polyetherimide
PEV	plug-in electric vehicle
PFC	power factor correction
PHEV	plug-in hybrid electric vehicle
PI	proportional integral
PIV	particle image velocimetry
PLZT	lanthanum zirconate titanate
PM	permanent magnet
PML	polymer multi-layer
POC	proof of concept
POD	proof of design
PP	polypropylene
PPS	polyphenylene sulfide
PSTTR	phase-sensitive transient thermoreflectance
PWD	pulse width modulation
PWM	pulse width modulated/modulation
R&D	research and development
RE	rare earth
Rms	root mean square
RTD	resistance temperature detection
SBD	Schottky barrier diode
SD	spinodal decomposition
SEM	scanning electron microscope
Si	silicon
SiC	silicon carbide
SMT	surface mount technology
SOI	silicon-on-insulator
SRM	switched reluctance machine
STEM	scanning transmission electron microscopy
TEM	transmission electron microscopy
TIM	thermal interface material
TDS	traction drive system
THD	total harmonic distortion
UDDS	Urban Dynamometer Driving Schedule
US06	US06 Supplemental Federal Test Procedure
U.S. DRIVE	Driving Research and Innovation for Vehicle efficiency and Energy sustainability (cooperative research effort between DOE and industry partners)
UVLO	under-voltage lockout
V	volt
Vac	volts of alternating current
VASP	Vienna Ab-initio simulation package
Vdc	volts of direct current (operating voltage)
VSM	vibrating sample magnetometer
VTO	Vehicle Technologies Office (DOE)
WBG	wide bandgap

WEG	water ethylene glycol
WFSM	wound field synchronous motor
ZS	zero sequence
ZSIN	zero sequence impedance network
ZVS	zero voltage switching

INTRODUCTION

1.1 Electric Drive Technologies Research and Development

DOE, the US Council for Automotive Research (composed of automakers Ford Motor Company, General Motors Company, and Chrysler Group), Tesla Motors, and representatives of the electric utility and petroleum industries make up the collaboration known as U.S. DRIVE (Driving Research and Innovation for Vehicle efficiency and Energy sustainability). U.S. DRIVE represents DOE's commitment to developing public–private partnerships to fund high-risk–high-reward research into advanced automotive technologies. It replaces and builds upon the partnership known as FreedomCAR (derived from "Freedom" and "Cooperative Automotive Research") that ran from 2002 through 2010 and the Partnership for a New Generation of Vehicles initiative that ran from 1993 through 2001.

The Electric Drive Technologies (EDT) subprogram within the DOE Vehicle Technologies Office (VTO) provides support and guidance for many cutting-edge automotive technologies now under development. Researchers focus on developing revolutionary new power electronics (PE), electric motor (EM), and traction drive system (TDS) technologies that will leapfrog current on-the-road technologies. This will lead to lower cost and better efficiency in transforming battery energy to useful work. Research and development (R&D) is also aimed at achieving greater understanding of, and improvements in how the various components of tomorrow's automobiles will function as a unified system.

In supporting the development of advanced vehicle propulsion systems, the EDT subprogram fosters the development of technologies that will significantly improve efficiency, costs, and fuel economy.

The EDT subprogram supports the efforts of the U.S. DRIVE partnership through a three-phase approach intended to

- Identify overall propulsion- and vehicle-related needs by analyzing programmatic goals and reviewing industry recommendations and requirements, and then develop and deliver the appropriate technical targets for systems, subsystems, and component R&D activities
- Develop, test, and validate individual subsystems and components, including EMs and PE
- Estimate how well the components and subsystems work together in a vehicle environment or as a complete propulsion system and whether the efficiency and performance targets at the vehicle level have been achieved.

The research performed under this subprogram addresses the technical and cost barriers that currently inhibit the introduction of advanced propulsion technologies into hybrid electric vehicles (HEVs), plug-in HEVs, battery electric vehicles (BEVs), and fuel cell powered automobiles that meet the goals set by U.S. DRIVE.

A key element in making these advanced vehicles practical is providing an affordable electric TDS. This will require attaining weight, volume, efficiency, and cost targets for the PE and EM subsystems of the TDS. Areas of development include

- Novel traction motor designs that result in increased power density and lower cost
- Inverter technologies that incorporate advanced wide bandgap (WBG) semiconductor devices to achieve higher efficiency while accommodating higher-temperature environments and delivering higher reliability
- Converter concepts that leverage higher-switching-frequency semiconductors, nanocomposite magnetics, higher-temperature capacitors, and novel packaging techniques that integrate more functionality into applications offering reduced size, weight, and cost
- New onboard battery charging electronics that build from advances in converter architectures for decreased cost and size
- More compact and higher-performing thermal controls achieved through novel thermal materials and innovative packaging technologies

- Integrated motor-inverter TDS architectures that optimize the technical strengths of the underlying PE and electric machine subsystems.

The EDT team conducts fundamental research, evaluates hardware, and assists in the technical direction of the VTO EDT program.

VTO competitively awards funding through funding opportunity announcement (FOA) selections, and projects are fully funded through the duration of the project in the year that the funding is awarded. The future direction for direct-funded work at the national laboratories is subject to change based on annual appropriations.

1.2 FY 2016 Accomplishments

1.2.1 High Power Density Ferrite PM Motor

Non-rare earth motors are critical to achieving low-cost high power density electric traction drives.

Most hybrid electric vehicle (HEV) and electric vehicle (EV) motors (machines) use permanent magnets (PMs) with heavy rare earth (HRE) materials such as neodymium and dysprosium because they facilitate the achievement of high power density, specific power, and efficiency. However, there has been significant market volatility associated with RE materials, including a price increase in dysprosium by a factor of 40 within 1 year (2011). Increasing the number of viable alternatives to HRE-based machines is a critical factor in providing greater certainty needed to enable mass production. A multidisciplinary research approach is required to achieve alternative motor technologies with competitive performance and efficiency, as well as comparable mass, volume, voltage, and other key metrics. Such a research approach includes the following capabilities: high accuracy modeling; research, use, and development of soft and hard magnetic materials; and comprehensive nonlinear computational optimization of geometric features and winding parameters. ORNL utilized its expertise in these areas to research and design a non-HRE-based alternative motor design, specifically a high power density ferrite PM motor.

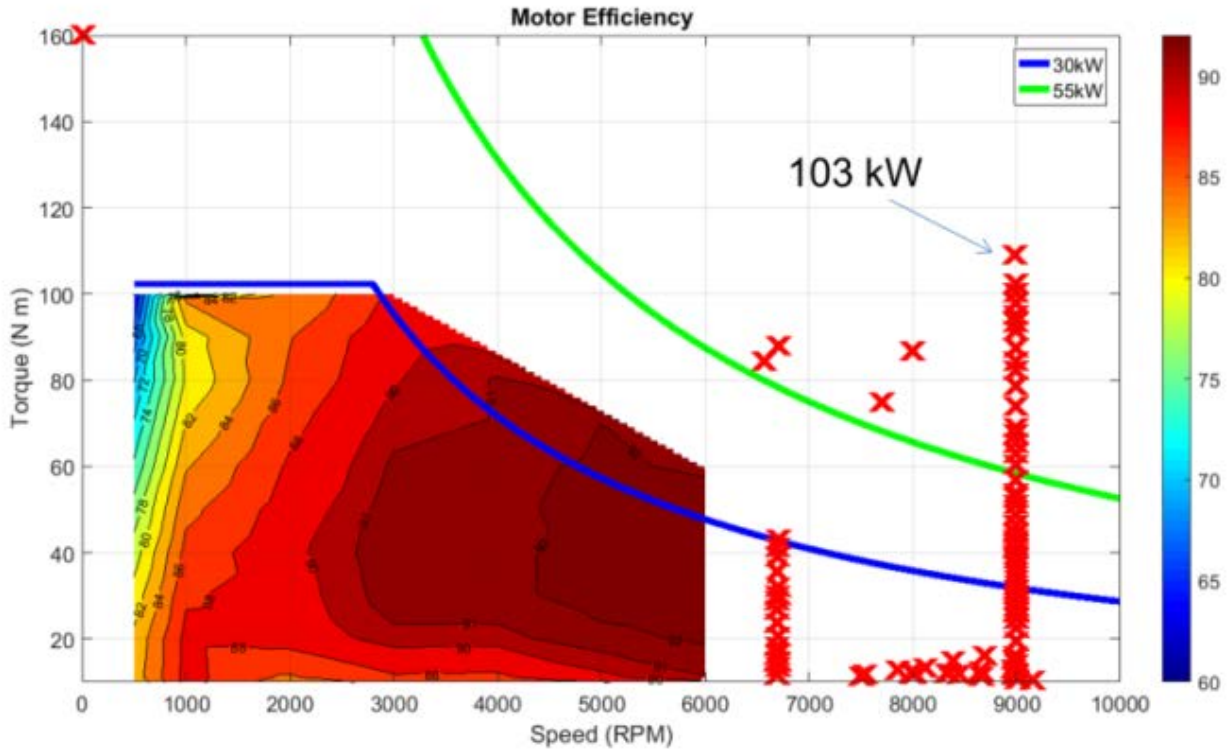

Figure 1-1: Performance and efficiency data from dynamometer testing of ORNL's ferrite PM prototype motor.

ORNL implemented a novel Guided Random Search method to optimize the ferrite PM motor design. After extensive optimization, the simulated peak power of the motor was 60 kW at 2,800 RPM, over 90 kW at about 4,500 RPM, and greater than 55 kW at 14,000 RPM. Figure 1-1provides an efficiency map for the motor design, and a summary of key simulated and measured performance metrics is given in Table 1-1. Detailed cost estimation efforts were conducted that include consideration of magnet grinding cost. Additionally, metrics associated with the measured power of 103 kW are also included in the table. ORNL estimates that the per-unit manufacturing cost at 100K units is projected to be less than $450. As shown in Table 1-1, DOE 2020 targets for power density, specific power, and cost are 5.7 kW/L, 1.6 kW/kg, and $4.7/kW, respectively. ORNL's non-HRE-based ferrite motor design exceeds these targets. Further materials and design research is critical to develop advanced HRE free machines.

Table 1-1: Simulated and measured performance data

Speed (RPM)	Peak Power [kW]	Power Density [kW/L]	Specific Power [kW/kg]	$/kW (Low)	$/kW (High)
DOE 2020 Target	55	5.7	1.6	4.7	4.7
2800 (simulated)	60.8	6.08	1.83	3.3	7.4
4500 (simulated)	93.5	9.35	2.81	2.1	4.8
9000 (measured)	103	10.3	3.10	1.9	4.4

1.2.2 Using Supercomputers to Develop Better Magnetic Materials

ORNL developed a unique simulation tool based on scaling laws and high performance computing for capturing domain formation and evolution under external magnetic fields. The simulations will be used to provide input for high accuracy finite element simulations of motor performance and efficiency.

ORNL conducted fundamental research to study the phenomena behind magnetization and loss characteristics of soft magnetic materials in electric motors to improve motor modeling accuracy. For example, it is important to understand the stresses induced during magnet manufacturing, since they have a considerable impact on losses and permeability. Soft magnetic materials are characterized by a remnant magnetic structure that consists of many magnetic domains. Each domain is a region where all the atomic magnetic moments are aligned in the same direction. The soft magnetic properties are determined by the ease with which the magnetic domains can respond to external magnetization and demagnetization, represented by a magnetic hysteresis loop.

Magnetic materials are used in several critical applications ranging from data storage and computing to electric motors and power generators. Their length scale ranges from nanometers (10^{-9} m) up to several meters. In order to design better devices that can meet the increasingly stringent demands of future technologies, it is necessary to (1) develop a fundamental understanding of the material chemistry and processing defects on the magnetic behavior at the atomistic length scale, and (2) predict the magnetic behavior at the device level length scale that accurately captures the underlying atomic level physics of magnetism as well as the coupling with the microscopic state of stress in the material. At ORNL, a unique simulation approach has been developed that utilizes the high computing power of the supercomputers to predict the magnetic constitutive properties - how the material responds to external stimuli - of materials used in electric motors to enable better motor design. This approach also enables development of high-efficiency, low loss magnetic materials through optimizing new material compositions and processing technologies. The example shown illustrates the ability of the simulations to predict the hysteresis loop for polycrystalline iron at the micrometer (10^{-6} m) scale that can be directly coupled with simulations of motor performance.

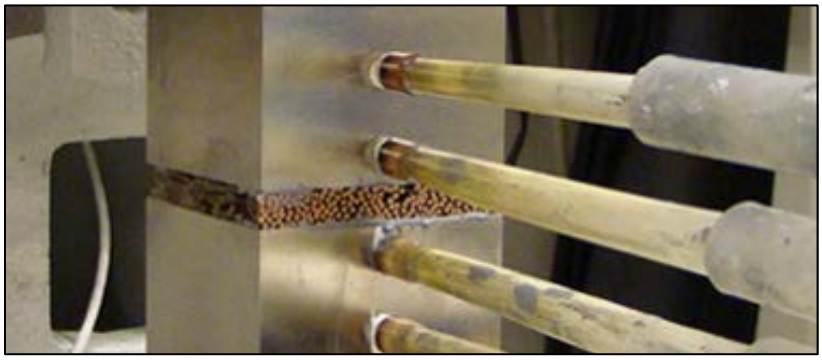

Figure 1-2: Test specimens with thermal transmittance setup for thermal measurements perpendicular to the wire axis.

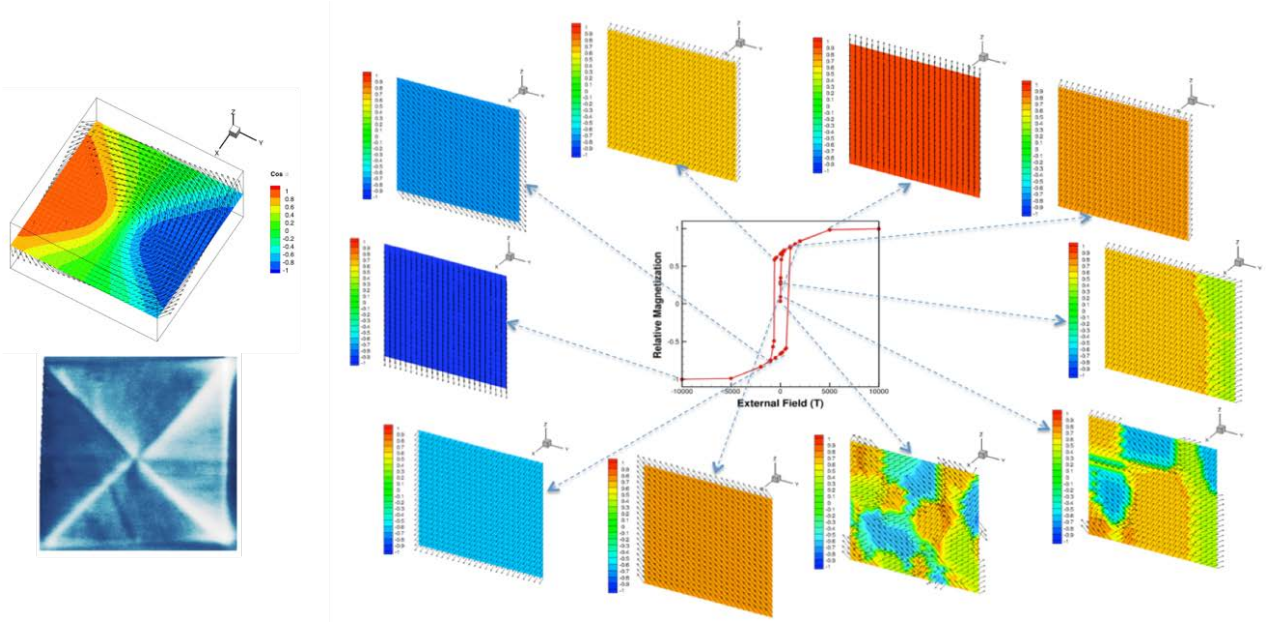

Figure 1-3: Simulation of a vortex domain structure in iron (top left) and experimentally observed vortex structure in iron (bottom left). Simulation of hysteresis loop for a polycrystalline grain structure in iron (right).

1.2.3 Materials Expertise Aids Manufacturers in Manufacturing and Commercialization of High-Performance Motors

ORNL and NREL demonstrated methods for measuring the thermal conductivity of motor winding materials, enabling characterization of new materials for high-performance motors.

Maximizing the efficiency, power density, and lifetime of motors requires thermal management of Joule-heating-losses in motor windings. Motor windings may be directly cooled via the exposed end turns of the winding, indirectly cooled with heat flowing into adjacent stator laminations to the motor housing, or both. Direct cooling applied to the motor end windings takes advantage of copper's high thermal conductivity as heat flows parallel to the copper wire axis. However, the efficiency of indirect cooling (i.e., heat transfer from the copper wires into the adjacent stator) is limited by the heat transfer perpendicular to the wound-wire and affected by the interstitial constituents that can include insulating wire-coatings, organic fillers, and porosity; constituents that all typically have low thermal conductivity relative to copper. Additionally, interface thermal resistances between each constituent further impede heat transfer. New materials such as composites could improve heat transfer, but the highly anisotropic or direction-dependent thermal properties inherent to composite materials require specialized equipment for measuring the thermal conductivity.

Table 1-2: Comparison of test procedures and ability to measure direction-dependent thermal properties of winding samples.

Test Approach	Parallel to Wire Axis	Perpendicular to Wire Axis
Laser Flash E1461	Y	Y
Transient Plane Source ISO 22007-2	N	N
Thermal Transmittance ASTM D5470	N	Y

ORNL and NREL measured the thermal conductivity parallel and perpendicular to the axis of the wire using laser flash, transient plane source, and transmittance test methods (Table 1-2). Each test method was compared for a range of materials from monolithic homogeneous materials to anisotropic wire bundles with different wire diameters. The tested wire samples had a copper volume fraction between 50%-60% and wire diameters of 670 to 925 µm. The thermal conductivity perpendicular to the wire axis was about 0.5 - 1 W/mK, whereas it was over 200 W/mK in the parallel direction.

The tests demonstrated that the anisotropic thermal conductivity of packed copper wire can be satisfactorily estimated with appropriate specimen preparation using the laser flash and transmittance test methods as summarized in Table 1-2. The thermal transmittance measurement uncertainty parallel to the wire axis was high for the tested sample geometry. The transient plane source (hot disk) method did not consistently produce trustworthy and defendable apparent thermal conductivity results for these specimens and their architecture. The test results provide a baseline for comparing new materials, and highlight methods for appropriately testing the thermal impact of new materials or winding structures relevant to motor windings.

1.2.4 High Temperature DC Bus Capacitor Cost Reduction & Performance Improvements

Reduces the cost, size, and weight of the DC-link capacitor by >50% while increasing durability in high temperature environments.

Sigma and their partners Delphi Automotive (Delphi) and Oak Ridge National Laboratory have made significant progress in developing improved DC bus capacitors, fabricating and packaging these capacitors, and developing a business plan for production. Full size (300µF, 500µF and 700µF) capacitors have been produced which meet or exceed technical targets for DC bus capacitor performance and packaged life testing shows stability under various environmental conditions, including high temperature automotive environments.

Table 1-3: Sigma PML capacitor performance compared to DOE capacitor development targets for a ~700 µF capacitor.

Characteristic	DOE Target	PML Capacitor
Temperature	-40 to 140°C	-40 to 140°C
Loss	1 %	< 1 %
Volume	< 0.6 L	< 0.3 L
Cost	< $30	< $20

Sigma has developed a solid-state Polymer-Multi-Layer (PML) capacitor comprising 1000s of radiation cured polymer dielectrics and aluminum electrodes to form a large area nano-laminate that can be segmented into individual capacitors.

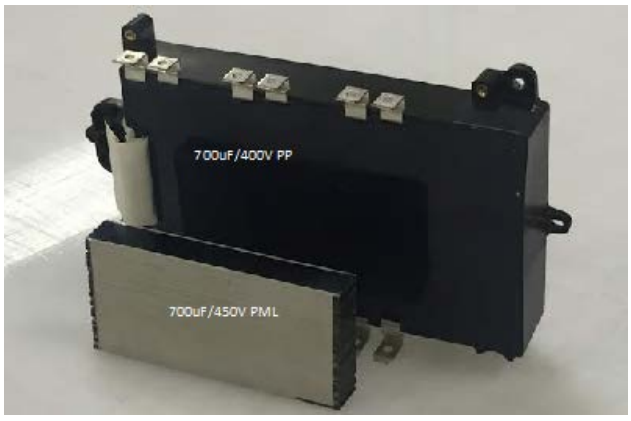

Figure 1-4: Comparison between current metalized polypropylene DC bus capacitor and the developed PML capacitor. Both are rated at 700 µF, but the PML capacitor can handle 140°C temperatures, an increase of 35 degrees over current capacitors.

This PML technology represents a transformational and potentially disruptive technology. The current supply chain to manufacture metallized polypropylene capacitors involves a film manufacturing operation, an electrode metallizing operation and a capacitor manufacturing operation. Virtually all capacitor manufacturers use the same base polypropylene dielectric films, which leaves little room for innovation and advancement of the technology to meet market needs. This PML material which comprises a large sheet of multilayer material is instead produced in a one step process using a liquid monomer and aluminum wire into a process chamber. This allows a capacitor OEM to control all key material and process parameters, including the dielectric formulation, dielectric thickness, electrode material, electrode thickness, capacitor shape, and capacitor size. This approach to capacitor production can reduce the cost of metallized polymer capacitors and allow a capacitor OEM to innovate and create application-specific products with different polymer dielectric properties.

Sigma is in the process of designing and fabricating a production scale machine to manufacture bulk PML capacitor material.

1.2.5 Vehicle Electric Motor Design Uses Permanent Magnets Without Any Rare Earth Content

Current motor designs use permanent magnets containing rare earth materials, which have shown unstable prices, supply constraints, and temperature limits.

Through a cooperative R&D project with the Vehicle Technologies Office (VTO), UQM Technologies, a company developing propulsion systems for electric, hybrid electric, plug-in hybrid electric and fuel cell electric vehicles, recently patented a new design for electric vehicle motors that use non-rare earth magnets.

Figure 1-5: Comparison between current metalized polypropylene DC bus capacitor and the developed PML capacitor. Both are rated at 700 µF, but the PML capacitor can handle 140°C temperatures, an increase of 35 degrees over current capacitors.

While most plug-in electric vehicles (PEVs) use motors with rare earth magnets, these magnetic materials are expensive, prices have been highly volatile, and their supply may be short as the future market demand is expected to be high. Electric motors that do not use rare earth magnets will potentially be less expensive and rely more on domestic resources and processing capabilities, improving economic, environmental and energy security. In the past six years, rare earth magnet prices have fluctuated between $80/kg to $750/kg, while the metal that will be used in the new motor has a much more stable price. Reducing the use of rare earth magnets in PEVs can also help alleviate future supply concerns for these materials, which have seen supply restrictions and reductions in recent years.

UQM's new motor design performs comparably to rare-earth motors, helping the company meet critical size, weight, and efficiency targets for vehicle applications. It also provides the company flexibility to adapt to the market. Once UQM develops the design, it can either use the original rare earth-based design or the new one, depending on the price and availability of rare earth materials.

Table 1-4: UQM motor performance compared to DOE 2015 Motor Targets.

Characteristic	DOE Target	Achieved
Efficiency	>90%	Comply
Peak Power	55 kW	55 kW
Maximum Speed	10,000 rpm	10,000 rpm
Torque	262 N-m	235 Nm
Total Volume	≤ 9.7 L	9.59 L

As part of this project, UQM is collaborating with DOE's Ames National Laboratory to improve the magnets' properties, the National Renewable Energy Laboratory to develop thermal management approaches, and Oak Ridge National Laboratory to test the motor.

UQM, a Colorado-based company, currently has the capability to manufacture at least 50,000 electric drive systems annually. The company is supplying motors to transit bus company Proterra and has supply agreements with energy management and vehicle companies around the world.

1.2.6 Application of SiC Power Devices in Hybrid Electric Vehicle Drive Systems

SiC MOSFETs can significantly reduce inverter losses, and have the potential to replace Si IGBTs for improved drive system efficiency and reliability with reductions in power inverter weight and size.

Present-day traction inverters are expensive, heavy, and bulky which ultimately can limit their adoption in the greater automotive market. This project has demonstrated the benefits of reduced system cost and extended reliability for electric drive systems through the application of 900 V Silicon Carbide (SiC) Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs) into advanced power modules and demonstrated traction drive technology. This new SiC MOSFET based module significantly reduces losses in an electric drive system modeled after the Ford Focus with project partner Ford, ultimately increasing vehicle fuel economy, range, and productivity.

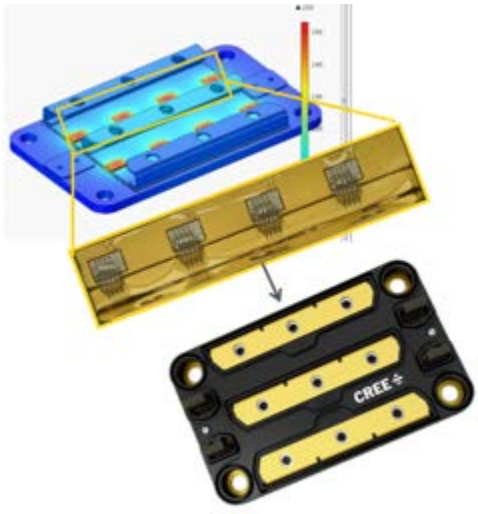

Figure 1-6: 900V, 1.25mΩ SiC power module with record-low on-state losses, based on new 900V SiC MOSFETs

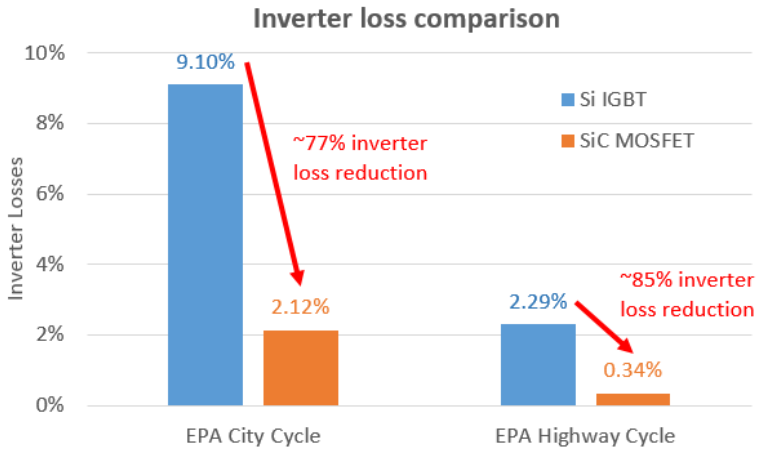

Figure 1-7: 78% combined inverter loss reduction is possible when using the 900V SiC power modules in place of Si IGBT power modules for a 90kW Ford Focus EV.

The 900V, 10mΩ SiC MOSFETs were fabricated with a total chip area of 32mm^2. In Figure 1-6, the advanced power module with SiC MOSFETs inside is shown. A record low 1.25mΩ on-resistance was measured, dramatically lowering on-state losses. The 900V SiC MOSFETs room temperature on resistance is approximately 41% less than the 650V Si MOSFET, and 63% less at 150˚C. Significantly, the overall total die size of the SiC MOSFET is ~1/3 of the currently used silicon Insulated Gate Bipolar Transistor (IGBT) and diode pair it replaced with similar power capability in power module testing. This reduction in required semiconductor area and losses for a similar power rating can significantly reduce costs associated with electric drive systems.

Figure 1-6 shows the comparison between a Si IGBT and Wolfspeed SiC MOSFET for traction drive operation. Compared to currently used Si devices, SiC reduces inverter losses by ~78% in electric-only drive mode for the EPA metro-highway cycle combined. Energy savings from using SiC devices can vary significantly with different drive cycles, and savings are greatest for cycles that include city or urban driving patterns and more aggressive drive cycles. Estimated volume die pricing of SiC should be attractive for mass adoption in automotive systems once it reaches a cost of <2 times that of Si.

1.2.7 High Temperature, Wide Bandgap (WBG) Inverter for Electric Vehicles

This SiC inverter is the first traction drive optimized for wide bandgap devices that utilizes a commercially available SiC power module and can operate in high temperature automotive environments.

Wolfspeed's high-temperature, WBG underhood inverter was developed in response to the need for smaller, lighter, and more efficient systems with higher power density in the electric vehicle market, and in collaboration with: the Toyota Research Institute of North America, the National Renewable Energy Laboratory, and the University of Arkansas National Center for Reliable Electric Power Transmission.

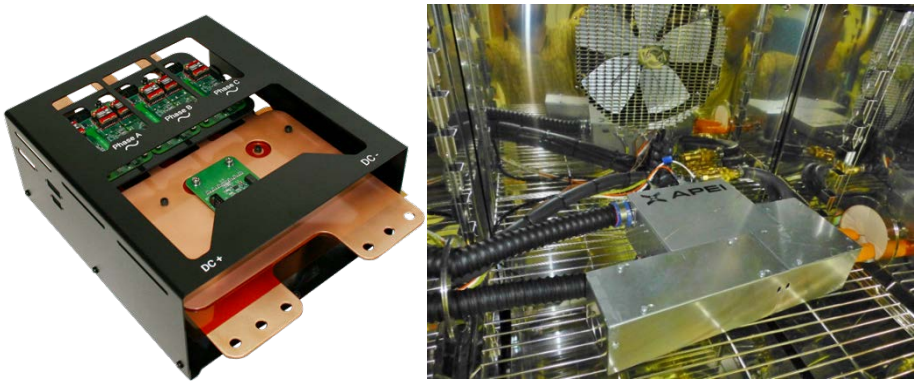

Figure 1-8: (Left) SiC-based traction drive inverter. (Right) Inverter under test in an environmental chamber.

Underhood inverters convert the DC power stored in hybrid, plug-in hybrid, or all-electric vehicle battery packs to three-phase AC power that can be used to energize one or more electrical loads, and traditionally employ industry standard silicon semiconductors. Utilizing Wolfspeed's WBG semiconductor devices and advanced packaging techniques in an underhood inverter allowed engineers to achieve faster switching with reduced system-level losses during high ambient (140°C) and high coolant (105°C) temperature operation. This WBG-based system significantly outperforms silicon technology for vehicle inverters—especially at light load conditions, and was named an R&D Magazine Top 100 Award winner as one of the top technical breakthroughs in 2015.

Table 1-5: Wolfspeed's Inverter Versus DOE 2020 Targets

Characteristic	DOE 2020 Target	Achieved
Efficiency (over 4 bus voltages, 6 thermal cases, & 3000+ operating points)	>93%	Avg. 96.3% Peak 98.9%
Peak Power	55 kW	81.8 kW
Weight	< 3.9 kg	4.0 kg
Volume	< 4.1 L	4.4 L
Cost	≤ $182	~$192

Wolfspeed's WBG technology increases the unit's peak power delivery by 2–3 times what is currently achievable with silicon-based devices, while operating at overall higher ambient temperatures.

1.2.8 Thermal Management of WBG Technology Critical for Power-Dense and High-Temperature Systems

NREL demonstrated WBG-enabling thermal management technologies for high-temperature and high-efficiency WBG devices within automotive power electronic systems.

Wide-bandgap (WBG)-based power electronics will increase driving range and reduce cost of electric-drive vehicles through increasing efficiency, supporting higher junction temperatures, enabling higher switching frequencies, and increasing power densities in automotive power electronics systems (e.g., inverter). Achieving these benefits requires thermal management of the devices as well as the surrounding system components. A challenge with WBG devices is that although their losses in the form of heat are lower, the area of the devices is also reduced to increase power density and reduce costs, which results in higher device heat flux. Additionally, the high junction temperatures of WBG devices will result in larger temperature gradients through the power module that will present reliability challenges and require high- temperature bonding materials. Another challenge with the higher junction temperatures is that they will expose other system components (e.g., capacitors and electrical boards) to higher temperatures. These challenges require system-level thermal management analysis and innovative thermal management solutions.

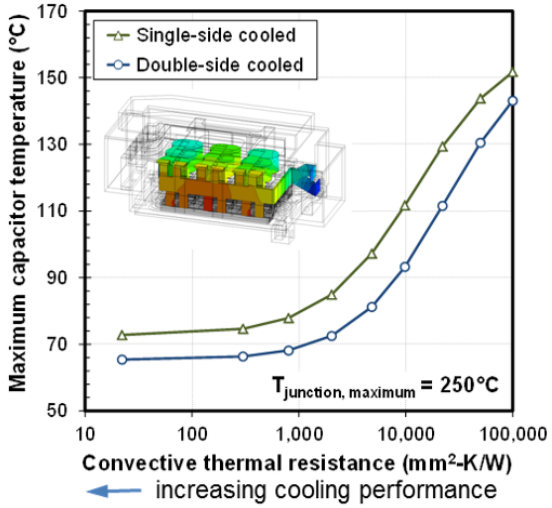

Figure 1-9: Simulation-predicted capacitor temperatures for a WBG operating condition with results showing that electrical interconnection cooling enables capacitor temperatures <85°C for WBG device temperatures up to 250°C.

Using high-performance computing resources, NREL quantified the three-dimensional steady-state and transient temperature and heat flow at the component and system level of an automotive inverter. The analysis quantified the inverter component temperatures resulting from the higher junction temperature enabled by WBG devices (from 175°C to 250°C). The results show that the capacitors, electrical boards, and module interface layers will exceed their allowable operating temperature limits under most WBG operating conditions. The resulting information is useful to component manufacturers and material suppliers working to commercialize WBG-based power electronics.

For example, capacitors are critical components in power electronics, but their low maximum operating temperatures (85°C) pose thermal management challenges when packaged within high-temperature WBG environments. NREL demonstrated and compared the efficacy of capacitor thermal management approaches, demonstrating that cooling the electrical interconnections was a more effective thermal management strategy than directly cooling the capacitors. The electrical interconnect (Figure 1-8) cooling approach was predicted to enable capacitors to operate within their allowable temperature limits at WBG junction temperatures up to 250°C. The cooling solutions developed in this project will enable high-temperature WBG packaging within automotive power electronics.

1.3 Small Business Innovative Research Grants

Steven Boyd, Technology Manager
Vehicle Technologies Office
1000 Independence Avenue, SW
Washington, DC 20585
Phone: (202) 586-8967
E-mail: steven.boyd@ee.doe.gov

Start Date: October 1, 2015
Projected End Date: September 30, 2016

Objectives

- Use the resources available through the Small Business Innovation Research (SBIR) and Small Business Technology Transfer (STTR) programs to conduct research and development of technologies that can benefit the Electric Drive Technologies (EDT) subprogram within the Vehicle Technologies Office.
- Achieve the four SBIR goals: (1) to stimulate technological innovation; (2) to use small businesses to meet Federal R/R&D needs; (3) to foster and encourage participation by socially and economically disadvantaged small businesses; and (4) to increase private sector commercialization of innovations derived from Federal R/R&D, thereby increasing competition, productivity, and economic growth.

Accomplishments

- Initiated three Phase I awards and two Phase II awards

Introduction

Small Business Innovation Research (SBIR) and Small Business Technology Transfer (STTR) are U.S. Government programs in which federal agencies with large research and development (R&D) budgets set aside a small fraction of their funding for competitions among small businesses only. Small businesses that win awards in these programs keep the rights to any technology developed and are encouraged to commercialize the technology. Each Fiscal Year, the 11 participating SBIR and STTR federal agencies set aside the following percentage of their extramural R&D budgets over $100 million. Extramural refers to federal funding that an agency awards to external entities such as universities, national laboratories, and large businesses to address the principal agency mission needs.

Recently the purpose of SBIR programs has evolved to have greater emphasis on commercialization. This is accomplished through the evaluation of commercial potential in Phase I and Phase II applications, and seed capital for early stage R&D with commercial potential. Furthermore, awards made are comparable in size to angel investments in the private sector, and accept greater risk in support of agency missions. A study performed by the National Research Council in 2008, “An Assessment of the SBIR Program at the Department of Energy”, reports that a significant percentage of DoE SBIR projects are commercialized to some degree. The cited survey data indicate that 41 percent of SBIR-funded projects reach the marketplace or have commercialization underway. Of the DoE SBIR award recipient firms that responded to the NRC Phase II Survey and reported sales of some type, 76 percent sold to domestic private sector firms and 14 percent to export markets.

Approach

Each year, DOE issues a solicitation inviting small businesses to apply for SBIR/STTR Phase I grants. It contains technical topics in such research areas as energy production (Fossil, Nuclear, Renewable, and Fusion Energy), Energy Use (in buildings, vehicles, and industry), fundamental energy sciences (materials, life, environmental, and computational sciences, and nuclear and high energy physics), Environmental

Management, and Nuclear Nonproliferation. Grant applications submitted by small businesses must respond to a specific topic and subtopic during an open solicitation.

SBIR and STTR have three distinct phases. Phase I explores the feasibility of innovative concepts with typical awards up to $225,000 for 9 months. Only Phase I award winners may compete for Phase II, the principal R&D effort, with awards up to $1,500,000 over a two-year period. There is also a Phase III, in which non-Federal capital is used by the small business to pursue commercial applications of the R&D. Also under Phase III, Federal agencies may award non-SBIR/STTR-funded, follow-on grants or contracts for products or processes that meet the mission needs of those agencies, or for further R&D.

Results

Phase I Topics for 2016

Below is the text for the Electric Drive Technology topic from the 2016 SBIR Phase I Release 2 topics. The full topic release can be found at:
https://science.energy.gov/~/media/sbir/pdf/TechnicalTopics/FY2016_Phase_1_Release_2_Topics_Combined.pdf

Power electronic inverters are essential for electric drive vehicle operation, and the Vehicle Technologies Office (VTO) has established cost and performance targets that need to be met so that these vehicles can decouple personal mobility from oil, cut pollution and help build a 21st Century American automotive industry that will lead the world. Specifically, inverter R&D targets and research pathways have been outlined by DOE in both the U.S. DRIVE partnership Electrical and Electronics Technical Team Roadmap [1] and EV Everywhere Blueprint [2]. Both of these technical documents specifically address the performance benefits of WBG semiconductors, but their current high cost is a barrier to high volume automotive adoption.

With large area (> 150 mm, or 6") Silion Carbide (SiC) epitaxial wafer availability from a large number of qualified suppliers, the SiC device industry is approaching the state of the cost-competitive silicon (Si) power device industry, where the cost of fabrication is the primary driver for device cost, and their high device yield allows for a low overall cost of devices.

Devices crucial for vehicle inverters which can take advantage of these SiC epitaxial wafers, SiC switches with either built-in free-wheeling Schottky diodes (lower cost) or in conjunction with Schottky diodes, offer significantly smaller on-state resistance as compared to current Si switches and enable very high power density, modular inverters for use in electric drive vehicles. The extremely high speed of SiC switches also allows for increased efficiencies and reduced passive device requirements for power inverter applications. While lower current (<50A) SiC switches offered by few SiC device suppliers have already penetrated solar and computer power supply manufacturers, the capability to handle currents > 100 A remains a key threshold for automotive applications.

This topic seeks to address this barrier through demonstrating the successful production of > 100A, > 600V rated switches with either built-in Schottky diodes (lower cost) or used with external Schottky diodes suitable for use in electric drive vehicle traction motor inverters. Specifically, devices produced should show automotive application readiness through passing qualification specifications or standards and high yields. Where possible, applicants should show a relationship to, and demonstrate an understanding of, automotive application requirements and environments. Examples include surface and/or substrate treatments and processing, and compatibility with existing power module packaging and processing. Proposals should also describe the cost of manufacturing SiC switches compared to competing Si switches, including details such as costs and availability of commercial SiC substrates, epi-layers, and additional equipment needed. These costs should be linked to a commercially viable business model for large scale manufacturing and should approach cost parity with Si switches on a cost per amp basis.

Phase I Awards Made in 2016

Integrated Silicon Carbide Power Electronic Block
Dr. Rahul Radhakrishnan
Global Power Technologies Group, Inc.

Advances in silicon carbide (SiC) MOSFETs promise to revolutionize power electronics, including for transportation. Adoption of SiC power devices in electric vehicle drives is hindered by high cost and unproven reliability in vehicle applications.

Fabrication of low on-resistance, high performance SiC DMOSFETs and monolithically integrated DMOSFET-JBS diodes on 150 mm wafers using an area-efficient integrated design will reduce device cost to parity with incumbent silicon power devices and speed adoption of this exciting new technology.

Silicon carbide semiconductor devices are predicted to become a $1B industry by 2023. Adoption of a new technology requires technical capability, competitive price and confidence in reliability. Extensive reliability testing will improve confidence in silicon carbide technology and accelerate adoption of SiC devices.

Silicon Carbide MOSFETs for Electric Vehicle Drive Applications
Dr. Kevin Matocha
Monolith Semiconductor Inc.

Silicon Carbide based power electronics have the opportunity to increase the power density and efficiency of on-board electric power conversion electronics for electric vehicles boost converters and electric traction drives. Utilizing these advanced SiC-based power electronics devices is expected to expand range and eventually reduce electric vehicle system costs. However, the current high cost for SiC power MOSFETs and diodes prevents widespread adoption in automotive applications. In this Phase I SBIR program, Monolith Semiconductor will advance the performance and cost of high-current SiC power MOSFETs to meet the demanding needs of automotive inverter drive applications. In addition to these performance advances, Monolith Semi will demonstrate SiC MOSFET technology that is suitable for high-volume manufacturing.

High Current SiC Cascodes for Electric Drive Vehicle Power Electronics
Dr. John L. Hostetler
United Silicon Carbide, Inc.

In 2014, approximately ~120,000 plug-in electric vehicles (PEV's) were sold in the US alone, representing a 23% increase from 2013 and a 128% increase from 2012 and nearly 1/3 of the PEV's sold worldwide, making the US the largest market for PEV and HEV adoption. It is expected that by 2023, there will be ~3.2 million PEV's on the road in the U.S. alone

Increasing the electric drive system efficiency has a significant impact as it extends battery life, vehicle range and allows for a reduction of heavy cooling components through the reduction of heat generating losses. Therefore much attention is placed on increasing the efficiency of the traction power inverter that drives the electric motor. It is well documented that inverter efficiency and power density can be increased while simultaneously reducing weight through the use of Silicon Carbide (SiC) wide bandgap semiconductors. For example, demonstrations of inverters utilizing SiC-JFETs and SiC-MOSFETs are emerging, where the efficiencies are reaching >99% with 10X increased power densities.

However, today's electric vehicle motor drive applications require high current (200-400A) power modules. SiC devices have been limited to lower current (<50A) due to the material defects, lower yields and higher costs associated with large area devices. For the electric vehicle traction inverters, it is of great interest to push up the SiC device current to 100-200A per device to make full use of the SiC system. Material defect densities have dropped dramatically in recent years as the commercial acceptance of the SiC Schottky diode have driven higher volume and more state-of-the-art semiconductor fabrication.

USCi proposes in Phase I to fabricate 100A 650V SiC Cascode Switches on 6" diameter wafers. The large area high current cascodes will be packaged in a stack format resulting in a very high power density potential. In Phase II, the cascodes will be packaged to assess performance with advanced high density modules. When integrated, the SiC cascodes will increase the efficiency of electric motor power conversion from the battery to

the drive train. In Phase II, the goal will be to qualify the high current cascodes on the system level for automotive applications.

Phase II Awards Made in 2016

Under the SBIR/STTR process, companies with Phase I awards from FY 2014 are eligible to apply for a Phase II award in FY 2015. Two Phase II awards were made in FY 2016 that resulted in the following projects:

900 V / 200 A SiC Schottky Diode fabrication on 150 mm substrates
Dr. Siddarth Sundaresan
GeneSiC Semiconductor

Reducing the size, weight, and increasing the efficiency of automotive traction power inverters requires the development of novel high-voltage, high current silicon carbide high-speed rectifiers, since the existing silicon technology is severely limited in terms of operating temperature, frequency and energy efficiency. However, the non-optimized device and manufacturing technology currently used for silicon carbide power diode fabrication results in higher energy losses and a non-competitive price point with respect to silicon.

Novel device and process technology in combination with the use of a high-volume manufacturing strategy on large diameter silicon carbide wafers is proposed in this proposed program for achieving near-theoretical device performance on high-current power Schottky rectifiers. The proposed device and manufacturing strategies will drastically reduce the manufacturing costs for silicon carbide Schottky diodes, making them cost-competitive with the existing silicon technology.

Phase I was focused on developing and optimizing the device and layout designs necessary to scale up the rated current of the silicon carbide Schottky rectifiers to 100 Amperes. A major task involved transferring the process technology to a large-scale, high-volume foundry identified in the proposal. A pilot wafer lot was implemented at the large-volume foundry and the device performance was benchmarked against the current state-of-the-art. Phase II will be focused on increasing the current rating of the diodes to 200 Amperes, while focusing on the 900 Volt market segment as required for automotive applications. Detailed reliability investigations pursuant to the industry standards is planned for Phase II. A detailed commercialization strategy will also be implemented during Phase II.

Electric vehicle power electronics manufacturers such as General Motors, Delphi Automotive and Cummins Power Systems are expected to be direct customers of the proposed silicon carbide devices to be developed in this program. Reducing the weight of the power module, which represents 23% of the total Inverter weight will extend its electric range and/or reduce the size and cost of the battery. Significantly reduced silicon carbide chip-sizes for the same current rating along with low-cost, high-volume manufacturing strategies proposed in this program will help meet the aggressive power electronics targets set for the electric vehicle industry by the DOE for the year 2022. This in turn will enhance the country's energy security by reducing dependence on foreign oil, save money by cutting fuel costs for American families and businesses, and result in a cleaner environment by reducing harmful CO2 emissions from gas-powered vehicles.

High Current SiC Schottky Diodes for Electric Drive Vehicle Power Electronics
Dr. John Hostetler
United Silicon Carbide, Inc.

The U.S. represents the world's leading market for electric vehicles and is producing some of the most advanced plug-in electric vehicles (PEV's) available today. PEV's are gaining widespread adoption every year, where 58% of all PEV sales occurred in 2013 and it is expected that by 2023, there will be ~3.2 million PEV's on the road in the U.S. alone.

Increasing the electric drive system efficiency has a significant impact as it extends battery life, vehicle range and allows for a reduction of heavy cooling components through the reduction of heat generating losses. Therefore much attention is placed on increasing the efficiency of the traction power inverter that drives the electric motor. It is well documented that inverter efficiency and power density can be increased while simultaneously reducing weight through the use of Silicon Carbide (SiC) wide bandgap semiconductors. For example, demonstrations of inverters utilizing SiC-JFETs and SiC-MOSFETs are emerging, where the efficiencies are reaching >99% with 10X increased power densities.

However, today's electric vehicle motor drive applications require high current (200-400A) power modules. SiC devices have been limited to lower current (<50A) due to the material defects, lower yields and higher costs associated with large area devices. For the electric vehicle traction inverters, it is of great interest to push up the SiC device current to 100-200A per device to make full use of the SiC system. Material defect densities have dropped dramatically in recent years as the commercial acceptance of the SiC Schottky diode have driven higher volume and more state-of-the-art semiconductor fabrication.

USCi proposes in Phase II to fabricate 200A 650V and 1200V 100A SiC Schottky Diodes on 6" diameter wafers. The high current diodes will complete reliability automotive qualifications in Phase II. The diodes will be co-packaged with Si switches to form hybrid modules and benefits estimated. When integrated, the SiC diodes will increase the efficiency of electric motor power conversion from the battery to the drive train.

Conclusions and Future Directions

The Electric Drive Technologies (EDT) subprogram hopes to continue with new Phase I and Phase II SBIR projects in FY2017.

RESEARCH AREAS

2 Electric Motor Research and Development

2.1 Advanced Electric Motor Research

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Contract No.: DE-AC05-00OR22725

Abstract/Executive Summary

Almost all hybrid electric vehicle (HEV) and electric vehicle (EV) motors (machines) use permanent magnets (PMs) with rare earth (RE) materials such as neodymium and dysprosium because they facilitate the achievement of high power densities, specific powers, and efficiencies. However, there has been significant market volatility associated with RE materials in recent years, including a price increase in dysprosium by a factor of 40 within 1 year. Therefore, alternatives to RE PM motors are of very high interest to original equipment manufacturers and suppliers and will continue to be, particularly as vehicles become more electrified and uses for RE materials in other applications expand in the future. Achieving competitive performance and efficiency with alternative motor technologies having comparable mass, volume, voltage, and other key metrics requires a highly advanced multidiscipline research approach including high accuracy modeling; the research, use, and development of soft and hard magnetic materials; and comprehensive nonlinear computational optimization of geometric features and winding parameters.

Accomplishments

- Machine design and development
  - Fully optimized several non-RE motor designs including the use of ferrite magnets. Simulations indicate that DOE 2020 targets for efficiency, power density, specific power, and cost are achievable with several ORNL motor designs
- Soft magnetic materials research and development (R&D)
  - Continued research on electrical sheet steel with high silicon (Si) content (>6%)
  - Confirmed capability for ingot-based processing vs. expensive chemical vapor deposition
  - Developed and confirmed a novel processing technique to reduce brittleness; otherwise, the workability of high-Si steel is not suitable for mass production of motor laminations
  - Performed extensive warm-rolling experimental trials and obtained extensive information indicating some approaches may only hold a very narrow processing window that is not robust enough for industrial exploitation

- Advanced modeling
  - Incorporated findings from research on soft magnetic materials properties using the newly developed characterization system into electromagnetics modeling
  - Developed detailed micromagnetics code and a corresponding simulation environment to study the fundamental behavior and impact of various conditions upon the magnetization and loss characteristics of electrical steel
  - Developed a new scaling approach and implemented on the ORNL Titan supercomputer.
    - Using the scaling approach, demonstrated the transition from a monodomain to a multidomain structure as the length scale of the system is increased
- Prototype fabrication and testing
  - Fabricated and tested a prototype ferrite PM motor
    - Confirmed it meets DOE 2022 targets. Targets for power density, specific power, and cost were met with a peak power of 103 kW
  - Identified key issues with magnet properties. Future studies need to be carried out to determine the availability and quality control for mass scale production

Introduction

As the electric motor is one of the main components of HEV and EV drivetrains, improving efficiency, performance, and cost-effectiveness is crucial to the hybridization and electrification of vehicles. PM motors are not easily surpassed in terms of efficiency, power density, and specific power, and therefore almost all HEVs and EVs use them. However, the cost of RE PM material accounts for at least 40% of the entire motor cost, and the high and unstable costs of RE materials have caused automotive manufacturers and suppliers around the world to seek alternative non-RE motor technologies that facilitate cost-effectiveness as HEV and EV markets continue to expand. Therefore, the development of alternative non-RE motor technologies plays an important role in future economic stability and achieving clean energy goals and energy independence.

Approach

The primary objective of this project is to develop low-cost non–RE motor solutions with high power density, specific power, and efficiency. Figure 2-1 illustrates the overall structure of the efforts in the project. Key efforts of the project include conventional motor design techniques, advanced motor modeling, motor materials research, and empirical verification.

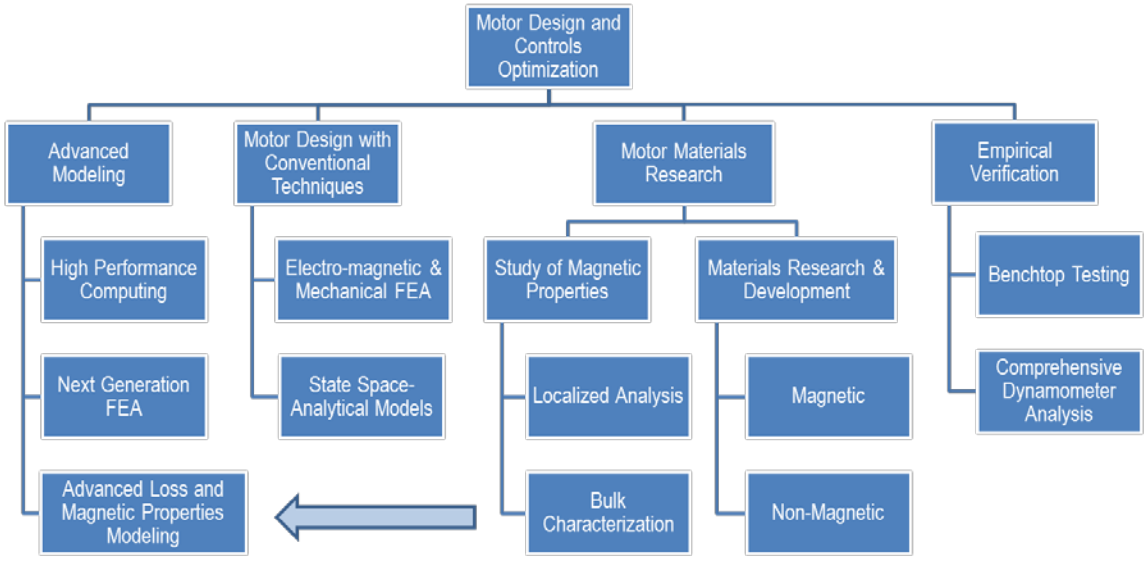

Figure 2-1: Motor research thrust areas and project structure.

In the initial stages of this project, many types of novel electric motor designs were developed and considered in coarse simulations to identify the most feasible designs with high potential for commercialization. The wide

range of motor types studied includes field excitation, synchronous reluctance, non-RE PM motors, and combinations of these machine types. Proof-of-principle components were built and tested to serve as a feedback mechanism for novel motor development and fundamental soft magnetic materials research. Novel motor designs were developed and optimized using high performance computing techniques, beginning with implementation and modeling on parallelized workstations, and preparations are under way for the use of computational clusters and ultimately the supercomputer at the computational facility at ORNL. Findings from fundamental magnetic materials research are being incorporated into new modeling tools to improve accuracy, and this has been greatly facilitated with parallelized computing.

In addition to novel motor and controls development, the development and use of new materials and materials processing techniques was carried out to improve magnetization and/or efficiency characteristics of soft magnetic materials (e.g., electrical steel). This effort is being conducted in coordination with the propulsion materials program. Additionally, new materials or manufacturing techniques were studied and used to obtain improvements in manufacturability (cost reduction), cooling (collaborating with the National Renewable Energy Laboratory), and improved mechanical integrity.

To improve motor modeling accuracy and complement new materials and processing developments, fundamental research was conducted to study the phenomena behind magnetization and loss characteristics of soft magnetic materials in electric motors, details that are still not fully quantified or understood in the scientific community. For example, residual stresses or induced stresses incurred during manufacturing or motor operation have a considerable impact upon losses and permeability. Additionally, temperature, pulse width modulation excitation, and other factors impact the magnetic properties in a way that is not considered or modeled with conventional finite element analysis (FEA) tools. These studies supported the development of high fidelity models and modeling tools, which are particularly important as high performance computing is used in the optimization of detailed geometric features to achieve high power density, specific power, efficiency, and cost-effectiveness. After comprehensive optimization, a ferrite PM motor was fabricated and analyzed in an ORNL dynamometer test cell.

Results and Discussion

Motor design optimization in FY 2016 was conducted with commercial FEA packages, in-house custom design tools, and other software packages for parametric optimization algorithms and state space simulations. Progress and results in the area of motor design are discussed in the following sections, including parallel efforts in materials R&D. These parallel efforts ultimately support improving motor designs through developing or facilitating the use of more efficient materials and conducting fundamental research to improve modeling accuracy.

Modeling of Magnetic Domains

In soft magnetic materials, such as iron (Fe) and Fe-Si alloys (electrical steels) used in motor laminations, the magnetic behavior during operation is linked to the evolution of the magnetic domain structure during external magnetization and demagnetization cycles. The effect of elastic strains and pinning due to nonmagnetic defects in the steel microstructure significantly influence the temporal evolution of the domain structure and hence the magnetic response. A simulation effort at the mesoscale was undertaken to quantify the magnetic behavior under such conditions and to provide realistic magnetic constitutive behavior to continuum level simulations of motor performance. Current approaches to simulate domain structure evolution involve solution to the micro-magnetics equations proposed by Landau, Lifshitz, and Gilbert (LLG). The LLG approach is based on treating magnetism as a continuous vector field and solving the temporal evolution of the effective magnetic field to minimize total magnetic energy. Typically, solution techniques involve the use of a phase field approach with a diffuse interface between two magnetic domains where the magnetization changes continuously. However, phase field approaches require many parameters that are based on averaging atomic level quantities. In many cases such parameters are not readily available. On the other hand, simulations of nanoscale magnetic behavior have used discrete magnetic moments at the atomistic scale to predict collective evolution of magnetic domains using atomistic techniques. Such an approach has been used, for example, in simulating magnetic domain formation in nanoscale thin films and magnetic switching in nanoscale devices.

In either of the two approaches, the length scale over which the simulations can be carried out is severely limited by the ability to calculate the magnetic dipole-dipole interaction energy that involves long-range

interaction terms for every volume element in the simulation domain. The general strategy has been to use simplifications based on the use of fast Fourier transforms (FFTs) that necessitate the use of periodic boundary conditions that may not be realistic in many cases. An alternative technique based on the fast multipole method has been widely used in similar problems but has not been readily adopted in micro-magnetics simulations. It is necessary to perform the simulations at length scales of several micrometers because the magnetic domains that form as a result of a competition between magnetic exchange energy and the dipole-dipole interaction energy exist only at such length scales. One approach to overcome this problem and observe domains at smaller length scales has been to scale down the exchange energy and establish a relationship between the reduced length scale and the equivalent realistic length scale. However, a universal relationship between the two has not been established.

In pursuit of the goals and objectives of this project, a new scaling approach has been successfully developed and has been shown to demonstrate the transition from a monodomain to a multidomain structure as the length scale of the system is increased. Such an approach has been made possible by the use of high performance computing in the calculation of the dipole-dipole interaction energy and exchange energy in a series of domain sizes. The scaling of the exchange energy and the dipole energy as a function of the system size is shown in Figure 2-2. The application of the scaling laws shows the transition from a monodomain structure at small simulation volumes, shown in Figure 2-3 (a), to the formation of vortex type structures in larger volumes, shown in Figure 2-3 (b). The simulations are also able to capture the experimentally measured domain wall thicknesses in Fe-3%Si steel. The simulations are being extended to polycrystalline grain structures to capture magnetization and demagnetization curves as a function of grain orientations.

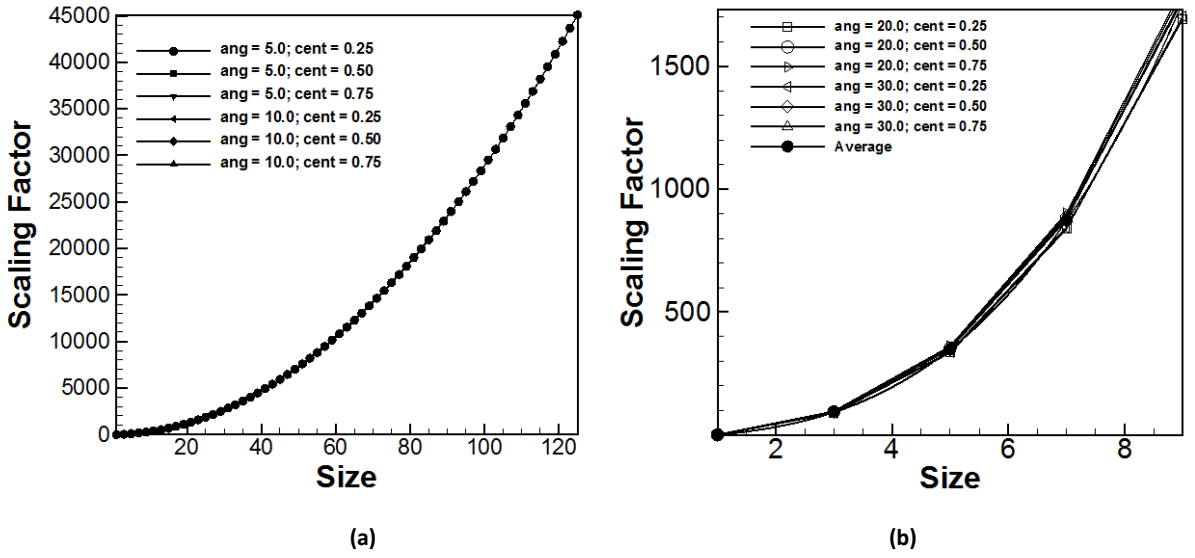

Figure 2-2: Scaling of the exchange energy (a) and dipole-dipole interaction energy (b) as a function of the system size for body-centered cubic iron.

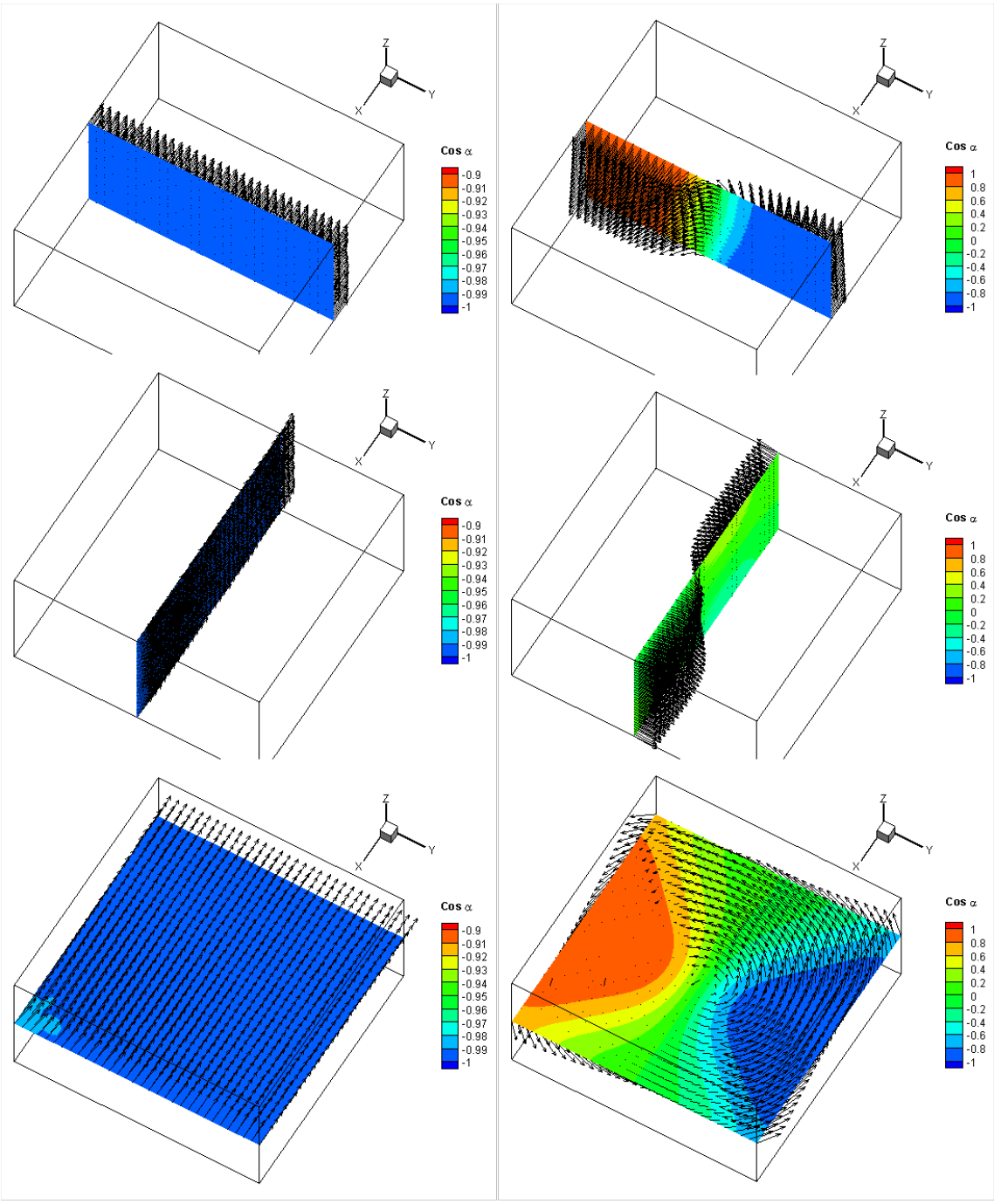

Figure 2-3: Evolution of the magnetic moment distribution as a function of system size showing the transition from monodomain (a) to vortex structure (b). [Note: Size in (a) = 1 (9.152 × 9.152 × 4.576 nm3) and in (b) = 51 (467 × 467 × 236.5 nm^3).]

High Efficiency Steel Research: Thermomechanical Processing of Fe–6% Si alloys

Increasing the Si content in soft magnetic steel (e.g., Fe-Si) to 6% can increase resistivity and reduce losses by about 35%. However, with high Si content, conventional stamping of laminations is no longer possible because the material becomes too brittle. Efforts were made on this project to develop a deeper understanding of the driving mechanisms, explore additives to improve ductility from ingot form, and develop modifications to conventional thermomechanical processes. Iron-silicon alloys containing greater than 3 wt % Si undergo congruent ordering on cooling from the processing temperature. This is a second order transformation that involves local hopping of the Si atoms to the body center of the body-centered cubic (BCC) unit cells of iron

and, therefore, a statistically higher occupancy of the body center compared to the corners of the BCC unit cell. However, molecular dynamics (MD) simulations using a recently formulated modified embedded atom potential for the Fe-Si system have shown the significantly higher yield strength of Fe-Si alloys in the congruently ordered condition compared to a disordered state. The summary of MD simulations is shown in Figure 2-4.

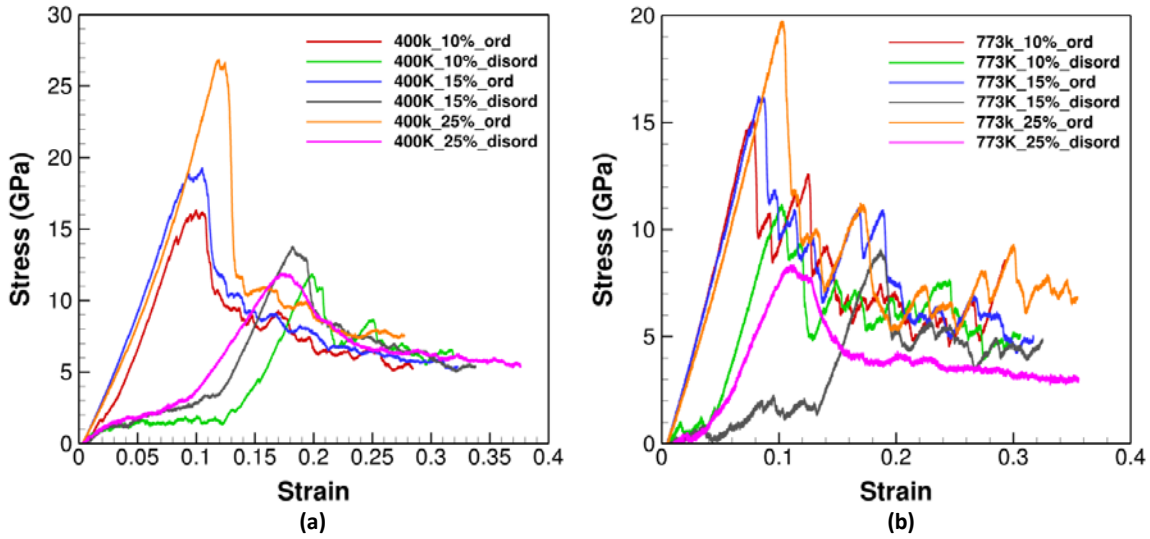

Figure 2-4: MD simulations of the deformation of Fe-Si single crystals containing 10 to 25 at. % (5 to 12 wt %) Si at (a) 400 K and (b) 773 K.

The ordering of Si atoms cannot be suppressed at the cooling rates encountered in conventional thermomechanical processing. However, it has been well documented in the literature that warm working the alloy in the temperature range from 400°C to 550°C followed by normal process cooling can recover the ductility of the alloy at room temperature and promote subsequent cold rolling. There is also sufficient evidence in the literature that large deformation around 900°C, which is higher than the ordering temperature of the alloy, followed by forced cooling allows cold rolling if it is performed without long holding periods at room temperature (less than 4 h). In FY 2016, a number of laboratory trials and rolling experiments were performed using Fe-6Si and Fe-6.5S alloys, with or without parts-per-million levels of boron, to test the above, suggested routes. The hot-working temperature, the extent of deformation, and the hold time and temperature were systematically varied. So far these efforts have had limited success whereas warm rolling at 300°C–350°C followed by cold rolling resulted in 0.8 mm thick sheet with significant extent of edge cracking. All of the other parametric studies failed, with the material exhibiting significant cracking during cold rolling. Therefore, it has been concluded that the above approaches may only hold a very narrow processing window that is not robust enough for industrial exploitation. Alloying strategies are being considered to either suppress the kinetics of ordering or completely eliminate ordering in Fe-Si-X alloys while simultaneously maintaining the magnetic properties and the required resistivity levels for high-frequency motor applications.

Motor Design and Power Density Optimization of a Ferrite Interior Permanent Magnet

The development of unconventional motor technologies was accomplished by improvising upon promising technologies from previous work and initiating work on novel motor concepts. Previous research includes the design of various motor types, including induction motors, switched reluctance motors, hybrid excitation motors, and flux coupling/field coil machines. Novel motor designs were generated and simulated, with consideration of various machine types such as switched reluctance, hybrid PM excitation, synchronous reluctance, and field coil excitation. Recent designs include the use of ferrite magnets for improved power density. ORNL used advanced optimization algorithms to optimize motor design and controls. Electromagnetic FEA tools were used to implement basic models to determine performance and operational characteristics of new motor designs. Analytical models were used to determine additional performance metrics and associated control methods.

Spoke-type ferrite interior permanent magnets (IPMs) have received attention in recent years due to the push for reduced RE content in PMs. The spoke topology refers to a method of arranging the magnets on the rotor

so the flux is produced and concentrated in the tangential direction before crossing the air gap to the stator. This topology allows a great increase in the magnet mass on the rotor and, because of this, is promising for ferrite-based machines intended to replace those using NdFeB magnets. However, most ferrite-based spoke IPMs explored in the literature use expensive techniques to reduce leakage flux (e.g., keyed beryllium hubs), result in limited speed ratings (less than 8,000 rpm, free rotor pole pieces with axial support posts), use more expensive high strength steel, or have not been optimized over a wide variety of parameters. This project has focused on optimizing a spoke-type machine to achieve an understanding of the achievable power density of ferrite-based IPMs. We consider a model with 13 parameters, 7 of which are free, 4 of which are fixed, and 2 of which are implicitly constrained. The main materials selected, namely the PMs and steel material, are also fixed in advance.

Free Parameters

The seven free dimensional parameters allowed to vary in the optimization routine are shown in Figure 2-5(a) and the overall base motor design is shown in Figure 2-5(b). Six of the seven parameters in the models are dimensionless, allowed to vary from 0 to 1, and normalized to the rotor outer diameter. The scale-dependent parameters are the stator back iron thickness, stator tooth length, stator tooth width, magnet thickness, rotor q-axis tooth width, and rotor d-axis depth. This is done so that models with the same unitless parameters are roughly comparable on a per-unit basis (with the unit being the rotor outer diameter).

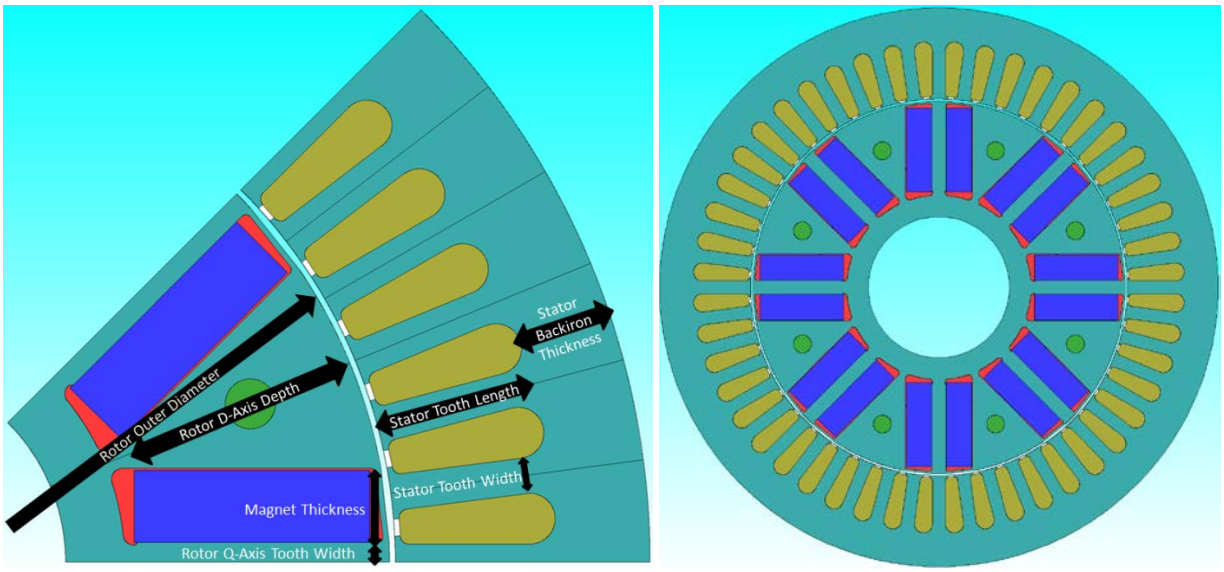

Figure 2-5: Free optimization parameters of a ferrite IPM (a) and full basic design (b).

Fixed Parameters

In addition to the free parameters, two parameters are fixed. First, the maximum speed of the machine is fixed at 14,000 rpm, but as part of our initial investigations, the maximum speed was allowed to vary from 7,000 rpm to 14,000 rpm. However, it was quickly apparent that the maximum power density designs converged on high speed operation, even when mechanical constraints were considered. Second, the maximum current density was limited to 13 Arms/mm^2 averaged over the slot area, or about 29 Arms/mm^2 in the conductors themselves. This is about the same as the 2010 Prius motor, and a relatively large value that has been observed to limit the peak torque of the delivery time in practice. Nevertheless, this is necessary for achieving high power densities in RE-free machines. Because of this, cooling must be designed carefully in production vehicles. The final two fixed parameters are the inverter voltage and current rating. These were set at 650 Vdc and 200 Arms, respectively. The models are evaluated by applying a fixed current density to the slot. A posteriori determination of the number of turns is made using the slot geometry, maximum current density, and an assumed slot fill factor of 45% (similar to the 2010 Toyota Prius).

Implicitly Constrained Parameters

Torque-Constrained Stack Length

The optimization procedure used two-dimensional FEA to determine design performance. Ignoring end effects, this gives an effective torque per unit length for a given design. This allows for all candidate designs to be sized to address the low speed torque requirements. In the initial design, a power level of 60 kW from 2,800 rpm to 14,000 rpm was targeted. A low speed torque of 225 Nm was chosen to give a 10% margin of error. Later, magnet material selection was changed (discussed later) and 55 kW/206 Nm was targeted.

Mechanically Constrained D-Axis Bridge Width

The thickness of the bridge on the d-axis of the rotor connecting the d-axis pole piece to the rotor hub and supporting the magnets is constrained by the yield strength of the lamination material. In particular, the bridge thickness was constrained to keep the Von Mises stress at 14,000 rpm to below half of the material yield stress. A thinner bridge reduces the leakage flux, so it is more advantageous magnetically. On the other hand, repeatedly cycling loads between low and high stress levels can induce fatigue-related failures, so it is desirable to keep the stress levels as low as possible. A rough rule of thumb is to keep the peak stress below half of the yield strength of the material. This is equivalent to having a safety margin of 2. A novel method for sizing the bridge was developed to avoid performing mechanical finite element simulations for every design.

Material Selection

The two main materials that must be selected for this design are the steel laminations and ferrite PM material. For the laminations, JFE Steel grade 35JN210 was selected. This is the lowest loss variety lamination of JFE's standard grade nonoriented steel. Most importantly, however, it has the highest rated yield strength out of all the grades at 450 MPa. This allows for the minimization of the rotor d-axis support bridge width, thus minimizing the main leakage flux path.

During initial optimization runs, Hitachi NMF-12J ferrites were used as the PM material. These magnets substitute lanthanum and cobalt for strontium/barium to improve the temperature stability of the demagnetization characteristics. This has the additional effect of greatly improving the magnet coercivity. The drawback is the relatively high cost of lanthanum and cobalt compared to strontium and barium. Unfortunately, after contacting suppliers for several months, we were unable to find a source for prototype magnet material. After additional investigations, a substitute material from two separate suppliers was found. The ferrite grade is called Y40 and is part of a standard that is emerging in popularity in Europe and China, and to a lesser extent the United States. The so-called Y-standard specifies magnets of much higher energy product than can be found using the C-standard typically used in the United States. Typical properties of both magnet types are given in Table 2-1. At 20°C, the properties are quite similar.

Table 2-1: Typical ferrite magnet properties at 20°C

Material	Br (T)	Hci (kA/m)	Hcj (kA/m)	BHmax (kJ/m3)
NMF-12J	0.44	430	340	37.4
Y40	0.44	340	330	37.5

Design for Manufacturability

The magnets are designed to slip into their rotor slots with a small clearance and are potted in place with a strong epoxy. In the prototype rotor, the magnets slipped in and out of the slot relatively easily while magnetized. In the final assembly step, the bottom of the rotor was taped and sealed. A small amount of epoxy-based material was placed in the bottom of the slot and the magnet was pressed into place. The excess material was cleaned off the surface before curing. Careful metering of the amount of epoxy would allow either manual or automated rotor assembly with ease. It should be noted that, although the epoxy is expected to improve the mechanical strength of the rotor, it has not been relied upon when calculating the mechanical safety margin of the rotor. That is to say, the epoxy may de-bond from the laminations or magnets without causing the rotor to fail. The rotor q-axis bridge is designed to support the full load of the rotor pole face and magnets with an adequate safety margin.

Optimization

Model Evaluation

Two key performance criteria must be evaluated for each model: maximum torque and peak power at maximum speed. Theoretically, the maximum torque capability at 2,800 rpm must be evaluated. In practice, however, designs around the optimum were able to deliver peak torque well above this speed. A truly accurate evaluation of the peak torque would also require determination of the current angle that produces this value. It can be shown using simply D-Q torque models, however, that for machines with significant reluctance torque, the maximum current angle does not deviate far from 45 (or 135) degrees. The error is insignificant when it comes to differentiating between designs and is easily accounted for by small increases in the stack length. Similarly, the maximum power at peak speed would require determination of the current vector, both magnitude and direction, that produces this value. Instead of performing this expensive operation for each design, a simpler approach was implemented that gives a lower bound on the maximum power. This is done through a determination of the characteristic current by simulating a few (usually two) different current vector magnitudes aligned with the negative d-axis. Along with the inverter voltage rating, the machine characteristic current gives the asymptotic peak power of the machine as the speed becomes large. When searching for a machine with an asymptotic power of 55 kW or 60 kW, it is guaranteed that the peak power at 14,000 rpm will be larger than this value. A tighter value can be obtained by iteratively reducing the required asymptotic value until the power at maximum speed is equal to the targeted value.

Optimization Algorithm

A novel guided random search method was implemented to optimize the design. To start, population of candidate designs is drawn randomly from a joint Gaussian distribution with a given mean and standard deviation. The mean of the distribution is moved from the value to the design on the Pareto front closest to the target values. A sigmoid function is used to update the standard deviations of the individual parameters based on the distance between the previous mean and the updated mean. The sigmoid function is calibrated so that the "Gaussian search spheroid" expands when searching far away from the optimum, contracts when searching close to the optimum, and changes shape when certain parameters are more influential on the optimal design than others. The adaptability of both scale and directionality results in a quickly converging algorithm.

Results and Trends

Initial optimization runs involved the use of Hitachi NMF-12J ferrite magnets. The population size of the algorithm was set to 72. Fourteen iterations were performed for a total of 1008 model evaluations. All optimization runs were performed assuming a temperature of 100°C. A scatter plot of the active volume versus the asymptotic power for the candidate designs is shown in Figure 2-6. The minimum volume design meeting the 60 kW target is marked with a black "X." Interesting trends are observed in the optimization results. In Figure 2-7 a scatter plot of the power density versus volume is shown for a subset of the candidate designs. Around the optimal design, where the Pareto front is well resolved, a trend of increasing power density with increasing volume can be observed. This implies that a higher power density can generally be achieved as the targeted power rating increases.

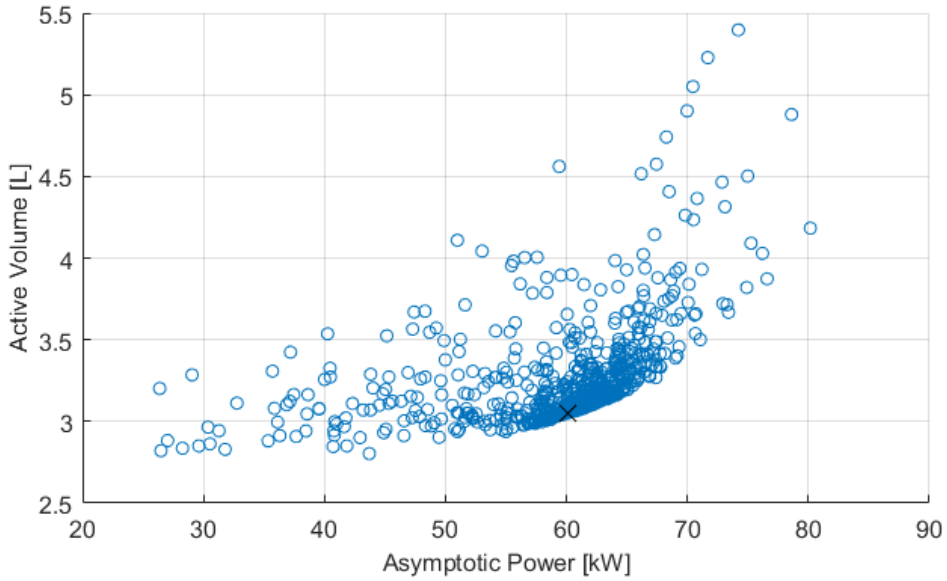

Figure 2-6: Optimization trend: Volume versus asymptotic power for 1008 candidate designs.

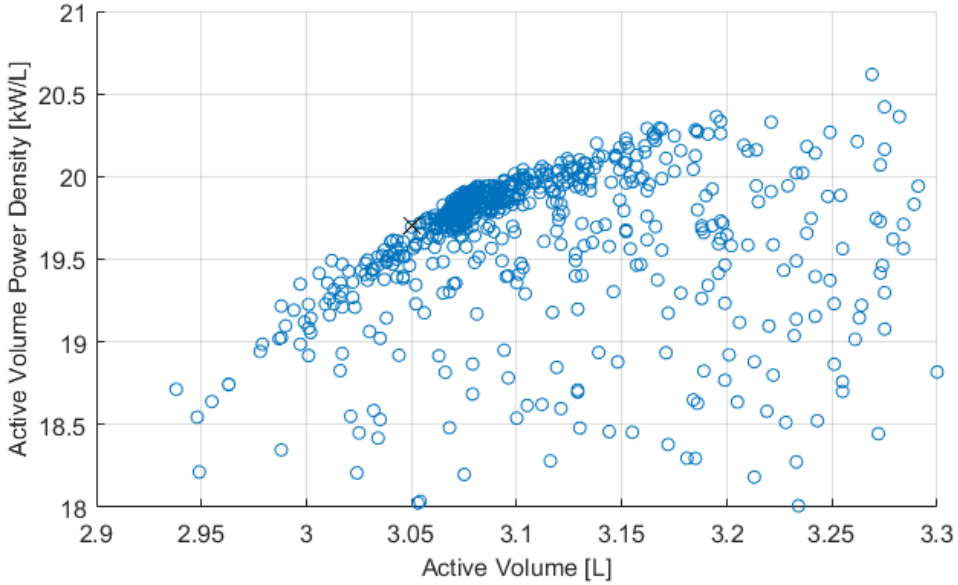

Figure 2-7: Optimization trend: Active volume power density versus active volume.

A scatter plot of the power density versus length to stator outer diameter (L/D) ratio of a subset of the candidate designs is shown in Figure 2-8. The observed trend here is increasing power density with increasing L/D ratio. This implies that, for electric machines with weaker magnets, it is much easier to achieve higher power densities in more elongated designs. For example, the 2010 Toyota Prius has an L/D ratio of about 0.19, whereas this optimal design has a ratio of nearly 0.49.

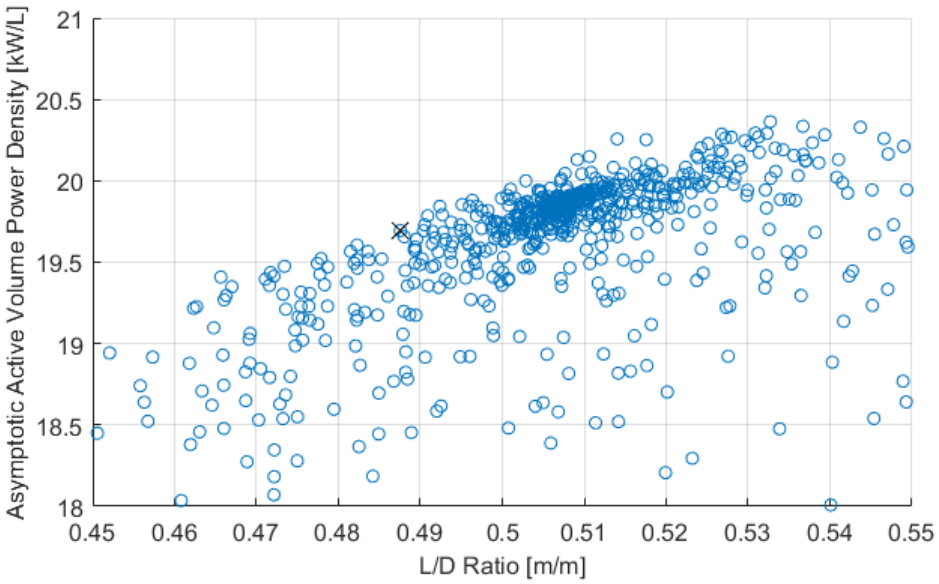

Figure 2-8: Optimization trend: Active volume power density versus L/D ratio.

A similar process was undertaken after the magnet material was switched from NMF-12J to Y40. The peak power/torque requirements were reduced to 55 kW/206 Nm, and the asymptotic power was modified to give a true top speed power closer to 55 kW. Even with these reductions, the machine volume ended up increasing slightly to 3.3 L (active) due to Y40's larger temperature coefficients compared to the lanthanum-cobalt-based NMF-12J. All optimizations were performed assuming a 100°C magnet temperature. A full characterization of the Y40 design was performed to verify the expected performance of the design based on the minimum number of simulations used during optimization. A motor efficiency map for an operating temperature of 100°C is provided in Figure 2-9. Notable in these plots are the broad regions of 96% efficiency, especially at high speed. This is a consequence of the relatively weak Y40 magnets (compared to NdFeB), which induce far less core losses at higher speeds.

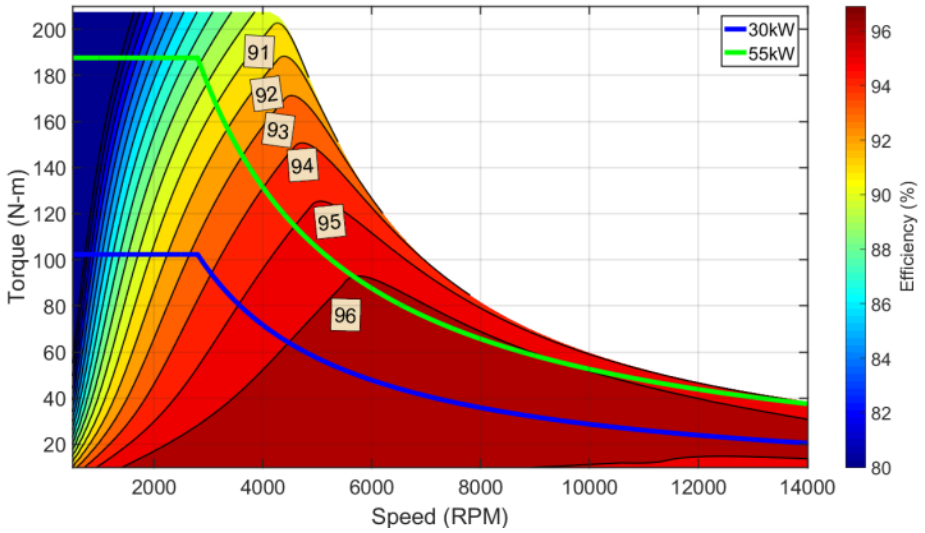

Figure 2-9: Simulated torque-speed efficiency map.

Prototype Fabrication and Dynamometer Testing

Magnets were ordered from two different suppliers. Before assembly of the rotor, the magnets were preliminarily tested using a Gauss probe and a crude push-force test. The actual magnet strength differed significantly between the different suppliers, with one providing consistently lower strength magnets than the other. Unfortunately, the higher strength magnets were still significantly weaker than the datasheet values.

Gauss probe measurements indicated that free-air measurements were about 80% of what was expected, and later, back electromotive force (back-emf) tests resulted in similar indications of inferior properties (80%).

The measured locked rotor torque versus electrical position for various currents is in Figure 2-10(a). A torque of 165 Nm was observed with a current level of 245 Adc (~173 Arms equivalent), and the motor was designed to operate at about 200 Arms. These results also indicate degradations in magnet performance, and a slight demagnetization occurred during these tests. The ratio of experimental locked rotor torque to simulated torque is shown in Figure 2-10(b). The discrepancy is about 20%. While some relative decrease in torque/current was expected with increasing current, the highest current (245 A) resulted in demagnetization. Back-emf tests following locked rotor tests indicated significant demagnetization. With the brief application of high currents, the magnets were restored to about 80% of their original strength, which resulted in all tests being completed with magnets having residual flux density at about 65% of what was anticipated. The issue with magnet quality and availability is being investigated further, as samples are being made for four-quadrant testing with a hysteresis graph.

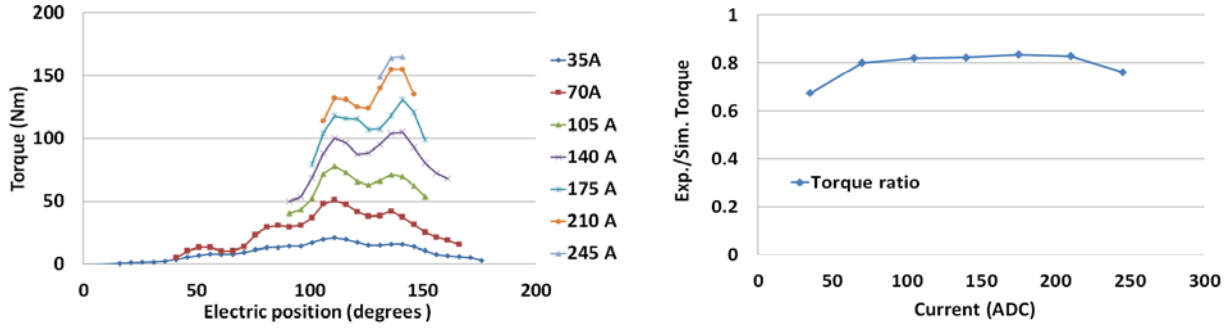

Figure 2-10: Locked rotor torque versus current test results (a) and ratio of experimental and simulated results (b).

An image of the prototype ferrite PM motor on the dynamometer is shown Figure 2-11(a). Despite significant issues with magnet performance, encouraging test results were obtained. High torque testing was avoided until high speed and high power measurements were made. Efficiency mapping for moderate torques and speeds are indicated in the graph shown in Figure 2-11(b). Other high performance measurements are also indicated with an overlay of red "x" markers, including the highest measured power of 103 kW at 9,000 rpm. The efficiency is above 90% for most operation points above 2,500 rpm, and the overall efficiency is considerably lower than expected due to the magnet flux density being ~65% of what was originally anticipated.

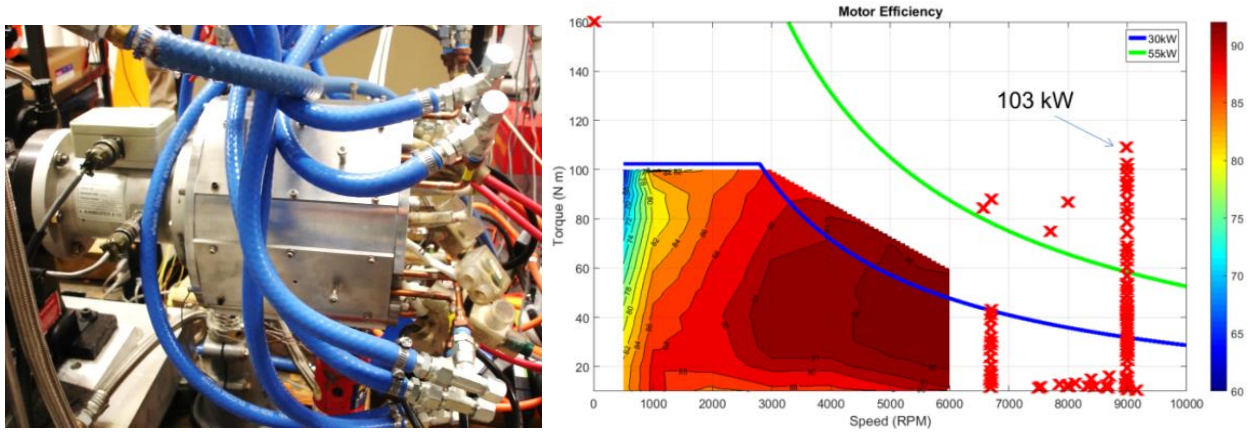

Figure 2-11: Ferrite PM prototype on dynamometer (a) and experimental test results (b).

Conclusions and Future Directions

The simulated peak power of the ferrite motor was 60 kW at 2,800 rpm, over 90 kW at about 4,500 rpm, and greater than 55 kW at 14,000 rpm. A summary of key simulated and measured performance metrics is given in Table 2-2. Detailed cost estimation efforts were conducted that include consideration of magnet grinding cost. Additionally, metrics associated with the measured power of 103 kW are also included in the table. It was estimated that the total motor material and manufacturing cost ranges from about $200 to $450. DOE 2022 targets for power density, specific power, and cost are 5.7 kW/L, 1.6 kW/kg, and $4.7/kW, respectively. It can be seen that the DOE cost and power targets are met by the ferrite motor, although the motor has limited torque production capability.

Table 2-2: Simulated and measured performance data

Speed (rpm)	Peak Power (kW)	Power Density (kW/L)	Specific Power (kW/kg)	$/kW (Low)	$/kW (High)
DOE 2022 Target	55	5.7	1.6	4.7	4.7
2,800 (simulated)	60.8	6.08	1.83	3.3	7.4
4,500 (simulated)	93.5	9.35	2.81	2.1	4.8
9,000 (measured)	103	10.3	3.10	1.9	4.4

This work has demonstrated that it is possible to design a ferrite-based IPM motor that achieves power density targets without using expensive rotor construction techniques or exotic lamination materials. The test results and magnet procurement have demonstrated that some difficulties still remain with magnet sourcing and quality. As the interest in ferrite-magnet-based motors continues to increase, the Y-series ferrites are likely to gain popularity. There is little public, independent information on these magnets and it will be useful to perform a more thorough investigation in the future.

FY 2016 Presentations/Publications/Patents

1. T. Burress, et al., “Advanced Electric Motor Development” presented at the DOE Vehicle Technologies Office 2016 Annual Merit Review, June 2016, Washington, DC.

2.2 Electric Motor Performance Improvements Techniques

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Contract No.: DE-AC05-00OR22725

Abstract/Executive Summary

This project focuses on the development of methods to reduce motor drive system size, mass, and cost while improving efficiency throughout the various speed, torque, and power operation regions of hybrid and electric vehicles. These methods are intended to be applicable to many types of motors, and are particularly useful for permanent magnet (PM) motor designs with reduced or no rare-earth material or even induction- or reluctance-based motors. While various methods were investigated, most research focused on reconfigurable (switched) winding approaches to achieve the targeted metrics. Various reconfigurable winding approaches were developed and comparisons are provided with those found in the literature. Additionally, design strategies for reducing magnet volume were developed and exemplary designs are provided.

Accomplishments

- Developed several reconfigurable winding approaches and demonstrated in simulations that due to the unique configurations, the switching components have lower cost and higher efficiency when compared with existing approaches.
- Designed, built, and performed benchtop testing with switching circuitry to confirm switching speed, efficiency, and effectiveness.
- Identified motor design strategies for reconfigurable windings.
- Designed a motor and demonstrated that considerable drive cycle efficiency and nearly double the power capability can be achieved with a reconfigurable winding approach.

Introduction

Since hybrid electric vehicles (HEVs) were introduced to the market in the late 1990s, high power electric machines for automotive applications have been heavily researched. Automotive manufacturers most commonly use interior permanent magnet synchronous motors (IPMSMs) for electric vehicles (EVs) (including HEVs, battery EVs, and range-extended EVs) because of their high efficiency and high power density despite the high costs associated with rare earth (RE) PM material. Motors with low-cost magnets or no magnets (such as synchronous reluctance or induction motors) struggle to match torque and power performance when compared to an RE PM motor of similar size and mass. The first of two main efforts on this project was the research and development of methods and switching arrangements to expand the operation range and efficiency of motors for operation throughout various drive cycles. This includes considerations of cost, complexity, and manufacturability as a part of the system optimization. The second primary effort on the

project involves the development of design strategies for reducing PM volume using reconfigurable windings. While reconfigurable winding approaches with IPMSMs were researched on this project, these approaches are applicable to almost all types of electric machines for both motoring and generating applications.

Approach

The efficiency map of an IPMSM for a commercial HEV [1] and qualitative output characteristics of an IPMSM with different winding configurations are shown in Figure 2-12. At low speeds, the motor currents can be selected according to the maximum torque per ampere rule so that the stator current in the motor is minimal, thus keeping the switching and conduction losses of the inverter and copper loss motor low. At higher speeds, flux weakening (FW) operation is implemented to weaken the permanent flux so that restraints due to higher back electromotive force (back-emf) can be mitigated. Because total current from the inverter is limited, the torque-producing current in FW mode is reduced due to increasing FW current and phase impedance, resulting in reduced torque as speed increases, as indicated in Figure 2-12. To achieve higher output power with the same motor, one possible solution is to use serial windings at low speed and then reconfigure the serial windings to parallel windings at high speed. In Figure 2-12(b), the torque and power characteristics versus speed of an IPMSM with serial (solid lines) and parallel windings (dotted lines) are depicted qualitatively. With parallel windings, the motor's back-emf is halved and the FW control is used at a higher speed, which roughly increases the constant torque range by 100% and therefore peak is also increased by about 100%. In the meantime, the peak torque with parallel windings is also roughly halved; the phase inductance of the parallel windings is one fourth of the serial winding phase inductance. When the motor is at low speeds, serial windings are selected to achieve high torque output, and parallel mode is selected to achieve higher power at high speeds. This two-speed range drive will have better torque-speed (T-ω) and power-speed (P-ω) characteristics than a one-speed range motor drive. This can be particularly useful for alternative motor technologies without RE materials, as they tend to have lower power densities than that of RE PM machines. Reconfigurable winding solutions were developed to reduce motor size for a given power rating, increase motor output power for a given size, and improve system drive cycle efficiency. Impacts on system volume/cost and advantages of changing torque-speed characteristics compared with mechanical hydraulic transmissions and their peripheral components were considered during these developments.

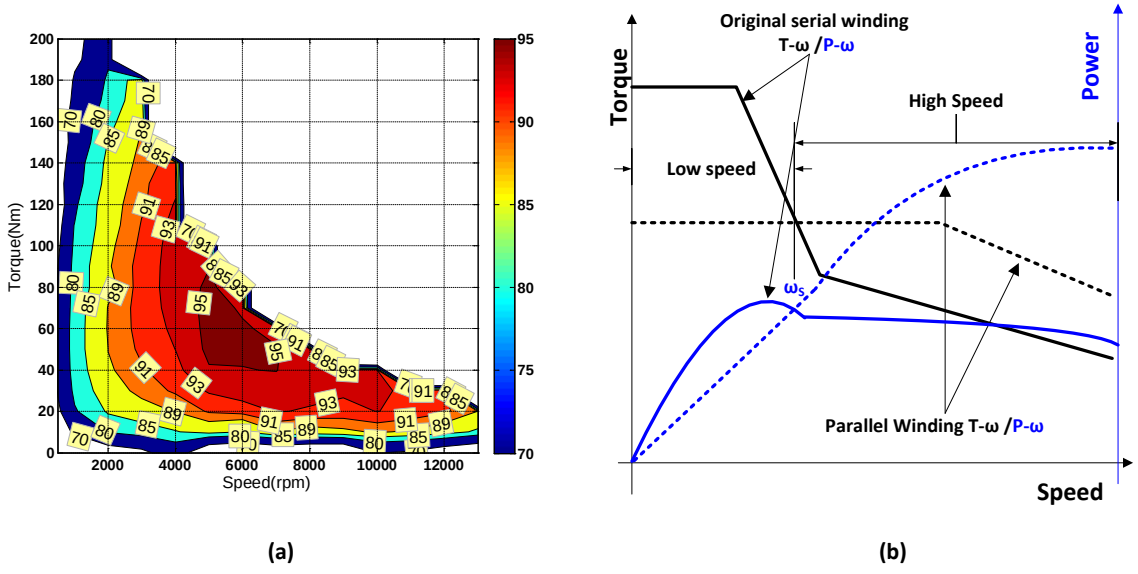


Figure 2-12: Efficiency contour of an IPMSM drive used in a commercial HEV (a) and comparison of characteristics of original serial and parallel windings of the drive (b).

Results and Discussion

Review of Previous Work

Reconfigurable windings, also known as switchable windings, have already been implemented in electric motors, and some products are already on the market. For example, some three-phase induction motors use a

star-delta soft-starter to reduce the inrush current when they start and operate with a fixed 60 Hz frequency. A star winding is initially selected, which has a larger impedance and back-emf; then when the motor builds up its speed and back-emf, it switches to a delta winding arrangement so that it can go to higher speed/higher power operation. Recently, more papers/patents have reported progress on reconfigurable windings approaches for automotive applications. For example, Eckart and Erik worked on reconfigurable windings for a surface-mounted PM synchronous motor and published several papers in the 1990s [2]. Chen and Cheng, by using relays, developed a motor with reconfigurable windings for electrical transmission applications and with brushless dc motors to expand the speed range [3–4]. Huang and Chang developed reconfigurable windings in an induction motor to achieve faster motor start-up [5]. Hsu, Fulton, Krieger, and Shum filed different patents recently for reconfigurable winding motors [6–8]. This approach uses ac switches to change the configuration of the windings so that the motor operating mode can be changed to achieve a wider speed range and faster motor starting. Another approach uses pole-changing motors to achieve expanded operation. Most methods under this approach are suitable only for induction motors.

Figure 2-13 illustrates two important industry patents on this topic. Figure 2-13(a) is a diagram representing patent A, for a system in which eight ac switches are used to change the star-connected stator windings between parallel and serial connections. In parallel mode, the five blue ac switches are on and the three orange switches are off; in serial mode, the five blue switches are off and the three orange switches are on. Figure 2-13(b) (patent B) represents a system patented in 2012 for electric bike applications. It uses only three ac switches rather than eight, which is a great improvement over patent A. In parallel mode, K_{P1} and K_{P2} are on and K_S is off; in serial mode, K_S is on and K_{P1} and K_{P2} are off. However, this system must use two small inverters instead of one. Further, note that all three switches must be installed in a dc bus; that arrangement may increase the total dc bus stray inductance, which will in turn increase the voltage spikes on the dc bus. This makes it less suitable for high-power applications. Note also that patent B has a dc short-circuit failure mode if all three switches are on at the same time, and some extra protection should be considered.

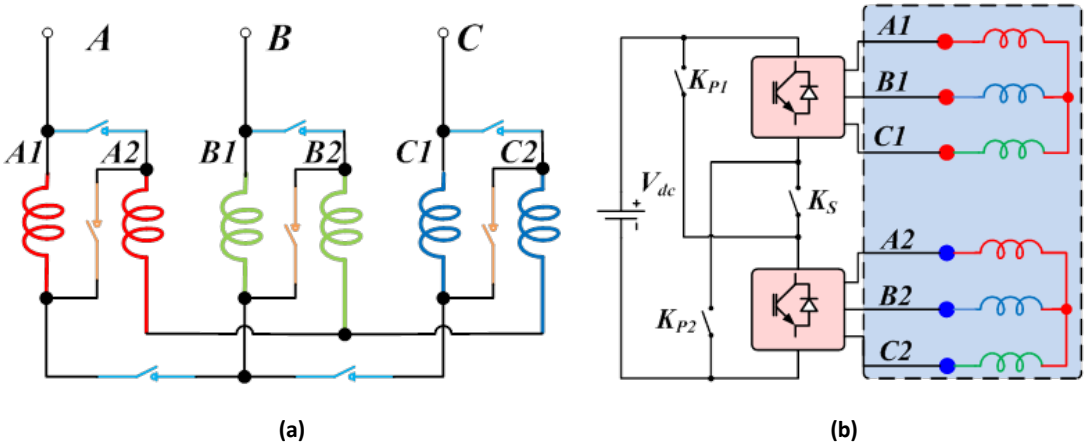


Figure 2-13: Schematics illustrating two industry patents: (a) Patent 20110234139 A1 (published in 2011 by Hsu) and (b) patent B-US20120086380 (published in 2012 by Krieger and Shum).

Proposed Designs

A new reconfigurable windings design was proposed to achieve expanded operation; the overall block diagram can be seen in Figure 2-14. Compared with the patent A approach shown in Figure 2-13, the proposed design uses fewer ac power switches, and because it does not insert ac power switches in the dc bus, it does not have the dc short-circuit failure mode that patent B has. To evaluate the advantages, the inverter losses of the design proposed in patent A were compared with those of the new approach, with the loss model including both switching and conduction losses. The basic equations used to calculate switching loss and conduction loss in a three-phase voltage source inverter can be seen in Eqs. (1)–(3). Equation (1) shows the inverter switching loss, where f_{SW} is the switching frequency, V_{dc} is the dc bus voltage, I_{PEAK} is the peak phase current, V_{ref} and I_{ref} are the voltage and current at which the switching losses are given, E_{ON_IGBT}, E_{OFF_IGBT} are the turn-on, turn-off loss of the insulated gate bipolar transistor (IGBT), and E_{OFF_DIODE} is the turn-off loss of the diode.

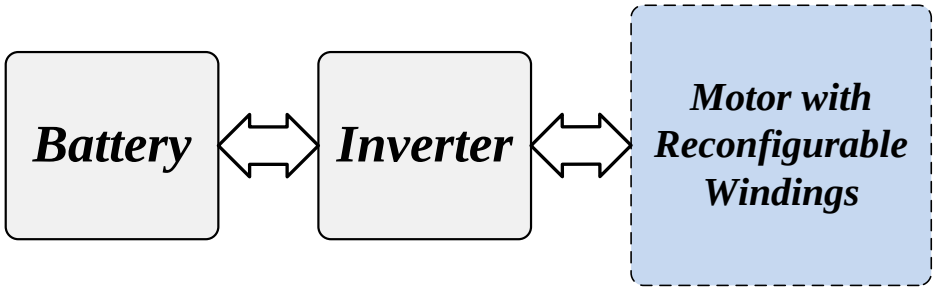


Figure 2-14: Proposed reconfigurable windings approach.

Equation (2) shows the conduction losses of the IGBT, in which V_{CEO} and r_{IGBT} are the zero current saturation voltage and equivalent resistance of the IGBT, m is the modulation index, and θ is the power displacement factor. Equation (3) shows the conduction losses of the diodes, in which V_{fO} and r_d are the zero current forward voltage and equivalent resistance of the diode. The voltage source inverter total loss can be calculated using Eqs. (1)–(3). The losses associated with the solid-state ac switches for changing windings configurations are also considered in Eq. (4), where V_{CER0} is zero current forward voltage drop and r_R is the equivalent resistance of the solid-state ac switch (relay). The key parameters of an off-the-shelf IGBT module with a 1,200 V/450 A rating were used in the simulation. A switching frequency of 7.5 kHz was used with a 650 Vdc bus voltage, and the motor peak phase current was 250 A.

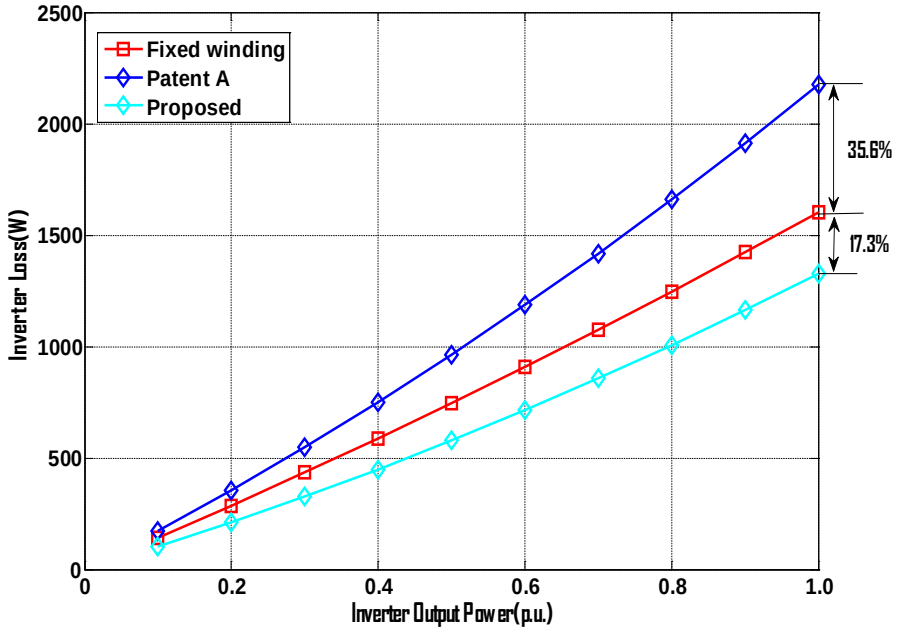
$$P_{SL} = \frac{6f_{sw}V_{dc}I_{Peak}}{\pi V_{ref}I_{ref}} \times \left(E_{ON\_IGBT} + E_{OFF\_IGBT} + E_{OFF\_DIODE}\right) \quad (1)$$

$$P_{CL\_IGBT} = I_{PEAK}V_{CEO}\left(\frac{1}{2\pi} + \frac{1}{8}mcos\theta\right) + I_{PEAK}^2 r_{IGBT}\left(\frac{1}{8} + \frac{1}{3\pi}mcos\theta\right) \quad (2)$$

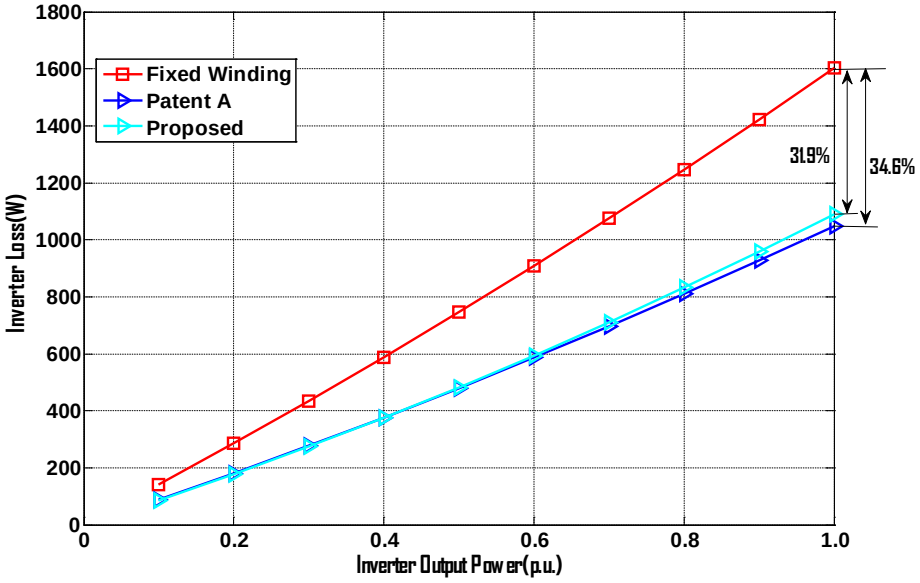
$$P_{CL\_D} = I_{PEAK}V_{f0}\left(\frac{1}{2\pi} - \frac{1}{8}mcos\theta\right) + I_{PEAK}^2 r_d\left(\frac{1}{8} - \frac{1}{3\pi}mcos\theta\right) \quad (3)$$

$$P_{CL\_R} = I_{PEAK}\left(\frac{2V_{CER0}}{\pi} + \frac{I_{PEAK}^2 r_R}{2}\right) \quad (4)$$

Figure 2-15 shows the total inverter losses of different approaches. The trace with red squares shows the inverter loss of a fixed windings motor at different peak phase currents from 50 A up to 250 A. The trace with blue diamonds shows the loss of the patent A design at high speed; the trace with cyan diamonds shows the loss of the proposed reconfigurable windings approach at high speed. The trace with blue triangles shows the loss of the patent A design in low speed; the trace with cyan triangles shows the loss of the proposed reconfigurable winding approach at low speed. It can be seen that the patent A design has the highest loss, while the fixed winding motor has the second highest loss. It is clear that the proposed reconfigurable winding approach has lower losses in both low-speed and high-speed operation compared with the fixed winding motor. For high speeds, the loss reduction is 17.3%, and for low speeds, it can be as high as 31.9%. Compared with the patent A approach, the proposed reconfigurable windings approach achieves a significant loss reduction of about 40% at high speed. Note that the loss at low speed is slightly higher (+2.7%) than that of the patent A approach. The results show the proposed reconfigurable windings approach can reduce power loss much more than the approach proposed in patent A.



(a)



(b)

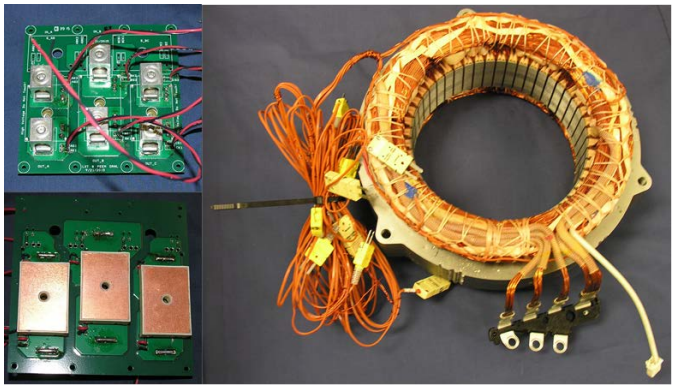
Figure 2-15: Simulated losses for the proposed design, fixed windings, and patent A system at high speed (a) and low speed (b).

Design of Low-Cost ac Switch Circuit and Benchtop Component Test of Switching Transients

As the winding configuration is changed, the drive will experience some switching transients, which must be considered with respect to switch selection and potential torque pulsations in vehicle propulsion. During the first transient, the controller firstly needs to bring all the phase currents down to zero. Secondly, the ac switches will turn on/off to change the windings' configuration. Finally, the controller will build up the three-phase currents to the new operating point. Because all three-phase currents are zero in switching transient, there is a torque interruption in the powertrain, which is not desirable. The duration of torque interruption is determined by the speed of the ac switches. If fast solid-state ac switches are used, each turn on/turn off takes only about 1–2 ms; the torque interruption time could be shorter than 10 ms. However, if slow ac switches like ac contactors are used, the undesirable torque interruption could be longer. Further, the ac contactors have

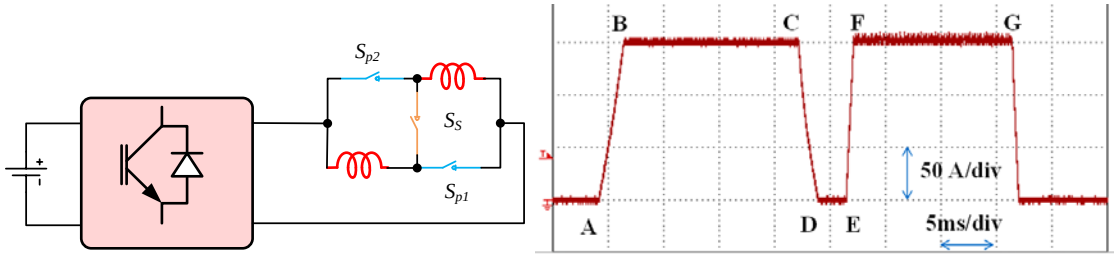
limited operating cycles because of the mechanical parts. All these drawbacks make the ac contactor unattractive for automotive applications. To minimize the torque interruption, fast and low-cost solid-state ac switches were selected in this project.

A 4.2 by 4.3 in. printed circuit board (PCB) was designed to switch the motor three-phase windings as indicated in Figure 2-16(a). Anti-parallel thyristor modules were used as the ac switches. There are some off-the-shelf, solid-state ac switches on the market. However, they are fairly expensive—around $100 for a switch with a 660 V/125 Arms rating. An anti-parallel thyristor module with a similar rating costs only about $15 (for quantity >1,680). It also has a smaller footprint than the off-the-shelf solid-state ac switches. An HEV motor with three-phase windings was used in the test. To simulate a switch winding transient, the windings were rearranged between series and parallel configurations. A single-phase inverter controlled by a digital signal processor was used for the real-time test. Figure 2-16 shows the ac switch PCB assembly and the motor winding. At top left is the top view of the PCB and at bottom left is the bottom view. Three solid-state ac switches were installed. Figure 2-16(b) is the motor, which was used in a commercial HEV drive system. Figure 2-17(a) shows the test diagram. The windings configuration can be changed between parallel and serial connection by turning the three ac switches on and off. Figure 2-17(b) shows the test waveform. The waveform shows the inverter output current in a transient from series mode (A-B-C-D) to parallel (E-F-G). The ac switches change the configuration of the windings between points D and E. The inverter current ramp-up/ramp-down time during the transient is about 2.45 ms (1.75 ms from C to D and 0.7 ms from E to F), and the total transient is only 5.0 ms. Because the serial windings configuration has higher inductance, it takes a longer time to ramp up/ramp down the current than it does in parallel mode. A dc bus voltage of 100 V was used in the test. Note that the current ramp-up/ramp-down time will be much faster with typical hybrid bus voltages in the range of 300–700 Vdc. The test results show the designed ac switch PCB assembly can change the motor windings configuration in a fairly short time. Research continues to be done to further reduce the transient.



(a) (b)

Figure 2-16: Solid-state ac switch board [(a) top, PCB top view; (a) bottom, PCB bottom view) and (b) motor windings used in benchtop test.



(a) (b)

Figure 2-17: Test circuit diagram with an inverter and three solid-state ac switches (a) and key test waveform of a series to parallel transient, output current 50 A/div, time 5 ms/div (b).

Design Strategies for Reducing PM Volume in EV Traction Drives using Reconfigurable Windings

Design strategies were developed for the use of reconfigurable windings to improve the performance of interior PM (IPM) machines while reducing the amount of PM materials consumed. An electric machine with a reconfigurable winding can be defined as any electric drive system which is able to change, by means of electronic switches, between two or more impedance modes as viewed at the machine terminals. Most of the literature on reconfigurable winding machines is for either induction machines or surface-mounted PM (SMPM) machines. Particularly, the goal of most of these investigations is to increase the constant power speed range (CPSR) of the machine.

One of the first reported reconfigurable winding devices was an induction motor for spindle applications requiring a wide CPSR. The authors reportedly achieved a CPSR of 1 : 12 using a delta–to–wye reconfiguration. The system successfully replaced a mechanical gearbox in a lathe cutting test. Another winding commutation approach for induction machines used two coil groups to effectively change the number of machine poles. Similar techniques exist for switching both the pole and phase configuration and the pole and turn configuration. Switched winding induction machines have also been investigated specifically in the context of EV applications.

Changing the stator windings by altering the number of turns is a strategy suitable for both induction and PM machines. For PM machines, it is possible to achieve a field weakening effect by putting a center tap in the phase coils and operating them in series or parallel. It is also possible to use a delta–to–wye changeover configuration with additional center taps for each phase, allowing four different modes of operation. A technique for switching between the three natural winding configurations—star, pentagon, and pentacle—for a five–phase PM machine was also explored.

There has been little investigation into IPM machines with reconfigurable windings. This may in part be due to the fact that IPM machines can be well designed with a wide CPSR. However, achieving a wide CPSR in this way imposes a trade-off between low speed torque, high speed power, and the relative balance of PM and reluctance torque. This trade-off is closely tied to the relationship between the rated and characteristic currents of the machine.

A significant difference between IPM topologies and the others previously investigated is the presence of reluctance torque. To achieve the high saliency ratio required for a large reluctance torque, there must be an easily saturable magnetic flux path in the machine. The nonlinear nature of magnetic saturation makes it difficult to study the effects of changes in the winding configuration using simple models. In these studies, numerical simulations of a simple IPM topology were used to examine the trade-offs that exist between torque and power density.

A simple design strategy for a machine that has windings reconfigurable between a series and parallel mode begins with designing the series configuration to maximize the torque produced by the machine while constraining the characteristic current to be equal to half the rated current. From there, increased power—both maximum and continuous—can be achieved above the series mode base speed by switching to the parallel winding configuration. Our studies show that by using a switched winding approach, it is possible to obtain torque and power versus speed characteristics similar to that of a standard IPM machine with a significant decrease in PM material.

Theory for Design of IPM Machine with Reconfigurable Winding

The fundamental equation for torque production of an IPM machine in the rotor D–Q reference frame is given by

$$\tau = \frac{3P}{4}\left[\lambda_{pm} I cos(\theta) + \frac{1}{2}\left[L_q - L_d\right] I^2 sin(2\theta)\right], \quad (5)$$

where I is the stator current amplitude, $\theta$is the stator current angle, L_d and L_q are, respectively, the direct– and quadrature–axis inductance, λ_{pm} is the PM flux--linkage (aligned with the direct axis), and P is the number of machine poles. The direct-- and quadrature--axis currents are given by $I_d = Isin(\theta)$ and $I_q = Icos(\theta)$.

The fundamental voltage equations for an IPM machine, ignoring the stator resistance, in the rotor D-Q reference frame is given by

$$V_d = \omega_e L_q I cos(\theta) \tag{6}$$

and

$$V_q = \omega_e(\lambda_{pm} - L_d I sin(\theta)) \ , \tag{7}$$

where V_d and V_q are the direct and quadrature axis voltages with voltage magnitude $V = \sqrt{V_d^2 + V_q^2}$ and ω_e as the electrical frequency in radians per second. An important quantity of interest for IPM machines is the characteristic current, obtained by setting $V_q = 0$, which is the ratio of the permanent flux–linkage to direct-axis inductance, $I_c = \frac{\lambda_{pm}}{L_d}$. The characteristic current is the direct–axis current amplitude required to completely cancel the PM flux linkage coupled to the stator, resulting in zero quadrature voltage. The characteristic current can be more generally defined as satisfying the equation $L_d(I_d, 0) = \lambda$ for nonlinear magnetic models, where the direct-axis inductance $L_d(I_d, I_q)$ is a function of I_d and I_q. Finally, there will be some operational limitations placed on the machine as a result of the inverter rating. We assume $I \leq I_e$ and $V \leq V_e$, where I_e is the rated current and V_e is the rated voltage.
For sufficiently high rated speeds, machines with $I_d > I_e$ cannot produce constant power over their entire speed range because they are not capable of full field weakening. Machines with $I_d < I_e$ are capable of full field weakening and can deliver constant power over a wide speed range. However, this power is generally less than the peak power over all speeds because the maximum current amplitude must decrease due to voltage limitations at higher speeds.

The torque equation reveals that around the maximum torque operating point, τ is about constant with respect to θ. Where $\tau = 0$ at $\theta = 90°$, τ varies about linearly with θ. Therefore, at worst, the torque is linearly decreasing as θ is adjusted for field weakening. When a significant amount of reluctance torque is available, τ will vary like I^2 at high torque levels and like I at low torque levels. The analysis for the voltage magnitude V is more complicated, but it can be estimated that the voltage varies linearly with both θ and I at any operating point. This means that if the current amplitude must be decreased because of voltage limitations and large inductances, the torque will decrease faster with I than the speed will be allowed to increase. This will result in reduced power output above the base speed of the machine.

A perfectly flat constant power speed range can be obtained by designs where $I_d = I_e$. These designs have peak constant power capabilities greater than the peak power delivered at the base speed due to the fact that τ is constant with respect to θ at the maximum torque operating point. Achieving the $I_d = I_e$ characteristic for a given peak torque requirement implies a precise relationship between the required torque, PM flux, direct–axis inductance, and saliency ratio. Under these constraints, the only method of reducing the amount of PM material is to increase the saliency ratio.

For a fixed saliency ratio, it is possible to decrease the amount of PM material while maintaining the same peak torque level by uniformly increasing L_d and L_q by, for example, increasing the number of turns in the stator or increasing the diameter of the stator bore. This, however, will decrease I_d and lead to a reduction in the peak power for the reasons previously discussed. A different way to state this is that for a given peak torque level, machines that more closely match the requirement that $I_d = I_e$ will tend to have higher power capabilities in the constant power region. This is demonstrated with two design examples below.

For an IPM machine with a reconfigurable winding structure and $I_d = I_e$ in series mode, switching to a parallel winding configuration does nothing to improve the performance of the drive. This decreases the peak torque and field-weakening capability by increasing the characteristic current to $I_d \approx 2I_e$. This also introduces a dangerous short circuit fault mode if the drive is not capable of handling twice the rated current.

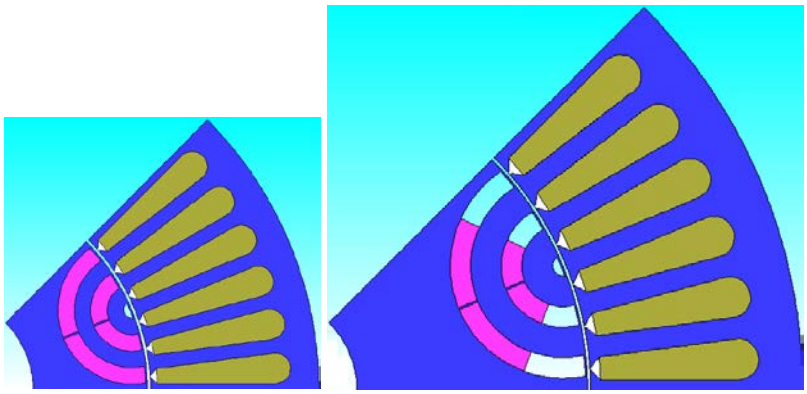
The situation is different for an IPM machine design with, for example, $I_d = 0.5I_e$. In this case, switching from a series to a parallel winding configuration will still decrease the peak torque, but the field-weakening capability in this mode will be improved because $I_d \approx I_e$ in parallel mode. That is to say, the peak torque in the

parallel mode will be deliverable at higher speeds than the same torque in the series mode. Moreover, the peak power in the constant power speed range in the parallel configuration will be flat above the base speed as there will be no need to decrease the current amplitude. Therefore, it is possible to think of the series winding configuration as a low speed/high torque mode, and the parallel configuration as a high speed/high power mode.

It is also possible to approach the design problem as requiring $I_c = I_r$ in parallel mode and view switching into a series mode as a method of increasing the peak torque capability. However, this would imply that significant headroom exists in the magnetic circuit to allow doubling the number of amp turns without too much saturation occurring. It is likely that existing designs with $I_c = I_r$ are already aggressively sized to maximize power and torque with respect to saturation of the magnetic circuit. When approaching a design from scratch with the intent of using a reconfigurable winding, either may be viable. The difference is whether the problem is approached as one of optimizing peak torque capability with the constraint that $I_c = 0.5I_r$ or peak power capability with the constraint that $I_c = I_r$.

Design Examples

To illustrate the trade-offs that can be made in achieving similar design goals in machines with and without reconfigurable windings, a coarse optimization of two machines was performed with different stack lengths, l_s, and stator outer radii, r_{si}, but fixed active volume given as $\pi r_{is}^2 l_s$ and maximum peak current density as 8 A-RMS. The inverter constraints were assumed to be 290 A peak per phase with a dc-link voltage of 375 V. The two resulting designs are shown in Figure 2-18. The base case machine has $l_s = 150$ mm, $r_{si} = 100$ mm, and very nearly matches the requirement that $I_c = I_r$ after being optimized to maximize the peak torque capability. The basic parameters for the optimization procedure were the stator bore, stator tooth thickness, and magnet thickness.



(a) (b)

Figure 2-18: Comparison of two different machine designs with different ratio of characteristic current to rated current: (a) machine design with stack length of 150 mm, stator outer radius of 100 mm, and $I_c \approx I_r$; (b) machine design with stack length of 75 mm, stator outer radius of 141 mm, and $I_c \approx 0.5I_r$.

The machine intended for use with reconfigurable windings was designed in two stages. First, the aspect ratio was changed so that $l_s = 75$ mm, $r_{si} = 141$ mm so that the active volume is the same as the base machine. Second, the machine was optimized over the same parameters as the base machine to maximize the torque output. The resulting torque is greater because the larger stator outer radius is able to accommodate more turns. Last, the arc length of the magnets was reduced to give the same peak torque capability as the base case machine. The reconfigurable winding machine ends up having the same peak torque capability as the base case machine with about 40% less PM material.

The torque–speed curves associated with both machines are given in Figure 2-19 and Figure 2-20. The peak torque capabilities of the base machine and the reconfigurable-winding machine (in series mode) are both about 320 Nm. The base machine has a base speed of about 2,500 rpm. In series mode, the reconfigurable winding machine has a base speed of 2,000 rpm and in parallel mode 4,500 rpm—more than double. Additionally, the peak torque available in parallel mode is 190 Nm, which is greater than 50% of the series mode torque and much more than predicted by the linear torque model. This is an important but subtle point:

saturation occurring in series mode means that switching to a parallel winding configuration will typically increase the power delivered at the new base speed. This is in contrast with reconfigurable winding schemes previously reported for SMPM machines, which have essentially the same power at base speed regardless of the winding configuration. That is, the linear model is more accurate for SMPM than for IPM machines.

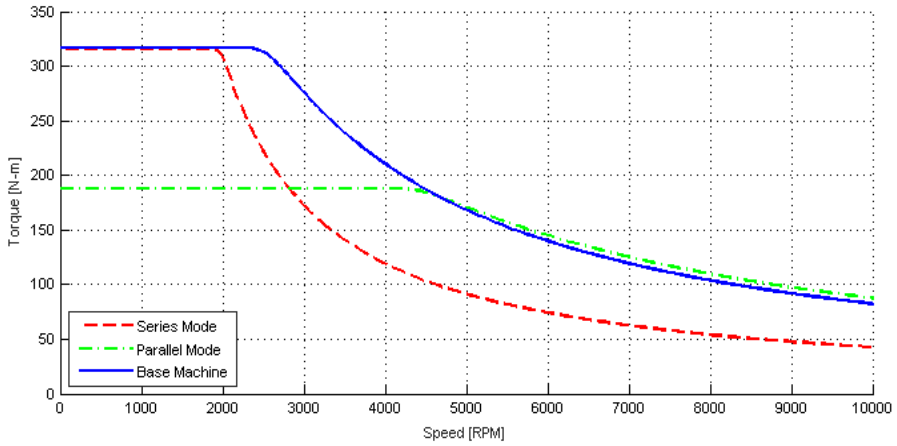


Figure 2-19: Torque-speed curve demonstrating the performance of both machines.

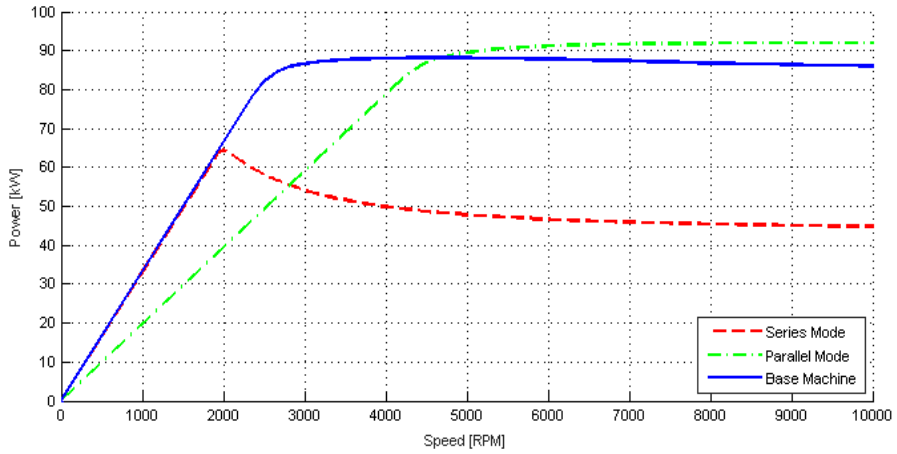


Figure 2-20: Power-speed curve demonstrating the performance of both machines.

The relationship between the rated current, characteristic current, and peak power capability is most easily understood by examining the power-speed curves. The base case machine has $I_c \approx I_r$ and a flat peak power above the base speed. Moreover, the power at the base speed is about 81 kW, while the peak power available from 3,000 rpm up to the maximum speed is greater than 85 kW.

The situation for the series-mode reconfigurable winding machine is different. In this mode, the machine has $I_c \approx I_r$ and a corresponding local maximum in the power-speed curve. The peak power at the base speed is 65 kW, which decreases to 45 kW as the machine approaches its maximum speed. Switching to a parallel mode allows us to achieve a peak power capability similar to the base machine's, with 89 kW available at the base speed, approaching 92 kW as the speed increases to 10 krpm. This is more than double the series-mode case.

It should be noted that the procedure used to arrive at this design does not necessarily minimize the PM material under the constraint that the peak torque capabilities be the same as those for the base case machine. This comprehensive optimization was beyond the scope of this study. Additionally, in comparing the torque- and power-speed curves of base and reconfigurable winding machines it can be seen that there are some drawbacks to the reconfigurable winding machine. In particular, there is a region on the torque-speed plane that is reachable by the base machine but not by the reconfigurable winding machine. It is unlikely that it is

possible to design a reconfigurable winding machine that has exactly the same torque-speed characteristic as a standard machine. The nonconforming regions are an important design trade-off that must be considered. In this instance, it was mitigated by reducing the PM volume to give the same peak torque capability. Another valid approach would be to choose the design so that the torque-speed curves of the base and the series-mode reconfigurable machine intersect at a given point (e.g., the base speed). This approach may still reduce the total PM volume—although to a lesser extent—but increase the performance of the machine.

The impact of reconfigurable winding on motor efficiency was studied using a PM motor similar to that of the Prius. Efficiency maps for both modes of operation were generated. A combined efficiency map is shown in Figure 2-21, with serial and parallel operational areas indicated. For this plot, the highest efficiency was selected for each torque-speed operation point. It can be observed that the parallel mode greatly expands the high efficiency regions for high power operation points. Using the same data, a differential efficiency plot, shown in Figure 2-22, was created by subtracting serial mode efficincies from parallel mode efficiencies. It should be noted that for clarity this map only illustrates differential efficiency in areas that overlap. Low speed, high torque efficiencies can be up to 10% higher in serial mode, whereas high speed, low torque efficiencies can be up to 10% higher in parallel mode.

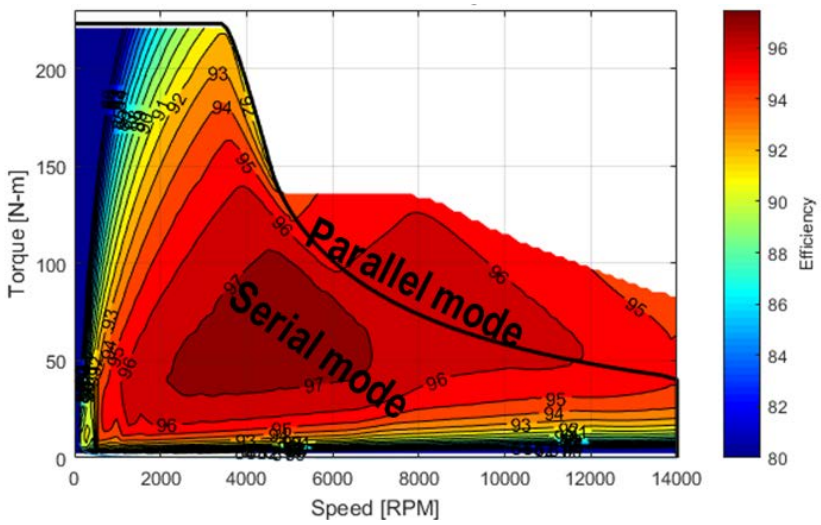


Figure 2-21: Combined efficiency plot for serial and parallel modes.

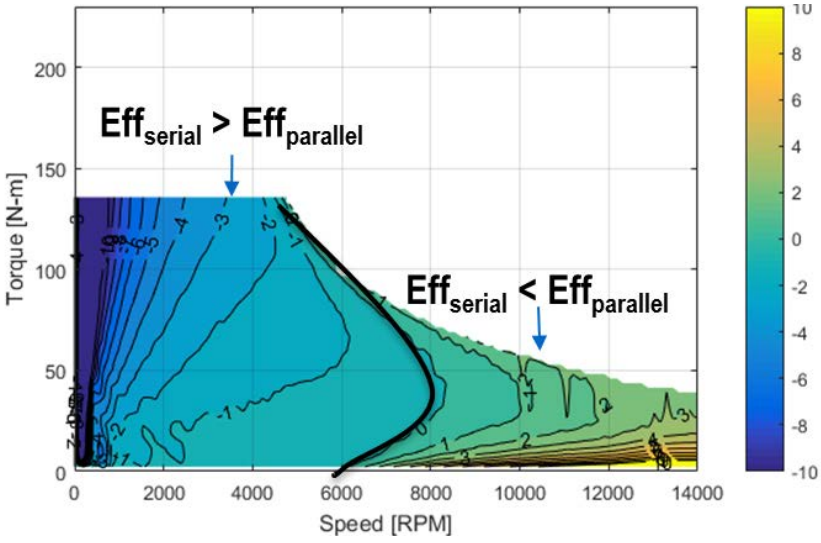


Figure 2-22: Differential efficiency plot for serial and parallel modes.

Conclusions and Future Directions

Several reconfigurable winding approaches were developed that have fewer solid-state switches and eliminate battery short-circuit failure modes. Fewer solid-state switches facilitate a reconfigurable winding solution with low cost and high switching efficiency. A low-cost solid-state switch circuit and PCB was designed, fabricated, and tested to demonstrate that acceptable switching times could be achieved. Initial test results show that reconfiguration can be achieved in about 5 ms. Future work will include a cost study with consideration of reduced motor size and additional component and material costs and comparisons with mechanical gearboxes.

From a motor design perspective, theoretical investigations were performed to understand when IPM machines can benefit from the use of reconfigurable windings. It was found that machines with characteristic currents equal to about half their rated currents can achieve much higher power operation at high speeds by changing from series to parallel mode. This effectively doubles the characteristic current and allows for field weakening to occur in the high speed region without having to reduce the current vector magnitude.

An exemplar design process was performed to illustrate one potential trade-off that can be made between machines with and without reconfigurable windings. First, a base case machine was developed with equal characteristic and rated currents. Second, a series-mode reconfigurable winding machine was designed to meet the torque capability of the base case machine with half the characteristic current and less PM material. Comparisons of the torque-speed and power-speed profiles of the two machines indicate they have similar performance characteristics, with the base case machine outperforming the reconfigurable winding machine only in a small region around its base speed. In addition to demonstrating performance improvements, this study shows that considerable efficiency improvements can be realized with a reconfigurable winding approach.

FY 2016 Presentations/Publications/Patents

1. T. Burress et al, “Multi-speed range electric motor R&D,” presented at the DOE Vehicle Technologies Program Electric Drive Technologies Electrical and Electronics Technical Team meeting, December 2015, Southfield, Michigan.
2. L. Tang et al, “Electric motor performance improvement techniques,” presented at the DOE Vehicle Technologies Office 2016 Annual Merit Review, June 2016, Washington, DC.

References

1. T. A. Burress, “Evaluation of the 2010 Toyota Prius Hybrid Synergy Drive System,” available at http://info.ornl.gov/sites/publications/files/Pub26762.pdf.
2. E. Nipp, “Alternative to field-weakening of surface-mounted permanent-magnet motors for variable-speed drives,” in *Proceedings of the IEEE Industry Applications Society Annual Meeting*, **1**, pp.191–198, 1995.
3. C.-H Chen and M. Y. Cheng, “Design of a multispeed winding for a brushless dc motor and its sensorless control,” *Electric Power Applications, IEE Proceedings*, **153**(6), pp. 834–841, November 2006.
4. Cheng-Hu Chen, Ming-Yang Cheng, and Ming-Shun Tsai, “Study on a wide speed range integrated electrical transmission system," *Power Electronics and Drives Systems, 2005 (PEDS 2005. International Conference)*, **1**, pp.781–786, 2005.
5. H. Huang and L. Chang, “Electrical two-speed propulsion by motor winding switching and its control strategies for electric vehicles,” *IEEE Transactions on Vehicular Technology*, **48**(2), pp. 607–618, March 1999.
6. John Hsu, “Electronically commutated serial-parallel switching for motor windings,” US Patent 20110234139 A1, published September 29, 2011.
7. D. A. Fulton, “Switch module for an electric machine having switchable stator windings,” US Patent 8415910 B2, published April 9, 2013; also published as US 20120068656 A1, March 22, 2012.
8. M. Krieger and H. Shum, “Electric motor having windings operable in parallel and/or series, and related methods,” US Patent 20120086380 A1, published April 12, 2012.

2.3 Electric Motor Thermal Management Research

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Abstract/Executive Summary

With the push to reduce component volumes, lower costs, and reduce weight without sacrificing performance or reliability, the challenges associated with thermal management increase for power electronics and electric motors. Thermal management for electric motors will become more important as the automotive industry continues the transition to more electrically dominant vehicle propulsion systems. The transition to such systems leads to higher-power duty cycles for electric-drive systems. Thermal constraints place significant limitations on how electric motors ultimately perform, and as thermal management improves, there will be direct tradeoffs among motor performance, efficiency, cost, and the sizing of electric motors to operate within the thermal constraints.

The goal of this research project is to support broad industry demand for data, analysis methods, and experimental techniques to improve and better understand motor thermal management. Work in FY16 focused on two areas related to motor thermal management: passive thermal performance and active convective cooling. Passive thermal performance emphasized the thermal impact of materials and thermal interfaces among materials within an assembled motor. Active convective cooling focused on measuring convective heat-transfer coefficients using automatic transmission fluid (ATF).

Accomplishments

- Completed construction of experimental test apparatus to measure large-scale variation in ATF convective heat transfer coefficients
- Completed measurement of fan jet nozzle for ATF heat transfer in collaboration with industry partner
- In collaboration with Oak Ridge National Laboratory (ORNL), measured and analyzed slot winding materials and submitted a manuscript summarizing the results to a journal for potential publication
- In collaboration with Ames Laboratory, measured mechanical and thermal properties of new magnet materials.

Introduction

Thermal management for electric motors is important as the automotive industry continues to transition to more electrically dominant vehicle propulsion systems. With the push to reduce component size, lower costs, and reduce weight without sacrificing performance or reliability, the challenges associated with thermal management for power electronics and electric motors increase. The transition to more electrically dominant propulsion systems leads to higher-power duty cycles for electric drive systems. Thermal constraints place significant limitations on how electric motors ultimately perform. As summarized by Dr. Thomas Lipo who researches AC motor drives at the University of Wisconsin, "[a]n optimized thermal design can help increase machine rated power substantially, almost without any increase of its manufacturing costs." [1]. The performance limitations caused by motor heating are highlighted in Figure 2-23. The motor's ability to increase running time at higher power levels within electrical operating limits is directly related to the ability to remove heat from critical components. As thermal management improves, there will be a direct tradeoff among motor performance, efficiency, cost, and the sizing of electric motors to operate within the thermal constraints.

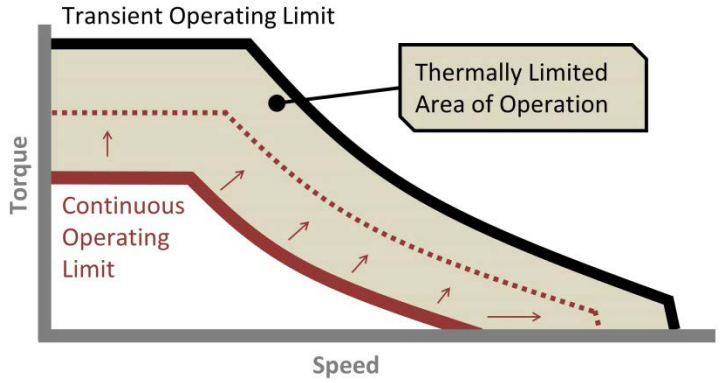

Figure 2-23: Thermal management impact on motor performance to support increased power
Image Source: NREL

Thermal management of electric motors is a complex challenge because of the multiple heat transfer paths within the motor and the multiple materials and thermal interfaces through which the heat must pass to be removed. The technical challenges to motor thermal management are summarized by Hendershot and Miller as follows: "Heat transfer is as important as electromagnetic and mechanical design. The analysis of heat transfer and fluid flow in motors is actually more complex, more nonlinear, and more difficult than the electromagnetic behavior" [2]. Figure 2-24 provides a cut cross-section view illustrating heat transfer and cooling paths for automotive traction drive applications. The heat generated by the electric motor is distributed throughout multiple components within the electric motor. For example, heat is generated due to losses within the stator slot-windings, stator end-windings, stator laminations, rotor laminations, and rotor magnets or conductors. The distribution of the generated heat within the components is dependent on the motor type and the operating condition (torque/speed) of the motor. The selected cooling approach for the motor impacts the path of heat flow through the motor and the temperature distribution of components. For example, as shown in Figure 2-24, a motor cooled with a stator cooling jacket will require heat generated within the slot windings to pass through multiple material layers and material interfaces before the heat is extracted through the cooling jacket. The thermal properties of the materials and the thermal contact resistances due to the material interfaces impact the temperature distribution inside the motor as heat flows into the cooling jacket. Alternatively, direct cooling of the windings with oil or ATF reduces the heat transfer path from the motor windings to the coolant. However, heat from the stator must pass through several interfaces. The resulting changes in the temperature distribution within the motor lead to hot spots within the motor that could be difficult to measure.

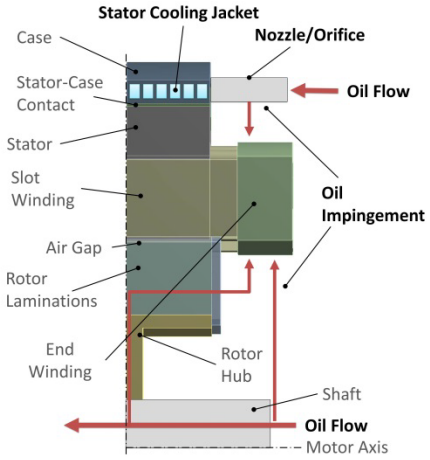

Figure 2-24: Heat must pass through several layers within the motor to be extracted through active cooling such as through a cooling jacket or spray cooling with oil such as ATF.
Image Source: NREL

Thermal management of the motor is not only important for the reliability of the motor, but the temperatures of the components within the motor affect material properties that directly relate to the torque production, control, and efficiency of the motor. For this reason, motor designers need accurate thermal models of the electric motor during the design and control development of the motor. Critical to the ability to accurately model the thermal behavior of the motor is access to data describing critical thermal characteristics of the motor. Such data include direction-dependent thermal conductivity measurements of nonuniform motor components such as lamination stacks and windings. It also includes data to quantify thermal contact resistances between components in the motor. Finally, it includes data to support the modeling and design of active cooling of the motor and the convective heat transfer coefficients possible from alternative cooling approaches.

Approach

The ability to remove heat from an electric motor depends on the passive stack thermal resistance within the motor and the convective cooling performance of the selected cooling technology. In addition, as new materials are developed, it is important to characterize temperature-dependent material mechanical properties and thermal properties. Characterization of new materials enables motor designers to evaluate the potential performance tradeoffs of new materials for motor applications. For this reason, the approach for the research project splits the efforts between three primary categories as illustrated in Figure 2-25.

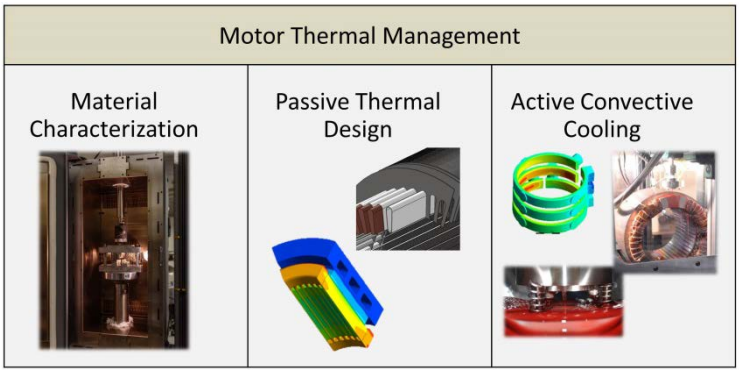

Figure 2-25: Approach to motor thermal management divided between passive thermal design and active convective cooling
Photo Credits: Doug DeVoto, Jana Jeffers, Kevin Bennion, NREL

Passive thermal design refers to the geometrical layout, material selection, and thermal interfaces that affect the heat-spreading capabilities within the motor. The ability for heat to spread through the motor affects the thermal temperature gradients within the motor. The active convective cooling technology is the cooling mechanism that ultimately removes the heat from the motor and transfers the heat to another location to reject the heat to the ambient environment. The material characterization work focuses on the measurement of

mechanical and thermal properties, in collaboration with project partners, of new individual materials relevant to motor applications.

Active Cooling

The two common approaches highlighted in Figure 2-24 for active cooling include: 1) directly cooling the motor with ATF, and 2) cooling the motor with a cooling jacket surrounding the stator. The advantages of either cooling approach depend on the application's coolant availability, the motor geometry, the motor winding configuration, and the motor loss distribution. The advantage of cooling using ATF is that it is possible to directly cool the motor windings or rotor. Past work focused on measurement of average convection coefficients of ATF jets passing through a circular orifice directly impinging on target surfaces representative of motor end windings. In the area of active cooling, the focus during FY16 emphasized an alternative spray pattern and spatial mapping of the heat transfer coefficients at the stator winding scale.

The heat transfer coefficient will vary along the larger-scale stator end-winding illustrated in Figure 2-26. As the ATF flows over the end-winding, the heat transfer will be different than around the impingement zone of the jet. The irregular surface caused by the wire bundles also complicates the fluid flow paths and the heat transfer. During FY16, the National Renewable Energy Laboratory (NREL) finished construction of an experimental setup and enclosure to measure the heat transfer variation on the motor end-winding. The initial experiments exclude the irregular surfaces caused by the wire bundles seen in Figure 2-26, but additional end-winding geometry complexity can be incorporated in future experiments using the same experimental setup. The following sections summarize the design and construction of the experimental equipment and the experiments are part of ongoing work.

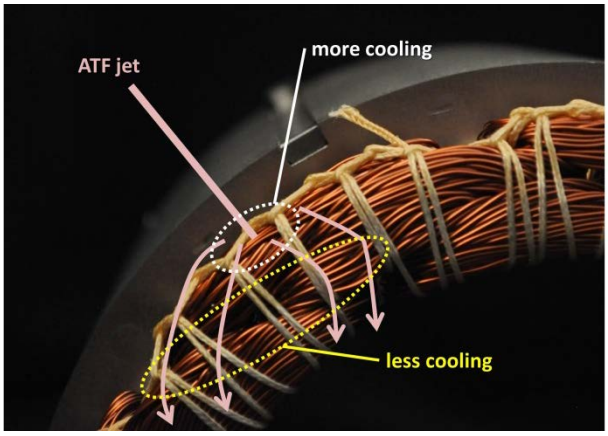

Figure 2-26: Heat transfer due to ATF jet impingement will vary over the end-winding surface.
Photo Credit: Kevin Bennion, NREL

Passive Thermal Design

The passive thermal stack elements illustrated in Figure 2-24 and Figure 2-27 are critical to designing effective thermal management systems for electric motors. The work supports improved thermal models for motor design, which also enables analysis to compare the potential impacts of new materials, fabrication methods, or material processing on motor heat transfer. Figure 2-27 illustrates a few of the critical elements that influence the passive cooling of the motor or the ability of heat to flow through the motor. A few of the items highlighted in Figure 2-27 include the stator-to-case thermal contact resistance, lamination through-stack and in-plane thermal conductivity, winding cross-slot thermal properties and thermal interface resistance between ground insulation materials and the respective motor elements in contact with the slot liner or ground insulation. Efforts continued in FY16 to measure passive stack elements within the motor as highlighted above in collaboration with industry, universities, and ORNL.

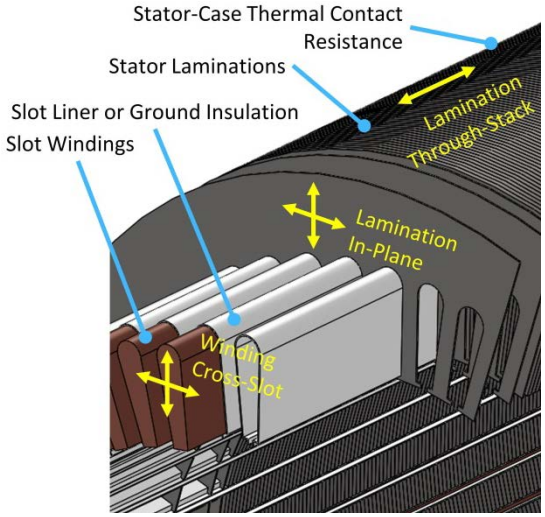

Figure 2-27: Passive stack thermal properties and terminology.
Image Source: NREL

Material Characterization

The material characterization work focuses on the measurement of mechanical and thermal properties of new individual materials relevant to motor applications in collaboration with project partners. For FY16, the work focused on collaborations with Ames Laboratory and its work to develop new magnet materials relevant for electric motor applications. NREL provided support to Ames for mechanically and thermally characterizing the new magnet materials. Tests focused on comparing the transverse rupture strength and thermal conductivity of the new magnet materials with currently available materials. The test fixture for the transverse rupture testing is shown in Figure 2-28. The transverse rupture strength (TRS) is determined by Equation 1 [3] using the force required to rupture the specimen (P), the distance between supports (L), the specimen width (w), and the specimen thickness (t).

Figure 2-28: Transverse rupture test apparatus.
Photo Credit: Doug DeVoto, NREL

$$TRS = \frac{3PL}{2t^2w} \quad (1)$$

Results and Discussion

The discussion included below is separated into the three main focus areas described above. The first section summarizes progress for the material characterization results. The second section focuses on passive cooling of the electric motor. The third section summarizes progress on active cooling with emphasis on using ATF for cooling electric motors.

Material Characterization

Measurements of both transverse rupture strength and thermal conductivity were made, in collaboration with researchers at Ames Laboratory, on new AlNiCo magnets developed at Ames. The transverse rupture strength tests were performed at NREL over a range of temperatures from -40°C to 150°C. The test fixture inside the environmental chamber is shown in Figure 2-29. The tests were performed both on the new Ames-developed material and two commercially available AlNiCo-based magnets (AlNiCo 8HE and AlNiCo 9). The results of the transverse rupture strength are shown in the left image of Figure 2-30. The new Ames material demonstrated higher transverse rupture strength at each of the tested temperatures. The significance is a mechanically stronger magnet that is easier for manufacturers to implement into motor designs.

Figure 2-29: Magnet materials (left) being tested for transverse rupture strength within a thermal chamber (right).
Photo Credit: Doug DeVoto, NREL

The thermal conductivity of the new Ames-developed magnet was also measured in comparison with the same two commercially available materials. The thermal conductivity measurements were performed at room temperature by measuring the thermal diffusivity by the xenon flash technique. For the tested samples, the average thermal conductivity of the Ames material was lower than the two commercial materials that were evaluated. The significance of the lower thermal conductivity in a motor application was not evaluated at this time.

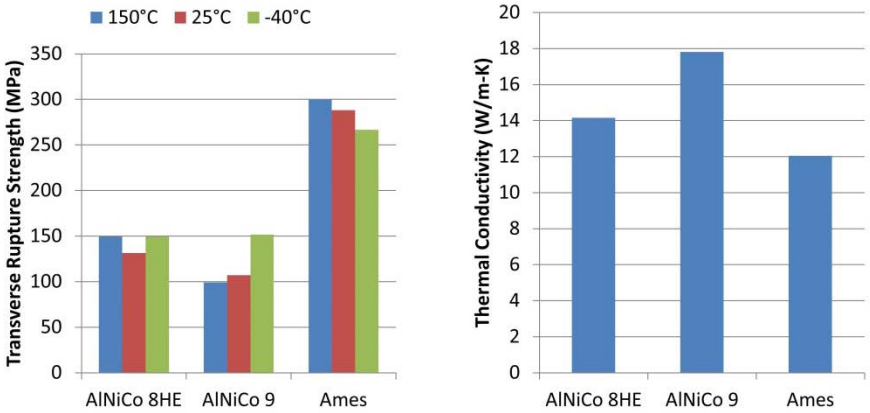

Figure 2-30: Transverse rupture test results of Ames material and commercial materials (left). Thermal conductivity test results of Ames material compared with commercially available materials (right).
Image Source: NREL

Passive Thermal Design

The work on the passive stack thermal design focused on evaluating methods for measuring thermal properties of composite wire bundle samples held together with varnish. Figure 2-31a highlights examples of wire bundles for the slot winding and end winding of the motor stator. The ability to measure the apparent thermal conductivity of the wire bundle samples will enable the ability to evaluate the impact of new motor winding materials. Having data on the performance impact of new materials will enable motor designers to evaluate the impact in particular motor designs.

During FY16, NREL worked in collaboration with ORNL to focus more closely on the winding materials within the electric motor. Figure 2-31b and Figure 2-31c show examples of the motor winding composite material samples prepared by ORNL. The samples were prepared to measure the apparent thermal conductivity parallel and perpendicular to the axis of the wire. ORNL and NREL compared three methods for measuring the thermal conductivity using laser flash, transient plane source, and transmittance test methods [4]–[6]. Each of the test methods was first compared by estimating the thermal conductivity of monolithic, isotropic, and homogenous soda lime silicate glass (low thermal conductivity) and polycrystalline silicon carbide (high thermal conductivity). The apparatus using the transmittance test method [6] with the composite wire bundle sample is shown in Figure 2-31d.

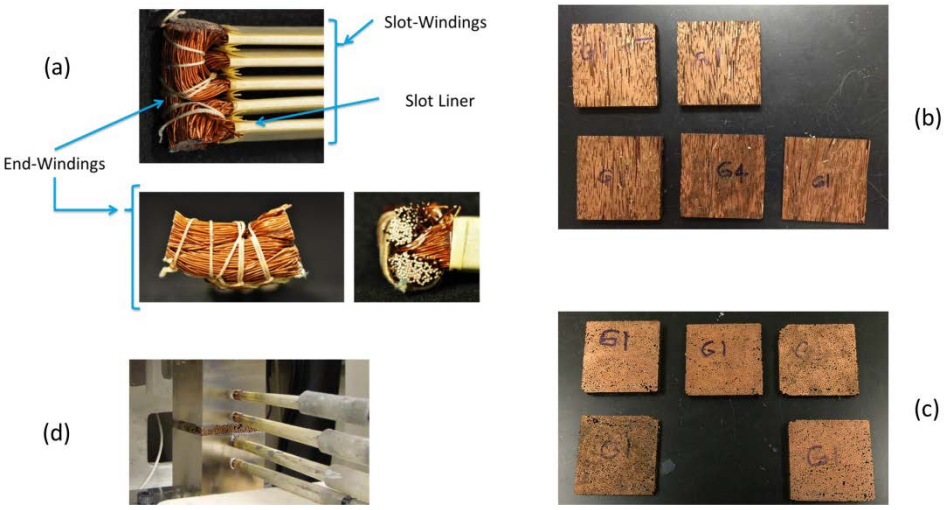

Figure 2-31: Sample wire bundles in motor slot and end winding (a), winding sample blocks prepared by ORNL for thermal property measurements perpendicular to wire axis (b), winding sample blocks prepared by ORNL for thermal property measurements parallel to wire axis (c), test sample under test using transmittance test method (d).
Photo credits: Kevin Bennion, Emily Cousineau, NREL

In addition to performing the sample measurements, an effort was made to compare the experimental results with derived estimates based on finite element analysis (FEA) models of the wire bundle. For the FEA model, the copper fill factor of the sample was determined using two methods. One method determined the fill factor for each individual sample using image analysis of the visible cross section of the wires. The second method determined the fill factor by measuring the density of the test sample. Figure 2-32 compares the experimental results and the FEA estimates for two wire-size samples. The FEA Low and FEA High represent the range for the low and high estimates for the copper fill factor of the sample. The measurement uncertainty of the data was determined with the 95% confidence interval including all known random and systematic sources of error [7].

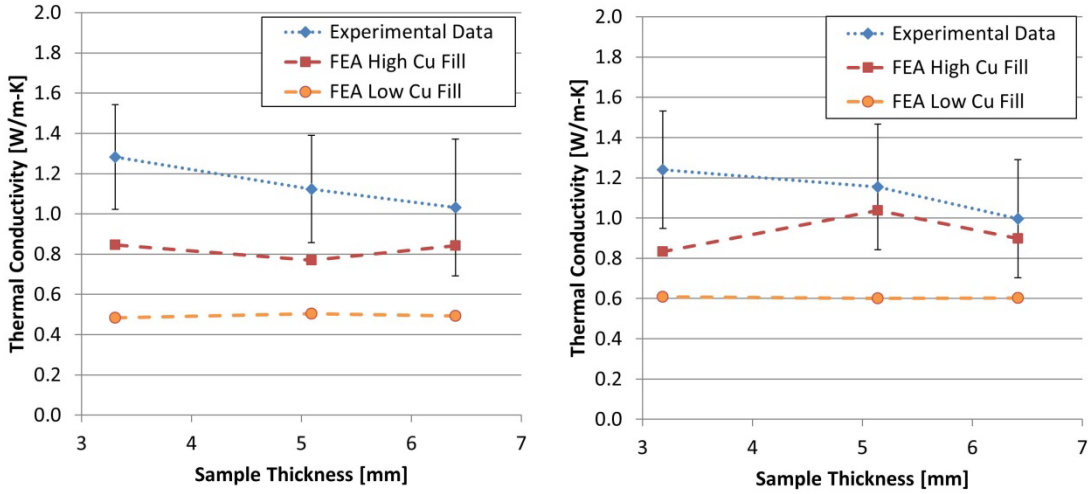

Figure 2-32: Transmittance test method results for thermal conductivity perpendicular to wire axis, and comparison of experimental data with FEA model results based on low and high estimates for the sample copper fill factor for 22 AWG (left) and 19 AWG (right).
Image Source: NREL

As seen in Figure 2-32, the measured thermal conductivity values are larger than the predicted values. The FEA modeling assumes ideal varnish fill (no voids) and no thermal interfacial losses between the materials within the wire bundle. With these assumptions, the FEA estimates would be expected to be higher than the measured data. However, the FEA model also assumes ideal or uniform packing of the wires with the sample which is not representative of the tested samples. The non-uniform packing of the wires could produce preferential pathways for heat transfer resulting in higher measured thermal conductivity. Full details of the testing and discussion of the results were submitted during FY16 for consideration of publication to the ASME Journal of Thermal Science and Engineering Applications.

Active Cooling

Work on active convective cooling during FY16 focused on using ATF for cooling electric motors. Past work measured the average convective heat transfer coefficients of circular orifice ATF jets directly impinging on stationary target surfaces with surface features representative of motor end-windings [8]. A schematic of the orifice jet test is shown in Figure 2-33a. An alternative ATF jet geometry was tested during FY16, as shown in Figure 2-33b. Figure 2-33b shows a flat planar fan jet that impacts the target surface for measuring heat transfer. The heat transfer coefficient is determined using the same approach as described in prior published papers [8]. A key difference in the test is that unlike the orifice jet, the ATF for the planar fan jet is not limited to impingement on the target surface.

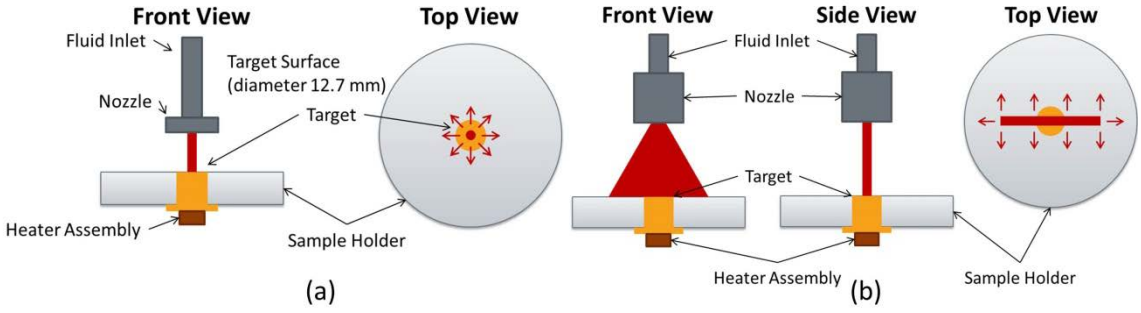

Figure 2-33: Test setup for circular orifice ATF jet (a). Test setup for planar fan jet (b).
Image Source: NREL

The assembled test apparatus is shown in Figure 2-34. The jet nozzle-to-target distance was fixed at 25.4 mm. The spray angle of the fan jet was dependent on the flow rate through the nozzle, as shown in Figure 2-34. Higher flow rates result in a larger spray angle. Depending on the spray angle, a portion of the ATF does not impinge on the 12.7-mm-diameter target surface used to measure heat transfer. For this reason, only a portion of the fluid is used to remove heat. The potential advantage of the planar fan jet is the ability to remove heat over a larger surface, such as a motor end winding.

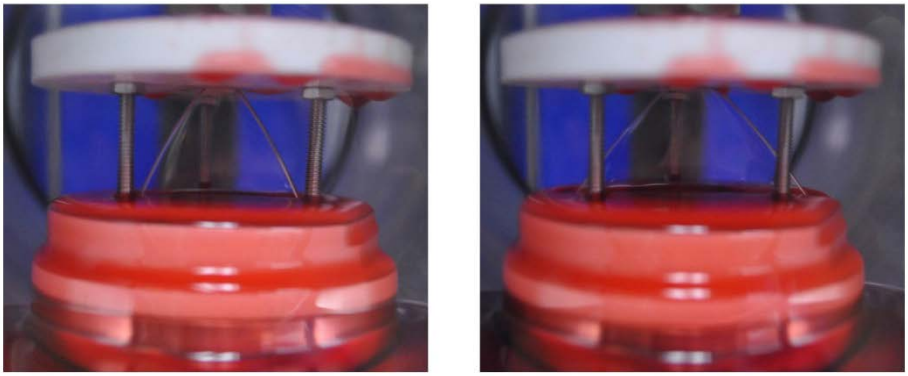

Figure 2-34: Flow rate of 0.6 L/min led to 58° spray angle (left). Flow rate of 1.0 L/min led to 78° spray angle (right).
Photo Credit: Xuhui Feng, NREL

The results of the planar fan jet test results are shown in the left graph of Figure 2-35. The heat transfer data can be compared with the data published for the orifice nozzle [8], shown in the right graph of Figure 2-35. For the same volumetric flow rate through the nozzle, the heat transfer coefficient averaged over the 12.7-mm-diameter target is higher for the orifice nozzle as compared to the planar fan jet. However, as mentioned previously, not all of the ATF impinges on the target surface for the planar fan jet. The advantage of the planar fan jet is the ability to impinge over a larger area. Figure 2-36 shows graphs comparing the heat transfer coefficient versus the fluid parasitic power, which includes the volumetric flow and the pressure drop. As seen in Figure 2-36, the difference in the heat transfer coefficient for the two tested nozzles is not as large for equivalent parasitic power.

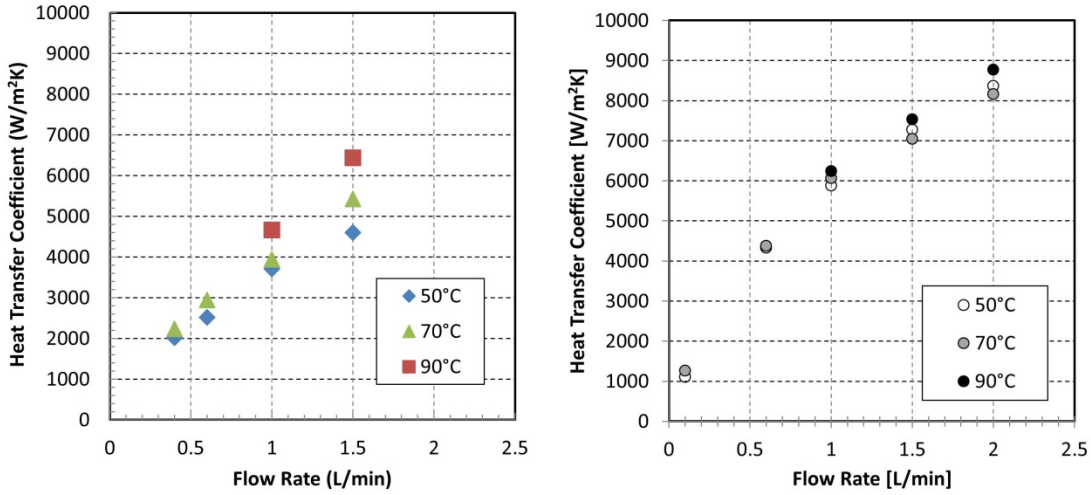

Figure 2-35: Average heat transfer coefficient versus flow rate measured over 12.7-mm-diameter target surface for planar fan jet (left) and orifice jet (right).
Image Source: NREL

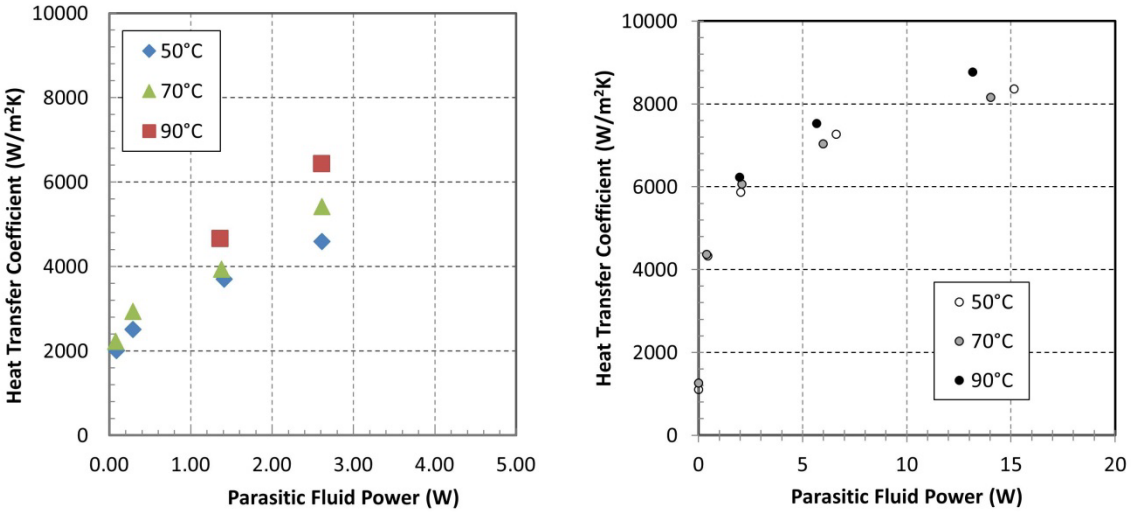

Figure 2-36: Average heat transfer coefficient versus parasitic power measured over 12.7-mm-diameter target surface for planar fan jet (left) and orifice jet (right).
Image Source: NREL

The ability to measure the spatial variation of the heat transfer coefficient over a larger area required construction of a larger test section for stator-scale ATF thermal measurements on motor end-windings. The image on the left of Figure 2-37 illustrates the goals of the experimental setup. The experiment was designed to enable the measurement of heat transfer on multiple surfaces of the motor end winding while allowing for the relative position between the heat transfer sensor and fluid jet impingement zone to change. Unlike prior measurements, the fluid jet is not constrained to be in a fixed location relative to the heat transfer sensor location. The experimental setup allows for the study of nozzle location, nozzle type, jet interactions, flow rates, gravity, and alternative cooling designs along the inner diameter, outside diameter, and outside edge of the motor end winding. The image on the right of Figure 2-37 shows the operating experimental setup with the orifice type nozzle spraying ATF on the heat transfer sensor installed in the motor end winding. The comparison of the orifice type jet and the planar jet is part of ongoing work.

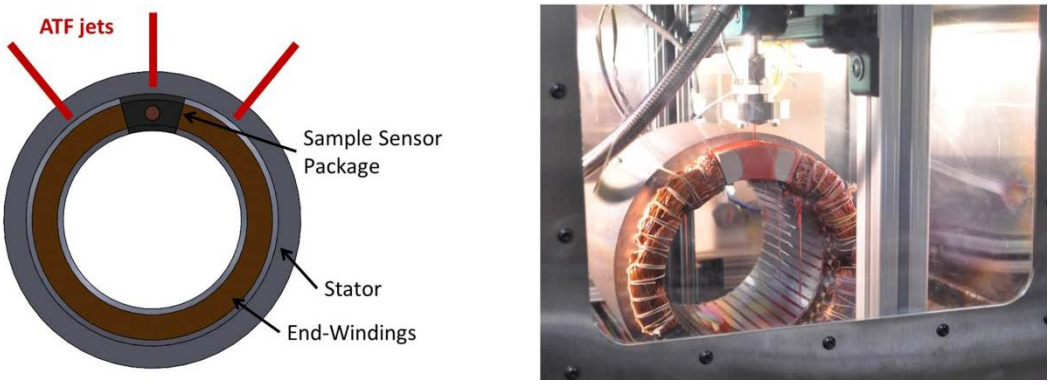

Figure 2-37: Illustration of sensor package installed in end-winding (left), sensor package installed in motor and ATF impinging on target surface (right).
Photo Credit: Kevin Bennion, NREL

Conclusions and Future Directions

Past work in the area of active convective cooling provided data on the average convective heat transfer coefficients of circular orifice ATF jets impinging on stationary targets intended to represent the wire bundle surface of the motor end-winding. The work during FY16 focused on the impact of alternative jet geometries that could lead to improved cooling over a larger surface of the motor winding. Results show that the planar jet heat transfer coefficients over a small (12.7-mm-diameter) target surface are not too much lower than the circular orifice jet in which all of the ATF from the jet impinges on the target surface. The planar jet has the potential to achieve higher heat transfer over a larger area of the motor end winding. A new test apparatus was

constructed to measure the spatial dependence of the heat transfer relative to the jet nozzle over a larger area representative of a motor end-winding. The tested planar flow geometry has the potential to provide more uniform cooling over the full end-winding surface versus the conventional jet configuration. The data will be used by motor designers to develop thermal management strategies to improve motor power density.

The area of passive thermal design saw the completion of work in collaboration with ORNL to measure the thermal conductivity of wire bundle samples representative of end-winding and slot-winding materials. Multiple measurement techniques were compared to determine which was most suitable for measuring composite wire bundle samples. NREL used a steady-state thermal resistance technique to measure the direction-dependent thermal conductivity. The work supported new interactions with industry to test new materials and reduce passive-stack thermal resistance in motors, leading to motors with increased power density.

The work in the area of material characterization was performed in collaboration with Ames Laboratory. The work focused on measuring the transverse rupture strength of new magnet materials developed at Ames. The impact of the improved transverse rupture strength is a mechanically stronger magnet that is easier for manufacturers to implement into motor designs. The thermal conductivity of the new magnet materials was also measured in comparison to two commercially available AlNiCo magnet materials. The impact of the thermal conductivity of the magnet material would need to be analyzed in the context of a motor application.

FY 2016 Presentations/Publications/Patents

1 Bennion, K. "Power Electronics Thermal Management Research." 2016 DOE VTO Annual Merit Review, Washington D.C., June 2016.

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References

1. T. A. Lipo, Introduction to AC Machine Design, 3rd ed. Wisconsin Power Electronics Research Center, University of Wisconsin, 2007.
2. J. R. Hendershot and T. J. E. Miller, Design of Brushless Permanent-Magnet Motors. Oxford, UK: Magna Physics Publishing, 1994.
3. "Standard Test Method for Transverse Rupture Strength of Powder Metallurgy (PM) Specimens." ASTM B524-12, ASTM International, West Conshohocken, PA.
4. "Standard Test Method for Thermal Diffusivity by the Flash Method." ASTM E1461, ASTM International, West Conshohocken, PA, 2013.
5. "Transient Plane Heat Source (Hot Disc) Method." ISO 22007-2, International Organization for Standardization, Geneva, Switzerland, 2008.
6. "Standard Test Method for Thermal Transmission Properties of Thin Thermally Conductive Solid Electrical Insulation Materials." ASTM D5470, ASTM International, West Conshohocken, PA, 2012.
7. R. H. Dieck, Measurement Uncertainty: Methods and Applications. ISA, 2007.
8. K. Bennion and G. Moreno, "Convective Heat Transfer Coefficients of Automatic Transmission Fluid Jets with Implications for Electric Machine Thermal Management," in ASME 2015 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems and ASME 2015 12th International Conference on Nanochannels, Microchannels, and Minichannels, San Francisco, CA, United States, 2015.

2.4 Brushless and Permanent Magnet Free Wound Field Synchronous Motors for EV Traction

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Abstract/Executive Summary

- Rare-earth permanent magnets (PMs) have been subject to market volatility and are largely single sourced from a foreign power. Permanent magnets in EV traction interior permanent magnet synchronous motors (IPMSMs) are a significant fraction of the cost and impose temperature limitations.
- Additionally, the PMs provide a fixed flux level which is always, "on", leading to safety concerns during inverter faults and requiring additional current to be injected into the machine during field weakening to buck the magnetic flux. This additional current lowers the power factor of the machine, requires that the traction inverter be oversized to supply the reactive current, and leads to increased ohmic losses in the stator and inverter. Induction machines (IMs) must also draw reactive current from the traction inverter to magnetize the machine.
- Wound field synchronous motors (WFSM) are a potentially advantageous alternative to commercially dominant IPMSMs and IMs for electric vehicle traction due to the following properties.
  - Permanent magnet free
  - Complete control of the field excitation with potential for optimal field weakening and loss minimization
  - Field magnetization can be drawn from the rotor side increasing the power factor of the machine
- EV traction applications require extremely high reliability and power density inhibiting the use of brushes and other classical field power transfer technologies such as brushless exciters. Capacitive power transfer (CPT) technology offers an attractive means of providing brushless power transfer to the rotor field windings.

Accomplishments

- A rapid WFSM magnetic and thermal design optimization environment has been created.
- Two capacitive power coupler (CPC) systems were designed and constructed; one for low speed (oil film journal bearing style) and one for high speed operation (air-gapped parallel plates).
- High performance WFSM prototypes were designed, prototyed, and experimentally characterized with brushes and slip rings and brushless capacitive power couplers (CPC).
  - The peak volumetric and specific torque and power density exceeded USDRIVE 2020 targets
  - The prototype machine exhibited a broad band of very high efficiency (>95%) and high power factor.
  - Operation with the air-gapped paralleled plates CPC was demonstrated to 55 kW power output at 4000 RPM.
- Kilowatt scale, 2 MHz switching CPC power electronics driver demonstrated.
- Voltage and field current regulation during generator operation was demonstrated with a journal style bearing CPC.
- A new prototype rotor has been designed which further increases the torque and power densities while lowering field winding power transfer requirements.

Introduction

This project will design, prototype, and demonstrate a brushless and permanent magnet free wound field synchronous motor (WFSM) for EV traction. The rotor field winding will be excited using non-contact capacitive power transfer (CPT) technology. In an EV traction application, a brushless and permanent magnet free WFSM would have several significant benefits and advantages over state-of-the-art interior permanent magnet synchronous motors (IPMSMs) and induction motors (IMs) including reduced cost through the removal of rare earth permanent magnets, higher system and machine efficiencies though power factor improvements and loss minimization field control, improved safety through field control during inverter fault conditions, and the possibility for power take-off and microgrid support. The key enabling technology for this project is the CPT technology which allows brushless operation of the WFSM.

IPMSMs and IMs are the commercially dominant electric motor types used in EV traction motor/generators. Compared to IPMSMs and IMs, WFSMs offer several advantages. Field weakening for a large constant power speed range (CPSR) can be achieved with the proper design of the IPMSM, i.e. the magnet flux can be bucked by the d-axis armature flux. This is a non-ideal solution however as the flux produced by expensive rare-earth permanent magnets is being bucked by injecting a large reactive current, -Id, into the machine, also reducing the power factor. To achieve this, the traction inverter kVA rating must be oversized increasing the cost and size of the entire EV electric drive. The DOE has estimated that the power factor of IPMSM increases the cost of the traction inverter by 15% [1].

The main defining feature of WFSM is the complete control of the field excitation from the rotor side. Near unity power factor and optimal field weakening can be achieved over the entire torque-speed range because of the direct handle on the field excitation. This control reduces stress on the inverter and other electronic components because additional reactive power for field weakening is not necessarily cycled through the inverter. The efficiency of the inverter increases and the inverter cost and volume can be minimized. The complete control of the field excitation in WFSM also brings other advantages including an extra control input for loss minimization at both a machine and system level.

Given the potential advantages of the WFSM in traction applications, why has it not seen wide spread use? Historically, power has been provided to the WFSM field winding using three methods: slip rings, brushless exciters, and rotating transformers. Recently three other brushless methods of transferring power to the rotor field winding have been developed: harmonic, inductive and capacitive power transfer. Slip rings, while being a well understood technology, are not suited to an automotive environment because of reliability and maintenance concerns (brushes need to be changed and introduce brush dust). Brushless exciters and rotating transformers add significant weight and shaft length to the overall machine. Power transfer of brushless exciters and rotating transformers is also speed dependent and introduces extra system dynamics (L/R time

constant). Circuit representations of inductive and capacitive power transfer systems are shown in Figure 2-38. Compared to inductive power transfer, CPT technology can operate at higher speeds and efficiency. CPT has similar system dynamics to slip rings. Other CPT advantages include rotor current sensing on the stator side and bearing current reduction or removal. The key enabling technology for leveraging the attractive attributes of WFSM as EV traction motors is the CPT.

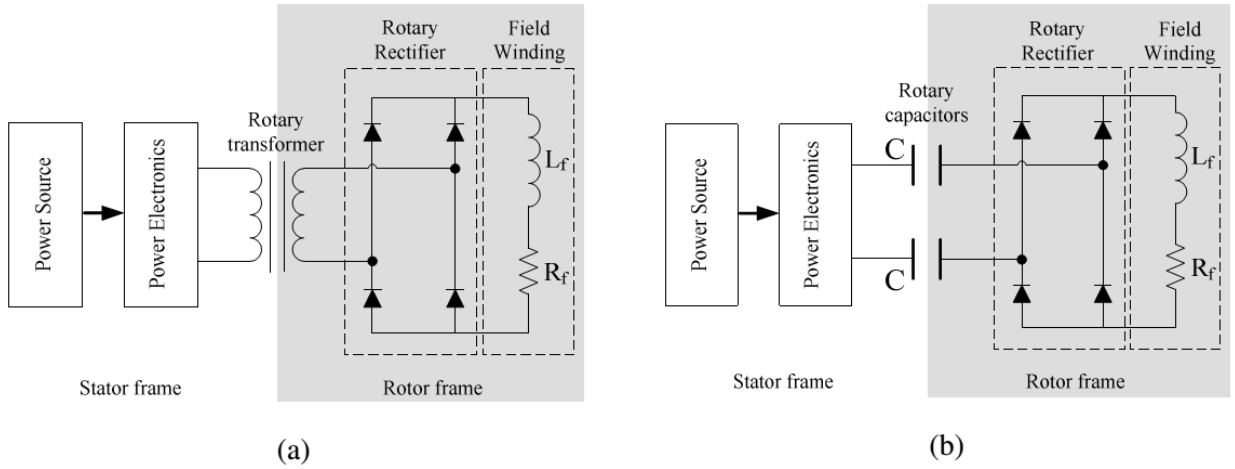


Figure 2-38: Circuit representation of field coupling for brushless: (a) inductive and (b) inductive couplers

Approach

To design a high performance EV traction WFSM prototype using CPT for rotor field excitation, a flexible design environment has been developed. An electromagnetic, thermal, and mechanical, thermal parametric WFSM model has been employed to explore the design space, and an optimization algorithm to find the best candidate for realization.

Development of WFSM Multi-Objective Optimization Environment

To rival or exceed the performance of state of the art IPMSMs in WFSMs, a combined electromagnetic and thermal multi-objective design optimization code was developed. The optimization code integrates a number of features that allow for automated operation and comprehensive exploration of the design space. A centralized MATLAB interface to different simulation packages has been developed using ActiveX commands to control the behavior of third-party software such as FEMM, Infolytica MagNet and Motor-CAD. A graphic illustration of the interaction is shown in Figure 2-39(a). The centralized interface allows for parametric rotor and stator geometry generation, material assignment, current loading and selection between static and transient magnetic simulations. After the simulations are carried out with external packages, the data conditioning and performance evaluation routines are executed in the MATLAB environment as part of the full population based optimization using the differential evolution algorithm. The resulting geometry and losses can be exported to the Motor-CAD package for thermal modeling. A considerable portion of the development effort was devoted to parallelization, with multiple simulation instances, to speed up the optimization process. Attention and care was paid to ensure that the electromagnetic simulation packages (FEMM and MagNet) have comparable results through control of the meshing and material properties. Critical to the full exploration of the WFSM design space is the use of a parametric geometry engine using dimensional and non-dimensional geometric quantities (stator and rotor) which does not allow non-physical geometries to occur when using a population based design optimization algorithm. The developed geometry engine allows for points to merge and collapse.

To determine rotor structural limits, finite element stress analysis was carried out using a central composite design of experiments approach with five rotor dimensional variables in Solidworks. The Von Mises stress, safety factors, and displacement were computed at 12,000 RPM (targeted maximum rotor speed) and 15,000 RPM. A representative stress analysis simulation is shown in Figure 2-39(b). The rotor laminations were initially modeled as an anisotropic combination of Voigt and Reuss composites in the radial and axial directions respectively [2]. In addition to the determination of maximum ranges for the five rotor dimensional

variables, the response surface calculated as a least squares linear regression was added as a rotor stress and safety factor estimate to the geometry generation routine. The resulting response surface sets the constraints that allow any final optimization results to meet a stress safety factor of 2.0 at the maximum design speed.

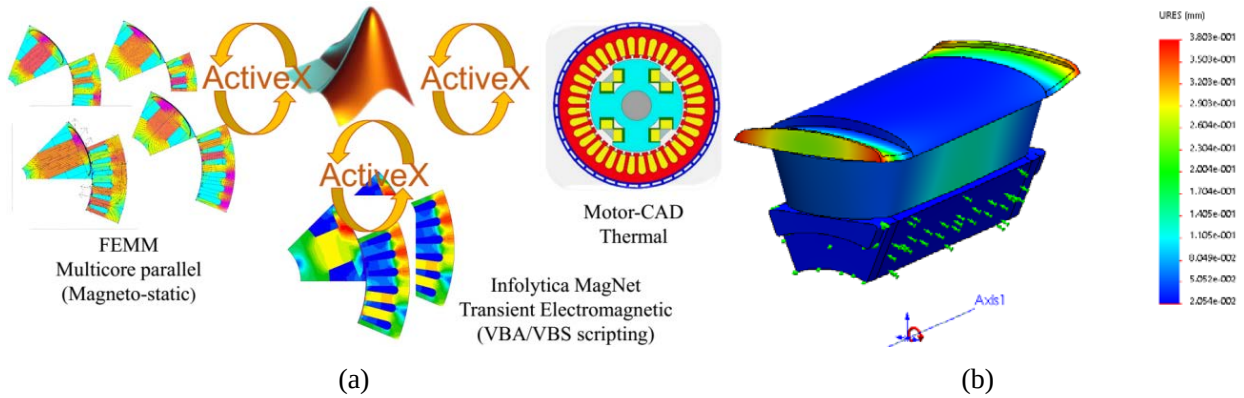


Figure 2-39: WFSM (a) multi-objective optimization environment with ActiveX software interfaces between solvers and (b) representive rotor stress analysis.

WFSM Prototypes 1 and 2 Design and Optimization

WFSM specifications for peak output power, continuous output power, specific power density, and volumetric power density were developed in consultation with DOE USDRIVE targets, Table 2-3. A base speed of 4000 RPM was selected along with a target constant power speed range of three (corresponding to 12,000 RPM).

The stator outer diameter was constrained based on typical packaging constraints in an automotive application and to fit the dynamometer available for experimental characterization. An additional minimum stator inner diameter constraint was imposed to allow the CPT to nest inside the stator end turns if desired. The CPT also imposed several constraints on the rotor field winding including a maximum rotor field winding power transfer of >2 kW, field winding terminal current of 7 A, and minimum field winding terminal voltage of 200 V. After extensive test runs of the optimizer to identify the most feasible initial topology a 48 slot 8 pole single layer winding design was selected compatible with automotive mass production. Using the differential evolution optimization method with extensive test runs showed that hard constraints act as additional objectives as long as a suitable population is found, and in general, it has been observed that adding hard constraints speed up convergence more than increasing the number of optimization objectives. The final optimization runs for the prototype 1 and 2 geometries had 14 input parameters including dimensional geometric, non-dimensional geometric and physical variables. Two optimization objectives were used to maximize the torque density and "goodness" (average electromagnetic torque divided by the square root of the losses). Additionally 7 hard constraints were imposed: torque ripple <5%, minimum average electromagnetic torque >140 Nm, maximum average electric torque <150 Nm, maximum rotor ohmic losses <2.5 kW, maximum stator total losses < 6 kW, stator current density 15 - 30 A/mm^2, and rotor current density of 15 - 25 A/mm^2. A graphical projection of the results on an inverse torque density versus "goodness" plane of the full population represented by black dots (7,500 total members) and only the designs that meet ripple and rotor loss constraints are shown in Figure 2-40(a) and Figure 2-40(b) respectively. The yellow dot represents the design selected for prototyping and experimental characterization.

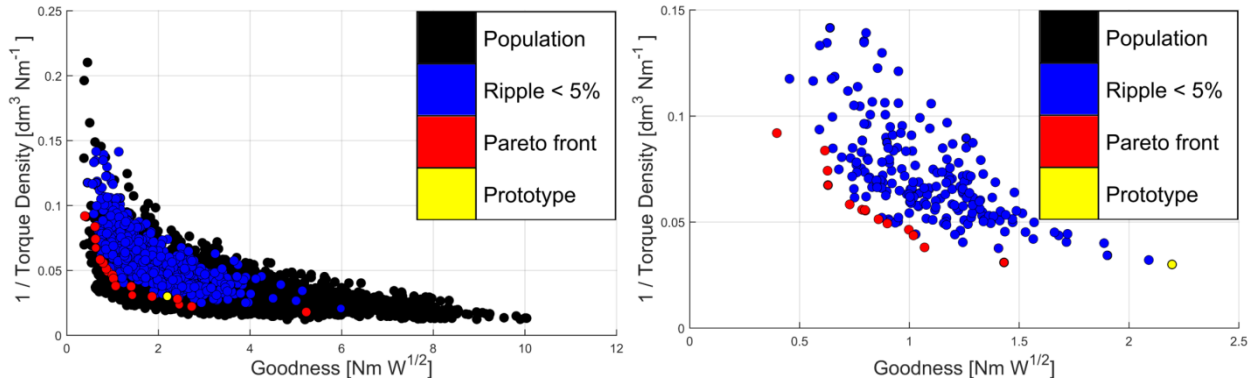


Figure 2-40: Optimization results for the design of prototypes 1 and 2 shown for the (a) total 7,500 member population and (b) designs which meet torque ripple and rotor loss constraints. The yellow dot indicates the design selected for prototyping.

For the selected design finite element stress analysis was carried out using an updated material model obtained by ultrasonic measurements of electrical steel test coupons. Filets were added to the most stressed sections of the rotor to produce a minimum safety factor of 1.5 at 15,000 RPM. Additional magnetic finite element analysis found that the addition of the filets did not adversely affect the electromagnetic power conversion performance.

To predict the WFSM performance and design, the stator and rotor windings, torque and voltage maps as a function of current angle, stator current density, and rotor current density were generated for the base speed, 4000 RPM, and the maximum constant power speed, 12,000 RPM. Based on these maps, the maximum torque per amp current angle (base speed) and the maximum torque per volt current angle (maximum constant power speed) were determined and used to select the number of turns based on the electric drive terminal voltage and current limitations while reaching the required torque output. The wire gauge and strands in hand were selected to maximize the achievable slot fill when using hand insertion. The stator winding design is a compromise between a maximum voltage at 3:1 constant power speed ratio of 350 V (limited by the inverter peak phase voltage) and a maximum stator terminal current of 300 A at the base speed. The resulting stator winding is 4 turns per coil, 10 AWG 16 strands in hand per turn, 2 slot per pole per phase distributed winding.

The CPC resonant class E inverter required the field resistance to be in the range of 20 to 45 Ω at the nominal voltage of 300 V for the entire possible operating temperature range of the WFSM, 20 to 19°C. In addition, structural modeling had shown that a wire size of at least AWG 24 must be used to guarantee structural integrity at high speed and temperature. Given these constraints, the rotor winding with 239 turns per pole of AWG 21.5, for which the rotor resistance remains in the range of 26 to 45 Ω over the operating temperature range, was designed. With the winding defined, predicted machine electrical parameters were calculated. The predicted torque map is shown later in Figure 2-42. The predicted efficiency maps at a winding temperature of 70°C are shown as a function of speed for peak efficiency, Figure 2-41(a), and as a function of field and stator currents at the maximum torque angle at 4000 RPM, Figure 2-41(b).

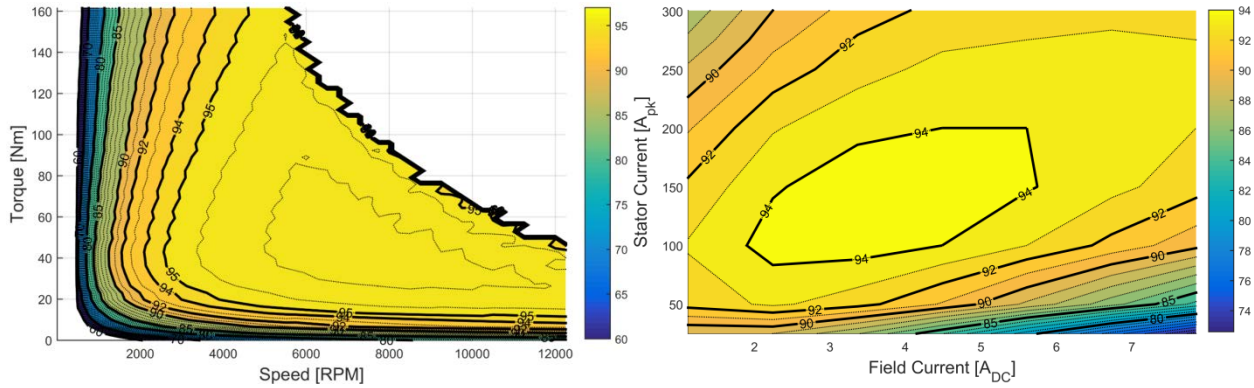


Figure 2-41: Predicted prototypes 1 and 2 efficiency with a winding temperature of 70° C versus (a) speed and torque for peak efficiency and (b) as a function of field and stator currents at the maximum torque angle at 4000 RPM.

WFSM Prototypes 1 and 2 Construction

Two wound field synchronous machine prototype designs have been constructed. The first prototype was found to have a distorted stator inner diameter resulting in a stationary saliency. The unintended saliency made regulation of the stator currents very difficult. The second prototype stator and rotor lamination stacks were laser cut, annealed, and unitized using laser welding from M15 29 Ga (stator) and M250-35A steel (rotor), Figure 2-42. Winding and insulation materials were selected for automatic transmission fluid (ATF) compatibility and class H, or higher, thermal performance. Twenty type T thermocouples were embedded in the stator for thermal characterization. To retain the rotor windings at 12,000 RPM, with potentially high rotor winding temperatures and avoid ATF degradation, rotor endcaps were machined from polyether ether ketone (PEEK). To further ensure rotor winding retention, Kevlar fiber banding was used as an overlay on a rotor endcap shelf. The shaft in the prototypes was oversized compared to what would typically be used in an automotive application, allowing for iteration of the rotor design without loss of structural integrity. ATF spray cooling of the stator and rotor end turns was implemented using a relatively simple system of coiled copper piping with one closed end and the other connected to the pump and heat exchanger system. The spray holes consist of two sets of 16 1.15 mm holes offset by 30 degrees with one set cooling the rotor end winding and the other cooling the stator end windings. For the current prototype, the brushes and CPC are located external to the motor housing to allow for easy access during testing. The CPC housing is designed, however, to allow it to operate in an ATF spray environment inside the machine shell.

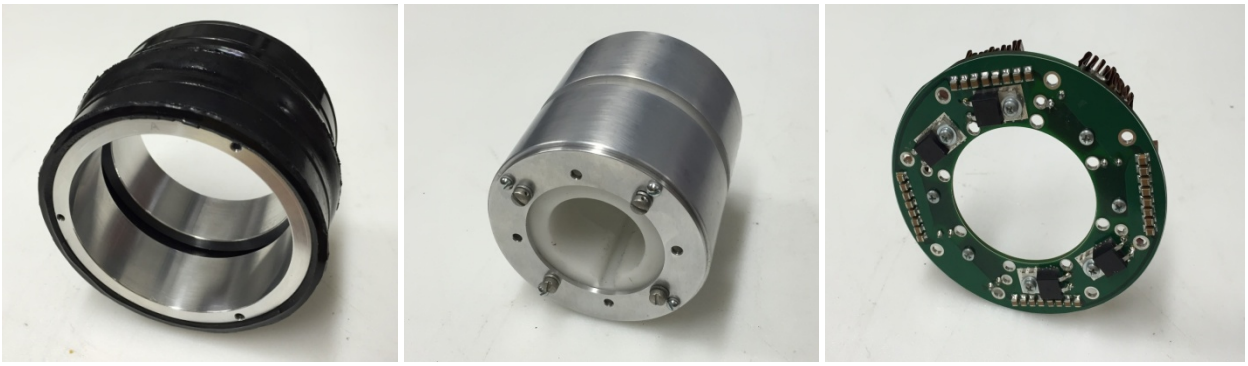
Figure 2-42: Wound field synchronous machine prototype

CPC Construction and Installation

Two styles of CPCs were designed and constructed. The first is a journal bearing type intended for synchronous generator applications. The second is formed by cascaded hydroflex plates for a WFSM traction motor and is the primary focus of the project.

Type 1: Journal Bearing CPC

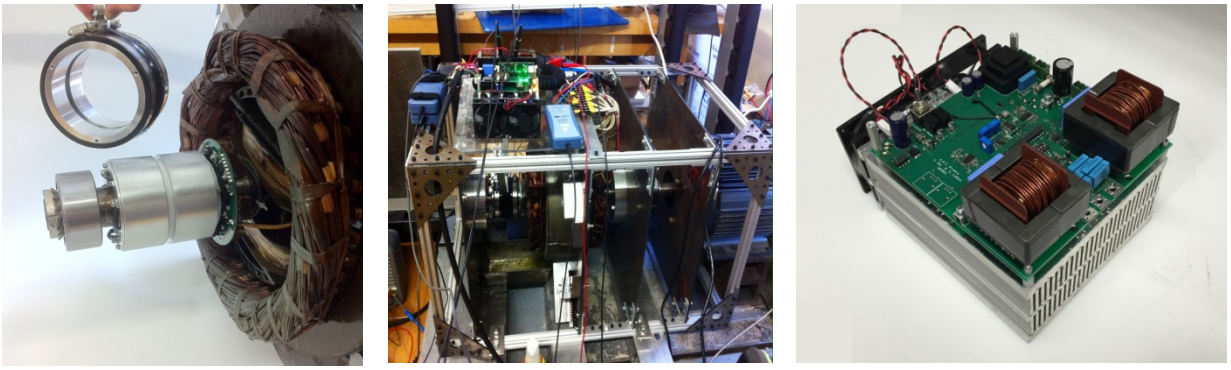
A rotating capacitive coupler, shown in Figure 2-43, was constructed with aluminum stator rings (a), and Parylene-coated aluminum rotor rings on a plastic hub (b). With a per-section capacitance of approximately 4 nF, the coupler was designed to achieve power transfer approaching 1 kW at a frequency of approximately 800 kHz to demonstrate the feasibility of transferring power to a rotor. A rotating diode bridge circuit (c) was installed on the same rotor hub to convert the high frequency alternating current passed through the capacitive coupler to direct current, as needed by the field winding of the bench test wound field synchronous machine (WFSM) on which the assembly was installed. Slip rings were provided on the opposite end of the WFSM rotor shaft to facilitate the connection of additional electrical load for the capacitive coupler, as well as allowing direct rotor field voltage measurements during generator operation.



(a) (b) (c)

Figure 2-43: Coupling capacitor stator (a), rotor (b), and rectifier board (c), which comprise the capacitive power coupler assembly.

The assembled capacitive coupler was installed on the WFSM rotor shaft, Figure 2-44(a), which was then coupled to the dynamometer prime mover and mounted on an open frame dynamometer (b). A high frequency inverter (c) was connected to the stator rings as input to the capacitive coupler.



(a) (b) (c)

Figure 2-44: Coupler mounted on WFSM rotor (a), dynamometer test stand (b), and inverter for capacitive power coupling to rotor (c).

Type 2: Cascaded Hydroflx plate CPCs

Additionally, a hydroflex coupling capacitor was also constructed per the original proposal. Here, the stator and rotor plates were water jet cut from 0.016" thick 6061 aluminum stock. These plates are pictured in Figure 2-45. The rotor plates are coated with parylene, a transparent dielectric, to ensure galvanic isolation at zero speed. These plates were then alternately stacked, 4 stators and 3 rotors, 0.001" apart, onto a dynamometer test stand to evaluate the resulting capacitance verses speed curve. The entirety of the hydroflex plate test dynamometer stand is pictured in Figure 2-46.

Figure 2-45: (left) stator plate, (right) rotor plate.

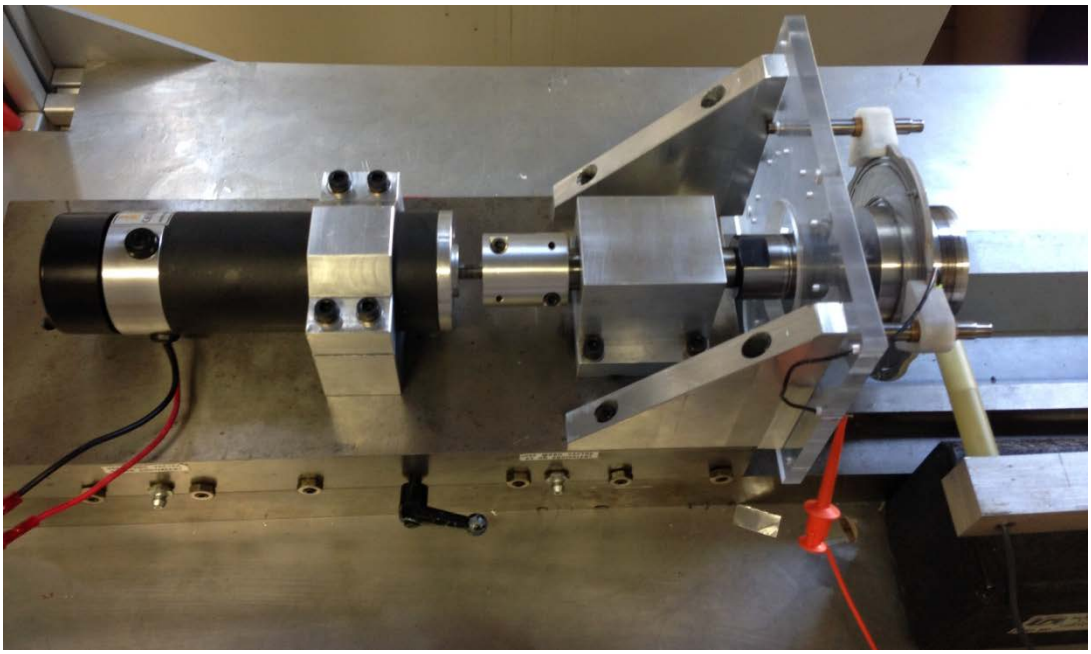
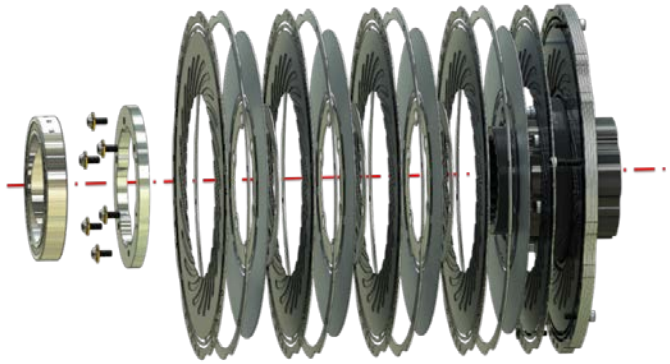


Figure 2-46: Photo of the hydroflex plate stack on a small dyne bed

Prior testing verified that a WFSM using brushes and slip rings to excite the rotor satisfies project power, torque, weight and volume metrics. Next, the brushes and slip rings were replaced with a CPC, to demonstrate that WFSM and CPC paired together can function at 55kW power levels in a traction application. The CPC was built by cascading multiple hydroflex plates, as seen in Figure 2-47. The engineering behind plates such as these is presented in [3]. The plates were laser cut from 6061 aluminum. Rotor plates were hard coat (type 3) anodized to create a dielectric boundary layer and dry lubricant for start up conditions. The assembled CPC on the WFSM and dynamometer is pictured in Figure 2-47.

The CPC relies on power electronics to synthesize high frequency AC voltage that can drive current through the CPC. High frequency, ~MHz scale, is required to push current onto the rotor as the coupling capacitance is small (nF) and low frequencies would otherwise be impeded. The circuit of choice in this case, was a push-pull class E amplifier whose circuit schematic and photos are presented in Figure 2-48.



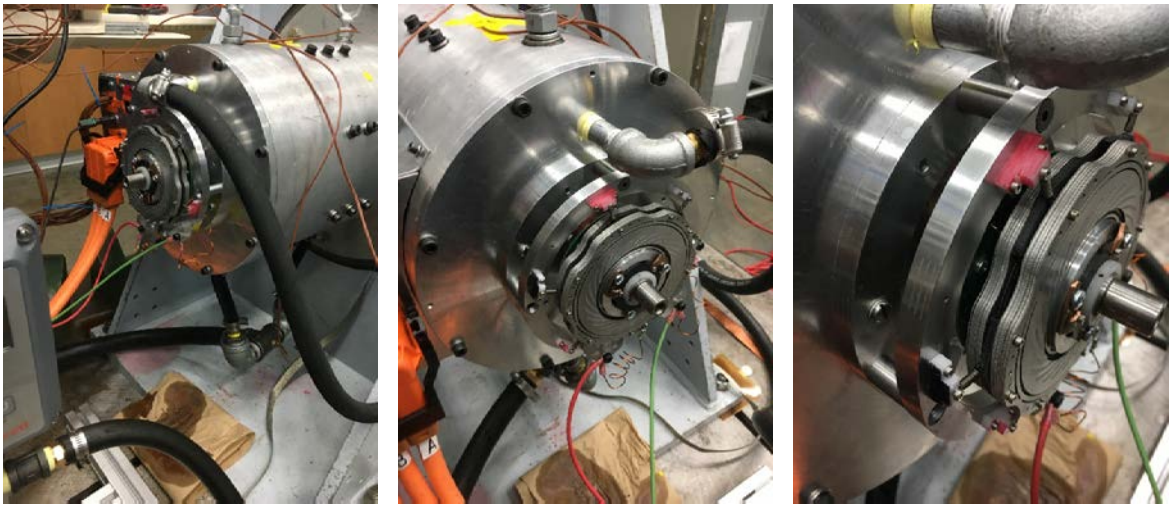
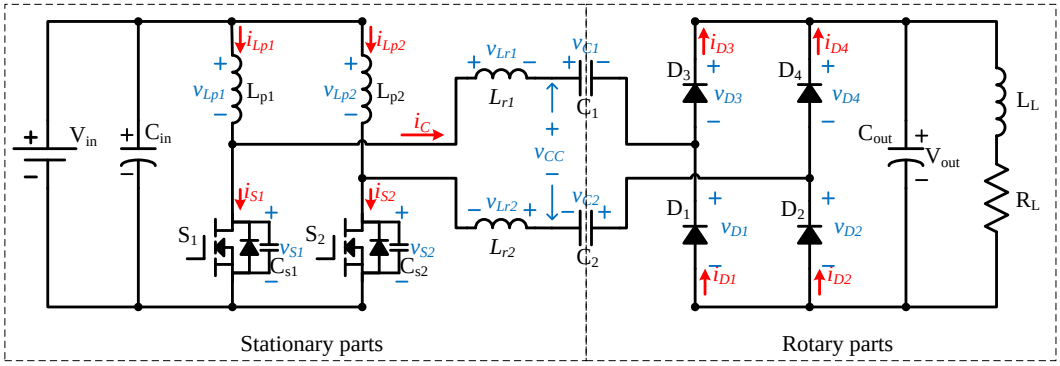


Figure 2-47: Top - Exploded View of Capacitive Power Coupler (CPC) assembly, Bottom - photos of CPC assembled and installed on WFSM rear shaft.



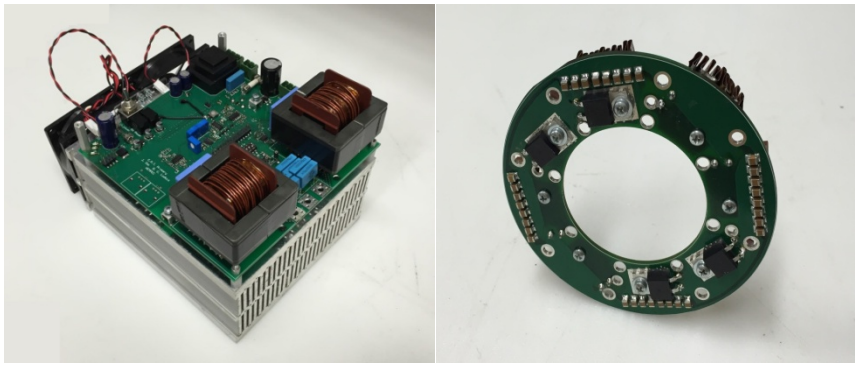
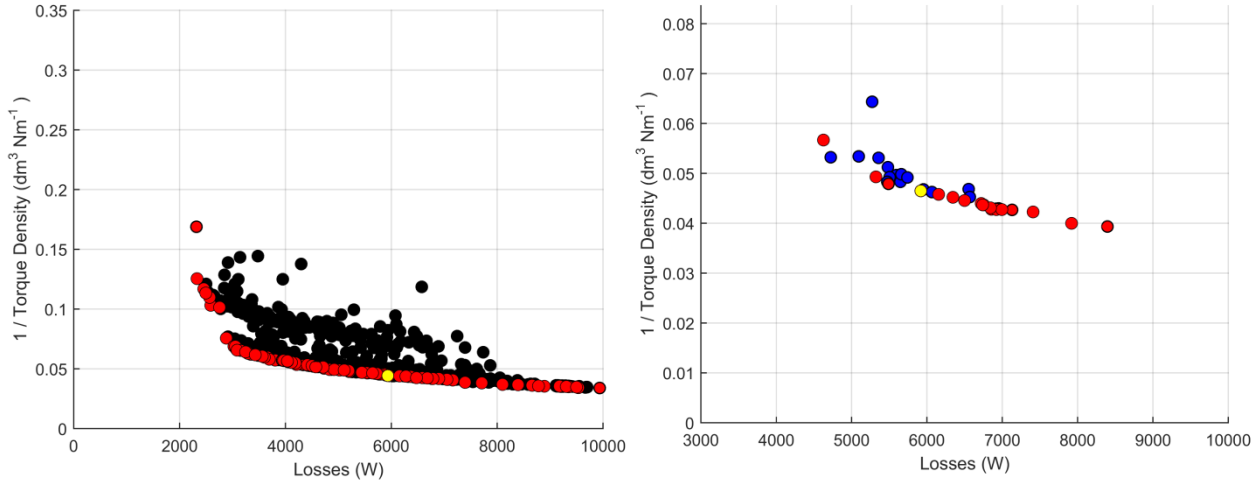


Figure 2-48: Top - Circuit Schematic for the CPC push-pull class E driver, Bottom - photos of push-pull Class E driver (left) and rotating rectifier board (right)

WFSM Prototype 3 Rotor Design

To gauge the impact of rotor flux barriers on WFSM performance, new rotor geometric templates were developed which include the addition of flux barriers in the rotor pole neck and the rotor pole shoe. Additionally a new rotor pole shaping algorithm was developed. Extensive optimization studies were carried out using the new rotor geometric templates and pole shaping algorithms for a range of electrical steel grades. To design a third rotor prototype with reduced field power requirements and increased torque density, a new optimization study was completed using the new rotor pole surface and wider geometric parameter ranges. The design that was selected from the Pareto front served as a base or seed design for the inclusion of flux barriers in a second Monte Carlo study where only flux barrier geometric and current density parameters were varied. This was termed an extended optimization. The new base speed design without rotor flux barriers, is the yellow dot in Figure 2-49. The cross-sections of the base design for the extended optimization (yellow dot), and the design selected for prototype rotor 3 with a moderate size flux barrier are shown in Figure 2-50 with the full load flux density shaded and magnetic field lines shown. The final lamination design for the prototype rotor 3 is shown on the right side of the same figure. The full load torque produced by this design is substantially higher than the current prototype 2 with substantially lower required field power. The rotor prototype 3 is currently under construction.



(a) (b)

Figure 2-49: New design optimization for selection of seed design for inclusion of flux barriers ; (a) full optimization population with design selected as seed design highlighted in yellow and (b) designs filtered which meet all hard constraints.

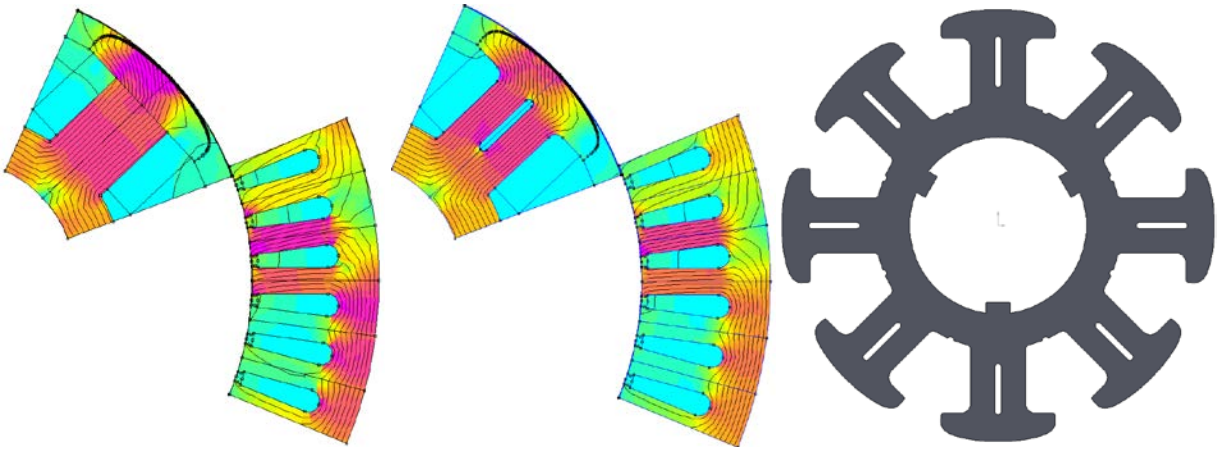


Figure 2-50: Base rotor design for extended optimization (left), rotor design selected for prototype 3 rotor after adding stress relief filets (center), and lamination design (right).

Dynamometer Testing of Wound Field Synchronous Machine Prototype 2

The WFSM prototype 2 performance was measured with both slip rings/brushes and CPC on a 180 kW Anderson Electric Controls dynamometer with a 1000 Nm HBM T40 torque flange, Figure 2-51. The prototype WFSM stator was driven by a Semikron Semikube IGBT Module Stack IGD-20424-P1N6-DH-FA inverter. A custom DSP board, based around the Spectrum Digital TI F28335 DSP, was designed to control the inverter, regulate currents in the WFSM, and perform field oriented control. To regulate the stator currents, a discrete-time complex vector current regulator has been implemented to decouple the stator cross-coupling.

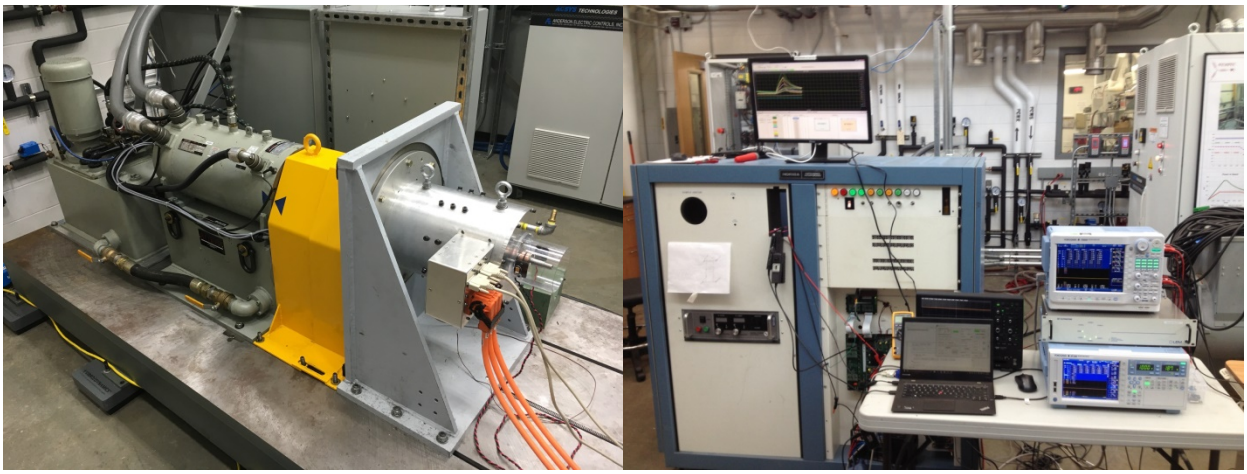


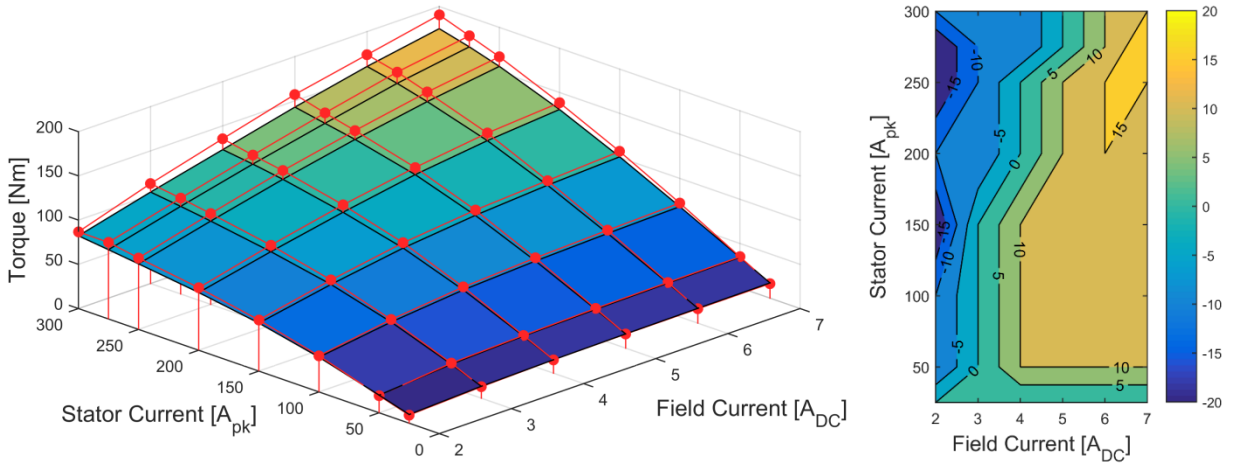
Figure 2-51: Dynamometer setup during wound field synchronous machine testing with brushes/slip rings.

For testing with slip rings/brushes, the field winding was connected to a Magna-Power PQ500-20 DC power supply through an added snubber circuit and diode to protect the power supply in the case of excessive field transients. The WFSM and drive efficiency were measured using Yokogawa WT1800 and PX8000 power analyzers when tested with slip rings/brushes. Stator phase currents were measured using Yokogawa 96031 current probes and LEM Ultrastab systems connected to the WT1800 and PX8000, respectively. Field current and voltage were measured both by the power analyzers and captured on a LeCroy HDO6034-MS. WFSM efficiency was measured during testing with the field excited by the CPC using a WT1800. CPC converter DC input voltage and current were measured with the power analyzer, and the CPC primary side switching current and voltage waveforms were captured on the LeCroy HDO6034-MS. To record the stator, case exterior, and ambient temperatures a 20 channel Agilent thermocouple reader was used.

WFSM prototype 2 dynamometer torque, efficiency, and power factor mapping was carried out for a range of field currents, stator current magnitudes, and current angles at 1000, 2000, 3000, and 4000 RPM. The mapping was carried out within a stator temperature range of ~35 to ~70 °C. The torque, current angle for maximum torque, machine efficiency (at 4000 RPM), and power factor (at 4000 RPM) mapping results for operation with slip rings are shown in Figure 2-52 and Figure 2-53. The predicted and measured torque maps agree closely. The higher experimental versus predicted torques at high field and stator currents is most likely due to lack of detailed BH curve data at high saturation levels. The measured efficiency map shows a very broad high efficiency band with >95% efficiency. The measured efficiency map corresponds well with the predicted efficiency map in Figure 2-41(b). The power factor map at 4000 RPM, Figure 2-53, shows the power factor at the current angle for maximum torque which is not necessarily the current angle for maximum power factor. The power factor is quite high over the lower half of the map.

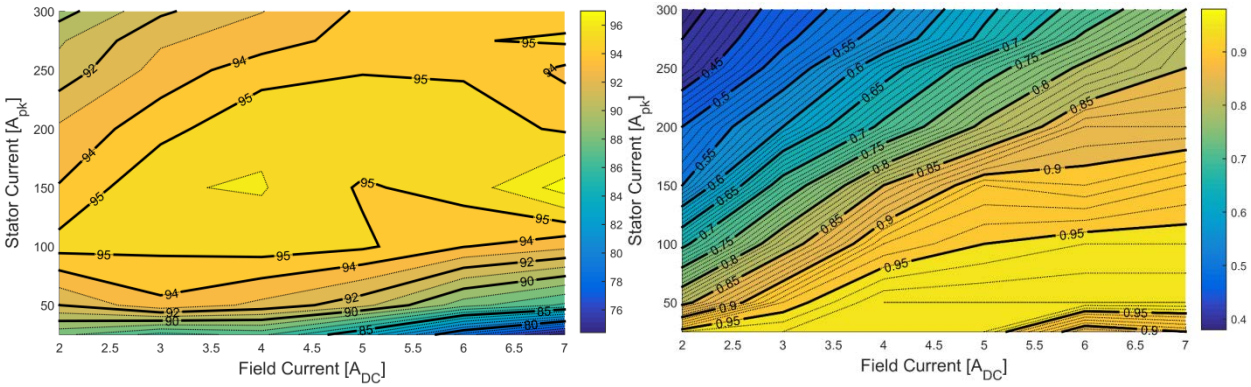
The WFSM performance metrics using slip rings and brushes are listed in Table 2-3 and compared to USDRIVE 2020 and predicted design values. The measured performance significantly exceeds USDRIVE 2020 targets without the use of permanent magnets. The peak power output can also be held for more than 30 seconds. The higher measured than predicted performance is because of the thermal properties of the machine. The predicted performance limited the stator and rotor current densities to 18 and 17 A/mm^2 respectively.

Due to the effectiveness of the spray cooling system, significantly higher values of current density and terminal currents were achievable resulting in very favorable peak volumetric and specific torque and power densities that compare favorably with commercial IPMSMs and IMs. The specific power density metrics would be further improved by the use of a shaft more appropriately sized for the application. Compared to the USDRIVE target of 55 kW peak power output, a peak measured power output of 79.6 kW was achieved.



(a) (b)

Figure 2-52: Predicted and measured shaft torque mapping (a) for wound field synchronous motor prototype 2 (The surface is the predicted torque and red dots are measured on dynamometer) and the (b) maximum torque current angle.



(a) (b)

Figure 2-53: Measured wound field synchronous machine (a) efficiency and (b) power factor at 4000 RPM uising Yokogawa PX8000 power analyzer. The temperature of the stator windings ranged from 45 to 70 °C. The efficiency and power factor maps are for maximum torque current angles.

Table 2-3: Comparison of Experimentally Measured Wound Field Synchronous Machine Performance with USDRIVE 2020 and Predicted Design Values

Machine Parameters	USDRIVE 2020 Target	Predicted Design Value	Measured Value	Units
Peak Motoring Torque	-	141	190.55*	Nm
Peak Motoring Power at 4000 RPM	55	59	79.6	kW
Peak Motoring Efficiency	-	93.5	95	%
Mass	-	40.64**	40.64**	kg
Volume	-	11.06***	11.06***	l
Volumetric Peak Torque Density	5.7****	12.75***	17.22***	Nm/l
Specific Peak Torque Density	-	3.47**	4.69**	Nm/kg
Volumetric Peak Power Density	-	5.36***	7.19***	kW/l
Specific Peak Power Density	1.6****	1.45**	1.95**	kW/kg

* Held for over 30 seconds.
** Includes stator, rotor, and shaft mass (shaft is oversized)
*** Cylindrical volume of active materials plus ATF spray cooling rings
****Cylindrical volume of active materials

Relevant CPC voltages and current were measured during the 55kW load test. Measured voltages and current are plotted in Figure 2-54 and correspond to quantities labeled in the circuit diagram in Figure 2-48. From these waveforms, it is seen that the converter operates at 2MHz and soft switches (zero voltage switching) for low losses at high frequency. The CPC tank current is 6.5 A rms, which corresponds to a DC field current of about 5 amps when losses and parasitics are accounted for. Power analyzer data of the WFSM running with the CPC is pictured in Figure 2-55 as evidence for meeting the 55kW WFSM metric. The output power of the WFSM is plotted as well for different combinations of stator current (constant torque angle) and CPC tank current.

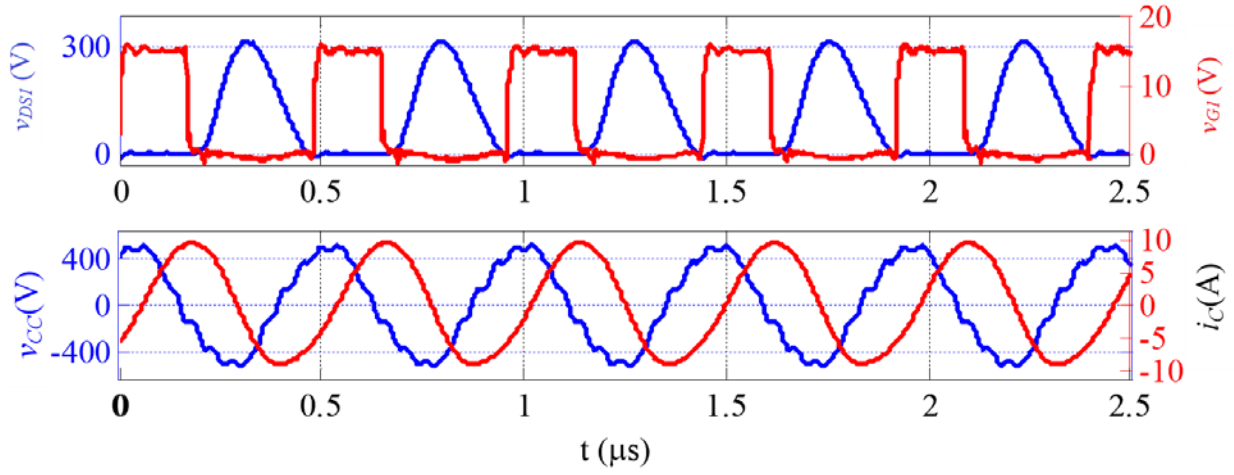
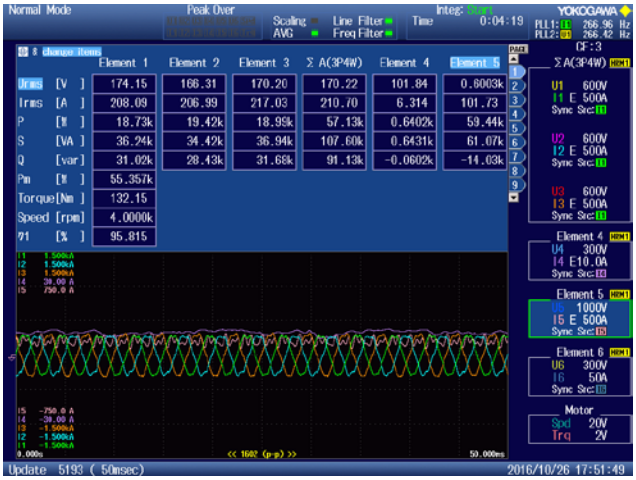


Figure 2-54: Top - Measured CPC circuit waveforms during 55kW WFSM test. 2MHz switching and 6.5 A rms CPC tank current. *note: labels correspond to circuit diagram.



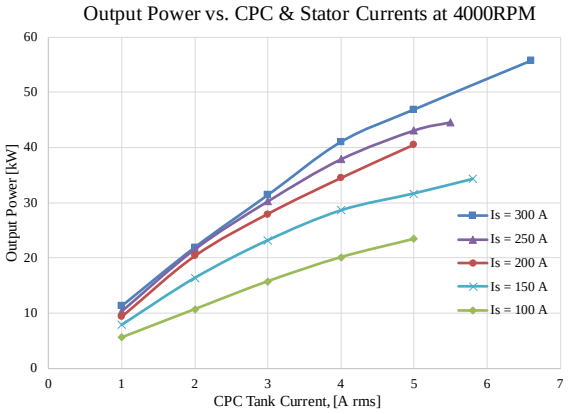


Figure 2-55: Screen capture of power analyzer during 55kW WFSM test with CPC (left), and WFSM output power verses stator and CPC currents (right).

Conclusions and Future Directions

A WFSM for EV traction with the rotor field winding designed to operate with a brushless CPT system has been designed, prototyped, and characterized. To achieve performance comparable to state of the art interior permanent magnet synchronous machines, a combined electromagnetic and thermal multi-objective design optimization program has been developed. Two capacitive power transfer couplers have been developed; one for low speed (oil film journal bearing style) and one for high speed operation (air-gapped parallel plates). These couplers are able to transfer >600 W of power from stationary to rotating components. Performance characterization of the WFSM with brushes and slip rings and the airgaped parallel plate style CPC has been carried out. The prototyped WFSM exhibits peak volumetric and specific torque and power densities exceeding DOE USDRIVE 2020 targets with a very broad band of high efficiency. Operation with the CPC has been demonstrated to achieve DOE targets of 55 kW output at 4000 RPM. A new rotor has been designed which should further increase the peak volumetric and specific torque density while lowering rotor power transfer requirements. The new rotor is currently under construction and will be tested in the coming months.

FY 2016 Presentations/Publications/Patents

1. Di Gioia, A., Brown I.P., Knippel R., Hagen S., Ludois D.C., Nie Y., Dai J.J., Alteheld, C., “Design of a Wound Field Synchronous Machine for Electric Vehicle Traction with Brushless Capacitive Field Excitation,” submitted to Energy Conversion and Conservation Expo (ECCE), Milwaukee, WI, September 18 – 22, 2016.
2. Hagen S., Knippel R., Ludois D.C., Dai J.J., Brown I.P., “Synchronous Generator Field Excitaton Via Capacitive Coupling Through a Journal Bearing,” In Proceedings of the Energy Conversion and Conservation Expo (ECCE), Milwaukee, WI, September 18 – 22, 2016.

References

1. “DOE Energy Efficiency and Renewable Energy Vehicle Technologies Program Multi-Year Program Plan 2011-2015.” Dec-2010.
2. M. van der Giet, K. Kasper, R. De Doncker, and K. Hameyer, “Material parameters for the structural dynamic simulation of electrical machines,” Electrical Machines (ICEM), 2012 20th International Conference, pp. 2994–3000, Sept. 2012.
3. Ludois DC, Erickson MJ and Reed JK (2014), “Aerodynamic fluid bearings for translational and rotating capacitors in noncontact capacitive power transfer systems”, IEEE Transactions on Industry Applications. Vol. 50(2), pp. 1025-1033. IEEE.

2.5 Alternative High-Performance Motors with Non-Rare Earth Materials

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Abstract/Executive Summary

- The goal of the project is to develop traction motors that reduce or eliminate the use of rare-earth materials and meet the DoE specification. This is accomplished by evaluating/developing multiple motor topologies in conjunction with advanced materials.

Accomplishments

- Ten motor topologies evaluated.
- Down-selected four topologies to be built and tested.
- First prototype is a flux-switching motor with reduced rare-earth magnets (built and fully tested).
- Second prototype is an interior permanent magnet (IPM) spoke motor with Ferrite (Non-RE) magnets (built and fully tested).
- Third prototype is a switched reluctance motor that has no magnets and a high-temperature insulation system as one of the advanced materials (built and tested).
- Fourth prototype is a scaled-down synchronous reluctance motor with dual-phase magnetic material in the rotor. (built and fully tested)
- Final prototype is a full-scale synchronous reluctance motor with a carbon-fiber rotor wrap. (built and testing underway)

Introduction

Electric drive systems, which include electric machines and power electronics, are a key enabling technology for advanced vehicle propulsion systems that reduce the petroleum dependence of the transportation sector. To have significant effect, electric drive technologies must be economical in terms of cost, weight, and size while meeting performance and reliability expectations.

The objective of the GE Global Research "Alternative High-Performance Motors with Non-Rare Earth Materials" program is to develop a higher power density traction motors at a lower cost while simultaneously eliminating or reducing the need for rare-earth materials. The DoE specifications for the motors are summarized in Table 2-4 and Figure 2-56. Successful completion of this program will accelerate the introduction of hybrid electric vehicles into the U.S. road vehicle fleet and bring the added benefits of reduced fuel consumption and environmental impacts.

(A) Motor Development

- Develop advanced motor concepts including electromagnetic, mechanical, and thermal concepts.
- Build proof-of-principle machines to verify the design process as well retire the key risks.

- Design and build 55kW/30kW machines that meet the DoE specifications
- Develop cost model to estimate the advanced motors cost based on 100,000 units/year
- Investigate the scalability of the developed concepts by evaluating 120kW/65kW machines

(B) Materials Development

The objective of the materials development tasks is to develop non-rare-earth containing component materials that enable non-rare-earth containing motor designs that meet project performance goals. In the first phase of research, the capability for improvement of four classes of materials is being studied:

- Improving the coercivity of an existing non-rare-earth-containing permanent magnet composition to enable operation at temperatures above 150°C.
- Improving the tensile strength of electrical steel to enable high speed motor operation with low iron loss
- Improving the ability of motor laminates to control magnetic flux distribution
- Improving the ability of dielectrics to withstand operating temperatures in excess of 280°C.

Table 2-4: Motor Specifications

Items	Specification
Maximum Speed	14,000 RPM
Peak Power	55 kW @ 20% speed for 18 seconds
Maximum Current	400 Arms
Continuous Power	30 kW @ 20-100% speed @ Vdc = 325
Efficiency	Refer to target efficiency map
Operating Voltage	200-450 V (325 V Nominal)
Back-EMF	< 600 Vpk line-to-line @ 100% speed
Torque Pulsation	< 5% of Peak Torque @ any speed
Characteristic Current	< Maximum Current
Weight	≤ 35 kg
Volume	≤ 9.7 L
Cost @ 100k per Year	≤ $275
Ambient (outside housing)	-40 - 140°C
Coolant Inlet	105°C, < 10 LPM, 2 psi pressure drop, < 20 psi inlet
Minimum Isolation Impendance Phase-Terminal to Ground	1 Mega-Ohm

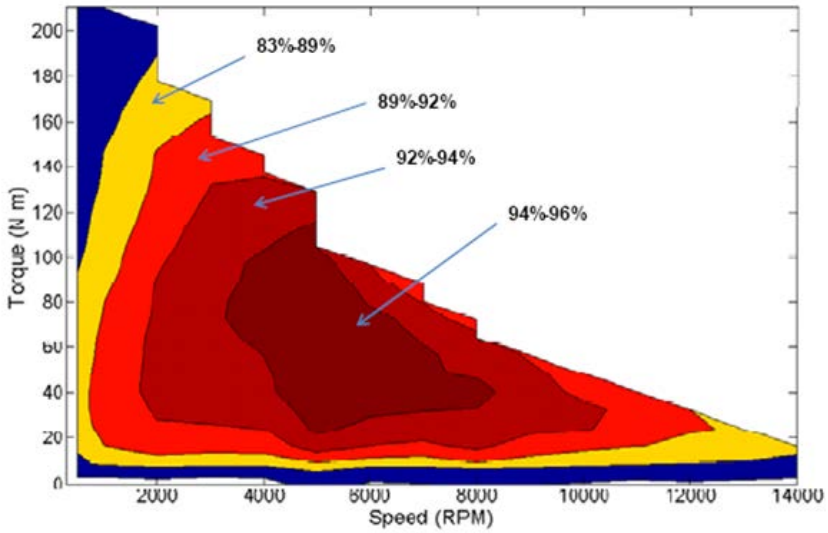

Figure 2-56: Motor Required Efficiency Map
DE-FOA-0000239

Approach

Motor Development

- Perform tradeoff study of various motor topologies
- Identify promising scalable materials and produce coupons showing the expected properties
- Down-select promising topologies/materials
- Design/build/test 2-3 proof-of-principle motors
- Down-select, build and test final motor topology.

Materials Development

- The materials development approach for the project is to develop the structure/ processing/properties relationships of four categories of motor components being made with novel materials. The materials tasks will produce and characterize samples of the new materials and will culminate in the selection of materials for scaled-up production sufficient to produce a prototype motor.
- The microstructure of the non-rare-earth containing permanent magnet alloy is being refined through the application of modern casting and annealing technology. A series of designed experiments is being conducted to probe the capability of these technologies to increase coercivity while maintaining energy product. Magnet post-processing and characterization is being performed at Arnold Magnetic Technologies. Atom-scale structural characterization is being performed in collaboration with Ames laboratory to produce in-depth structure/processing/properties relationships.
- A novel processing route is being applied to conventional silicon steel alloys to improve the tensile strength by while retaining comparable power loss. The approach relies on understanding and controlling the trade-off between coercivity (and hence power loss) and tensile strength. The processing technology is being developed to form the new material into sheets suitable for motor laminates.
- Novel processing technology is being developed to enable improved control of magnetic flux contained within motor laminates. This approach requires the development of new alloys that are operable with this processing method and the demonstration of scalable processing at dimensions specified by the motors teams.

- High temperature dielectrics are being developed that maintain high dielectric strength with resistance to degradation by oxidation. This requires the selection of suitable materials components, production of sample films, and verification of electrical and mechanical properties as a function of time at temperature.

Results and Discussion

1. Motor Development

A ten-pole, carbon-fiber-wrapped synchronous reluctance motor (SyncRM) was built as the final protoype to demonstrate a motor without rare-earth materials that also uses a standard converter. It is currently undergoing testing. Synchronous reluctance motors are particularly appealing due to their simple passive rotor structure, comparable power density to induction motors, low rotor losses, synchronous operation and simple control. The key disadvantages of the SyncRM are low power factor and typically limited constant power speed ratio (CPSR). These disadvantages are mainly due to the presence of magnetic iron bridges and/or center-posts in the rotor, which are especially necessary in high speed machines. The leakage inductance created by the flux leakage through the magnetic bridges and posts leads to higher operating voltages than an IPM at high speeds. Ultimately, the maximum power capability of a conventional SyncRM is determined by the voltage limit placed on the motor. In other words, the conventional SyncRM must be significantly oversized to achieve a comparable CPSR as an IPM. The composite over-wrap consisting of PEEK and carbon fiber is used to maintain the structural integrity of the overall rotor at high speeds.

A cross-sectional view of the motor is shown in Figure 2-57. A carbon fiber wrap is wound directly onto the outer diameter of the rotor core in order to provide preload on the rotor core. The non-magnetic pockets that form each rotor pole are filled with an epoxy with a low thermal coefficient of thermal expansion. An optimization routine was used to determine the size, shape and number of pockets that form the rotor poles. The stator winding is a simple sixty-slot, single-layer, full-pitch winding with two parallel circuits. All of the coils within each phase circuit are also wound continuously without any braze connections between coils. An ethylene-glycol stator cooling jacket and six oil-spray nozzles per motor end cool the stator winding. Finished rotor and stator components are shown in Figure 2-58.

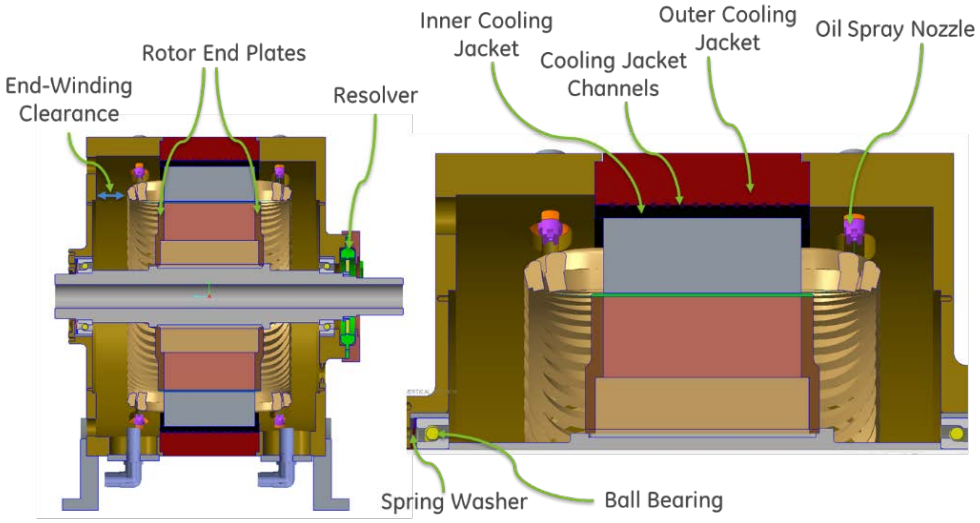

Figure 2-57: Salient Motor Features Horizontal Cross-Section

Figure 2-58: Carbon Fiber-Wrapped Synchronous Reluctance Rotor and Distributed Winding Stator Hardware

An instrumented spin test served to validate the mechanical model of the rotor. Radial growth probes were installed in a spin pit to measure in-situ growth at the rotor sleeve surface. A simplified 2-layer design was used to verify the mechanical integrity of the carbon overwind. Three different combinations of the rotor configuration were built to investigate various aspects of the design, as shown in Table 2-5.

Table 2-5: Spin Test Rotors

Rotor	Sleeve Material	Outer Diameter Surface
1	AS4 CF/PEEK	Rough Lamination Stagger
2	AS4 CF/PEEK	Machined Smooth (Iron)
3	Glass + AS4 CF/PEEK	Rough Lamination Stagger

Rotor 2 was the first rotor tested, which had a machined outer diameter to provide a smooth surface for the overwind. The rotor was balanced to G2.5 specification and installed in the pit. Baseline measurements were taken from the growth probes at 5000 RPM to be used as a reference for the test. The rotational speed was increased in 2000 RPM increments up to 14000 RPM while monitoring rotor growth and vibration. After reaching this maximum operating speed, the rotor was spun down to 5000 RPM to check for any change from the baseline measurements, which would indicate plastic deformation. No such deformation was detected at this point. Testing continued in 2000 RPM steps starting at 16000 RPM, returning to 5000 RPM after a short dwell time at each speed point. A shift in the baseline growth numbers was indicated after the 20000 RPM test point, and speed was then increased in 1000 RPM increments with a return to 5000 RPM after each point. Shifts in the baseline were measured after the 21000 and 22000 RPM points, and while accelerating to 23000 RPM the rotor burst.

Subsequent testing was limited to low-cycle fatigue testing for remaining rotors to determine how the rotors behave under repeated stress cycling. Rotor 3 was subjected to 150 cycles between 3000 and 12000 RPM and inspected. Rotor 1 was tested for 400 cycles in four 100 cycle steps: 3000-6000 RPM, 3000-8000 RPM, 3000-10000 RPM and 3000-12000 RPM and completed these cycles without issue.

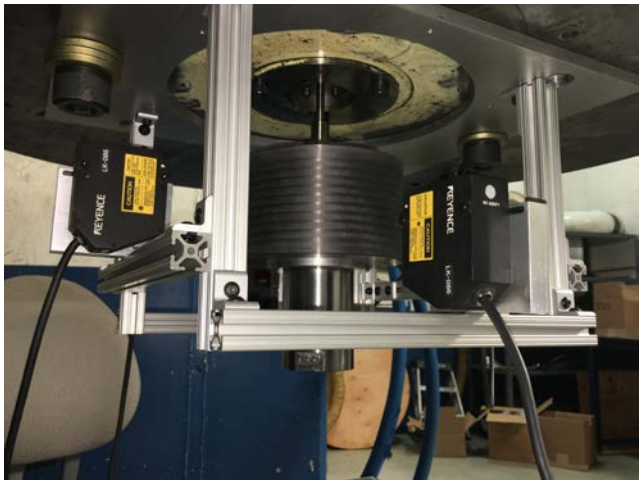

Figure 2-59: Spin Test Setup

The completed motor is in the process of being tested, as shown in Figure 2-60. As a precaution, the machine will be tested with a lower coolant inlet temperature of 60°C. The measured temperature rises in the machine can be used to easily predict the temperature with 105°C coolant inlet temperature.

Since there is no rotor MMF source such as permanent magnets, the motor does not produce a back-EMF. Due to this fact, the no load mechanical drag losses were much easier to measure by simply spinning the motor with a dynamometer while measuring the shaft torque with a torque-meter. The no-load drag torque and loss up to 4000 RPM are shown in Figure 2-61; since the testing is first completed at low speeds for risk reduction, the no-load loss above 4000 RPM has not yet been completed. The no-load drag loss is shown for a dry cavity (no oil spray) and with the oil spray, and it is shown that the oil spray has an appreciable effect on the drag loss. The no-load drag loss has proven to be consistent with past motors designed with similar rotor diameters and the same bearing size and type.

Torque versus current measurements are taken at a low speed of 2800 RPM. The comparison is made based on air-gap torque by removing the rotor drag and electromagnetic losses. This testing has been performed up to 400 Arms, as shown in Figure 2-62. As can be seen, there is a 4-7% difference between the predicted and measured torque. The difference in torque was expected due to a deformation of the rotor poles that presented itself during processing of the rotor. This deformation can be avoided with future designs but time did not allow for changes to be incorporated into this prototype.

A peak power heat run of approximately 18 seconds was tested at 2800 RPM. The current was ramped up to 400 Arms over 5 seconds and the torque was held at its steady-state value for 18 seconds, as can be seen in Figure 2-63. A summary of the steady-state performance is shown in Table 2-6. The output torque and power are both 4% lower than predicted for the same reason previously mentioned. Figure 2-63 also shows the winding temperature over the duration of the transient heat run. Note that the opposite drive end (ODE) is hotter than the drive end (DE) due to the extra resistive losses in the winding connections and leads, which wrap around the end-winding on the opposite drive end. This bulk of copper also prevents the heat from escaping the inner-most wires of the ODE end-winding. In general, the end-winding temperatures are greater than the mid-stack slot temperatures, which is an indication that the oil spray cooling is not as effective as expected, perhaps due to a low flow rate. The tooth temperature of the stator core is hotter than the yoke temperature, as expected, due to the cooling jacket proximity to the stator yoke. Partial and rated load testing is still to be completed.

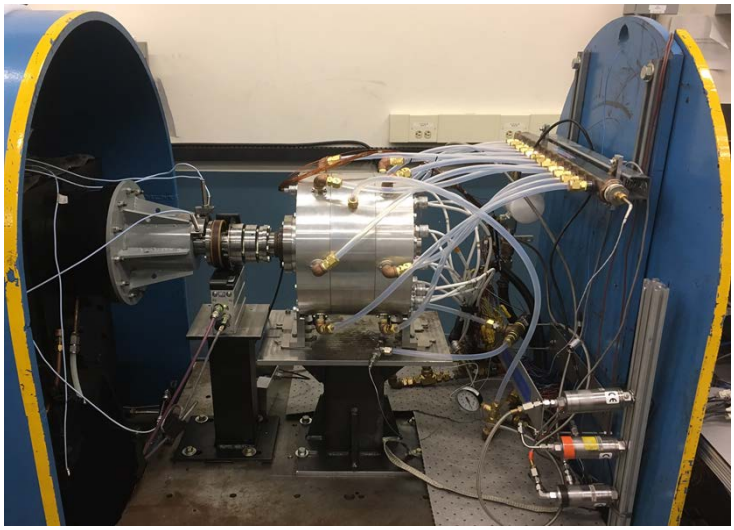

Figure 2-60: Synchronous Reluctance Motor on Test Stand

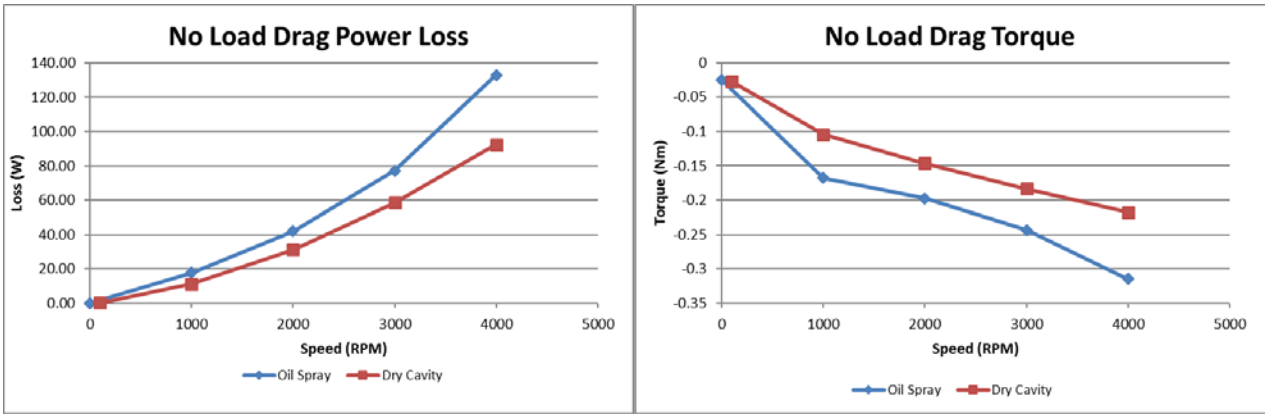

Figure 2-61: No-Load Drag Torque and Loss

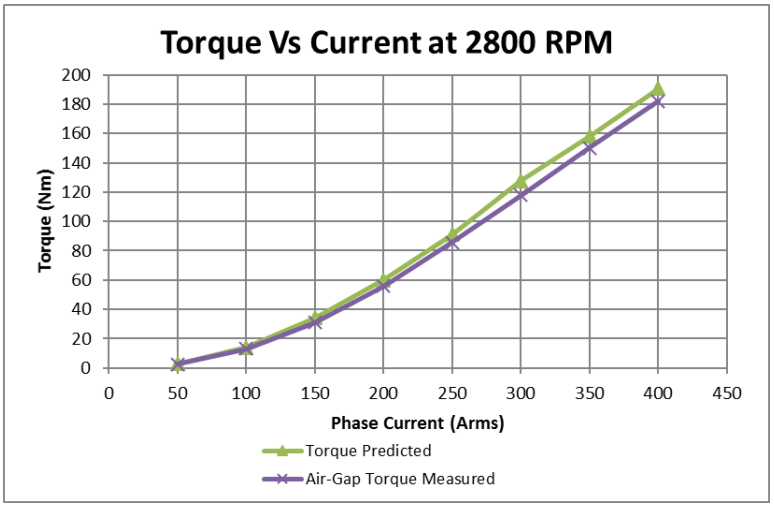

Figure 2-62: Air-Gap Torque Versus Current

Figure 2-63: Peak Power Transient Heat Run Results

Table 2-6: Peak Power Performance Summary

Items	Performance Value
Speed (RPM)	2800
Phase Current (Arms)	402.0
Phase Voltage (Vrms)	116.4
Torque (Nm)	181.8
Input Power (kW)	60.7
Output Power (kW)	53.3
Efficiency (%)	87.9%
Power Factor	0.44

2. Materials Development

No new work was performed on the materials development during FY2016.

Conclusions and Future Directions

Significant progress has been made in developing motor topologies. The first prototype, a flux-switching machine using Dy-free magnets, was built and fully tested. The second prototype, an interior permanent magnet spoke design with ferrites, was built and fully tested. The third prototype, a doubly-excited SRM, was built and tested with a high temperature (280°C) stator insulation system. Dual-phase magnetic laminations were produced and used in the fourth scaled-down prototype, a synchronous reluctance motor, which was tested and compared to a synchronous reluctance motor design without dual-phase material. The final prototype, a carbon-fiber-wrapped synchronous reluctance rotor with distributed winding is currently under test and provides a completely rare-earth-free option without a specialized inverter or control scheme.

Although motor designs containing some level of rare earth permanent magnets continue to be the most power-dense designs. Several rare-earth free designs are possible that meet most of the specifications provided for this program. The very wide constant power speed range makes it quite challenging to limit the mass and volume of the motor while meeting the required efficiency map.

Non-rare earth motor designs using dual-phase magnetic materials are an exciting opportunity for the future. Dual-phase magnetic materials can enable improvements in several motor topologies including permanent magnet, induction, switched reluctance and synchronous reluctance.

FY 2016 Presentations/Publications/Patents

1. J. P. Alexander, S. Galioto and A. M. El-Refaie, "First order mechanical sizing equations for the electromagnetic optimization of spoke IPM machines," 2016 XXII International Conference on Electrical Machines (ICEM), Lausanne, Switzerland, 2016, pp. 357-363.
2. Ayman El-Refaie, Tsarafidy Raminosoa, Patel Reddy, Steven Galioto, Di Pan, Kevin Grace, James Alexander and Kum-Kang Huh, “Comparison of Traction Motors that Reduce or Eliminate Rare-Earth Materials”, to be presented at ECCE 2016, Milwaukee, WI
3. Tsarafidy Raminosoa, Ayman El-Refaie, David Torrey, Kevin Grace, Di Pan, Stefan Grubic, Karthik Bodla and Kum-Kang Huh, “Test Results for a High Temperature Non-Permanent Magnet Traction Motor”, to be presented at ECCE 2016, Milwaukee, WI.
4. Tsarafidy Raminosoa; David A. Torrey; Ayman M. El-Refaie; Kevin Grace; Di Pan; Stefan Grubic; Karthik Bodla; Kum-Kang Huh, “Sinusoidal Reluctance Machine with DC Winding: An Attractive Non-Permanent-Magnet Option”, IEEE Transactions on Industry Applications, Year: 2016, Volume: 52, Issue: 3 Pages: 2129 - 2137

2.6 Unique Lanthanide-Free Motor Construction

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Contractor: UQM Technologies, Inc.
Contract No.: DE-EE0005389

Abstract/Executive Summary

Objectives

This project pursues new motor construction that eliminates, or significantly reduces the use of rare earth elements while maintaining the attractive size, weight and efficiency features of rare earth permanent magnet motors. The primary drivers for this work include:

- Lack of transparency in the rare earth magnet supply market and its pricing structures
- Significant rare earth price escalation in calendar year 2011
- Need for small, lightweight, high efficiency, low cost motors for electric traction drives
- New architectures and/or materials that eliminate rare earth materials while maintaining performance that is attractive for electrified vehicles.

Technical Barriers

The low coercivity of the AlNiCo magnets requires an unconventional rotor design for power density. This unconventional rotor design requires an innovative magnet retention system for high speed operation. The proof-of-concept (POC) rotor involves the use of retention bars, adhesive and fiber wrap to accomplish the retention.

A second item of concern is also related to the AlNiCo magnets and their characteristic of de-magnetizing if not magnetically coupled with a conductive outer sleeve. This sleeve must be over the rotor any time it is not fully inserted in the stator. UQM has worked with the company magnetized the rotor to insure a sleeve can be designed to maintain the magnetization.

Technical Targets

The DOE motor specifications that are targeted for this work include:

- 55 kW baseline design
- Scalable to 120 kW or higher

Accomplishments

- Phase 1 - The items originally identified as milestones for the Phase 1 (BP1) have been completed and show that it is possible to produce a motor using non-rare earth, Lanthanide free magnets. In addition, this motor can be competitive with a motor using the costlier rare earth magnet technology. Specific milestones completed in Phase 1 included:
  - The development of an Interface Control Document (ICD) that captures the design targets/specifications of the motor including those defined by the DOE
  - Review of the current state of the target magnet technology and what improvements may be possible within the time frame of the project
  - An development of an electromagnetic model using the ANSYS finite element analysis tool, to be used in the initial design and any subsequent refinement/redesign work
  - Analysis of the motor commutation, using Matlab/Simulink to determine interaction between the motor electromagnetics and the inverter (drive)
  - Preliminary motor package design including magnet/rotor configuration, housing/cooling jacket and overall package size and weight.
- Phase 2 - Proof-of-Concept Build and Test, the specific milestones that were achieved in the second phase include:
  - Finalized the electromagnetic design, including;
  - Final design rotor/magnet configuration
  - Stator winding and requirements for magnetizing the magnets
  - Complete design package to be used for POC build
  - The assembly of two (2) POC motors to be used for dynamometer testing
  - Dynamometer testing at UQM's facility to demonstrate technology feasibility, a "Go/No-Go" milestone. Based on results from this testing UQM believes the technology is feasible and the next phase of work should be pursued.
  - During this period Ames has made good progress on the development of an enhanced version of the AlNiCo magnet material (referred to as AlNiCo 8X). As such UQM will be incorporating the AlNiCo 8X into the second iteration proof-of-design (POD) motors for the BP3 effort.
  - Delivery of a POC motor to ORNL for independent performance evaluation.
- Phase 3 - Proof-of-Design Build and Test, the specific milestones that were achieved in the second phase

Introduction

Project Objective

This project pursues the development of a non-rare-earth permanent magnet motor architecture. It incorporates a novel rotor geometry that allows the use of lower energy Al-Ni-Co, Fe-Co-W, or other high flux, low coercivity magnet material. These materials are not currently adopted due to demagnetization within existing magnetic circuit designs, a problem that is overcome with this proposed design.

Project Description

Three unique design features of this motor architecture are proposed to enable the use of low coercivity magnet technology: magnet shape along with magnetization direction, a nonmagnetic support structure, and design features that reduce demagnetization fields. The project relies upon incremental improvement in the non-rare-earth magnet properties (collaboration with Ames Laboratory) and this is where the project starts. From there, UQM develops a motor design and integrates thermal technology in collaboration with the National Renewable Energy Laboratory. Finally, motors are built in years two and three (initial proof-of-concept motor followed by refined hardware). These will be tested at UQM and delivered to Oak Ridge National Laboratory for independent confirmatory testing. The project concludes with designs scaled to higher power and detailed cost estimating activities. Cost is key to the adoption of electrified vehicles, so substantial focus is placed on the tasks related to the detailed costing of the technology.

Project Impact: Benefits and Outcomes

The outcome of the technology development and the resultant scalable hardware will be motor designs that apply to a full range of vehicle electrification, from mild hybrid to heavy hybrid to fully electric vehicles. This unique permanent magnet motor technology has an efficiency advantage over wound-field or induction machines (no energy consumed to create the magnetic field), and therefore, will decrease petroleum consumption relative to other non-rare-earth motor technologies. Economically, the magnet material used for this program is one-third the cost of NdFeB magnets on a per-pound basis, and therefore, supports lower cost if the material content can be maintained to be less than three times the amount of NdFeB for a given power level. UQM is confident that the total magnet cost of the proposed technology will be lower than the equivalent rare-earth motor. This will provide economic benefit to the end-use consumers (lower vehicle cost) and improve electrified transportation industry with products that compete more favorably with traditional petroleum engine driven vehicles.

Approach

Pursue design that enables the use of low coercivity magnets

- Unique magnet and supporting rotor geometry
- Stator and rotor design features that reduce demagnetization fields.

Collaborate with FFRDC partners

- Ames Laboratory for incremental improvements in high flux, low coercivity magnet materials
- National Renewable Energy Laboratory for thermal management
- Oak Ridge National Laboratory for testing.

Phase 1: Focused on the design of the electromagnetic circuit that will meet the DOE targets and be capable of manufacturing

- UQM's focus was the electromagnetic design with existing AlNiCo technology
- Ames Laboratory is pursuing increased performance of the AlNiCo material
- NREL will provide assistance in the thermal management of the motor design
- ORNL will provide testing of the motor.

Phase 2: Focused on the build proof-of-concept (POC) motor and test with standard three-phase inverter

- Tests at UQM showed the performance is achievable
- Unit submitted to ORNL to validate results.

Phase 3: Build and test proof-of-design (POD) motor

- Development of the enhanced AlNiCo 8X magnets by Ames
- Implement enhanced AlNiCo 8X magnet material developed by Ames in POD motor
- Bill of materials with costs and higher power design at program completion.

Results and Discussion

UQM Technologies Efforts

Phase 1 & 2: Proof-of-Concept Motor Design, Build and Test

The POC motor final assembly was completed and testing commenced, the motors are shown in Figure 2-64 on the dynamometer test apparatus. Testing was conducted to verify motor characteristics such as Back-EMF, Torque, and power. The initial tests on the dynamometer measured back EMF. The back EMF screen captures from the oscilloscope are shown below in Figure 2-65.

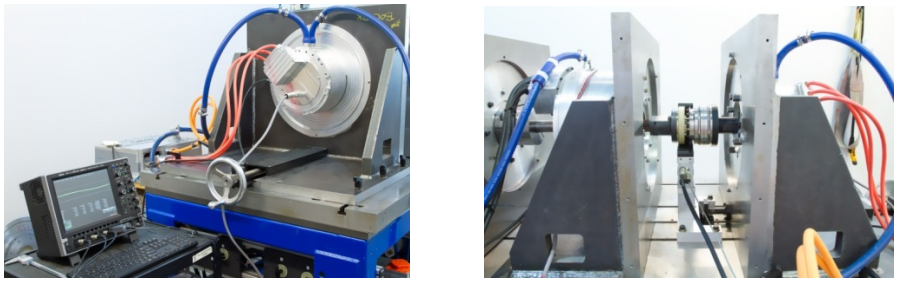


Figure 2-64: Dynamometer Testing Apparatus

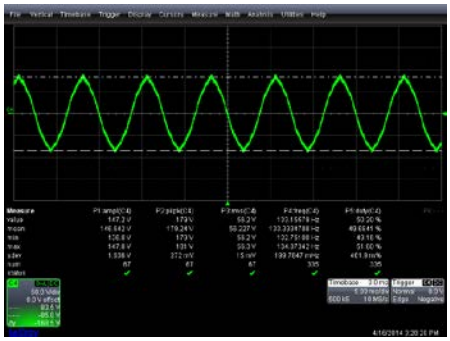
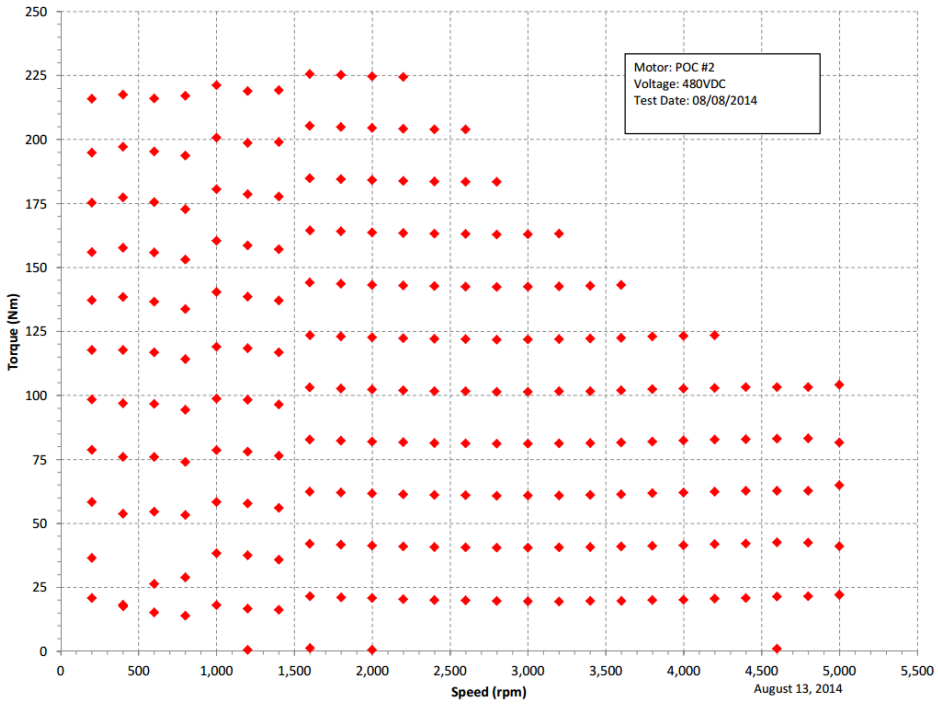


Figure 2-65: Back EMF POC Motor 1

Performance validation tests had been performed to determine the peak torque and power on POC motor 2. The speed was limited to 5,000 rpm to prevent damage due to cracks in the magnet material. The torque was limited to 85% of full torque, or 225 Nm, to avoid a demagnetizing. The results of these tests are shown in Figure 2-66.



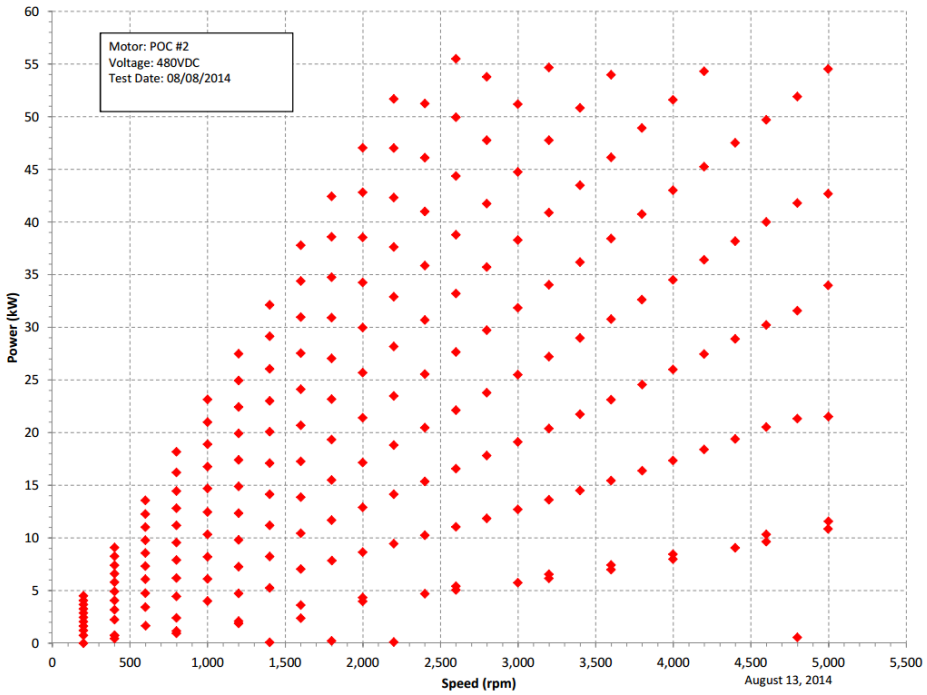


Figure 2-66: Torque and Power vs. Speed Results

As can be seen from the results of this test, the motor was able produce the DOE Goal of 55 kW from 2000 rpm to 5000 rpm.

In conclusion, the test results verified the design EMF and reached the power goal of 55 kW. The design also proved capable of producing 90% of the torque goal 235 Nm relative to the goal of 262 Nm.

Phase 3: Proof-of-Design Design, Build & Test

The proof-of-design (POD) phase focused on improving the POC design in two key areas, they included:

- Rotor / magnet retention
- Incorporating improved AlNiCo magnet material

During the testing of POC motor 1 a failure occurred in the magnet retention structure and the magnets contacted the stator during high speed (10,000 rpm) operation. UQM analyzed this failure and determined that several issues contributed to the failure, including:

- Excessive temperature
- Insufficient adhesive fill
- Magnets with internal cracks (occurred during processing)

To address these issues UQM took the following steps in the POD design, the steps and details are listed below.

To address the excessive temperature issue UQM adjusted the maximum operating temperature (measured at the rotor) to prevent reaching the limit of the adhesive and structural wrap material.

Using ANSYS for finite element analysis UQM revised the retention structure and material to insure the magnets would remain in place during high speed, high temperature operation. Figure 2-67 shows the analysis results of total deformation of the magnets on the rotor during high speed, elevated temperature operation.

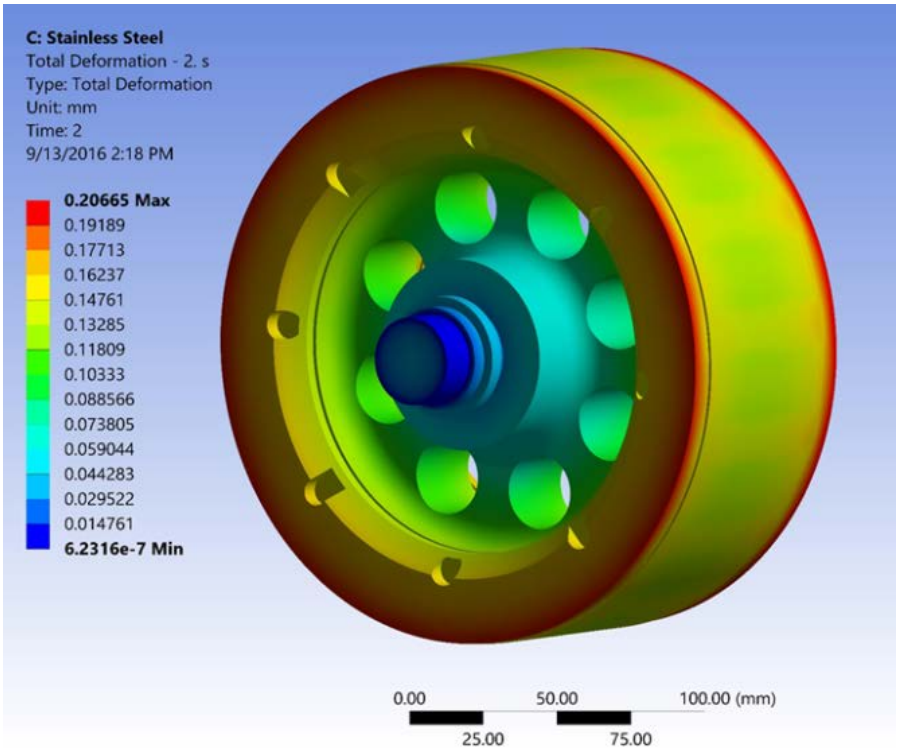


Figure 2-67: Deformation of the Magnets at 10,000 rpm and 120°C

To address the issue with the cracks within the magnets UQM selected the AlNiCo 8HE material. The AlNiCo 8HE is a "much tougher / less brittle" material compared to the AlNiCo 9 material used in the POC motors. However, the use of the AlNiCo 8HE material required some changes to the control methods to make up for a lower maximum energy (Bd x Hd). Figure 2-68 shows the comparison of the AlNiC0 8HE versus the AlNiCo 9.

Magnetic and Physical Properties (Typical Values)

	Max. Energy Product Bd x Hd		Residual Induction Br		Required Magnetizing Field		Coersive Force Hc		Recoil Permeability		Permeance Coefficient B/H @ (BdHd) Max.		Induction at Maximum Energy Product	
	MGOe	KJ/m³	G	mT	Oe	KA/m	Oe	KA/m	G/Oe	10⁻³Tm/KA	G/Oe	10⁻³Tm/KA	G	mT
Alnico 8B	5.50	43.8	8300	830	6000	480	1650	131	2.0	2.5	4.5	5.5	5000	500
Alnico 8HE	6.00	47.7	9300	930	6000	480	1550	123	2.0	2.5	5.5	7.0	5750	575
Alnico 8H	5.50	43.8	7400	740	6000	480	1900	151	2.0	2.5	3.5	4.5	4400	440
Alnico 9	10.50	83.6	11200	1120	6000	480	1375	109	1.3	1.6	7.5	9.5	8900	890

	Density		Electrical Resistivity	Tensile Strength		Transverse Modulus of Rupture		Coefficient of Thermal Expansion	Hardness Rockwell C
	lb./in.³	gr/cm³	25° C (μΩ cm)	PSI	N/mm²	PSI	N/mm²	per ° C x 10⁶	
Alnico 8B	0.262	7.25	50	9000	60	30000	205	11.0	56
Alnico 8HE	0.262	7.25	50	10000	70	30000	205	11.0	56
Alnico 8H	0.262	7.25	50	8500	60	30000	205	11.0	56
Alnico 9	0.262	7.25	50	7000	50	8000	55	11.0	56

Figure 2-68: Magnet Properties of AlNiCo 8HE versus AlNiCo 9

POD Motor Build and Testing

Since the POD motors are similar to the POC motors no issues were experienced in the assembly. However, lessons learned and extra care was applied to insure the best chance of success. Figure 2-69 shows the rotor during assembly and end the final assembled condition.

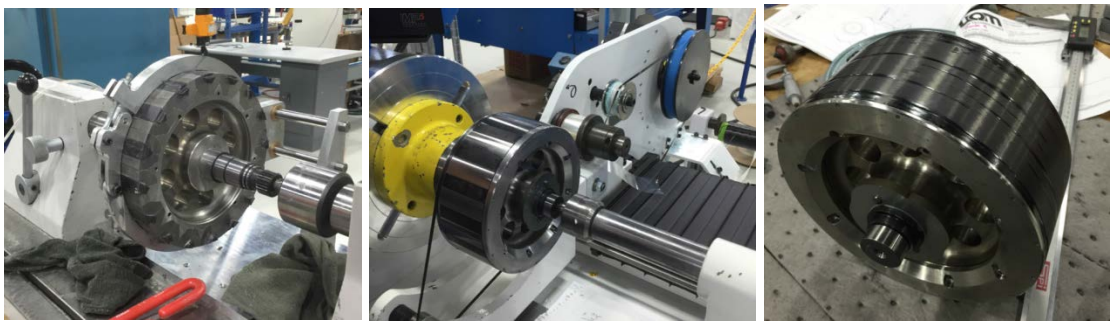


Figure 2-69: Rotor Assembly

Upon the completion of building, the motor was tested to ensure basic motor parameters were indeed met. The test was completed on a production End of Line (EOL) tester at UQM. Most parameters were acceptable with the exception of motor back EMF, which was low (56 v/krpm), see Figure 2-70

Parameter	Value	
Temperature (Celsius)	20	120
Ke (Vpk/Krpm L-L)	77.877	76.631
R (Ohm L-L)	0.042	0.058
L (uH L-L)	125.000	
Kt (Nm/Arms) reference only	0.890	0.880
	Note: Ke/Kt have a temperature compensation of 0.02 %/C for Alnico Material Properties	

Figure 2-70: POD Estimated Parameter List – Alnico 8HE Magnets

120 kW Scaled-up Design

The final effort in this phase was to develop a 120 kW scaled-up design based on the lower power POD design. The design extended the magnet geometry to 6.42 in (163.1 mm), 2.5 times the length of the POD geometry. The maximum torque was calculated to be 574 Nm and peak power was 120.2 kW. Figure 2-71 shows the electromagnetic analysis, conducted in ANSYS of the 120 kW design.

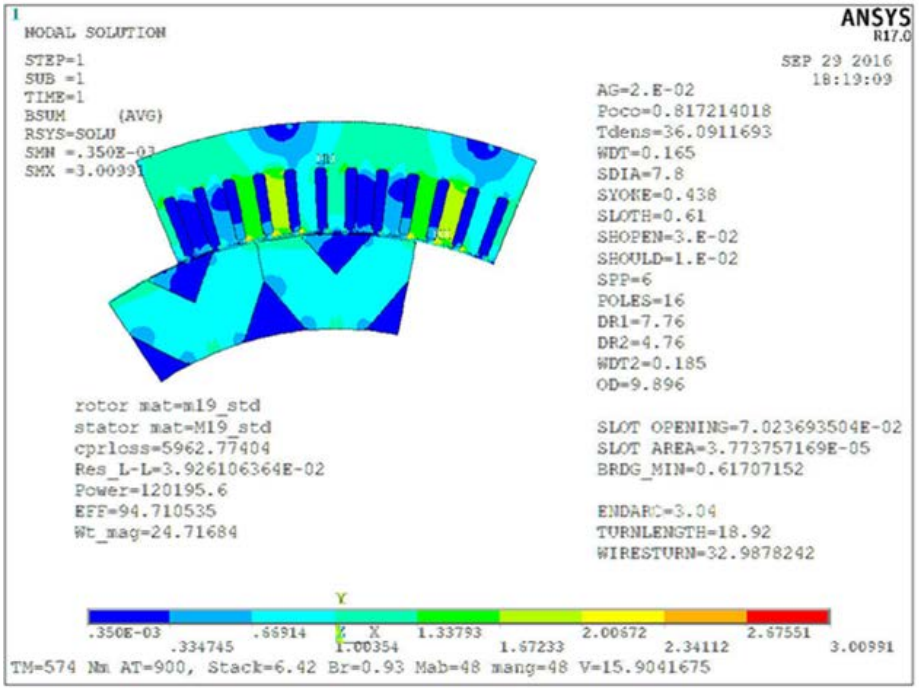


Figure 2-71: 120 kW ANSYS Solution

The analysis showed that the POD can be feasibly be scaled up to 120 kW, via addition of length of the electromagnetic (magnets and stator). However, additional work will be required to finalize the rotor / magnet retention structure for this added length.

Ames Laboratory Efforts

Phase 1 & 2: Magnet Improvement Analysis
During the period Ames Laboratory (Ames) focused on refining the AlNiCo material, AlNiCo 8(X) showed the most promise for improvement, due the initial higher coercivity. Ames produced a pre-alloy powder (AlNiCo 8(X)) that had very spherical shape and a low content of satellite particles. Additionally, this powder had excellent flowability and powder packing. It was determined that compression molding is the preferred method for producing inexpensive bulk magnet shapes.

From these successes Ames has determined that an improved magnet composition (increased coercivity) can be produced for use in the POD motors for the next phase.

Phase 3: Development of Enhanced AlNiCo 8(X)
During the final phase Ames focused on the development of their AlNiCo 8(X) material into the shape that is required for POD motor, the following describes this effort.

The first effort was to produce a "half" length section of the magnet with the required profile, Figure 2-72 shows a half-length sample and density improvements due to the use of finer powder and higher uniaxial pressure during compression molding.

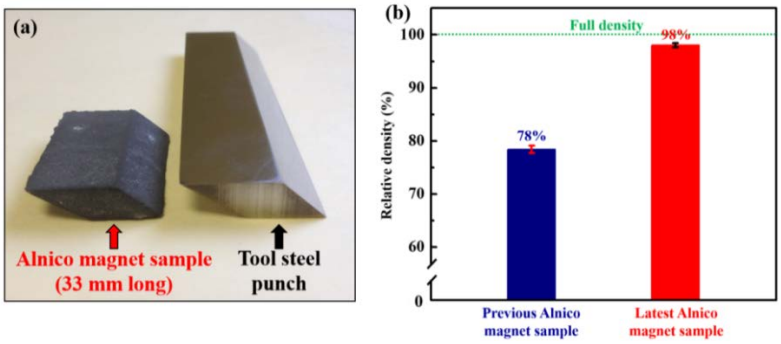


Figure 2-72: (a) Half-length Alnico magnet sample next to tool steel punch, (b) Relative density of two sintered AlNiCo magnet samples

Density uniformity is equally important as high density for a sintered magnet product. The density variation of the sintered Alnico magnets was investigated by two methods, i.e., porosity measurement and microstructural analysis. Figure 2-73 shows porosity variations from edge to center sections of the 78% dense Alnico magnet sample.

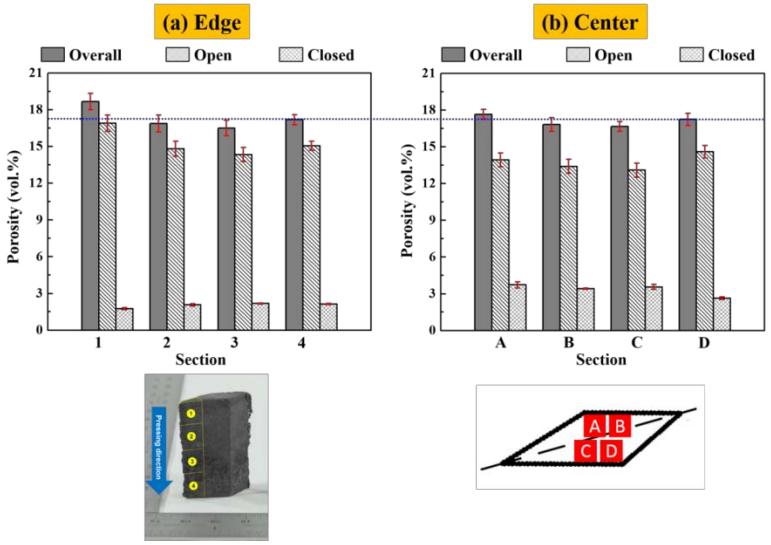


Figure 2-73: (a) Porosity variations along the pressing direction, (b) porosity data of the edge sections vs. compared to center sections

To achieve the uniform density and produce full magnet blanks AMES developed a single pass furnace system. As mentioned this furnace system enables processing of the full scale AlNiCo 8(X) magnets, the size of which is too large to fit into the existing quench furnace at Ames Laboratory. The sintering, solution heat treating, and quenching were conducted in two separate furnace runs. The new furnace system combines the two runs in one single run, significantly reducing production time.

Figure 2-74: One Pass (sinter/solution heat treat/quench) Furnace System Ames Laboratory

The manufacturability of bulk alnico magnet alloys in near-final shapes was demonstrated, permitting further processing and alloy modification experiments that can target higher coercivity.

The recent development of a compression molding die and punch set and a sinter/solution heat treat/quench furnace system paves the road to scale up the pre-alloyed powder processing for the production of UQM magnets in near-final shape.

Unfortunately, the phase 3 timing and budget did not allow AMES to produce and process an adequate quantity of their AlNiCo 8(X) magnet blanks for use in the POD build.

National Renewal Energy Laboratory Efforts

Phase 1 & 2: Thermal Management
In support of UQM, NREL provided thermal management analysis and design support. The first two phases involved the following work:

- Full stator cooling jacket flow and thermal analysis
- Thermal parameter sensitivity study
- Investigation of alternative cooling techniques
- Stator-to-case thermal contact resistance measurements
- In-situ motor testing.

Cooling Jacket Flow and Thermal Analysis
Phase 1 work focused on developing a simplified thermal analysis model of the motor, shown in Figure 2-75. In the second phase NREL worked to verify the accuracy of the and the process from which it was derived by running a full conjugate heat transfer model using computational fluid dynamics (CFD) for the stator and cooling jacket to integrate the thermal performance and fluid flow.

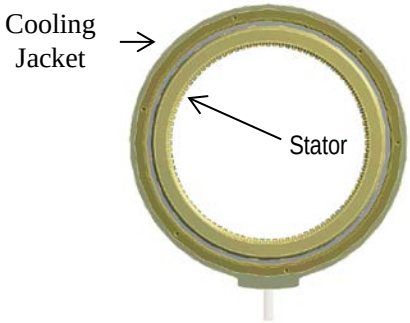


Figure 2-75: Full CFD model (top) and FEA section model (bottom).

Results showed that the section FEA model was accurate enough to be used in lieu of a full conjugate heat transfer CFD model for most analyses that focused on the motor stator. The agreement between the full CFD and FEA section models confirmed the approach used to develop the FEA section model. Therefore, the FEA model was used in a material sensitivity analysis, details in the following sections.

Thermal Parameter Sensitivity Study

Results of the material and interface sensitivity study are shown in Figure 2-76. For the analyzed cooling configuration, the most important properties were the in plane lamination thermal conductivity and the stator-case contact thermal conductivity or contact resistance. It is through these two parts that all the heat must flow out of the motor for the case cooled configuration.

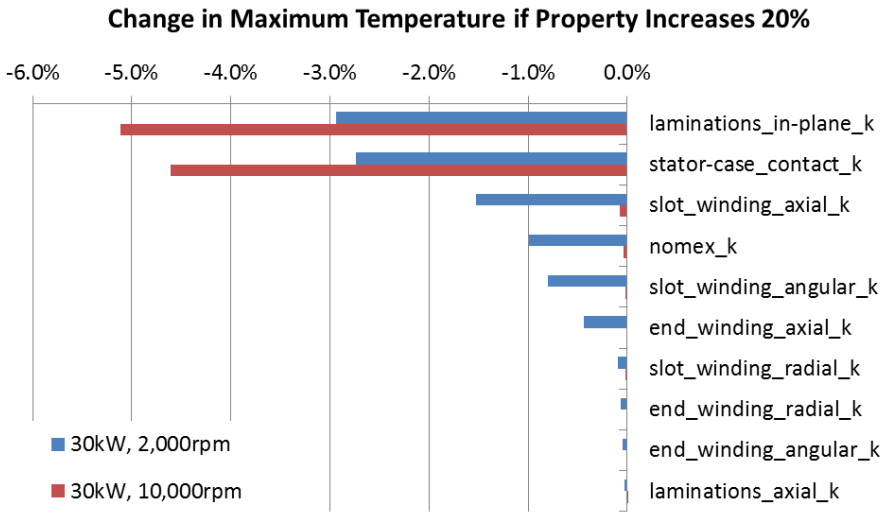


Figure 2-76: Summary of Material Sensitivity Study

Alternative Cooling Techniques

Two design alternatives were considered that focused on cooling the motor end windings, based on the observation that the hottest part of the motor was the end windings. The two alternatives were; 1) encapsulating the end winding with a thermal potting compound and 2) direct cooling the end windings with oil.

The results of the FEA showed that encasing the end windings in a potting compound has potential of a 30% improvement in performance when in the high torque mode, where maximum heat is generated in the winding. The results shown in Table 2-7 show this potential improvement and that encapsulating the end windings is effective in the heat transfer out of the stator.

Table 2-7: Summary of FEA Results Incorporating Potting Encapsulate for End Windings

	Operating Point	30 kW @ 2,000 RPM	30 kW @ 10,000 RPM
Original Design	Max Winding T [°C]	153	170
Design with Potting Compound	Max Winding T [°C]	125	152
	change*	30%	16%
*winding to coolant, coolant at 60°C			

It was determined that direct oil cooling can be an effective method to cool the motor end windings, however the challenges and added complexity of the oil within the motor does not make it feasible for this application.

Case-Stator Thermal Contact Resistance

As mentioned in the thermal sensitivity study, the lamination thermal conductivity and the thermal contact resistance between the stator and the cooling jacket are critical parameters in the overall motor thermal management. In the second phase NREL set up an experiment to measure both the lamination thermal conductivity and the thermal contact resistance between the stator and case. In this test a one-dimensional heat flux is imposed across the sample and uses the temperature gradient across the sample to determine the thermal resistance. A schematic of the setup and the actual hardware are shown in Figure 2-77.

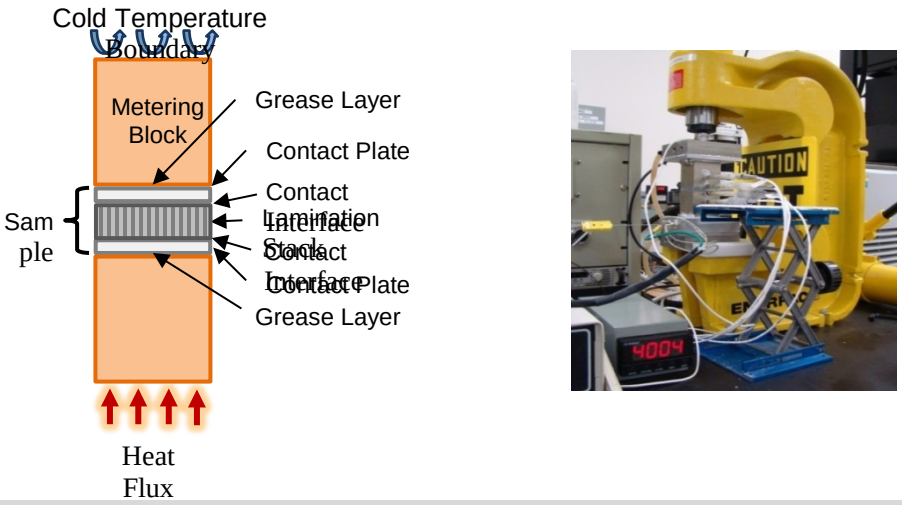


Figure 2-77: Schematic of ASTM Setup and Test Apparatus

By performing measurements with varying lamination heights the thermal resistance of the lamination stack can be separated from the contact resistance. The main set of experiments will be performed during phase three of the project.

In-Situ Thermal Testing

UQM supplied a motor stator to conduct in-situ thermal testing. The experiment involved heating the stator windings using a DC current to simulate winding losses. In addition, CFD and FEA models were developed and validated against the experiment to improve thermal modeling. The test bench for the stator in-situ experimental setup is shown in Figure 2-78.

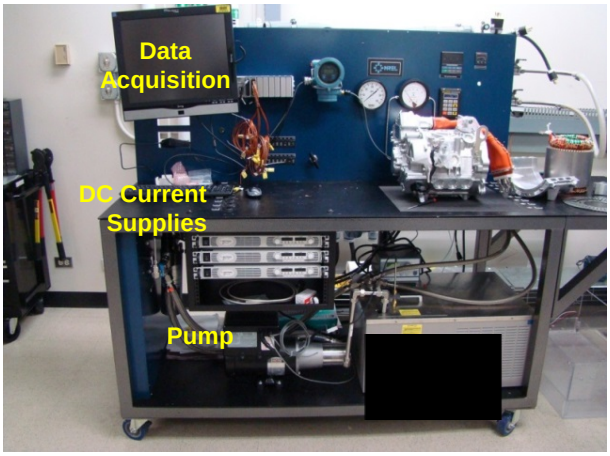


Figure 2-78: Motor Stator Thermal Test Bench

Phase 3: Thermal Measurements and Results

Slot Liner Insulation Thermal Conductivity Measurements

Three slot liner papers were sent by UQM to be tested on NREL's ASTM D5470 test stand. The samples were all 2 in x 2 in square and mounted in the test fixture as shown in Figure 2-79.

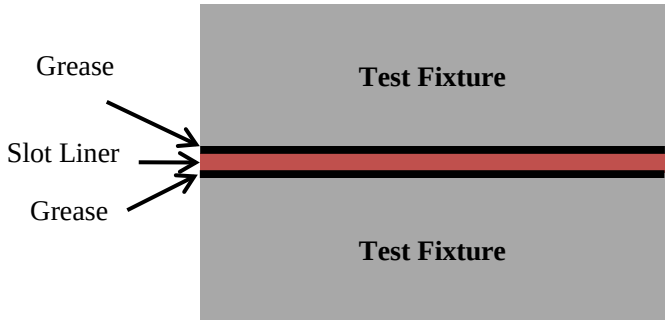


Figure 2-79: Slot Liner in Test Fixture

Slot Liner to Stator Thermal Contact Resistance Measurements

Similar to the slot liner thermal resistance measurements, the slot liner thermal contact resistance measurements were performed in the ASTM stand, the stack-up is shown in Figure 2-80.

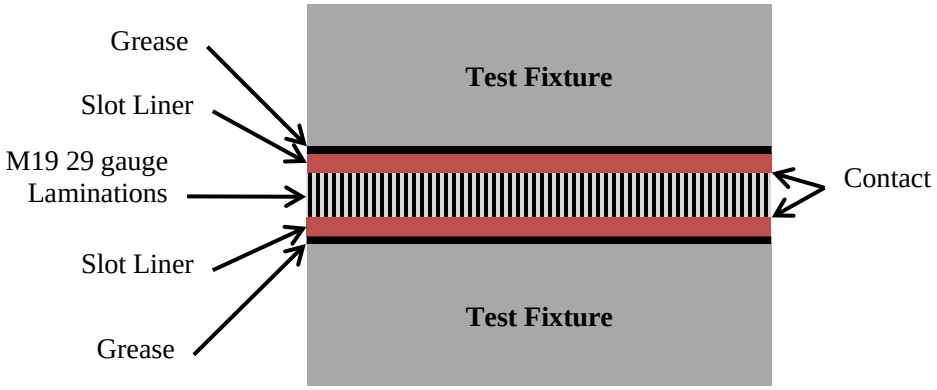


Figure 2-80: Stack-up to Measure Slot Liner to Stator Thermal Contact Resistance

End Winding FEA

Figure 2-81 shows the geometry used for the FEA thermal analysis. The motor was encapsulated in a potting compound with a thermal conductivity of 1 W/m-K. S1 and S2 refer to the distance between the case and end winding on the output shaft end. L1 and L2 refer to the distance between the case and end winding on the lead exit end.

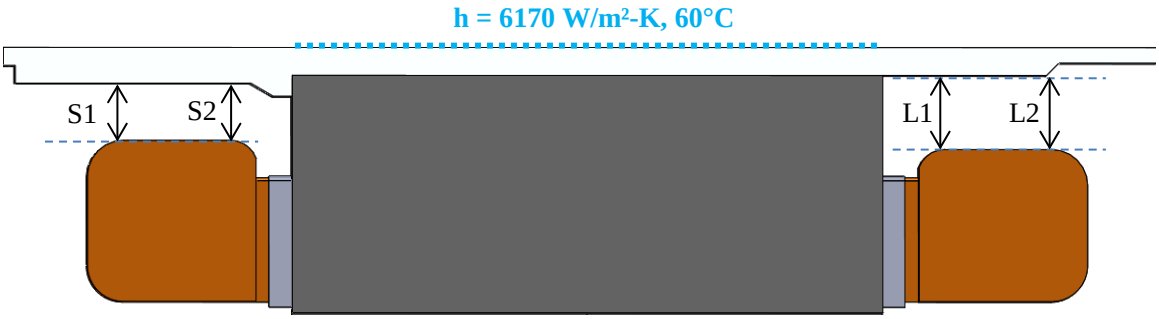


Figure 2-81: Geometry for FEA Thermal Analysis

Results

Slot Liner Insulation Thermal Conductivity Measurements

The slot liner bulk thermal conductivity results are shown in Figure 2-82.

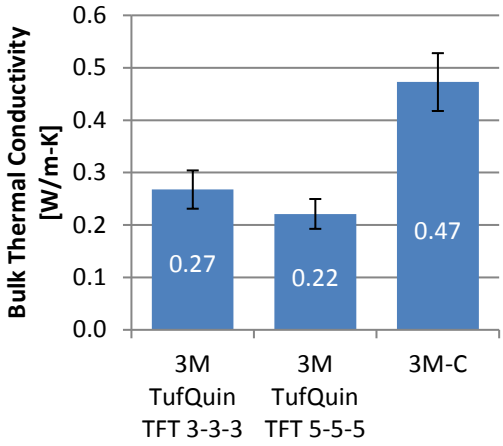


Figure 2-82: Slot Liner Insulation Thermal Conductivity Results

Slot Liner to Stator Thermal Contact Resistance Measurements

The slot liner to stator thermal contact resistance measurement results are shown in Figure 2-83.

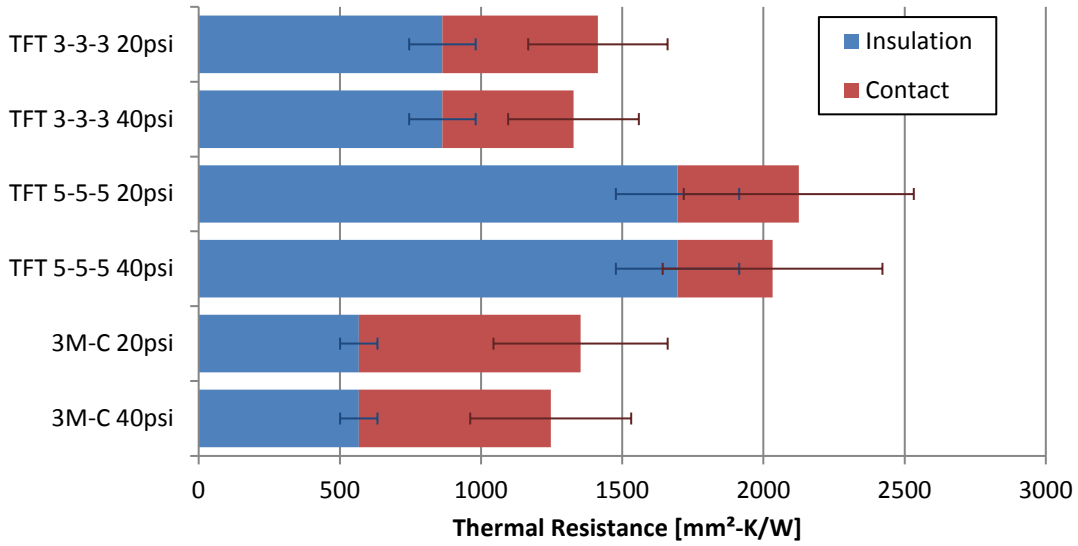


Figure 2-83: Slot Liner Thermal resistance with Slot Liner to Stator Contact Thermal Resistance Stacked

End Winding FEA

The results of the end winding FEA are summarized in Figure 2-84.

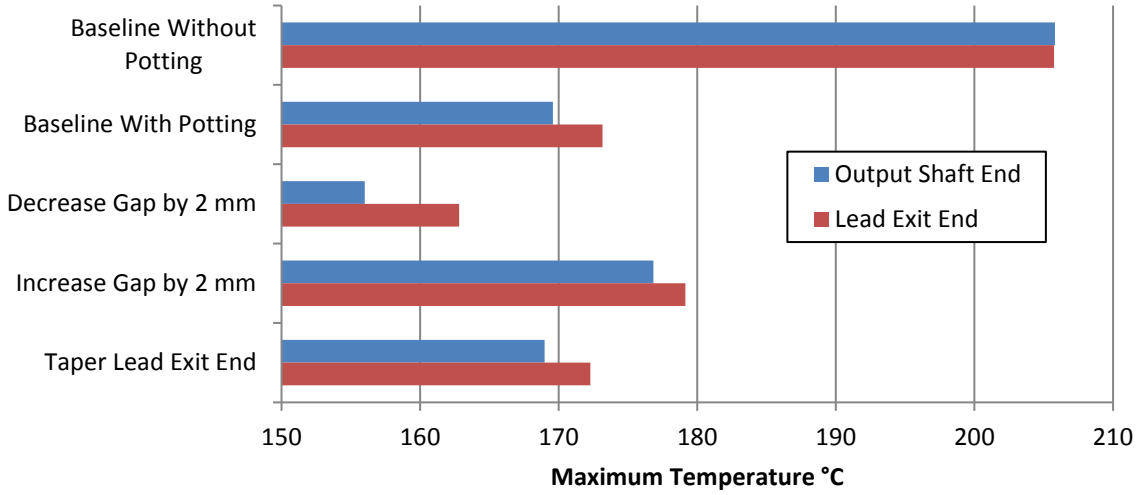


Figure 2-84: FEA results summary

Oak Ridge National Laboratory Efforts

Phase 2: Testing POC Motor 2

The second POC motor (w/ controller) was delivered to Oak Ridge National Laboratory (ORNL) for independent validation testing. The system was installed on ORNL' dynamometer and testing commenced. The testing was limited to a maximum of 5,000 rpm due to the concern of rotor damage experienced on POC motor 1. In addition the testing was further limited due to an error in the control software input values that ultimately caused a partial demagnetization of the rotor. Results of these limited tests are shown in Figure 2-85.

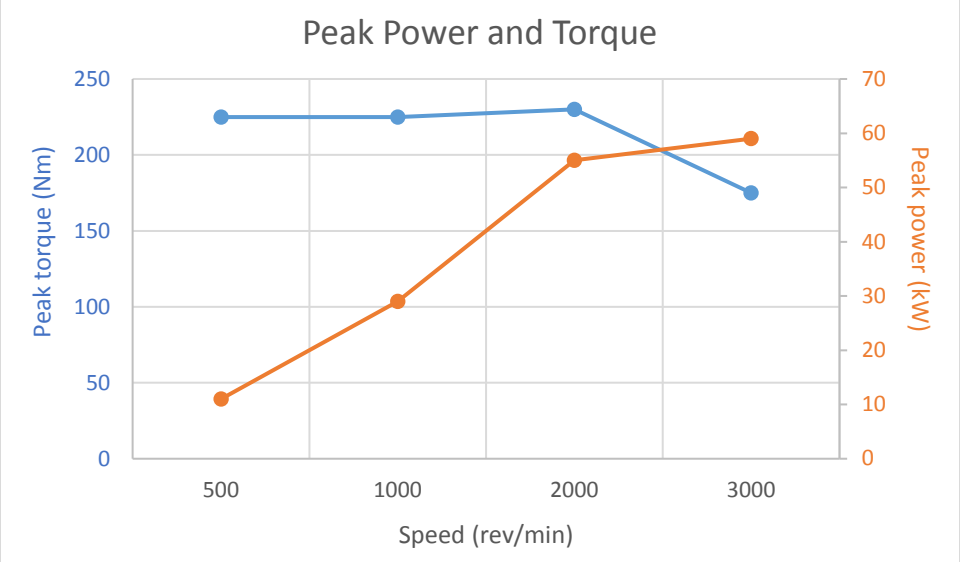


Figure 2-85: ORNL Test Results From POC Motor 2

From the limited testing done at ORNL the performance of the motor correlated with the results from the testing conducted on UQM's dynamometer.

Unfortunately, the time and budget did not allow for any further testing of either the POC or POD motors at ORNL.

Conclusions and Future Directions

UQM Technologies

From the lessons learned, results from the POC motor and the improvements made to the POD motor design UQM is confident the Lanthanide-free permanent magnet motor can be produced and will have performance comparable to the current permanent magnet motors using the "rare-earth" based magnets. In addition, a scaled-up version (120kW) has been shown to be feasible.

Ames Laboratory

The AlNiCo 8(X) magnet material developed by AMES provides further advantages to the Lanthanide-free permanent magnet motor. As mentioned additional funding and time will be required for AMES to produce and process adequate quantities of the magnets so that a motor can be build and tested. Alternative funding is being pursued for this effort.

National Renewable Energy Laboratory

The thermal management and heat transfer work that NREL conducted will be of great value in the next iteration of the Lanthanide-free permanent magnet motor design since removal of heat is critical to avoid an over temperature in the magnets resulting in demagnetization. In addition, this same information and results can be used in any of UQM's permanent magnet motor design, allowing for more removal of heat and a higher continuous rating.

Oak Ridge National Laboratory

Although ORNL was limited in their ability to test the POC and POD motors the results from these limited tests confirmed that the performance of Lanthanide-free permanent magnet motor can be on par with the typical permanent magnet motor using rare-earth magnets.

FY 2016 Presentations/Publications/Patents

1. Presentation - DOE Vehicle Technologies Office FY15 Kickoff Meeting (April 2016)

3 Power Electronics Research and Development

3.1 Electric Drive Wide Bandgap Power Electronics

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Contract No.: DE-AC05-00OR22725

Abstract/Executive Summary

The overall objective of this project is to design and develop a high-voltage–wide bandgap (WBG) 30 kW continuous, 55 kW peak power traction drive system including a dc-dc boost converter and a three-phase inverter. This project is targeted toward the application of WBG technology and novel circuit topologies with advanced packaging to address inverter cost, weight, volume, and efficiency goals. Specific research and development efforts in FY 2016 include new WBG device evaluation consisting of short circuit capability test and failure mechanism analysis; gate driver and protection function improvement for high-reliability, high-frequency, high-density boost converter design with advanced substrate layout and packaging techniques; and high-density three-phase inverter design. The new concepts developed under this project will increase the power density and decrease the volume and weight for electric vehicle traction-drive inverters and will achieve the DOE 2022 weight, volume, and efficiency targets.

Accomplishments

- Completed static and dynamic evaluation of a 600 V trench-type silicon carbide (SiC) metal oxide semiconductor field-effect transistor (MOSFET) and a 900 V SiC double-implanted MOSFET (DMOSFET)
- Completed short circuit capability evaluation and post-failure analysis of 600 V trench-type SiC MOSFET
- Completed module and heat sink design of a 30 kW WBG-based boost converter prototype using ORNL's WBG modules
- Completed design, build, and test of a gate driver with improved short circuit protection function
- Completed system level layout design of a 30 kW WBG-based liquid-cooled inverter.

Introduction

The need for high-temperature operation of power electronics in automotive applications is increasing. The ability of components to operate reliably at elevated temperatures can enable cost and weight savings by making it feasible to reduce the sizes of heat sinks and eliminate secondary cooling loops. Additionally, devices capable of increased-frequency operation can reduce requirements for passive components, leading to further reductions in cost, weight, and volume. WBG devices, specifically SiC and gallium nitride (GaN) semiconductors, are emerging technologies that enable operation at higher temperatures and frequencies with efficiency and reliability improvements. The development of WBG devices promises to help achieve cost, weight, and volume goals, as well as DOE Vehicle Technologies Office targets. WBG technology assessment performed under this project will help determine when a viable market introduction of these devices for automotive use will occur. The independent assessment of devices for the automotive industry is carried out to monitor progress and provide data readily when the need arises.

None of the electric drive vehicle traction drive systems on the market can meet cost and efficiency goals. Efficiency is achieved by using lower loss devices and materials, which tend to be expensive, even as quantity levels increase. A case in point is motor lamination steel, the lower loss grades of which are manufactured using novel processes that add more cost.

Problems associated with power electronics for advanced vehicle applications include the following.

1. Low efficiency at light load conditions for inverters and converters
2. Low current density and device scaling issues for high-power converters
3. Lack of reliable higher junction temperature devices
4. High cost of devices and power modules, especially for WBG and advanced silicon devices
5. High number of components for low-voltage electronics (e.g., gate drivers, controllers, sensors)
6. Lack of standardized high-power-density, low-cost power modules for scalable and modular power converters
7. Substrates that use expensive ceramics for thermal stability and reliability
8. Low-cost, low-loss magnetics and high-temperature films for capacitors

The goal of this research is to reduce the size and weight of power converters to meet the 2022 DOE inverter targets. The overall strategy for addressing the limitations of the state of the art is shown in Figure 3-1.

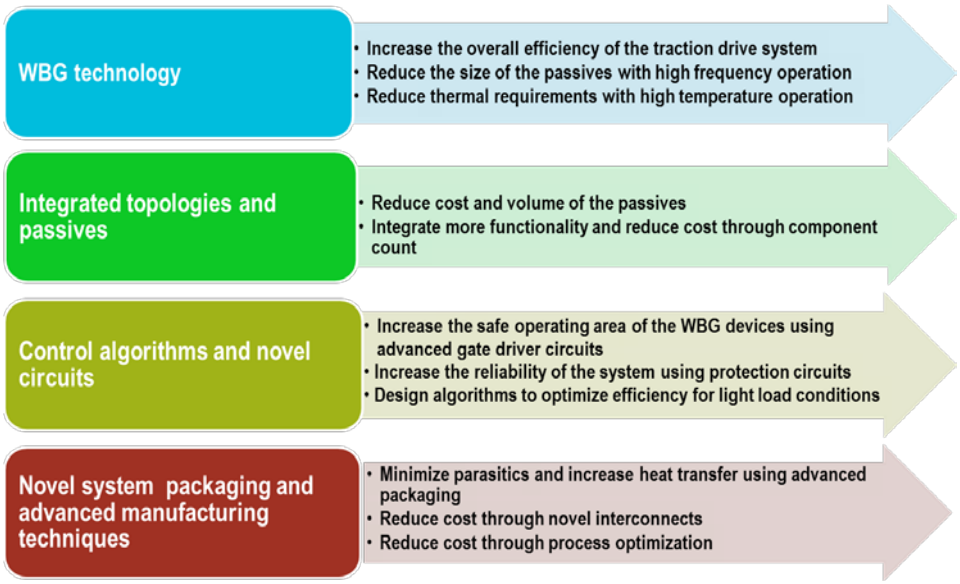


Figure 3-1: Overall strategy to address limitations of the state of the art.

Approach

The overall objective of this project is to design and develop a WBG 30 kW continuous and 55 kW peak power inverter. WBG devices offer some distinct advantages over their silicon components. Primarily, they can operate at higher junction temperatures. This benefit allows for hotter coolant and smaller heat sinks and can potentially facilitate air cooling without sacrificing performance. Many of the components in a typical commercial inverter cannot withstand the desired operating temperature of WBG devices (e.g., the capacitor and gate driver). Thus, the inverter as a whole must be considered in the development of new high-temperature packages.

The design innovations in this project include the following.

1. The design concept uses layers of high-temperature thermal insulating material to separate the low-temperature components from the high-temperature zone.
2. The design uses the high-temperature operating capability of WBG devices to enable air cooling and uses newer fast-switching SiC devices for high-temperature-liquid designs.
3. The heat sink design minimizes thermal resistance.
4. The design is optimized for the most frequently operated points.

These new concepts will increase the power density and decrease the volume and weight for electric-based vehicle traction-drive inverters and will achieve the DOE 2022 weight, volume, and efficiency targets. The specific approach to address the limitations of the state of the art is described in Figure 3-2.

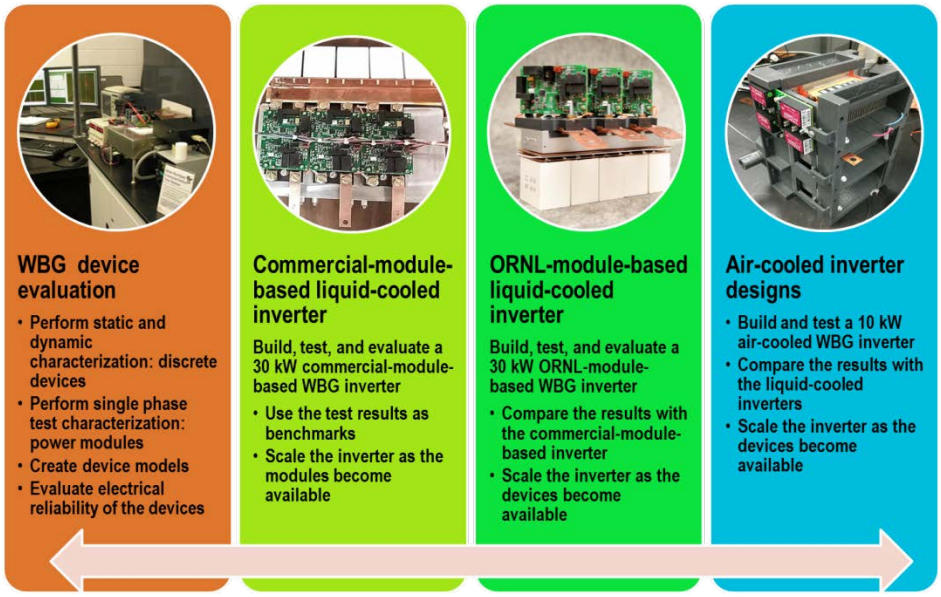


Figure 3-2: Specific approach to address limitations of the state of the art.

Results and Discussion

1. Device Testing

1.1 Static Characterization

The new WBG devices acquired this year are 650 V trench-type SiC MOSFET samples and 900 V SiC DMOSFET samples. On-state characteristics and switching energy losses of the devices were obtained over a wide temperature range. All the devices obtained were experimental samples. Static characterization, including output characteristics, body diode characteristics, third quadrant characteristics, and device capacitances, has been conducted for both devices. Due to space limitations, only the temperature-dependent output characteristics are included in this report, as shown in Figure 3-3.

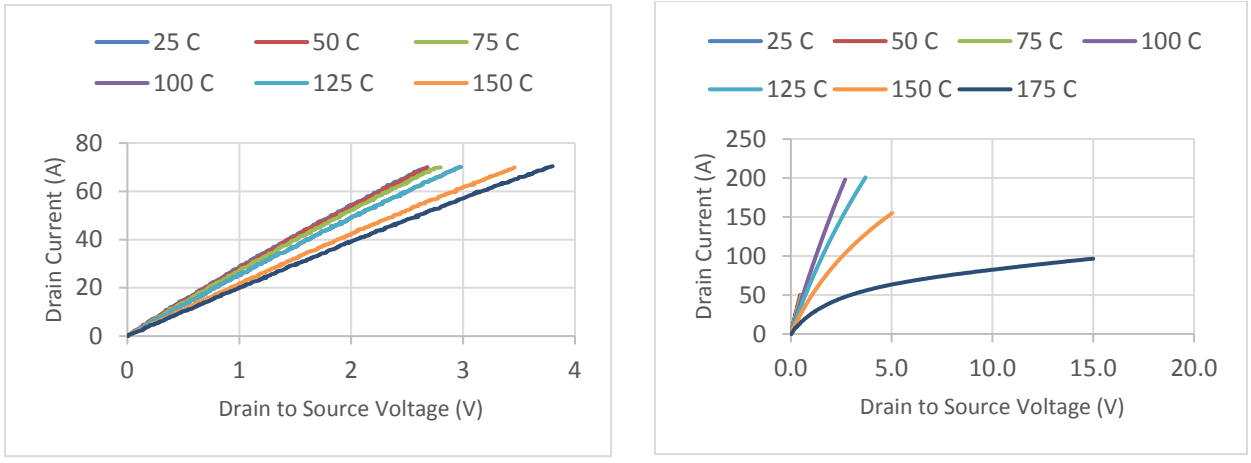


Figure 3-3: Temperature-dependent output characteristics of 600 V trench-type SiC MOSFETs (a) and 900 V SiC DMOSFETs (b).

The dynamic performance of both kinds of SiC MOSFETs is characterized by the "ORNL Wide Bandgap Device Evaluation Facility." Specifically, a universal double pulse power test setup is used to test their switching performance. The test setup has several advanced features such as (1) built-in solid-state circuit breaker for overcurrent and short circuit protection, (2) compatibility with silicon/WBG devices featuring various device packages (TO-220, TO-247, etc.), and (3) compatibility with different measurement methods (shunt, Pearson, current probe).

To maintain the consistency of the test, the same freewheeling diode (FWD), gate resistance, and gate voltage are used. A CREE C3D10170H is used as FWD. The inductance, gate resistance, and applied gate voltage parameters are as follows: 148 µH, 5 Ohm, and -2/+20 V. The gate driver used for this testing was a commercial gate driver chip with high-sourcing and high-sinking current capability.

1.2 Dynamic Characterization

The turn-on and turn-off switching energies for the 650 V trench MOSFETs at 400 V are shown in Figure 3-4, under 25°C and 175°C case temperatures. The switching energy for temperature variation is also plotted in Figure 3-5. The turn-on switching energy decreases with the increase of temperature while the turn-off energy increases with the increase of temperature.

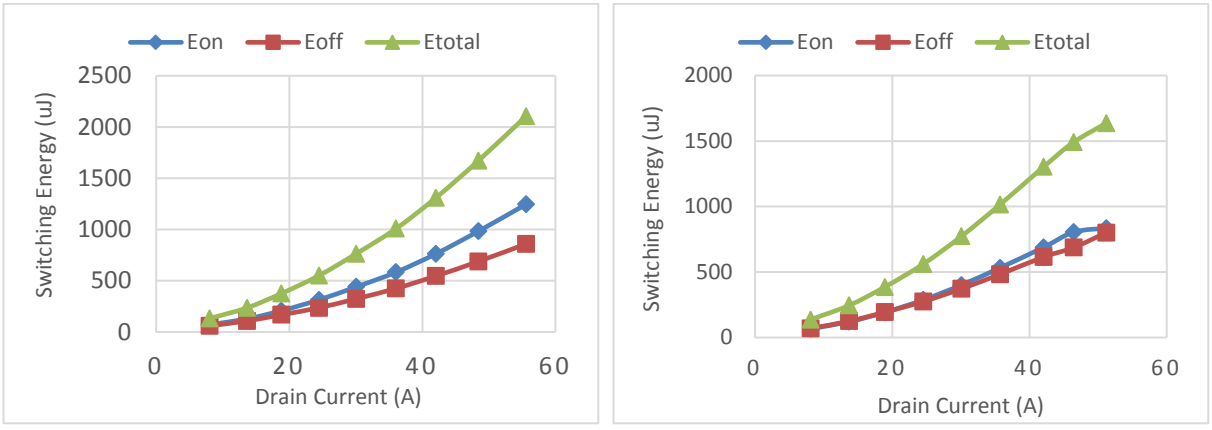


Figure 3-4: Turn-on and turn-off switching energies for a 650 V trench-type SiC MOSFET at 25°C and 400 V (a) and at 175°C and 400 V (b).

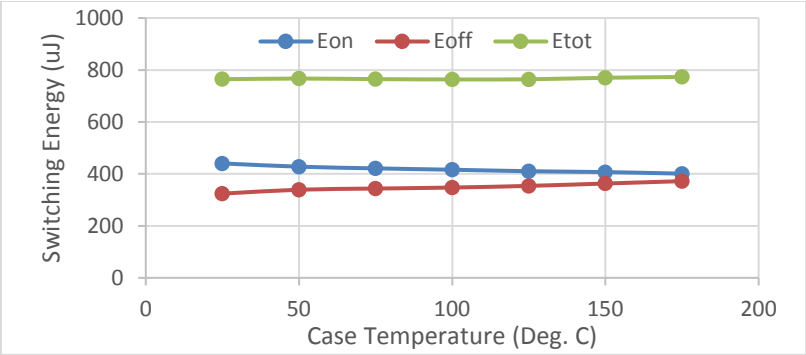


Figure 3-5: Switching energy as a function of temperature for a 650 V trench-type SiC MOSFET at 400 V.

The trench MOSFETs exhibit much lower total switching energy compared to DMOSFETs tested in previous years. Compared to the 1200 V trench SiC MOSFET tested in FY 2015, the trench MOSFET tested in FY 2016 provides higher switching energy. The main reason is that the 600 V trench device has much higher input capacitance.

The turn-on and turn-off switching energy for the 900 V SiC DMOSFET at 600 V dc bus voltage is shown in Figure 3-6 under case temperatures of 25°C and 175°C. The switching energy at 600 V bus voltage for temperature variation is also plotted in Figure 3-7. The turn-on switching energy reduces with the increase of temperature while the turn-off energy is increased with the increase of temperature.

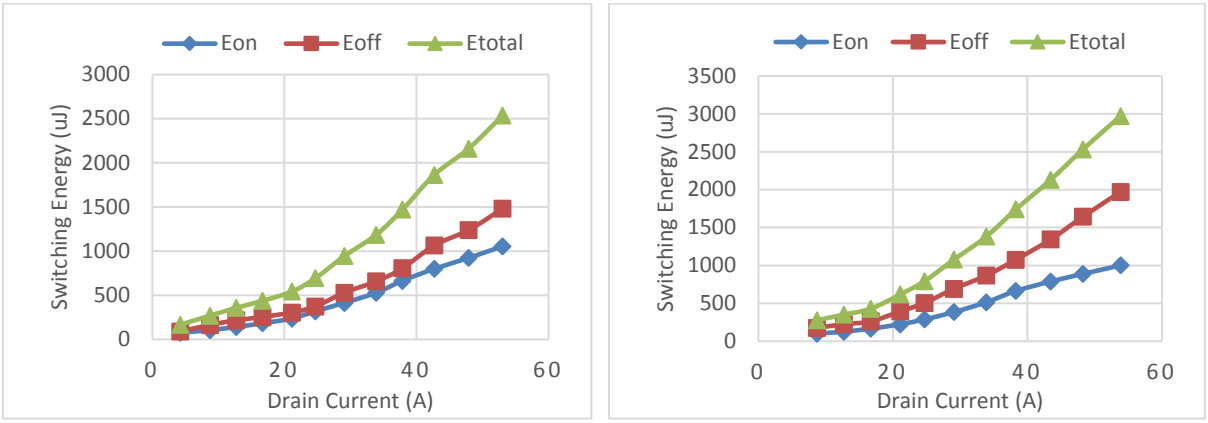


Figure 3-6: Turn-on and turn-off switching energies for a 900 V SiC DMOSFET at 25°C and 600 V (a) and 175°C and 600 V (b).

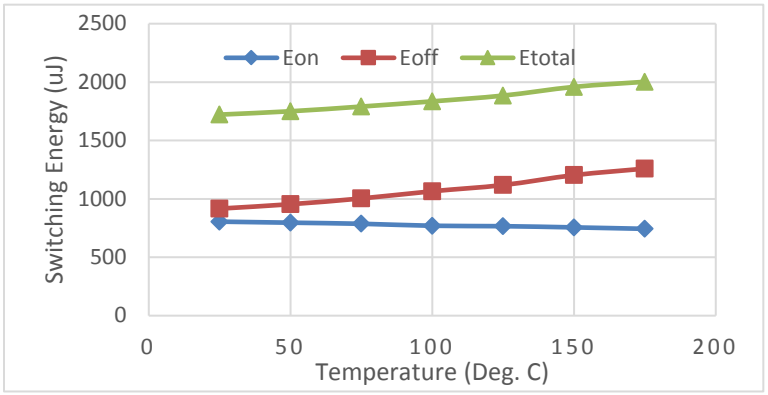


Figure 3-7: Switching energy as a function of temperature for a 900 V SiC DMOSFET at 600 V.

1.3 Short Circuit Test

The short circuit test provides a good understanding of device operation with the design of the protection circuit. Due to limited available research samples, the short circuit test is only conducted on 650 V trench SiC MOSFETs. The test setup is similar to the setup published in [1], [2]. The turn-off gate resistance is increased to 25 Ω to prevent avalanche failures caused by turn-off voltage spikes. The gate voltage is kept at the same level -2/+20 V (turn-off/turn-on). Because it is a 650 V trench device, the short circuit test is conducted with a dc bus of 300 V. For real usage realization, the short circuit test is conducted at 75°C and 100°C case temperatures.

During the short circuit test, two sets of short circuit tests are considered—protected and unprotected short circuit tests. The protected short circuit test is the scenario where the protection circuit can turn off the gate signal. The unprotected short circuit test is the scenario where the protection is not applied. The unprotected short circuit test is shown in Figure 3-8(a). The device withstands the short circuit current for about 20 µs. After 21 µs, thermal runaway is observed, which leads to very high current until the current is cut by a solid state dc circuit breaker.

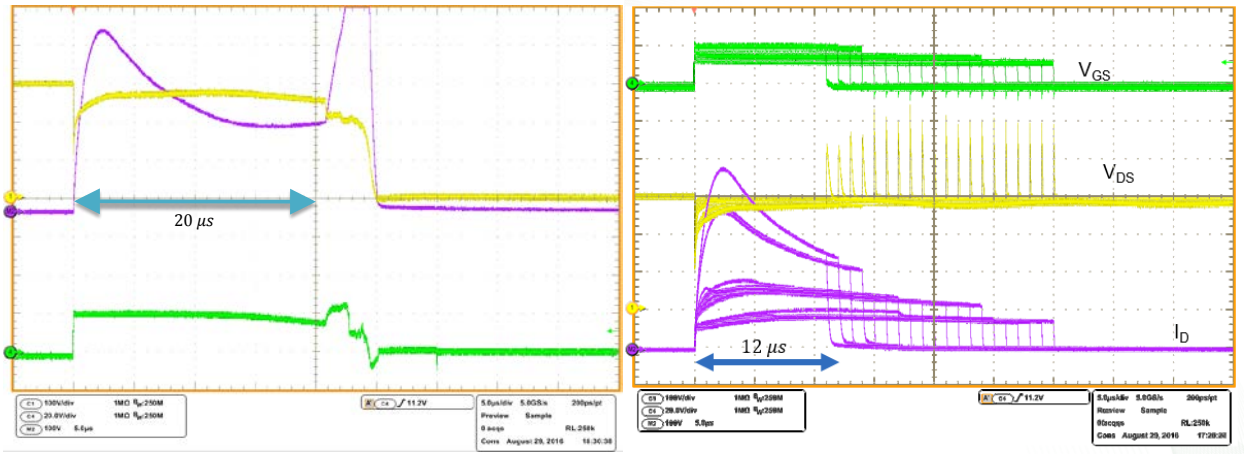


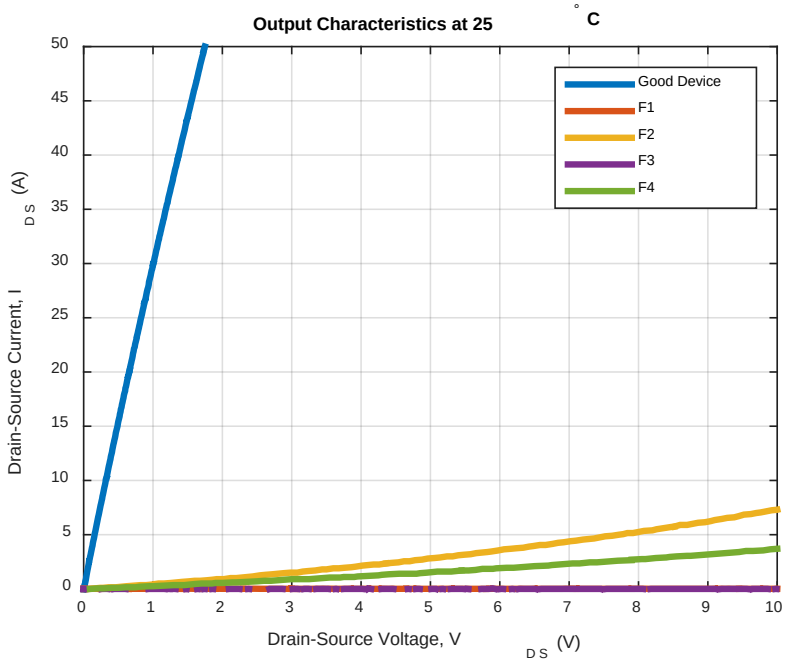
Figure 3-8: Short circuit test at 100°C with unprotected mode (a) and protected mode (b).

In the protected short circuit test [Figure 3-8(b)], the device is short circuited using a controlled gate pulse. The gate signal is gradually increased from 1 µs to 30 µs. The device presents consistent short circuit behavior before 12 µs, with a peak current of 470 A. With a short circuit pulse of 13 µs, the current peak value decreases to 380 A, and the saturation current also decreases. The possible reason is that the electron mobility of the device decreases with the increase of junction temperature. After 14 µs, the device degrades further and the bulk resistance increases. This phenomenon leads to further reduction of short circuit current. After 24 µs, the short circuit current is clamped to around 100 A.

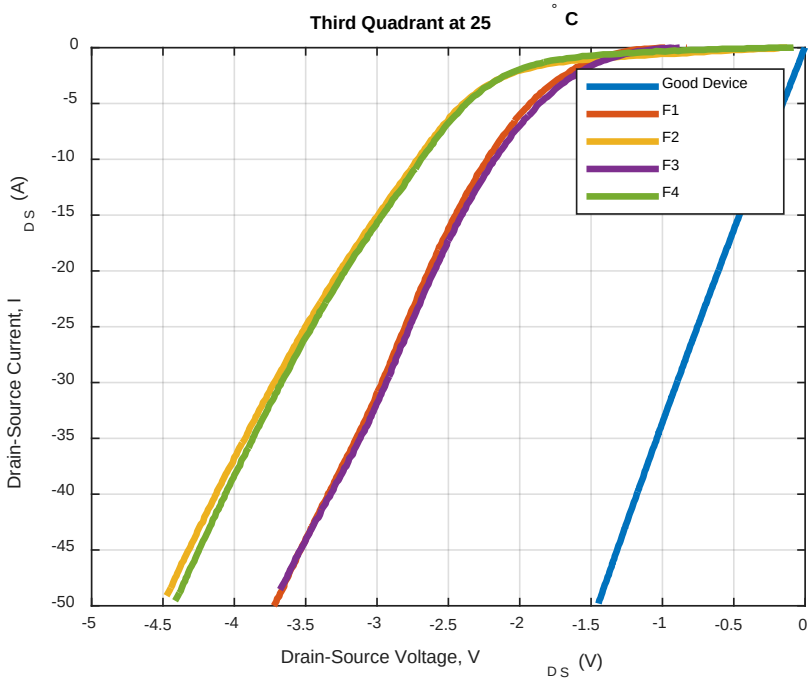
The test provides a very interesting example of the short circuit tolerance of the trench device. After the short circuit, the degraded devices show significantly increased drain-source impedance. This increased impedance effectively reduces the short circuit current, regardless of increased short circuit pulses. No delayed thermal runaway is observed during the gradual increase of the protective short circuit pulse. After conducting the short circuit test, the devices are labeled and saved for post-failure analysis. In the post-failure analysis, the damaged or degraded devices will be compared with a good device.

After conducting the short circuit test for both 75°C and 100°C for both protected and unprotected failure, static characteristics analysis is conducted to characterize the property changes of the device and get some idea of the damage that occurs for trench MOSFETs under these conditions. The post-failure analysis is performed at 25°C.

The output characteristic comparison in Figure 3-9(a) shows significant increase in the device on-resistance and when 20 V gate voltage is applied. The significant on-resistance increase indicates an open-circuit-like behavior of the devices. The output characteristics are also checked at 0 V for all the damaged devices. No current flow is observed for this condition. This is a fairly positive finding as it indicates the device did not cause a short path even after failure.



(a)



(b)

Figure 3-9: Comparison among failed devices: output characteristics (a) and third quadrant characteristics (b). F1 = protected short circuit test conducted at 75°C, F2 = unprotected short circuit test conducted at 75°C, F3 = protected short circuit test conducted at 100°C, and F4 = unprotected short circuit test conducted at 100°C.

The third quadrant characteristic indicates that the channel conduction has been significantly impacted. For the F1 and F3 samples, the gate has a small amount of control, a very small current is flowing through the channel, and most of the current is flowing through the body diode. For F2 and F4, which suffered unprotected short circuit failure, the channel conduction has been lost and the body diode conducts all the current.

2. Gate Drive/Protection Improvement

A two-channel gate drive board has been designed based on the available commercial gate drive chips for the SiC power module. In the design of the gate driver, in addition to meeting the basic driving requirements of SiC MOSFETs (e.g., sourcing and sinking current, positive/negative voltage level, power consumption), several key issues associated with the high switching speed of SiC devices are considered. First, an auxiliary circuit is designed to suppress the crosstalk phenomenon for the phase-leg module, and the switching power loss can be reduced with less or no cross-conduction between the upper and lower side switches. Second, a soft turn-off circuit is used to safely cut off short circuit current without causing avalanche breakdown.

In the layout design, the gate driving loops are minimized to lower the gate loop inductance, thus reducing gate voltage oscillations during fast switching transients. The power copper plane and signal copper plane are designed to be well separated so that the induced printed circuit board parasitic capacitance, degrading switching performance, can be eliminated.

Another key improvement on the gate driver is the flexible shut down mode for desaturation protection, as shown in Figure 3-10. For the adopted commercial SiC MOSFET gate driver, there is no permanent shut down function, and the maximum fault output holding time of the chip is around 200 ms. Users must rely on the central controller to permanently shut down the converter, which is not reliable under strong electromagnetic interference and solid fault conditions. To address this issue, an auxiliary control circuit is added to realize local shut down. (The circuits involved will be discussed in detail in a future publication.)

Figure 3-11 illustrates the protection mode of the desaturation function without and with the auxiliary control circuit. As can be seen from the testing results, when the desaturation protection function is triggered, the pulse width modulation (PWM) signal is blocked for around 200 ms. However, after the holding duration, the PWM signal is reactivated automatically. For a solid short circuit condition, this protection mode causes periodic short circuit current and protection activation for semiconductor devices, and eventually the devices will be degraded and damaged due to thermal fatigue. With the developed auxiliary control circuit, gate drive can be shut down locally (i.e., holding fault status permanently), as shown in Figure 3-11(b). Any short circuit fault condition in the inverter will be detected, and semiconductor devices and inverters will be protected locally, without notifying the central digital controller.

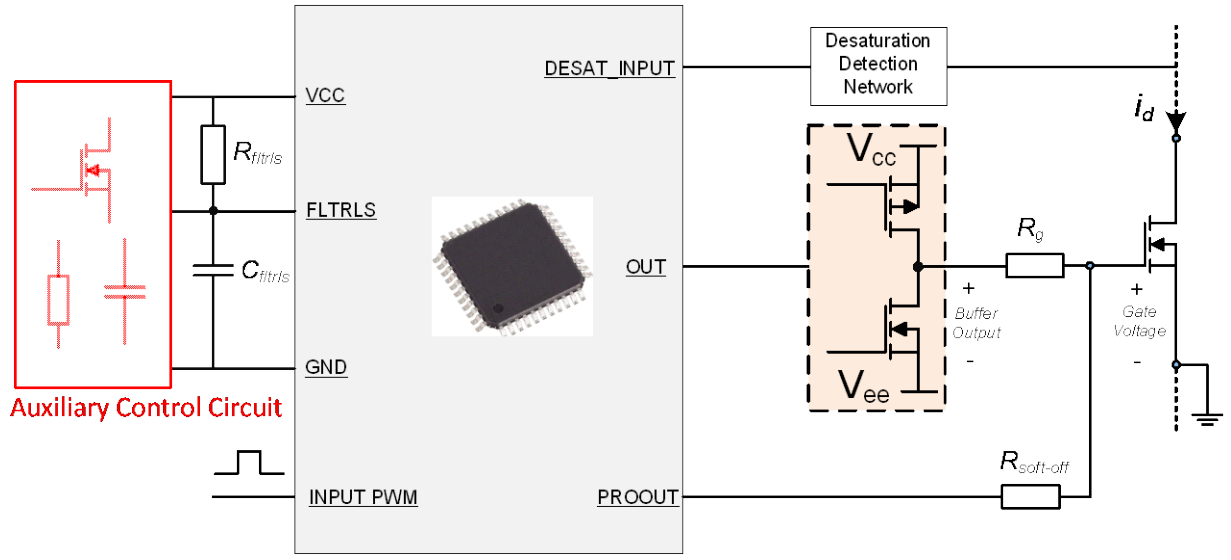
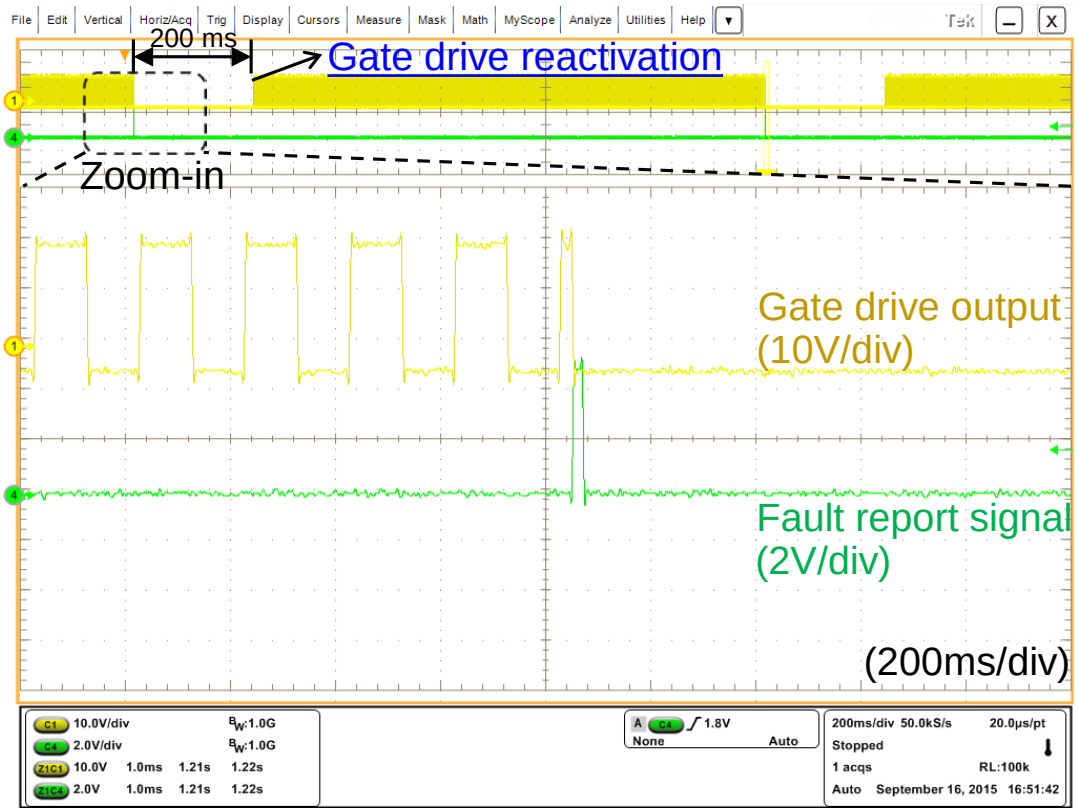
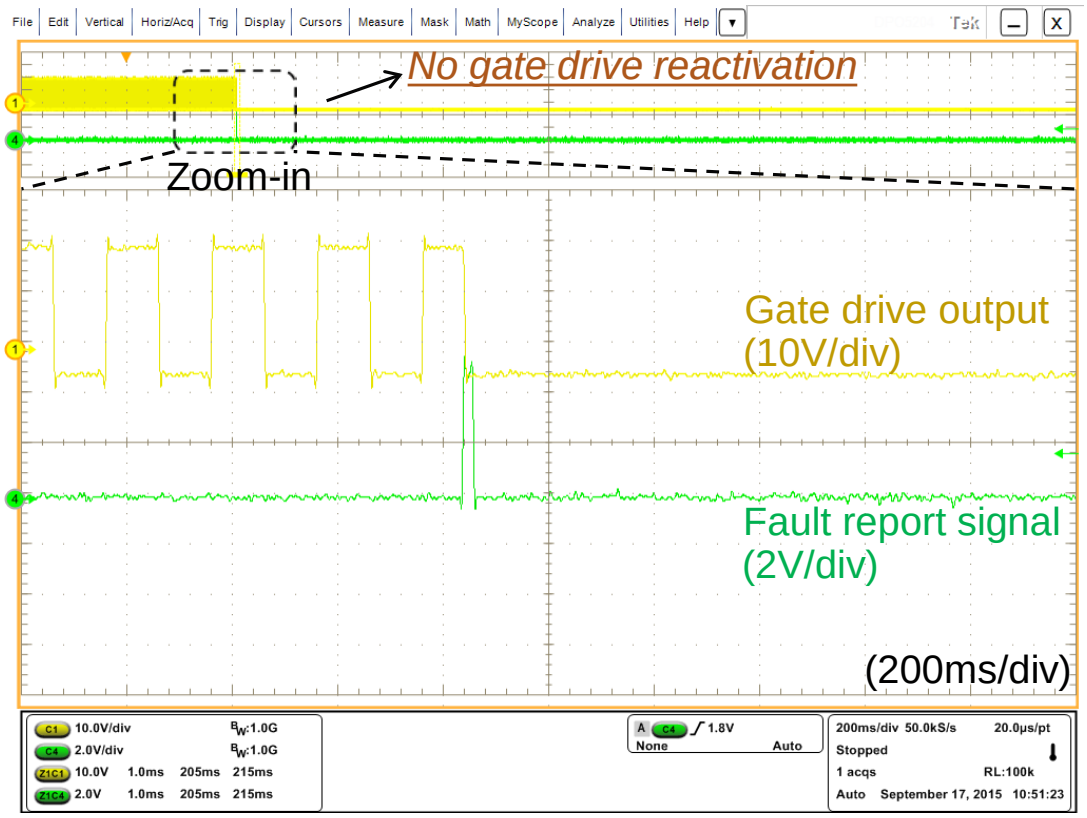


Figure 3-10: Commercial gate drive chip with auxiliary control circuit.



(a)



(b)

Figure 3-11: Desaturation protection mode without auxiliary control circuit (a) and with auxiliary control circuit (b).

3. WBG Inverter Design and Development

Device packages able to withstand high temperatures are required to take advantage of the high-temperature operating capability of WBG devices. Various organizations are working on high-temperature packaging for high-temperature devices. Several high-temperature packages, which include discrete device packages for power modules, have been reported in the past several years. Novel packaging concepts focus primarily on improving the existing packages or on designing new packages using new materials and or processing techniques for better reliability and performance. Even though the novel packages enable the devices to work at higher temperatures, theoretical advantages such as the current density of WBG devices are not realized because of the limitations of the interconnects needed for the power module to access the device terminals. In addition, the novel device packages need further development to be used in full systems.

Other factors that prevent system designers from reaping the benefits of WBG technology are the low-voltage electronics and the passive components. This is because even though the packages and the power devices can handle high temperatures, the low-power electronics that drive the power devices, silicon-on-insulator (SOI)–based technologies, are limited to a maximum temperature of 200°C. Silicon-based electronics are limited to 125°C operating temperatures. Although SOI-based electronics can work at up to 200°C, they are expensive. High-temperature (over 200°C) electronics have been reported as being feasible; however, as they have not been built, their performance capabilities are still in question. It could be many years before a logic-level high-temperature transistor can be built. This time lag creates a void in the power module industry, especially for intelligent power module products, which include the electronics inside the module.

Similarly, the passive components in an inverter have lower operating temperatures and cannot be operated in close proximity to high-temperature WBG devices. This situation leads to an increase in the volume and a reduction in the power density of the system. High-temperature passive components are currently being developed to address the high-temperature-operation requirement. However, as with the electronic components, they will be much more expensive than the low-temperature components.

To address these problems, a system-level approach for packaging design needs to be developed. Complex 3-dimensional (3-D) packaging structures with integrated interconnects can reduce the required assembly steps and increase the power densities of power electronic systems. Recent advancements in additive manufacturing (AM) promise an exciting future, with WBG technology making inroads in the power electronics industry. AM techniques enable the development of complex 3-D geometries that will result in size and volume reductions at the system level by integrating low-temperature components with high-temperature active devices and reducing the material needed to build the heat exchangers in inverters. ORNL has developed expertise in AM in the last few years. ORNL's Power Electronics and Electric Machinery team recognized the potential of this technology for power electronics system packaging and took the first step toward achieving a completely printed inverter concept.

A 10 kW all-SiC inverter incorporating an aluminum-based printed power module with an integrated cooling system and a printed plastic lead frame was built using AM techniques. By leveraging previous research achievements, this project aims at the design and development of a high-power (>30 kW), high-frequency (>50 kHz) boost converter to meet the 2022 power density target. To develop the boost converter, high-frequency, high-density WBG power modules capable of high switching speeds need to be designed as a first step. To meet this requirement, a 1200 V, 200 A, all-SiC module, discussed in the following sections, is being designed.

Power Module

The phase-leg power module uses research samples of trench SiC MOSFETs and commercial SiC Schottky diodes. To reach the rated current, six MOSFETs and three diodes are paralleled in each switch position. Figure 3-12 shows the circuit schematic and layout design of the power module.

The phase-leg power module is built on a single substrate soldered onto the flow channel. The aluminum flow channel is electrically insulated from the positive (P terminal) and negative (N terminal) dc bus by the aluminum nitride substrate. The phase trace (O terminal) of the direct-bonded copper (DBC) is connected to the external inductor, as seen in the mechanical layout diagram. In the design of the DBC layout, the following key considerations are taken into account.

1. All semiconductor devices are integrated into one substrate, and decoupling capacitances are embedded for small switching commutation loop, and thus low-power loop, parasitic inductances. Also, the embedded decoupling capacitances can potentially help to suppress electromagnetic noise issues during continuous operation.
2. The "P-cell–N-cell" concept [3] is adopted to minimize the power loop parasitic inductance for high-frequency operation. The switching commutation loops between high-side MOSFETs and low-side diodes, and high-side diodes and low-side MOSFETs, are the main targets to be shrunk.
3. Lossy devices (i.e., lower MOSFETs) are located in the center of the module to improve thermal performance.

The power loop parasitic inductances and current distribution of the designed substrates are obtained through finite element analysis (FEA) simulation using the ANSYS Q3D Extractor. According to the simulation results, the lumped parasitic inductance is 4.11 nH for the high-side MOSFET and low-side diode commutation loop and 3.44 nH for the high-side diode and low-side MOSFET loop, as shown in Figure 3-13. Moreover, current is evenly distributed within both switching loop areas, as shown in Figure 3-14.

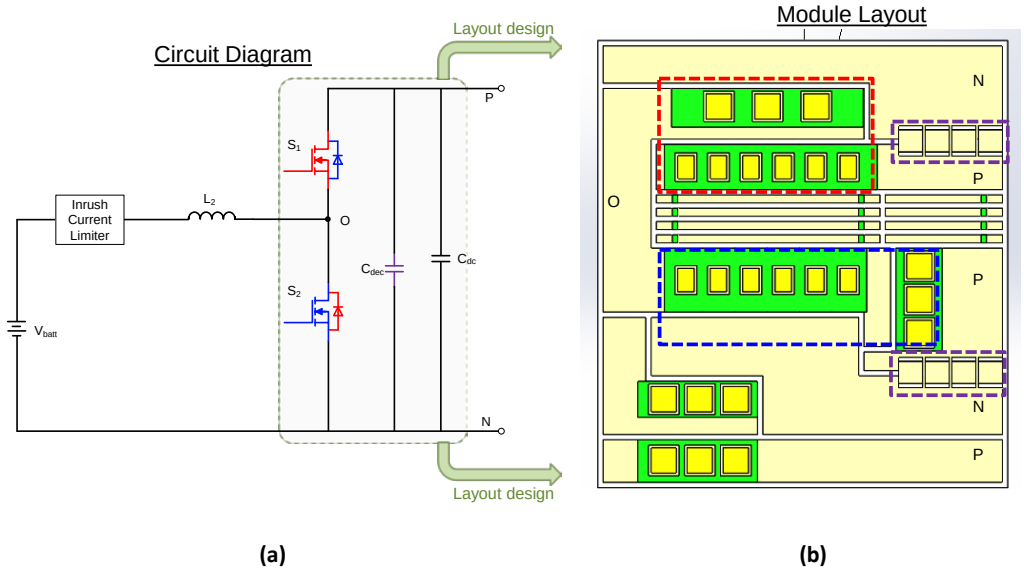


Figure 3-12: Boost converter diagram (a) and DBC layout design of the power module (b).

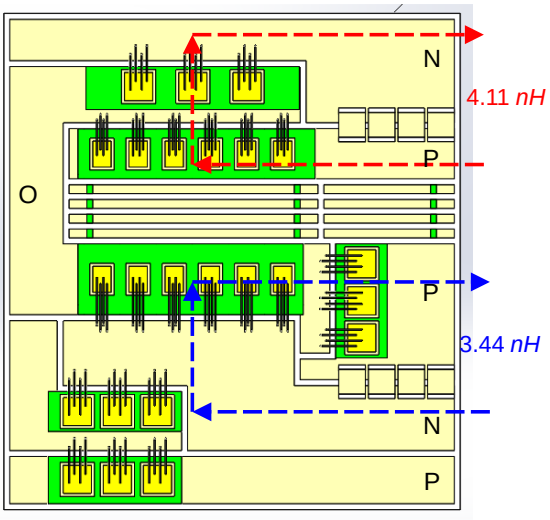


Figure 3-13: Power loop parasitic inductance of the boost module.

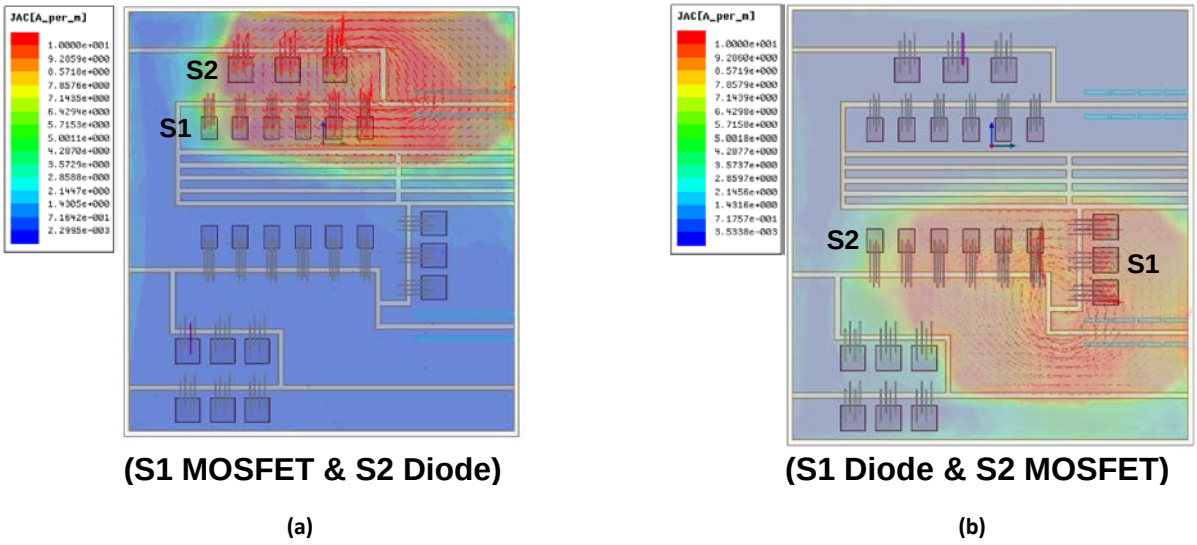


Figure 3-14: Current distribution of the boost module: S1 MOSFET and S2 diode (a) and S1 diode and S2 MOSFET (b).

Heat Sink

A genetic algorithm (GA) –based approach is applied for designing heat sinks based on total heat generation and dissipation for a prespecified size and shape. This approach combines random iteration processes and GAs with FEA to design the optimized heat sink. With an approach that favors "survival of the fittest," an optimal heat sink can be designed uniquely for this particular boost converter.

For the boost converter heat sink design, four main steps are included: initialization, evaluation and selection, crossover and mutation, and reproduction. The initialized population is implemented by the random walking process. In a nutshell, with a predefined inlet and outlet position, one branch of channels is created by separate steps, with random direction and random step distance, under predefined constraints. Multiple branches of channels together become an individual. As a corresponding, the direction and distance data are the chromosome, the FEA heat sink geometry in COMSOL is the character, and the evaluated maximum junction temperature by the right-hand side COMSOL simulation process is the fitness value. Based on individual chromosome and fitness values, better ones have higher survival possibility, and as a result, the optimal result will evolve itself iteration by iteration. Eventually, after certain iterations, the best result can converge as shown in Figure 3-15.

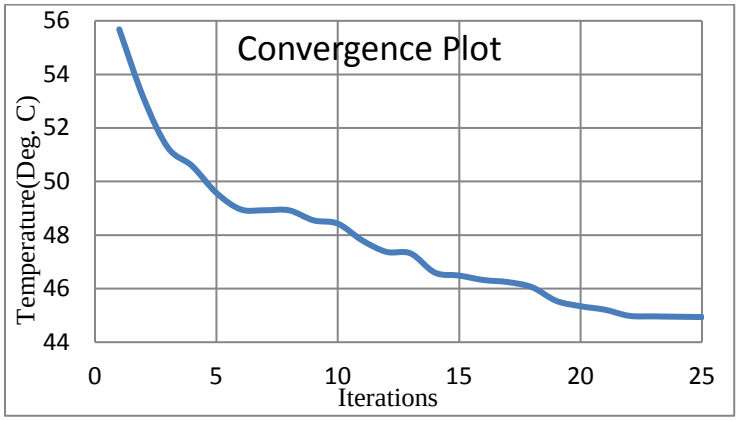
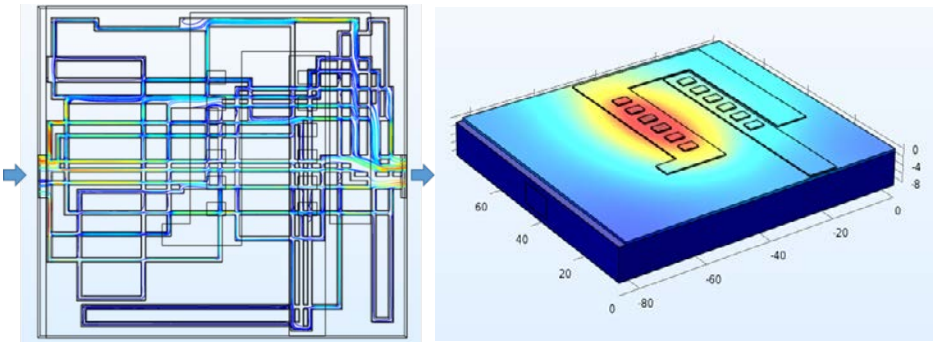


Figure 3-15: Convergence plot of the heat sink optimization.

The final optimized heat sink with the streamline plot and the temperature map of the heat sink with the designed power module are shown in Figure 3-16. According to the simulation results, the maximum junction temperature is about 103°C and the overall heat sink volume is 86 mm × 77 mm × 8 mm, which is about 53,000 mm³; the total weight is about 120 g.

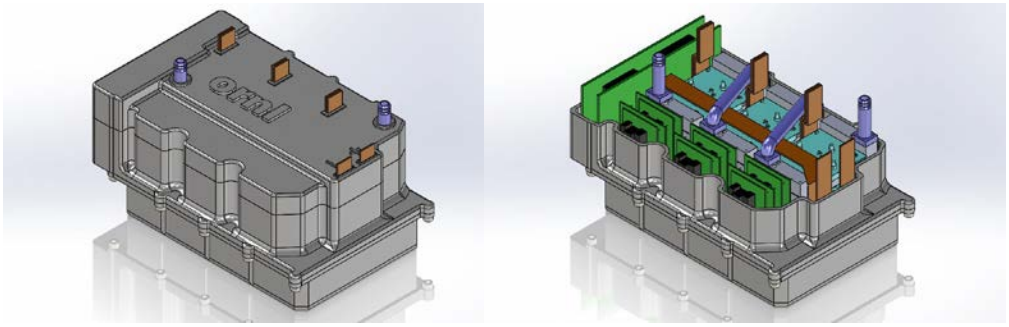


(a) (b)

Figure 3-16: Simulation results for the optimized heat sink: streamline plot (a) and temperature distribution (b).

Inverter Layout

A 30 kW all-SiC three-phase inverter is also under development using commercially available 1200 V SiC MOSFET modules. The layout of the inverter is shown in Figure 3-17.



(a) (b)

Figure 3-17: Conceptual 3-D drawing of the 30 kW three-phase liquid-cooled inverter: overview (a) and uncovered view (b).

Commercially available gate drivers from Rohm will be used. The performance of the power module will be evaluated before the inverter is built. The modules are mounted on the cold plate, with thermal grease as the heat transfer medium, from the lower side of the power modules. This prototype model will be packaged as shown in Figure 3-17, with controls and capacitors packaged close to the heat sink. The capacitors used in this design are not a brick type but small individual capacitors in series to ensure better cooling and reduced costs. The key advanced features of this new design include lower convection thermal resistance by using a new optimized 3-D–printed cold plate, higher power density compared to the previous 30 kW liquid-cooled inverter, and modular design (wire-bond module, cold plate, bus bars, etc.) for easy fabrication.

Conclusions and Future Directions

The electric drive inverter R&D activities in FY 2016 include performance evaluation of the latest WBG devices; gate drive and protection function improvement; and high-frequency, high-density boost converter and three-phase inverter design. The WBG device evaluation results, including static, dynamic, and short circuit characterization, provide realistic data for design of reliable high-density inverters. The improvement in protection function further ensures robust operation of the WBG inverters under development. The innovative power module design results in low-switching commutation loop inductance, enabling full exploitation of WBG power device capabilities such as fast switching speed. In addition, the heat sink optimization based on GA has resulted in reducing thermal impedance. The benefits gained from these innovations can lead to high-efficiency, high-density system operation beyond the limits of state-of-the-art technologies.

WBG device evaluation will continue until the technology is transitioned to industry. The innovative technologies used in FY 2016 design work will be demonstrated to show the improvement in power density

and reliability. The testing results will also show that WBG technology will aid in achieving U.S. DRIVE targets for volume, efficiency, power density, and system costs.

FY 2016 Presentations/Publications/Patents

1. Zhiqiang Wang, Madhu Chinthavali, and Steven Campbell, "Characterization and comparison of planar and trench silicon carbide (SiC) power MOSFETs," *ECS Transactions*, PRiME 2016/230th ECS Meeting, accepted for publication in October 2016.
2. Madhu Chinthavali, "Additive manufacturing technology for power electronics applications," presented at the industry sessions on 3D Power Packaging, IEEE Applied Power Electronics Conference and Exposition, March 2016, Long Beach, California.
3. Madhu Chinthavali, "Electric drive inverter R&D," presented at the 2016 DOE Vehicle Technologies Office Annual Merit Review, June 2016, Washington, DC.
4. Madhu Chinthavali, "Future of semiconductor technology development," presented at the 2016 DOE Vehicle Technologies–EDT Industry Engagement Meeting, August 2016, Knoxville, Tennessee.

References

1. Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, F. Wang, and B. J. Blalock, "Design and performance evaluation of overcurrent protection schemes for silicon carbide (SiC) power MOSFETs," *IEEE Transactions on Industrial Electronics*, **61**(10), pp. 5570–5581, October 2014.
2. Z. Wang et al., "Temperature-dependent short-circuit capability of silicon carbide power MOSFETs," *IEEE Transactions on Power Electronics*, **31**(2), pp. 1555–1566, February 2016.
3. S. Li, L. M. Tolbert, F. Wang, and F. Peng, "Stray inductance reduction of commutation loop in the P-cell- and N-cell-based IGBT phase-leg module," *IEEE Transactions on Power Electronics*, **29**(7), pp. 3616–3624, July 2014.

3.2 Wide Bandgap Converters and Chargers

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Contractor: UT-Battelle, LLC, managing and operating contractor for ORNL
Contract No.: DE-AC05-00OR22725

Abstract/Executive Summary

- The overall objective of this project is to develop low-cost, high-efficiency, high-power-density all–wide bandgap (WBG) dc-dc converters and onboard chargers (OBCs). The goal is to reduce charger converter cost by 50% and weight and volume by a factor of 2 compared with the state of the art and to provide charger efficiency of more than 96%.
- A major objective for FY 2016 was to develop a gallium nitride (GaN)–based charger dc-dc converter. A compact, lightweight, highly efficient, 6.6 kW isolated three-port charger converter was designed and built using the latest GaN Systems GaN transistors; a three-dimensional (3-D) printed cold plate; high-voltage (HV) heavy copper printed circuit board (PCB) power planes; low-voltage (14 V), high-current PCB power planes; and a planar transformer. The prototype has a power density of 10.5 kW/L and specific power of 9.6 kW/kg. The volume and weight were reduced, respectively, to 47% and 21% of that of a silicon (Si) –based counterpart. Testing and characterization of the prototype was successfully completed, with the results showing greater efficiency than the Si-based counterpart, even at 2.5 times the switching frequency.
- Another objective for FY 2016 was to integrate the GaN charger converter with a silicon carbide (SiC) traction drive system to test and characterize the functionality as an OBC at the level 2 charging power of 6.6 kW. To this end, the isolated GaN charger dc-dc was integrated with a 100 kW segmented traction inverter that uses commercial SiC metal oxide semiconductor field-effect transistors (MOSFETs) and 3-D printed components. Testing and evaluation of the integral onboard charging functionality was successfully completed at power levels up to 6.6 kW.
- Test results on magnetic cores that were three dimensionally printed using nanocomposite magnetic powders revealed issues with the current printing process and possible future work to address these issues was identified.

Accomplishments

- Completed design for a 6.6 kW charger converter using the latest GaN transistors manufactured by GaN Systems Inc.; a 3-D-printed cold plate; HV heavy copper PCB power planes; low-voltage (14 V), high-current PCB power planes; and a planar transformer. Completed building and testing a prototype with a power density of 10.5 kW/L and specific power of 9.6 kW/kg. Comparing the prototype to a Si-based counterpart, the GaN-based converter achieved the following:
  - 50% reduction in volume
  - 75% reduction in weight

    - peak efficiency of 99% vs. 98.4% for the Si-based counterpart (even at a 2.5 times higher switching frequency).
- Successfully tested an integrated OBC using the 6.6 kW GaN charger converter and a 100 kW segmented traction drive system that was built using SiC MOSFETs. An improvement of 2.2 percentage points in charger system efficiency over a Si-based counterpart was observed.
- Completed testing and evaluation of magnetic cores that were 3-D printed at ORNL's additive manufacturing facility using nanocomposite magnetic powders produced by Aegis Technology Inc. Test results indicated very low core losses but a small relative permeability of 2. Future work needs to focus on increasing the relative permeability by reducing the air gaps in the cores.

Introduction

Most plug-in electric vehicles (EVs) and battery EVs on the market use a stand-alone OBC to charge the HV traction battery packs. However, a stand-alone OBC is not cost-effective because of its large number of components. Moreover, its performance in terms of weight, volume, and efficiency is limited by the operating frequency capabilities of existing Si-based semiconductor and magnetic materials. Bulky and expensive passive components, including inductors, capacitors, and transformers, are needed in OBCs because of low switching frequencies with Si switches (< 100 kHz) at power levels of several kilowatts and low saturation flux densities (~0.3 T) and high core losses at high frequencies with soft ferrite magnetic materials. As a result, OBCs (1) add significant cost (~$106/kW), (2) have low power-density and specific-power numbers (~0.6 kW/kg, ~0.8 kW/L), (3) are relatively inefficient (85–93%), and (4) are unidirectional (i.e., can charge the battery but are incapable of vehicle-to-grid support, a highly desirable function in future smart grids).

The problems and limitations of existing Si-based OBC technology are addressed in this multiyear project by using WBG devices, advanced magnetic materials, and novel integrated charger topologies and control strategies to significantly increase power density, specific power, and efficiency at lower cost. Emerging WBG devices—including those made with SiC and GaN—and advanced soft magnetic materials enable significant improvements in ac-dc and dc-dc converters, major components of OBCs. Their ability to operate with reduced conduction and switching losses over higher frequencies and temperatures minimizes requirements for the passive components and reduces cooling demands. In addition, a novel control strategy developed under this project and reported in the FY 2014 annual report was shown to reduce the dc link capacitor (the largest single component) in the ac-dc stage by 60%. Because passive components currently contribute more than 30% to the charger cost, weight, and volume in state-of-the-art Si-based technology, the approach proposed in this project provides enabling technologies to produce low-cost, light, compact, and highly efficient OBCs and converters.

Approach

Our strategy to address the problems of state-of-the-art OBCs and dc-dc converters is multifold.

- Push the envelope on functional integration of the traction drive, 14 V dc-dc converter, and OBC
- Take up the challenge of introducing WBG materials, specifically GaN, into automotive applications to determine what performance, packaging, cost, and efficiency benefits can be gained
- Perform analysis, modeling, and simulation that lead to a functional prototype meeting VTO OBC specific power, power density, and efficiency requirements while significantly reducing the current cost levels
- Design, build, test, and demonstrate prototypes
- Work with U.S. DRIVE to develop insights and lessons learned from the automotive community pertinent to dc-dc converters and OBCs
- Collaborate with industry stakeholders, universities, and other national laboratories to maximize the impact of this work.

Three technical approaches, based on converter topology, advanced semiconductor and magnetic materials, and control strategy, are being pursued. First, in power conversion topology, integrated bidirectional WBG OBCs (Figure 3-18) are being developed that (a) use traction drive inverters and motors as part of the charger

converter, (b) provide galvanic isolation, (c) provide an integrated function for dc-dc conversion of HVs to 14 V, and (d) use soft switching at the dc-dc stage to reduce electromagnetic interference and improve efficiency. A key component in the proposed technology is a WBG isolation converter that is used to charge not only the HV traction battery but also the 14 V battery for vehicle accessory loads. It includes a high-frequency transformer, dc filters, and WBG switches (Figure 3-19).

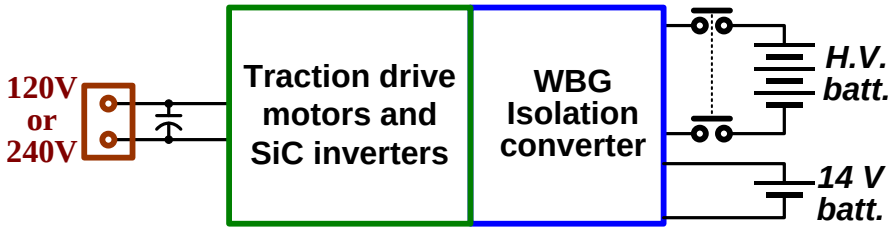


Figure 3-18: Conceptual diagram of an integrated OBC.

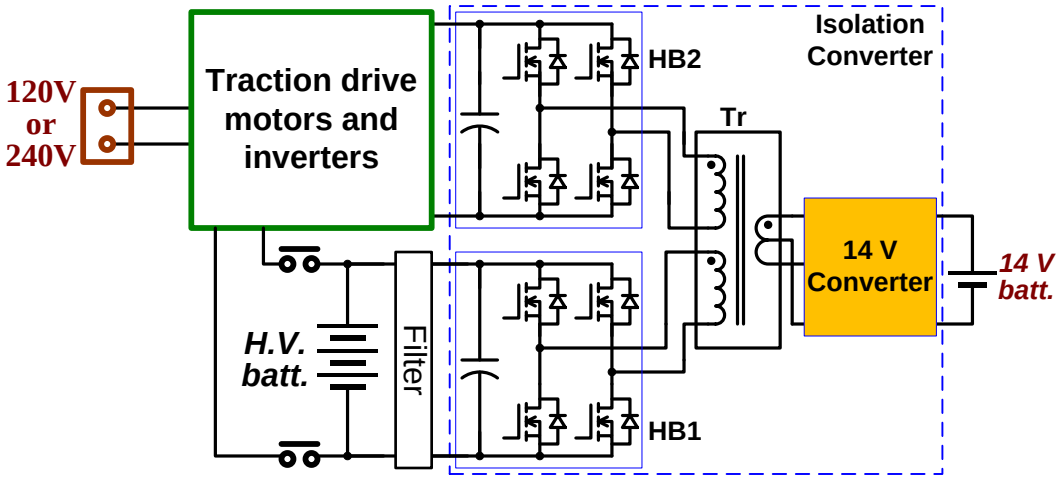


Figure 3-19: Proposed integrated OBC using a three-port isolation converter.

Second, increasing power density and specific power without compromising efficiency is being aggressively pursued by exploiting high switching frequency with WBG devices (especially GaN switches) and using advanced soft magnetic materials (nanocomposites) to drastically reduce the cost, weight, and volume of the ac and dc filters and isolation transformer. Because the availability of WBG power modules is limited, SiC and GaN devices are purchased or obtained directly from device vendors; they are tested, characterized, and packaged for use in converter design and prototype development. Prototypes will be built and tested, first using SiC devices—for which wafer processing and device fabrication technologies have advanced to a stage such that SiC MOSFETs and other switches are available commercially—and then GaN switches as that technology matures and devices with high current ratings become available.

Finally, a control strategy for the isolation converter has been developed to shrink the bulky dc link capacitor. Without adequate control, this bulky capacitor is necessary to filter out the large voltage ripple—with twice the grid supply frequency—inherent in single-phase ac-dc converters. The proposed control strategy enables a 60% reduction in the ripple current and thereby a significant size reduction in the bulky dc link capacitor in the front ac-dc converter.

Figure 3-19 shows a proposed integrated OBC that uses the traction drive as the OBC front converter and a three-port isolation converter for charging both the HV propulsion battery and the 14 V accessory battery. The three-port isolation converter uses dual active H-bridge converter with soft switching and synchronous rectification and shares the converter (HB1) and transformer with the 14 V battery charger. The proposed integrated OBC is capable of bidirectional power flow, a desirable function for smart grid applications.

The proposed integrated OBC is flexible and can be applied to most traction drive systems, including (a) single/dual inverter and motor (Figure 3-20), (b) segmented inverter traction drive (Figure 3-21), and

(c) systems with a boost converter (Figure 3-22). Moreover, the isolation converter can be applied to stand-alone OBCs (Figure 3-23).

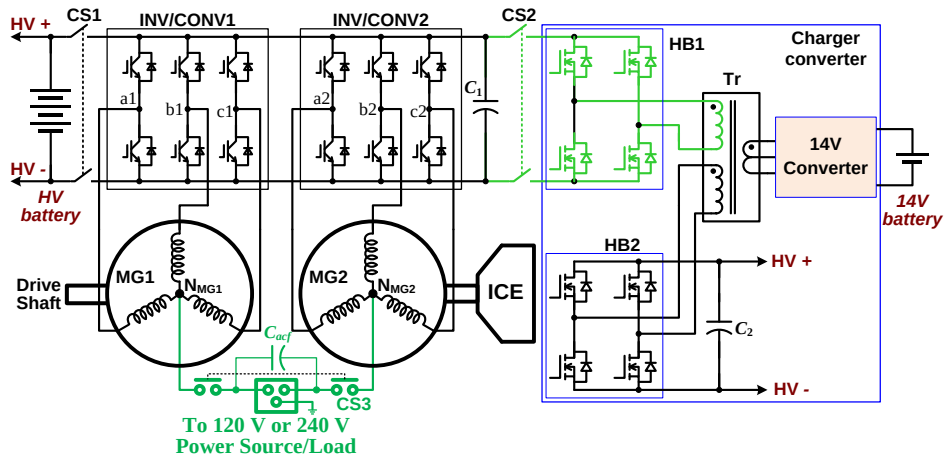


Figure 3-20: Integrated OBC applied to traction drive system with dual inverter and motor.

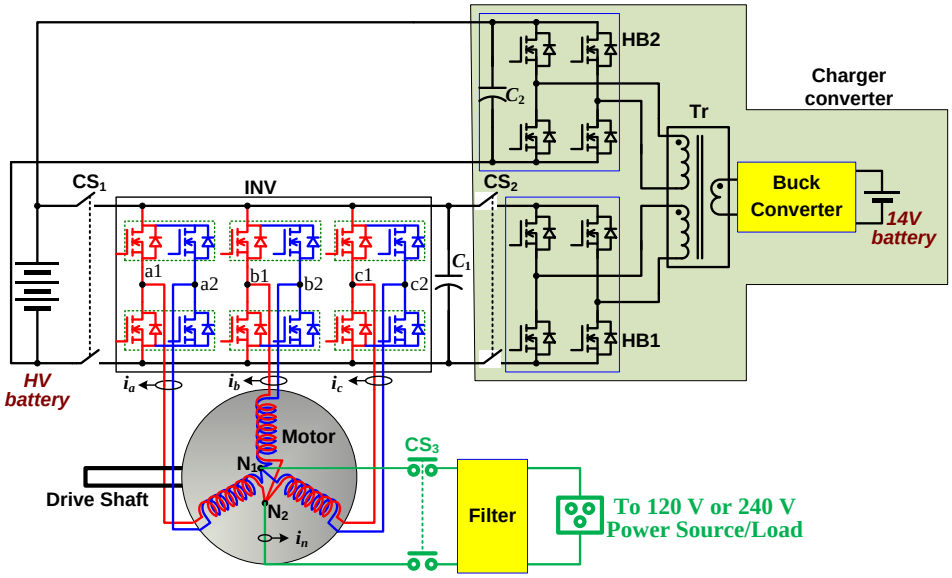


Figure 3-21: Integrated OBC applied to a segmented traction drive.

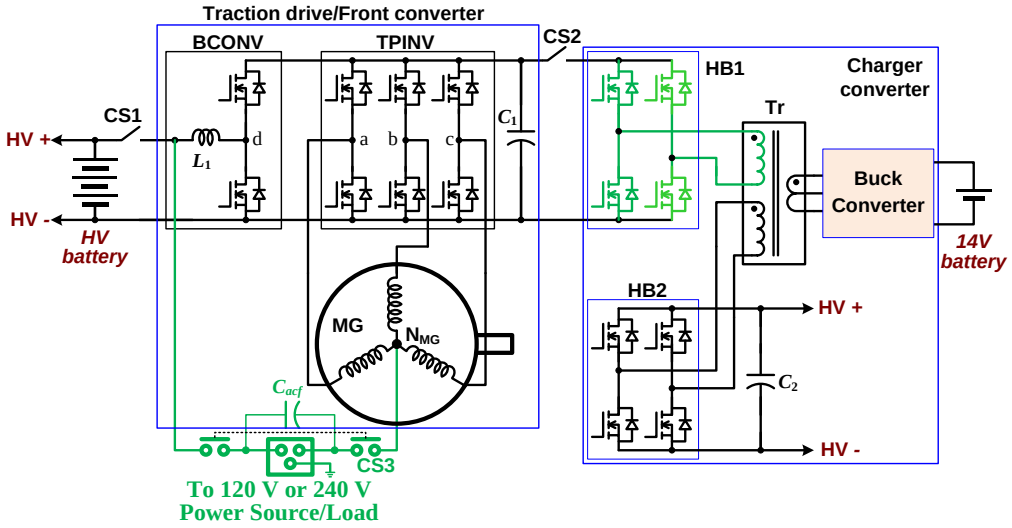


Figure 3-22: Integrated OBC applied to traction drive system with a boost converter.

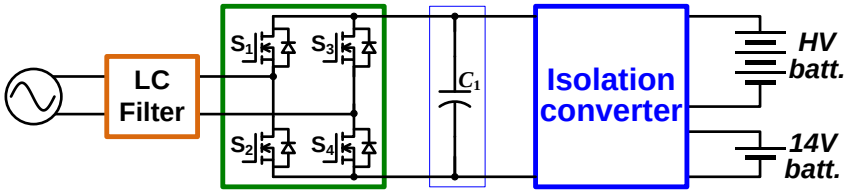


Figure 3-23: The isolation converter applied to a stand-alone OBC.

Results and Discussion

Work for FY 2016 focused on developing a 6.6 kW GaN-based isolation converter and an integrated OBC using the GaN isolation converter.

Because of the HV rating of 650 V and normally off nature, the latest GaN switches made by GaN Systems were tested and characterized. The following tests were performed and design data were collected for use in designing a 6.6 kW GaN isolation converter: (1) static characterization tests, (2) pulse tests, and (3) H-bridge converter tests.

Figure 3-24 shows the static characterization test setup. Header pins were used to make connections to the small pads for gate, source, and drain on the switch, and a steel cylinder and springs were used to adjust contact pressures to ensure good electrical conductions. Figure 3-25 shows the static characterization test results. Test results indicated a relatively low threshold voltage (~1.4 V), which must be considered in designing gate drive circuits for these switches. Results on spread of on-resistance were used to select and match the switches for use in the isolation converter design.

Figure 3-26 shows the pulse and H-bridge converter test circuits for the GaN Systems devices. Tests were conducted at a dc bus voltage of 400 V and a maximum current of 32 A. Figure 3-27 shows test results. Fast switching times of less than 10 ns and low switching losses were observed, indicating these devices are well suited for high frequency and efficiency dc-dc converter and OBC applications.

Figure 3-28 plots GaN H-bridge converter test results for efficiency vs. load power at dc bus voltages of 350 V and 400 V and switching frequencies of 100 kHz and 200 kHz. Measured peak efficiencies are 98.5% at 350 V and 100 kHz, 98.3% at 400 V and 100 kHz, 96.3% at 350 V and 200 kHz, and 96.4% at 400 V and 200 kHz.

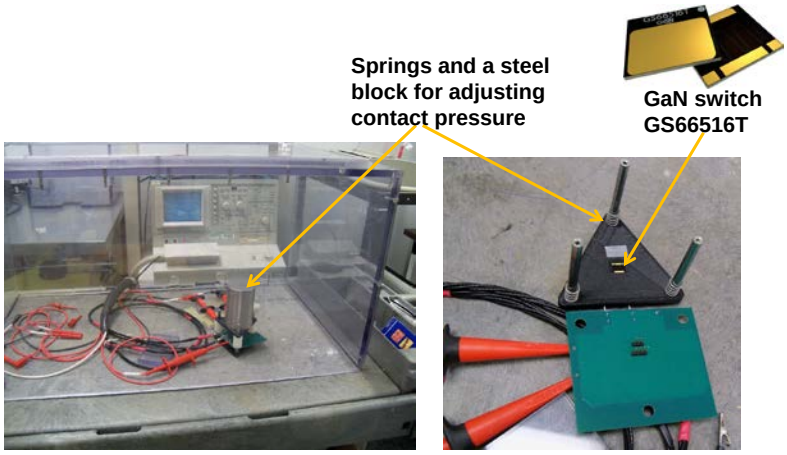


Figure 3-24: Static characterization test setup using pressure contacts.

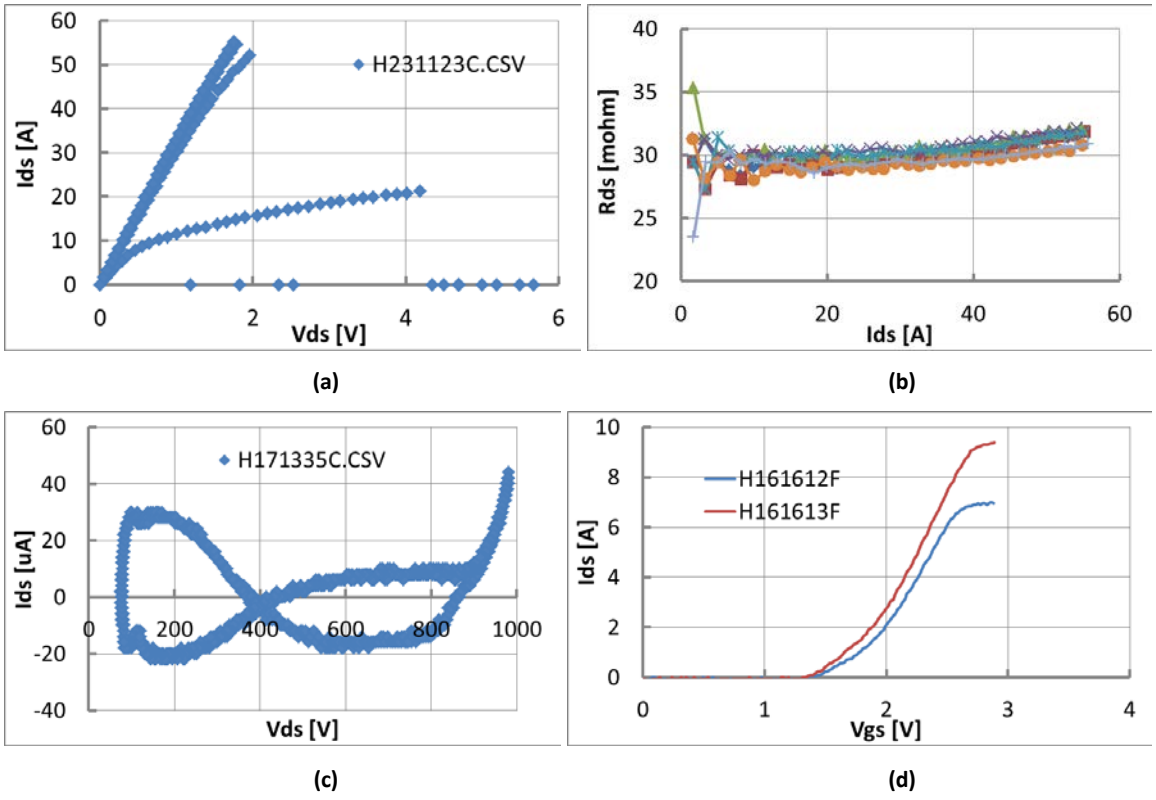


Figure 3-25: Static characterization test results: (a) I-V curves as the gate source voltage (Vgs) stepped from 0.5 V to 6.5 V in increments of 1 V, (b) spread of on-resistance [Rds(on)] of eight samples at Vgs = 6.5 V, (c) breakdown voltage, and (d) gate threshold voltage.

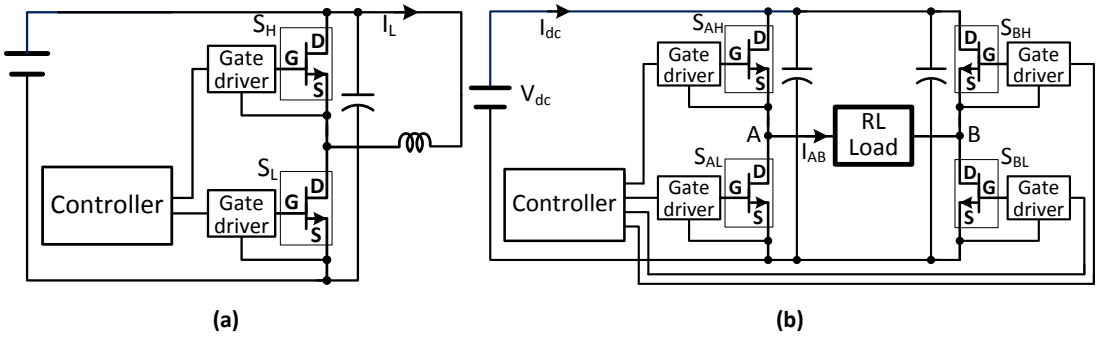
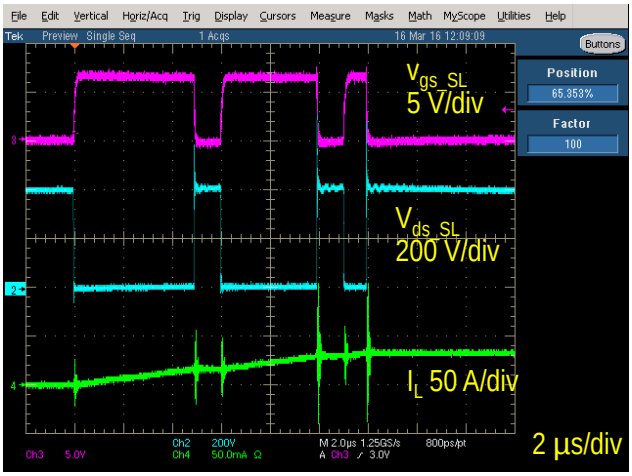
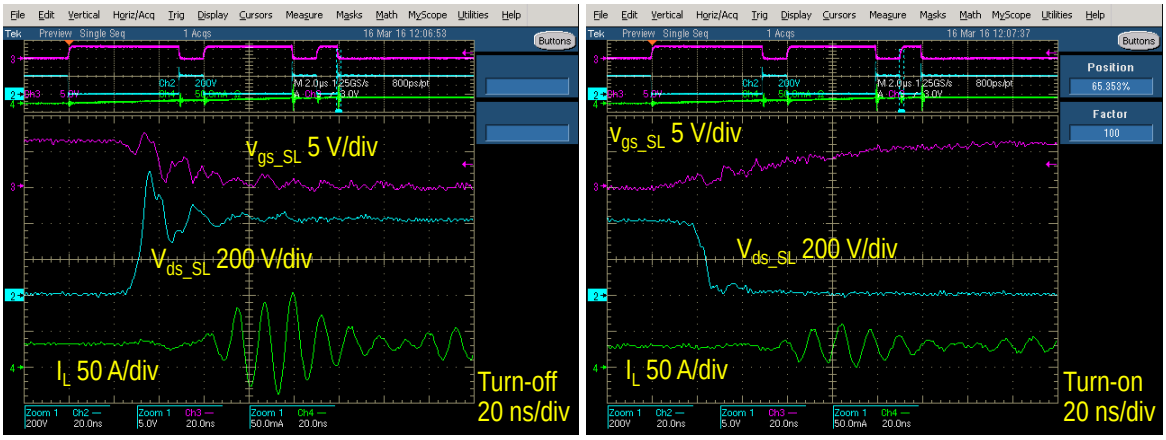


Figure 3-26: Pulse and H-bridge converter test circuits [(a) and (b), respectively] for the GaN Systems devices.



(a)



(b) (c)

Figure 3-27: Pulse test results: (a) pulse test waveforms, (b) turn-off, and (c) turn-on.

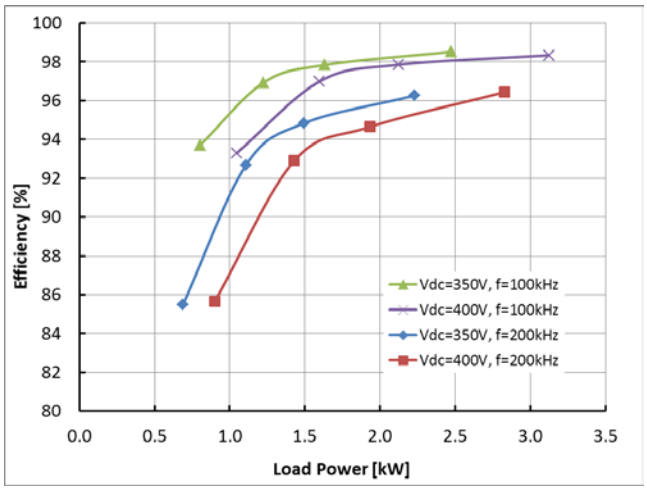
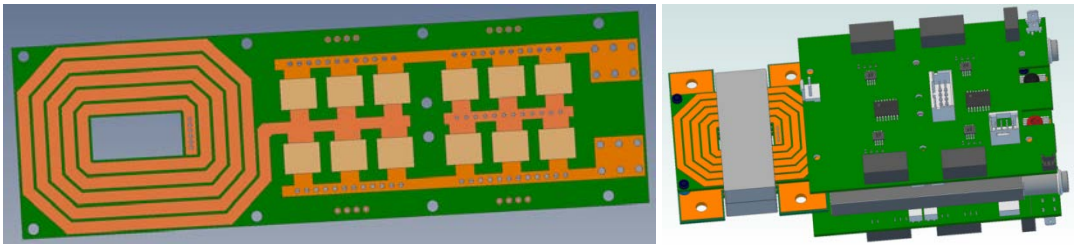


Figure 3-28: GaN H-bridge converter test results on efficiency vs. load power at different frequencies and dc bus voltages.

Incorporating the test results, a final design for the 6.6 kW GaN isolation converter was completed. The following optimization steps were taken in producing the final design: (1) losses in the ferrite cores and copper winding were analyzed to determine transformer core size and number of turns for minimizing the total transformer losses and (2) PCB trace layout simulations were performed for the primary and secondary

transformer to minimize the parasitic inductance for the H-bridge converters. Figure 3-29 shows 3-D drawings for the final design for the 6.6 kW GaN-based three-port isolation converter. The converter has dimensions of.6.6 in. × 3.2 in. × 1.8 in.



(a) (b)

Figure 3-29: Final design for the 6.6 kW GaN-based three-port isolation converter: (a) PCB for planar transformer winding and GaN power plane board and (b) complete assembly.

An aluminum pin fin cold plate measuring 3.18 in. × 4.18 in. × 0.375 in. was designed and built for use in the 6.6 kW GaN isolation converter (Figure 3-30). 3-D printing was used to facilitate the fabrication of this thin (4 mm thick) pin fin cold plate with fine geometries. Finite element thermal analysis results indicate satisfactory cooling performance as shown in Figure 3-31.

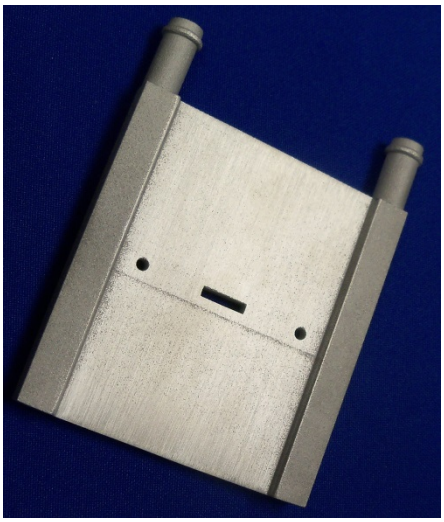


Figure 3-30: 3-D printed aluminum pin fin cold plate.

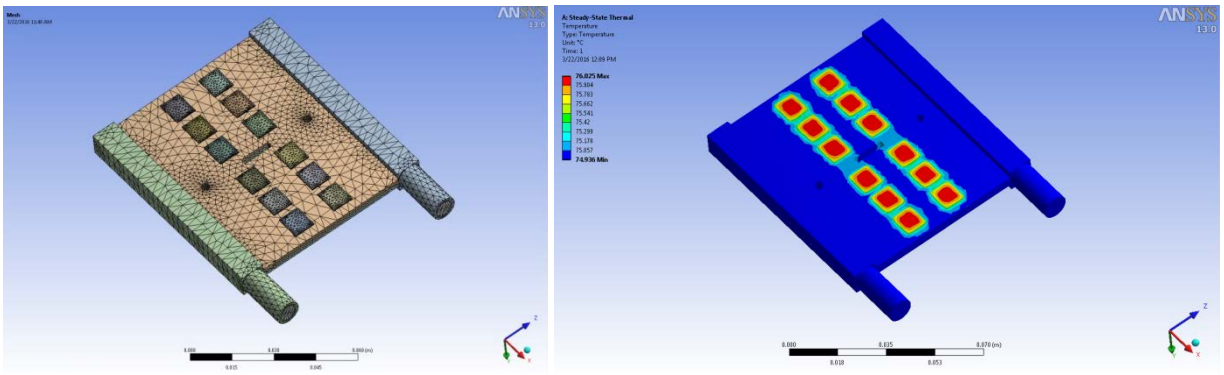
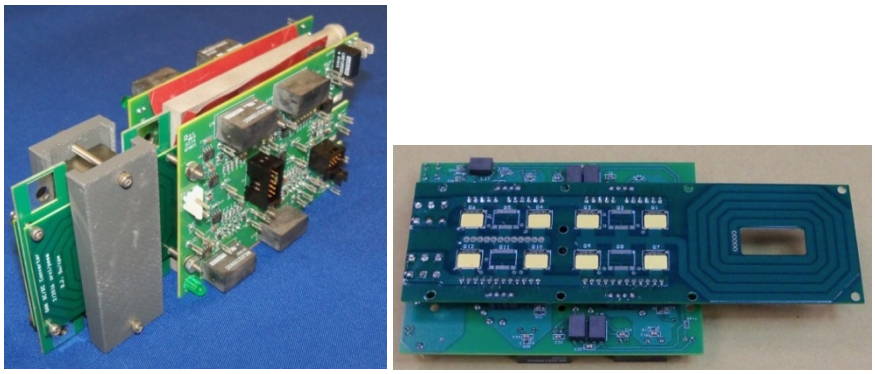


Figure 3-31: Finite element analysis results for the 3-D-printed cold plate.

A reflow oven at the ORNL packaging laboratory was used to solder the GaN devices to the transformer winding and power plane boards. Measures were taken to ensure the GaN devices were flush at their top sides after soldering so they all will make good contact with the cold plate. The gate drive circuit and PCB layout were designed with emphasis on minimizing gate loop inductance to avoid ringing on the gate source voltage at switching. Working with a magnetic vendor, customized ferrite cores for the planar transformer were designed and fabricated. Figure 3-32 shows photos of the 6.6 kW GaN isolation converter prototype. A digital signal processor (DSP) control board using the latest Texas Instruments dual-core chip, TMS320F28377D, was used to implement high-speed, high-resolution PWM control loops (Figure 3-33).

The 6.6 kW GaN isolation converter was tested with a resistive load bank at different switching frequencies. Figure 3-34–Figure 3-36 show a photo of the test setup, typical operating waveforms at switching frequencies of 100 kHz and 200 kHz, and measured converter efficiency, respectively. Measured peak efficiencies are 99.0% at 100 kHz and 97.5% at 200 kHz.



(a) (b)

Figure 3-32: Photos of (a) the 6.6 kW GaN isolation converter prototype and (b) the assembled power and gate drive boards.

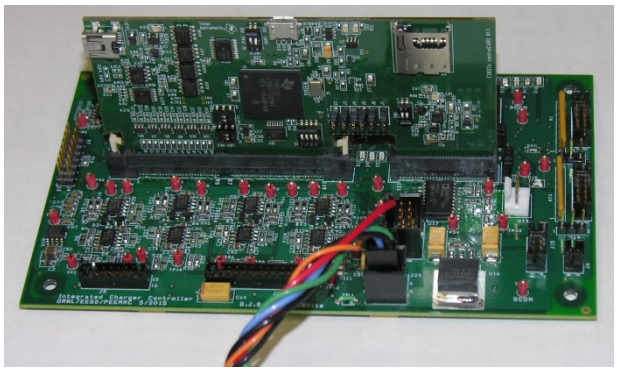


Figure 3-33: Digital signal processor board using the latest Texas Instruments dual-core chip.

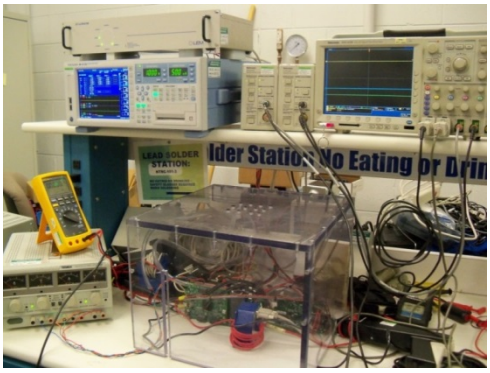


Figure 3-34: GaN isolation converter test setup.

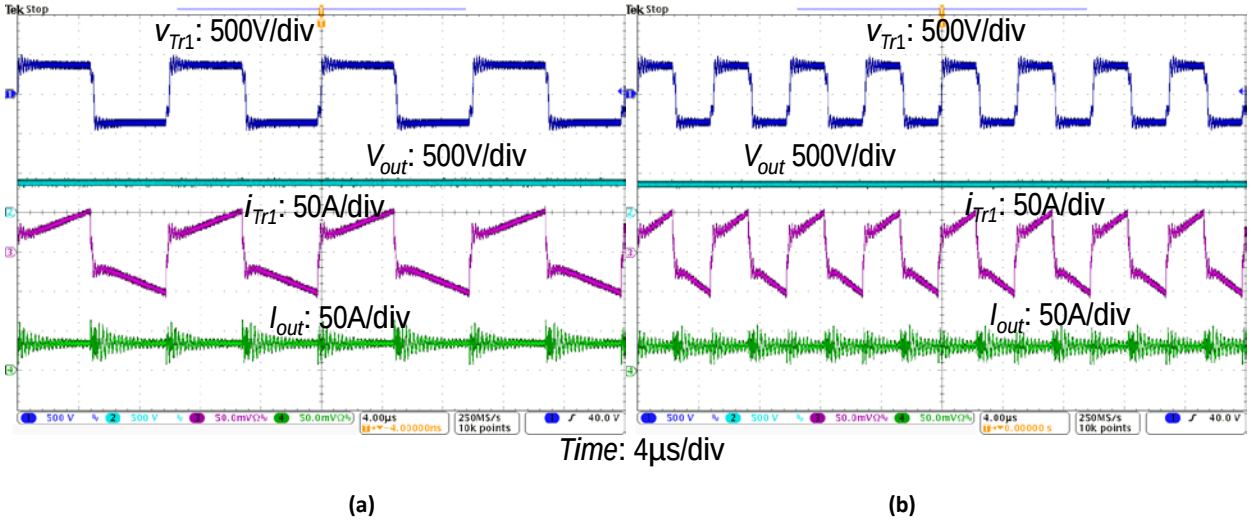


Figure 3-35: GaN isolation converter test results showing operating waveforms (a) at fsw = 100 kHz and (b) at fsw = 200 kHz.

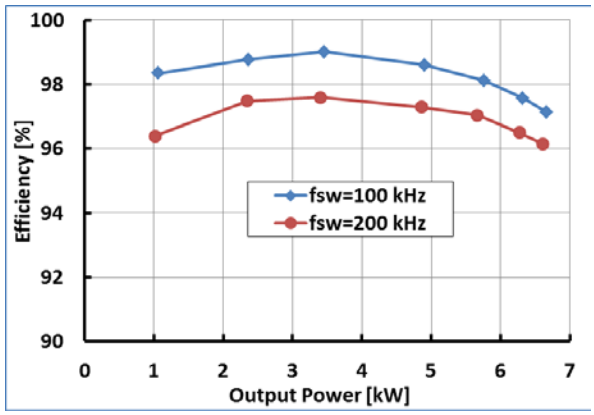


Figure 3-36: GaN isolation converter test results showing measured GaN converter efficiency.

Table 3-1 gives a comparison of the GaN-based isolation converter and a 5 kW Si-based counterpart. The GaN-based converter achieved a 50% reduction in volume, 75% reduction in weight, and peak efficiency of 99% vs. 98.4% for the Si-based counterpart at 2.5 times the switching frequency. The GaN converter prototype has a power density of 10.5 kW/L and specific power of 9.6 kW/kg vs. 3.7 kW/L and 1.5 kW/kg for the Si-based converter.

Table 3-1: Comparison of GaN- and Si-based isolation converters

Text	Si isolation converter	GaN isolation converter	GaN to Si ratio
Volume (L)	1.34	0.63	0.47
Mass (kg)	3.27	0.69	0.21
Peak efficiency (%)	98.4 (40 kHz)	99.0 (100 kHz)	1.0

The 6.6 kW GaN charger converter was then integrated with a 100 kW segmented inverter to test its functionality as an integrated OBC. The segmented inverter was built using six 1,200 V, 120 A dual-pack SiC MOSFET modules and four film dc bus capacitors with a total capacitance of 880 µF, and a 36 cm by 12.7 cm cold plate. 3-D-printed parts were used to make the inverter easily reconfigurable as a dual three-phase inverter or a segmented three-phase inverter. In addition, an induction motor with ratings of 14.92 kW, 230 Vrms, and 45.4 Arms were used as a traction motor in the tests. The motor has two sets of stator windings with all leads accessible and thus is well suited for the segmented inverter.

Figure 3-37–Figure 3-39 show a photo of the test setup, typical operating waveforms at charging power levels of 3.6 kW and 6.6 kW, and measured OBC system efficiency at a grid voltage of 240 V, respectively. Measured OBC system peak efficiency is 96.6%, a 2.2% point improvement over the Si-based counterpart.

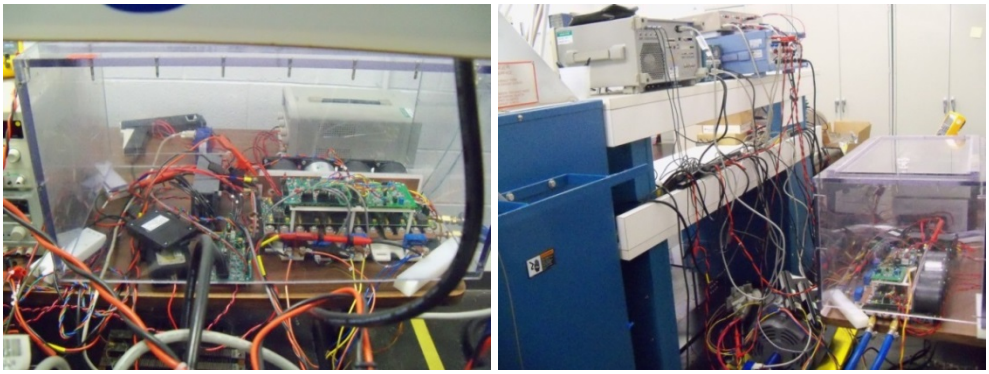


Figure 3-37: Setup for testing the integrated OBC using the GaN converter and a segmented traction drive.

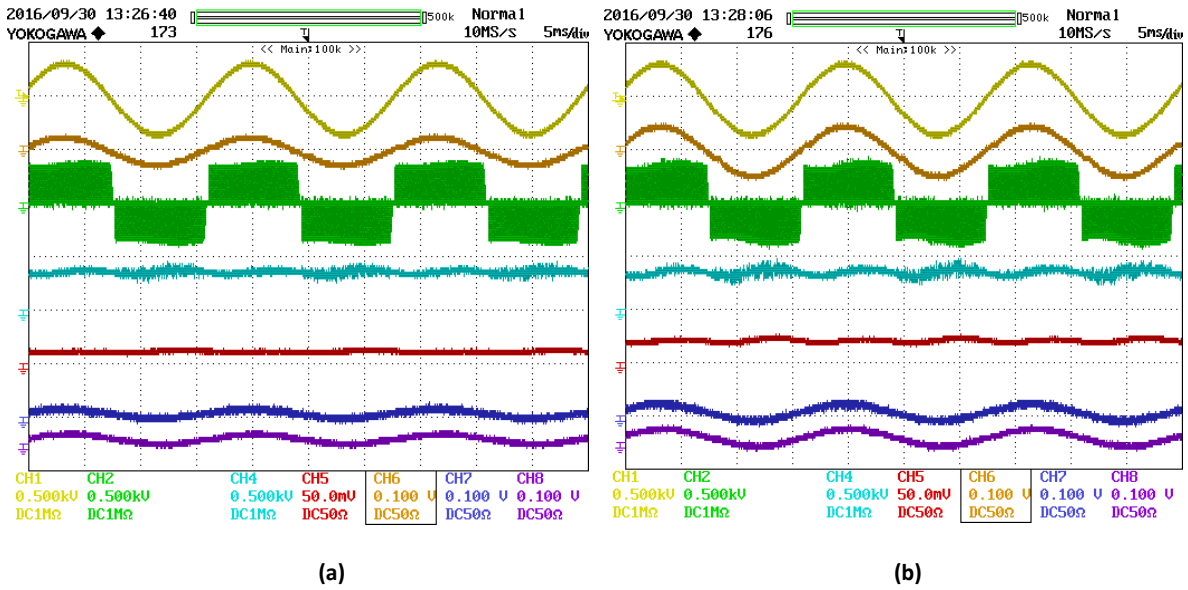


Figure 3-38: Test results–typical operating waveforms for the integrated onboard charger system at charging power levels of (a) 3.6 kW and (b) 6.6 kW.

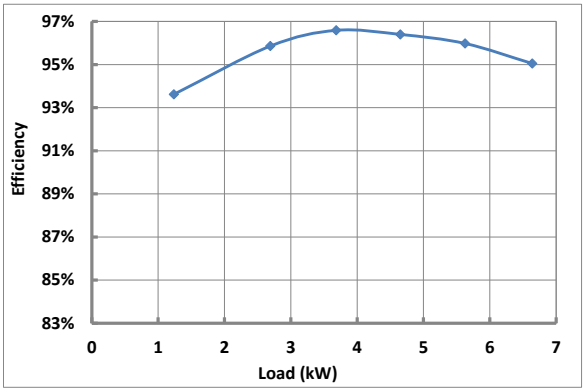
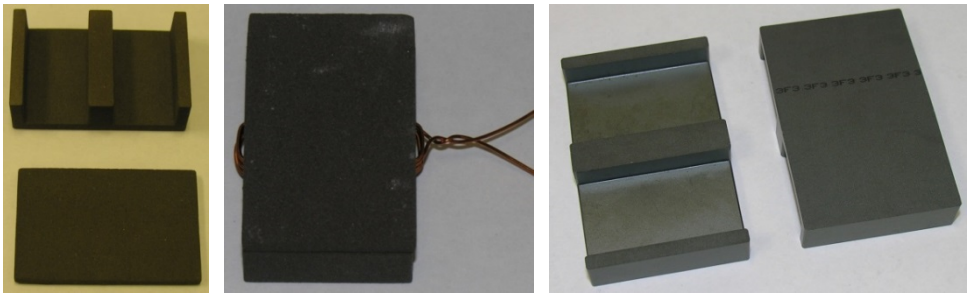


Figure 3-39: Integrated onboard charger system test results showing measured system efficiency at grid voltage of 240 V.

Working with Aegis Technology, ORNL had generated a transformer core design using Aegis's low-loss nanocomposite magnetic powder material and had printed E-cores at ORNL's manufacturing demonstration facility in FY 2015. In FY 2016, an inductor using the printed cores was fabricated and characterization tests

were carried out. Figure 3-40 shows photos of the printed cores and inductor and similarly sized commercial ferrite cores for comparison.

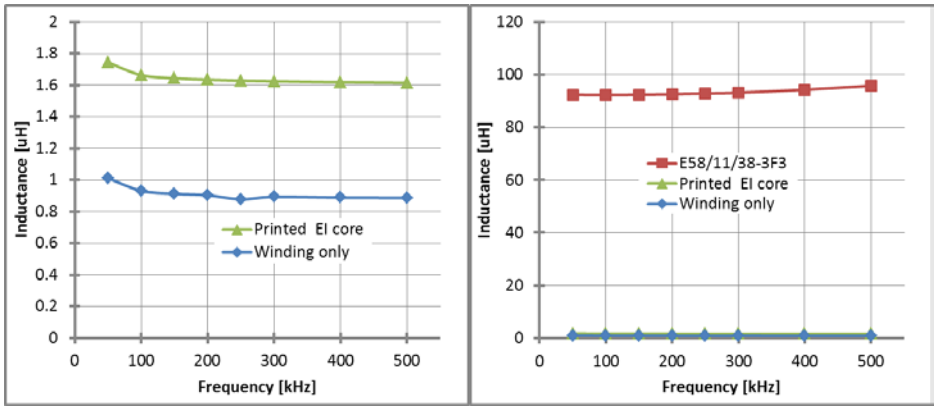


(a) (b) (c)

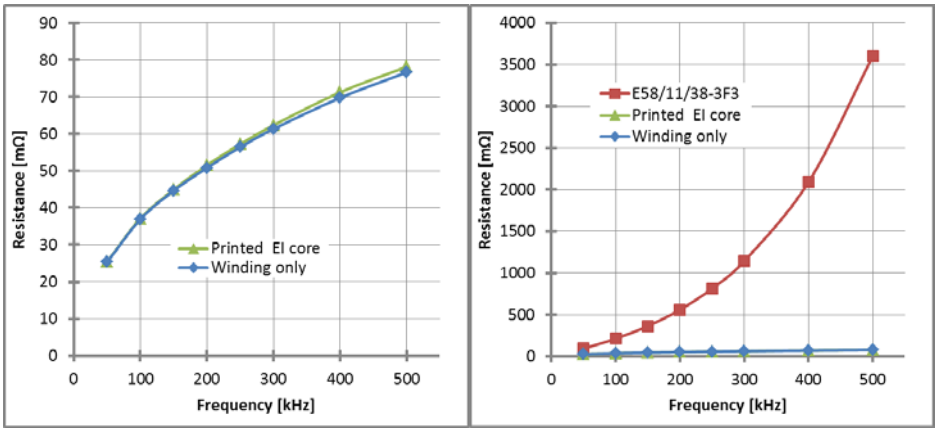
Figure 3-40: Photos of the ORNL printed cores (a) and inductor (b) and commercial ferrite cores (c) for comparison.

Figure 3-41 shows measured inductance and resistance for the inductor using the printed cores, an air core (winding only), and an inductor using the commercial ferrite cores (E58/11/38-3F3). Compared to the air core, the inductance values increased less than 2 times with the printed inductor while an increase of about 100 times was measured with the commercial ferrite cores. However, no changes below 300 kHz in resistance with or without the printed cores were observed in comparison to a 4 to 47 times increase with the commercial cores.

The test results indicate there are a significant number of pores or air gaps in the printed cores that substantially reduce the effective permeability of the cores. Future work is needed to improve the printing processes to enhance the density. Another option would be to create 3-D-printed molds with a desired shape and geometry for cores and sinter nanocomposite magnetic powders in the molds.



(a)



(b)

Figure 3-41: Measured inductance (a) and resistance (b) of the inductor using the printed cores or an air core and an inductor using a commercial ferrite core.

Conclusions and Future Directions

This project is aimed at leapfrogging existing Si-based charger technology to address charger and converter cost, weight, volume, and efficiency by overcoming the limitations of current Si semiconductor and magnetic materials. The multipronged approach involves using WBG devices, including those made with SiC and GaN; advanced magnetic materials; and a novel integrated charger architecture and control strategy.

Under this multiyear project, a new integrated OBC and dc-dc converter architecture has been developed that integrates the segmented traction drive, a 14 V dc-dc converter, and an HV battery charger dc-dc converter. The new topology significantly reduces the number of components: it achieves a 47% reduction in power circuit components alone, not counting savings in the gate driver and control logic circuits, translating to a 50% reduction in cost and volume compared with existing stand-alone OBCs. In addition, WBG-based devices are used in the converter and inverter to further reduce the cost, weight, and volume of the passive components and improve system efficiency. A control strategy for the charger isolation converter was also developed to reduce the battery ripple current inherent in single-phase ac-dc converters. The control strategy was shown to reduce the ripple current by 60%, enabling a corresponding reduction in the bulky dc link capacitor in the active front end converter.

A 6.6 kW GaN charger converter was designed and built using the latest GaN Systems GaN transistors; a 3-D printed cold plate; HV heavy copper PCB power planes; low-voltage (14 V), high-current PCB power planes; and a planar transformer. The converter has a high power density of 10.5 kW/L and specific power of 9.6 kW/kg vs. 3.7 kW/L and 1.5 kW/kg for a Si-based converter. Test results also show higher efficiency for the prototype converter than for Si-based analogues—even at a 2.5 times higher switching frequency.

A 6.6 kW integrated WBG OBC prototype using the GaN-based charger converter and a SiC segmented traction drive was assembled and successfully tested. Test results showed it to have a peak efficiency of 96.6%. The test results also show an improvement of more than 2 percentage points over the Si-based counterpart.

Test results for a 3-D-printed magnetic core using nanocomposite magnetic powders indicate the printing processes need to be improved to enhance the degree of densification. Another option would be to 3-D-print molds with the desired shape and geometry for cores and sinter nanocomposite magnetic powders in the molds.

FY 2016 Presentations/Publications/Patents

1. G. J. Su, “Innovative technologies for converters and chargers,” presented at the DOE Vehicle Technologies Office 2016 Annual Merit Review, June 7, 2016, Washington, DC.
2. G. J. Su and L. Tang, “An integrated onboard charger and accessory power converter for traction drive systems with a boost converter,” presented at the 8th IEEE Energy Conversion Congress and Exposition (ECCE 2016), pp.1–6, September 18–22, 2016, Milwaukee, Wisconsin.
3. G. J. Su, “Innovative technologies for converters and chargers,” presented at the United States Council for Automotive Research LLC, U.S. DRIVE Electrical and Electronics Technical Team meeting, September 29, 2016.

3.3 Gate Driver Optimization for WBG Applications

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Contract No.: DE-AC05-00OR22725

Abstract/Executive Summary

This project addresses a technology gap resulting from the consequences of repeated fast current and voltage transitions in wide bandgap (WBG) –based drive systems and the deleterious effect they can have on system and motor reliability over time. By providing enhanced control and optimization of the gate drive, through dynamic closed-loop slew rate limiting of di/dt (instantaneous current change rate) and dv/dt (instantaneous rate of voltage change over time), fast-switching WBG-based drive systems can achieve higher system reliability, power density, and efficiency, leading to increased market acceptance at a lower system cost point.

This project will further the minimization and integration of the electronics required for traction motor drive systems. A gate drive specifically optimized for silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) will be designed, fabricated, and tested in two phases. The first prototype will be built in a benchtop circuit using commercial off-the-shelf (COTS) components, and its operation will be evaluated. This will be followed by the second phase of the project, focusing on the development of the gate drive in a monolithic integrated circuit, advancing high-frequency WBG design-based size reduction benefits.

Accomplishments

The following tasks were addressed during FY 2016. All reporting and presentation requirements were met.

- Board Level Gate Driver Prototyping using COTS Components
  - A board level gate driver design was completed based on commercially available integrated circuits and components. SPICE (Simulation Program with Integrated Circuit Emphasis) simulations of the primary building blocks were performed using models provided by commercial suppliers. In some cases, SPICE models were not available and suitable representative models were generated.
  - The design was broken into two primary building blocks: the waveform generator and the feedback circuits. Two separate designs were completed for the waveform generator. The initial design was based on steering current sources to generate the complex multistep gate drive waveform and relied on emitter-coupled logic (ECL) circuits for the fast timing requirements of this architecture. A fast timing board was designed and fabricated implementing this approach. A second design allowed significantly reduced timing requirements and used a complex programmable logic device (CPLD) for timing generation coupled with four commercial gate driver integrated circuits, diode summing circuits, and a high-performance signal buffer for the gate drive. A printed circuit board (PCB) design was completed for each of the building blocks, and the boards were fabricated and loaded with components.

- The second, less timing intensive method was selected for use in the prototype system, and each of the associated PCBs was tested and functioned as expected.
- These two custom boards were combined with a clamped inductor test board to form a complete drive system having a variable threshold gate drive waveform.

- Bench Test COTS Gate Driver with WBG Devices
  - The two circuit PCBs of the previous task were combined to drive a SiC power MOSFET. The power device source lead inductance was used as a sensing element and the associated voltage (Ldi/dt) was input to the feedback circuits to provide the gate drive rising edge threshold value (V_{T1}) and the gate drive falling edge threshold value (V_{T2}).
  - The SiC power MOSFET was configured to switch a clamped inductor load, allowing observation of the associated fast switching transients: dv/dt of the device drain to source voltage (V_{DS}) and di/dt of the device drain to source current (I_{DS}).
  - Testing of the combined system was initiated. Initial results show that although the individual system modules function as expected, additional effort is needed to fully realize a working, closed loop, benchtop prototype system.

- Iterate and Finalize Gate Driver Design
  - Although several iterations of the active gate drive (AGD) system modules were completed and tested in FY 2016, closed loop testing of the complete benchtop AGD prototype as a system was completed in only a limited fashion due to a number of technical challenges that occurred throughout FY 2016. These challenges limited the full realization and characterization of a closed loop, benchtop, AGD prototype constructed entirely from COTS components.
  - The experience of building and testing a closed loop, benchtop AGD prototype based on COTS components supports the assertion that a design of this level of performance (fast rise and fall times, precise timing requirements, wide gate drive voltage swings) is much better suited for custom integrated circuit implementation than for COTS implementation.

- Integrated Circuit Fabrication Process Selection
  - Using the design requirements generated during this research in FY 2015 and FY 2016, a set of general requirements was generated for the ideal integrated circuit process targeted for eventual single-chip integration of this design.
  - General specifications for the target process include the availability of a number of device types including NMOS and PMOS transistors with operating voltages ≥ ~20 V, elevated temperature operation (≥175ºC), multiple metallization layers including a “thick” metal for power routing, and available cell libraries with associated SPICE models and process design kits to minimize circuit design time. Both silicon and silicon-on-insulator (SOI) processes were considered.
  - An SOI fabrication process was selected from present commercial offerings for full integration of the AGD circuit (XT06 0.6 micron Modular Trench Isolated SOI Technology Process available through X-Fab). This process includes the basic device types needed [low-, medium-, and high-voltage NMOS and PMOS transistors; three metal layers with a thick third metal layer for power routing; and an extensive library of passive devices, digital circuits, and complex analog functions including operational amplifiers (opamps), comparators, bandgap references, and analog-to-digital and digital-to-analog converters]. In addition, the process uses trench-isolated SOI technology capable of operating at temperatures up to 225ºC, making it ideal for automotive and industrial applications.

Many of the technical challenges encountered in the COTS realization of the proposed advanced gate drive system were addressed during FY 2016, further supporting the assertion that improved gate drives for SiC devices are feasible and should produce the expected benefits. These lessons learned will provide a strong technical foundation for future closed loop AGD realization and validation.

Introduction

WBG devices, primarily SiC and gallium nitride, have characteristics that can lead to dramatic benefits in a variety of power electronics applications. These include higher temperature and higher frequency operation, smaller device and overall system sizing, and greater operational efficiency. Their ability to switch at higher frequencies than their silicon counterparts can also lead to significant volume reduction in associated passive components, yielding second-order benefits in reduced material costs and weights. For every 10% reduction in the weight of a vehicle, a 6%–7% increase in fuel economy can be realized. For this reason, significant attention has been given to the miniaturization and light-weighting of all components and systems in a vehicle by automotive original equipment manufacturers. The rapidly escalating move from the use of power silicon to WBG devices to capture some of these advantages entails revisiting and optimizing their interplay with ancillary circuits and systems to truly exploit their unique characteristics.

Available commercial gate drives are not optimized for use with WBG devices. They have historically been developed for silicon devices and cannot exploit the distinctions that WBG semiconductors can offer traction drive systems. The faster di/dt and dv/dt switching capabilities of WBG devices can impose implications that need to be addressed at a system level. Fast switching can reduce the reliability of motor insulation by creating pinholes in the insulation that eventually can cause arcing and failure of the motor. To combat this possibility, additional costs must be incurred for higher rated winding insulation, imposing increased motor and cabling costs and resulting in larger and heavier motors. Additionally, fast switching transients can induce unwanted circulating currents, resulting in pitted bearings. Fast voltage and current transitions can also necessitate added electromagnetic interference (EMI) filtering requirements to protect sensitive electronic systems from electronic interference, adding further costs and increased system volume and weight.

This project addresses the cost and volume barriers to achieving the DOE traction drive system goals of $8/kW and >4 kW/L power density. To achieve these goals, a cost-effective, efficient topology for monitoring and controlling the dynamic slew rate of a WBG gate drive will be developed to drive a SiC MOSFET motor leg. The design will ultimately be implemented in an integrated circuit to minimize the volume and reduce packaging issues.

This work can serve as an enabling technology, which, if implemented in a high-temperature process, can be used for future integrated motor/inverter systems.

The design will result in

- higher inverter reliability and efficiency through monitoring and using dynamic slew control
- 50% reduction in gate drive electronics volume by drive integration
- higher temperature capability (>200°C) through use of SOI technology
- higher motor reliability
- reduced insulation breakdown
- reduced bearing currents
- lower cost gate drive systems through parts reduction
- gate driver integration
- decreased EMI filtering.

This project will advance the technology of gate drives and hasten the deployment of WBG devices in vehicular traction drives by significantly increasing power density and lowering cost, circuit volume, and weight while increasing reliability and allowing the opportunity to move toward an integrated, high-temperature-capable traction drive system.

Approach

An active gate driver topology was developed to address the technology gaps associated with WBG-specific gate drives. This architecture was simulated using a custom-designed circuit topology with a vendor-supplied WBG device model in PSpice (a commercial SPICE derivative) and prototyped using COTS components. The four tasks identified for carrying out the project goals in FY 2016 are as follows.

- Task 1. Board Level Gate Driver Prototyping using COTS Components
  - Design and implement a benchtop prototype AGD system based entirely on commercially available components (COTS components).
- Task 2. Bench Test COTS Gate Driver with WBG Devices
  - Test the fabricated advanced gate driver prototype system using a SiC power MOSFET load.
- Task 3. Iterate and Finalize Gate Driver Design
  - Optimize the AGD benchtop prototype through improved prototype design and construction to maximize performance.
  - Produce a final AGD benchtop system architecture.
- Task 4. Integrated Circuit Fabrication Process Selection
  - Investigate commercially available integrated circuit processes for implementation of an AGD system chip.

The project strategy was to incorporate lessons learned from previous gate drive research at ORNL and the University of Tennessee, as well as synergies with previous projects focused on SiC gate drivers; to incorporate di/dt and dv/dt control through di/dt sensing; to generate a variable threshold gate drive waveform with feedback electronics; and ultimately to develop a high-temperature-capable gate driver integrated circuit suitable for integration with a traction motor to realize size, volume, and DOE cost targets.

Results and Discussion

Beginning with the advanced gate driver architecture developed and simulated in FY 2015, the AGD topology was modified to incorporate a variable threshold gate drive waveform instead of the variable slew waveform type used in FY 2015 circuit simulations. SPICE simulation results indicated that this new gate drive waveform provided improved control of the di/dt and dv/dt of SiC power switching devices, as compared to more conventional methods based on shaping or slew rate limiting.

The modified AGD general topology is shown in Figure 3-42(a) and the variable threshold gate drive waveform produced in Figure 3-42(b). A timing generator circuit provides synchronized timing control for generation of the variable threshold waveform. Feedback circuits capture the di/dt peak voltage generated during both the rising and falling edges of the gate drive waveform, filter these voltages, and then apply appropriate gain and offset to produce the two variable thresholds V_{T1} and V_{T2} [Figure 3-42(b)] used by the waveform generator.

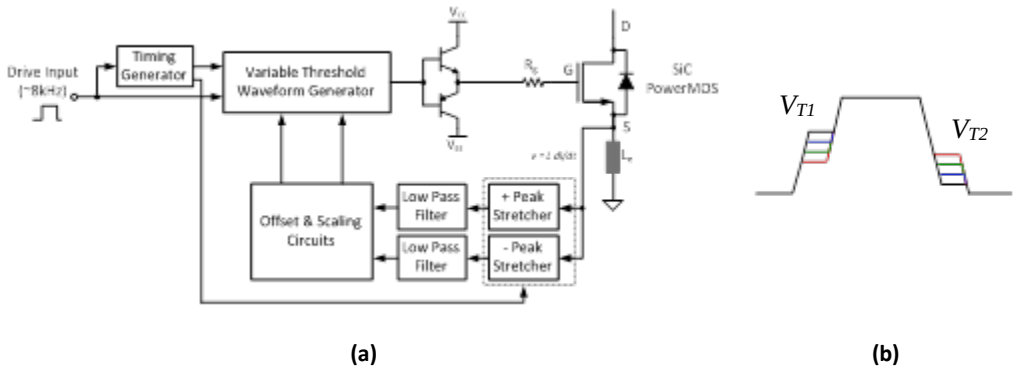


Figure 3-42: AGD circuit topology selected for COTS implementation incorporating WBG source inductive current sensing for di/dt feedback control (a) and the associated variable threshold gate drive waveform produced (b).

Two different designs of the waveform generator were explored for this research. The initial design used switched current sources to charge a capacitor with the desired waveform followed by two buffering stages to produce the desired gate drive waveform. This design was extensively simulated in PSpice using vendor provided models for all components except for the timing generator function. Realizing a COTS-based design proved to be very challenging due to the unique requirements of this circuit module: 20 V signal swing, high slew rate (~1,300 V/ms), relatively high bandwidth (23.3 MHz), and high output current (1.5 A peak). Only two commercially available opamps were found to meet all of these specifications. The current mode ADA4870 opamp (Analog Devices, Inc.) was selected and incorporated in the design. To provide additional high-current buffering, a bipolar transistor-based diamond driver was placed at the output for driving the SiC power MOS load. Figure 3-43 shows the initial waveform generator block diagram and a PSpice simulation result performed using commercially available circuits for all components except for the timing generator.

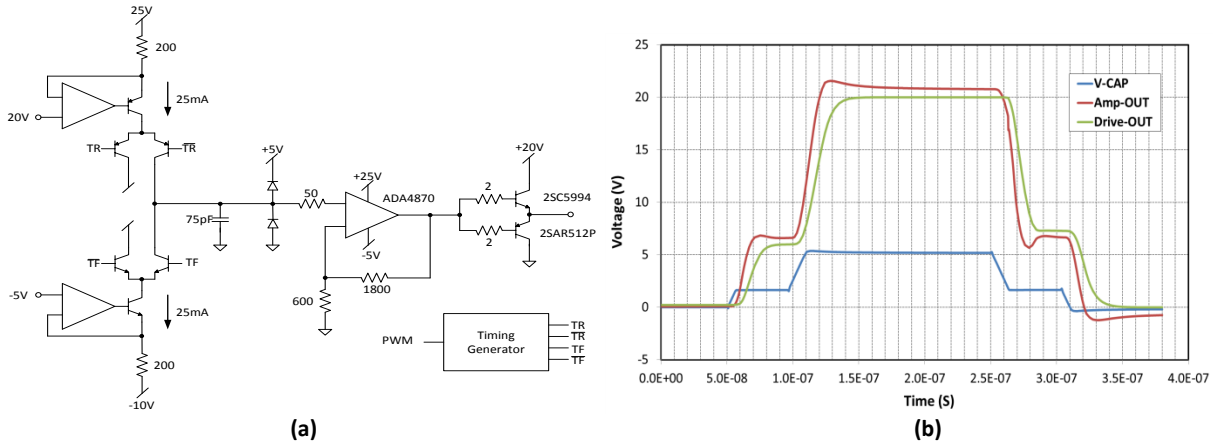


Figure 3-43: Version 1 waveform generator block diagram (a) and PSpice simulation output waveform (b).

Timing generator circuits were also required for this waveform generator design to control the current sources used to generate the shaped drive waveform. A careful investigation into the requirements for these circuits indicated that using field programmable gate arrays or CPLDs was not acceptable, primarily due to the 1–2 ns delays associated with getting the signals in and out of these reprogrammable digital circuits. These stringent timing constraints are associated with the need for precise control of the current sources for producing signals with very short rise times (5–10 ns). Figure 3-44 shows an example simulation with these timing requirements produced using PSpice (a commercial SPICE derivative) with circuits modeled using an integrated circuit fabrication process. To meet these demanding timing requirements for the COTS design, a timing generator block was designed and fabricated based on ECL. The fabricated module is shown in Figure 3-45.

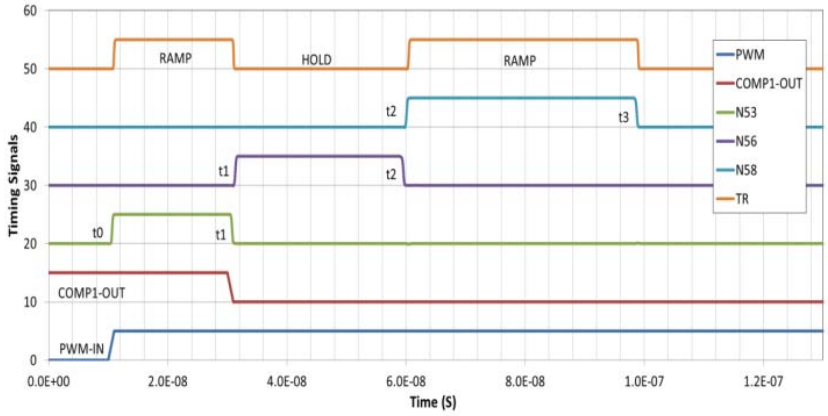


Figure 3-44: Timing generator PSpice simulation using circuit models from a modern integrated circuit process.

Figure 3-45: ECL-based timing generator PCB for the initial waveform generator design.

To reduce the waveform generator dependency on highly precise and difficult to produce timing controls, an alternative design was generated that significantly relaxed the timing requirements. In this design, COTS gate drivers were used with a diode network to generate the desired waveforms [Figure 3-46(a)]. Within the operating supplies of the commercial gate drivers, the supplies can be varied to produce the four desired output voltages: ground, rising threshold voltage (V_{T1}), maximum output amplitude, and falling threshold voltage (V_{T2}). The precise width of the two threshold voltage regions is not critical in this design as the AGD loop will adjust to accommodate variability in these widths. The general topology of WaveGen2 is shown in Figure 3-46(b). A CPLD generates timing control signals that are galvanically isolated from the gate driver using commercial isolators. This provides both electrical isolation and signal level shifting. Commercial gate drivers are used to provide a high-current drive capability for charging a hold capacitor through the diode network. Care was taken to properly select diodes to minimize the forward voltage drop and minimize the parasitic capacitance to minimize charge injection. The opamp buffer and diamond driver used in the initial waveform generator design were used here as well to buffer the gate drive signal.

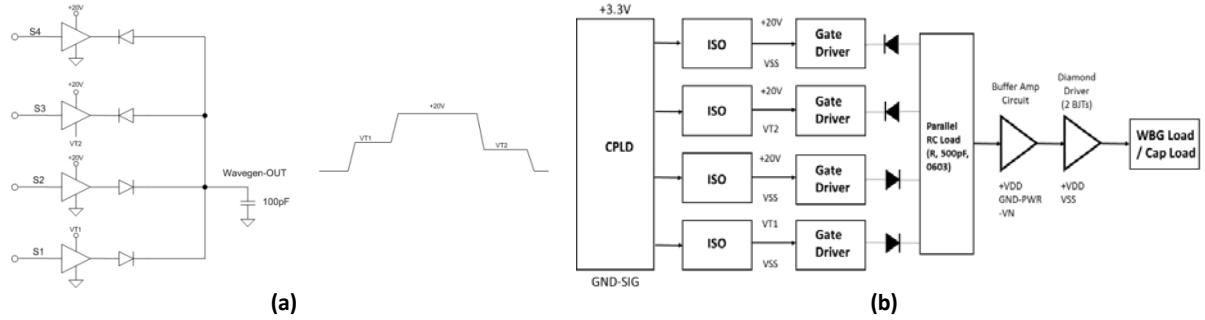


Figure 3-46: Alternative waveform generator (WaveGen2) simplified functional diagram (a) and overall circuit block diagram (b).

The fabricated WaveGen2 circuit is shown in Figure 3-47. The board was populated with a load capacitance of 2nF to simulate a large SiC power MOS gate load. Testing this unit produced a very fast gate drive waveform with the ability to separately adjust the rising plateau voltage (V_{T1}) and the falling plateau voltage (V_{T2}). Plots showing measured output waveforms while driving a 2nF load are provided in Figure 3-48. Some signal overshoot at the edges was observed, which can be minimized through additional circuit optimization. However, the design worked very well and produced very fast rise and fall times (on the order of 15–20 ns total), as demonstrated in Figure 3-48(b). Theoretically, significant variations in the signal overshoot and threshold plateau width will be readily tolerated by the overall AGD topology, as the control loop will modulate the threshold voltage values to drive the di/dt toward the set point value.

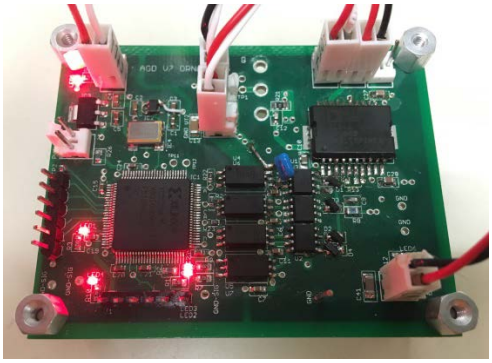


Figure 3-47: Fabricated WaveGen2 waveform generator module.

Figure 3-48: WaveGen2 Measured Waveforms: Rising and falling edges showing the two variable threshold values (a) and a zoom view of a rising edge showing ~7ns and ~5ns rise times in the two transition regions (b).

A feedback circuit board was also designed and fabricated to generate the two threshold values (V_{T1} and V_{T2}) for the waveform generator from the sensed di/dt signal (Figure 3-49). This board incorporates two similar channels that can be configured to accommodate the specifics of the rising and falling edge di/dt values. Each channel has a peak hold circuit with reset that holds the peak di/dt signal associated with the appropriate drive transition. The held signal is low-pass filtered, and gain, offset, and inversion are applied to produce the threshold voltage signals for the waveform generator module. Test results for this module indicated proper operation with input signals representative of the expected sensed signal. Each channel was configured to provide the appropriate polarity of operation—increasing di/dt produces an increase in V_{T1} and a decrease in V_{T2} for the rising and falling gate drive waveforms, respectively.

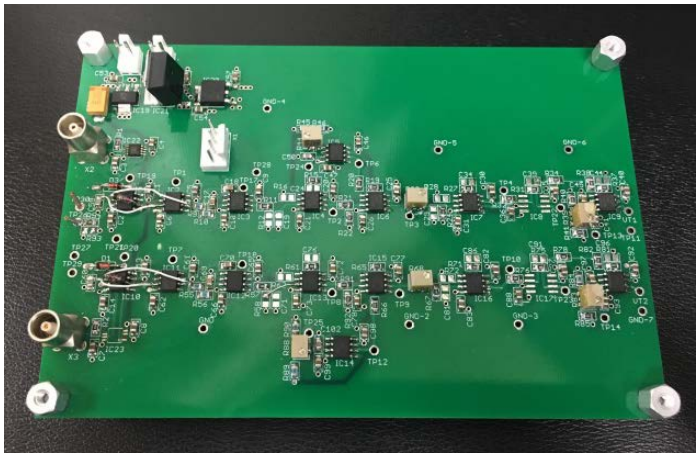
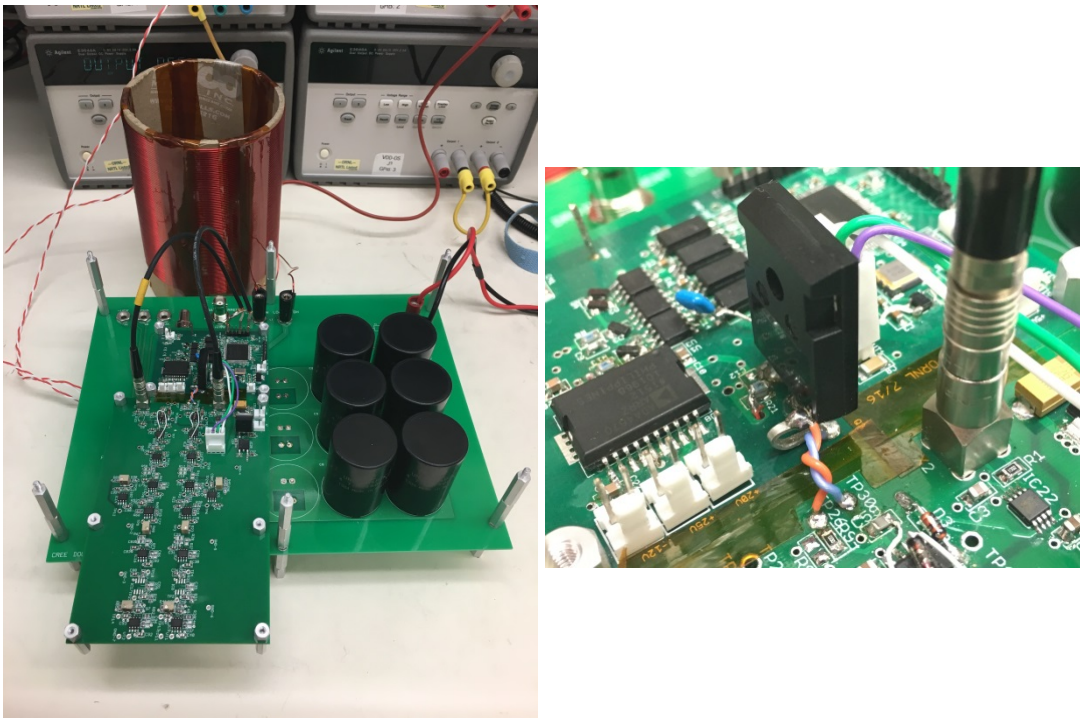


Figure 3-49: AGD Feedback PCB used in AGD benchtop system testing.

The AGD benchtop prototype unit was assembled by integrating the system modules: the WaveGen 2 PCB, the feedback PCB, and a clamped inductor test board (Figure 3-50). The clamped inductor test board design (Cree, Inc.) enabled measurement of the power MOS device drain current and drain-to-source voltage. The SiC power MOS switch was mounted on the waveform generator PCB in close proximity to the diamond driver to minimize stray inductance. A small loop was added to the source leg of the SiC switch as a source inductance for monitoring di/dt [Figure 3-50(b)], and a small pair of twisted wires were used to input the di/dt feedback signal to the feedback PCB. The outputs of the feedback board (V_{T1} and V_{T2}) were input to the waveform generator PCB threshold inputs. Timing signals for resetting the feedback board peak stretcher circuits were provided by the waveform generator PCB CPLD and were connected using short coaxial cables. The leads of the SiC power MOS device were passed through the waveform generator PCB directly into the socket on the clamped inductor test module. The CPLD was designed to be operated from an external pulser and generated the timing signals to enable straightforward control of the gate drive waveform pulse width (duty cycle) and repetition rate (frequency) for testing flexibility. External power supplies were used to power these units, and each board was configured with local voltage regulators and filtering to minimize noise injection.



(a) (b)

Figure 3-50: Benchtop prototype AGD composed of the WaveGen2, feedback, and clamped inductor modules (a) and close-up view of SiC Power MOS device with added source lead inductance (b).

Initial testing of the integrated system indicated that further system integration work was needed for full evaluation of this design. Optimization of each individual unit was performed during testing and construction, but further optimization as an integrated system is needed to fully assess the AGD performance.

In addition to the AGD design and prototyping activities, candidate integrated circuit processes were investigated in preparation for eventual single chip integration of the AGD design. General specifications for the target process were identified; among them are available device types, including NMOS and PMOS transistors with operating voltages ≥ ~20 V; elevated temperature operation (≥175ºC); multiple metallization layers for interconnects, including a "thick" metal for power routing; and analog and digital cell libraries with associated chip layouts, test results, and SPICE models. Both silicon and SOI processes were investigated.

An SOI fabrication process was selected as the best of the current commercial offerings for full integration of the AGD circuit (XT06 0.6 micron Modular Trench Isolated SOI CMOS Technology Process available through X-Fab). This process provides the basic device types needed (low-, medium-, and high-voltage NMOS and PMOS transistors); three metal layers with a thick third metal layer for power routing; and an extensive library of passive devices, digital circuits, and complex analog functions including opamps, comparators,

bandgap references, and analog-to-digital and digital-to-analog converters. In addition, the process uses trench-isolated SOI technology capable of operating at temperatures up to 225ºC, making it ideal for automotive and industrial applications. This process is an excellent candidate for AGD integration as it meets all of the device needs for the AGD.

Conclusions and Future Directions

This project is focused on achieving DOE volume, weight, and cost targets for advanced traction drive inverters while providing a high-temperature gate drive solution enabling an integrated motor-inverter system. It includes development of a circuit to actively monitor and optimally respond to the fast switching characteristics of SiC switches to ensure system reliability, enabling safe use of SiC MOSFETs in drive inverter modules to increase inverter efficiency and reduce system volume and cost.

The research activities of FY 2016 have culminated in the realization of a benchtop prototype of the advanced gate drive system. The system uses an advanced gate drive waveform variable threshold gate drive, which putatively provides improved control of undesired WBG device switching transients, as compared to RC– and slew rate–based conventional approaches to gate drive control. Building on the architecture developed and simulated in FY 2015, efforts were directed toward implementation of the AGD architecture using COTS components for system demonstration and testing. The most difficult module of this system was determined to be the waveform generator. Two waveform generator designs were investigated, the first requiring very fast timing circuits and the final architecture having much relaxed timing requirements. The second design was successfully implemented and functioned well with a 2nF capacitive load. A fast timing generator PCB was also designed and built based on ECL circuits but was abandoned as the alternative design became the apparent technology of choice. In addition, a feedback board was designed to process the di/dt-based waveform and produce the variable threshold values used by the waveform generator to produce the rise and fall plateau voltages. This board was tested on the bench, and modifications were made to optimize its performance. Finally, the three modules (WaveGen 2, feedback, and clamped inductor) were integrated for operation as a complete AGD. Bench testing as a system was initiated using a SiC power MOS device. More testing will be needed before translation of the design to a single integrated circuit.

In many instances, the circuits involved in this design are much better suited to chip integration than to implementation using COTS components due to the much reduced parasitic capacitance and inductance associated with monolithic construction. In addition, as previously detailed, there are commercially available modern integrated circuit processes incorporating the device types needed capable of meeting all specifications of the AGD design.

With the maturation of WBG devices and their continued penetration of the automotive sector, it is expected that a more system level approach to their implementation will be needed in the near future. Optimization of the gate drive for performance, reliability, and cost will be paramount in these efforts. This research will position the ORNL team to initiate SOI integrated circuit implementation of the AGD, an enabling technology for realizing reliable and highly compact WBG-based traction drive systems.

FY 2016 Presentations/Publications/Patents

1. N. Ericson, C. Britton, L. Marlino, S. Frank, D. Ezell, L. Tolbert, and J. Wang, “Gate driver optimization for WBG applications,” presented at the DOE Vehicle Technologies Office 2016 Annual Merit Review, June 8, 2016, Washington, DC.
2. N. Ericson, C. Britton, L. Marlino, S. Frank, D. Ezell, L. Tolbert, J. Wang, and B. Blalock, “Gate driver optimization for WBG applications,” presented at the United States Council for Automotive Research, LLC, U.S. DRIVE Electrical and Electronics Technical Team Project Update Meeting, July 21, 2016.

3.4 Power Electronics Thermal Management Research

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Abstract/Executive Summary

The objective for this project is to develop thermal management strategies to enable efficient and high-temperature wide-bandgap (WBG)-based power electronic systems (e.g., emerging inverter and DC-DC converter). Reliable WBG devices are capable of operating at elevated temperatures (≥ 175°C). However, packaging WBG devices within an automotive inverter and operating them at higher junction temperatures will expose other system components (e.g., capacitors and electrical boards) to temperatures that may exceed their safe operating limits. This creates challenges for thermal management and reliability. In this project, system-level thermal analyses are conducted to determine the effect of elevated device temperatures on inverter components. Thermal modeling work is then conducted to evaluate various thermal management strategies that will enable the use of highly efficient WBG devices within automotive power electronic systems.

Accomplishments

- We created steady-state thermal models of an automotive inverter that included all the major system components. The models were used to estimate the effect of high-temperature (175°C, 200°C, and 250°C) WBG devices on inverter component (e.g., capacitor, electrical boards, and solder layers) temperatures. Results indicate that capacitor temperatures are predicted to exceed the maximum operating temperature of typical polypropylene-film capacitors at the lowest junction temperature evaluated (175°C).
- We used the inverter thermal models to evaluate various under-hood temperature environments on inverter component temperatures. The under-hood temperatures evaluated were intended to simulate all-electric and hybrid-electric under-hood temperature environments. Model results suggest that the under-hood environment does not have a significant effect on inverter component temperatures.
- We created a transient thermal model of an automotive inverter. The transient model capacitor versus time response compared well with Oak Ridge National Laboratory (ORNL) experimental results. The model was used to estimate the time it takes for the capacitor and electrical board to exceed their temperature limitations when exposed to 250°C junction temperature conditions.
- We evaluated various capacitor thermal management strategies. The thermal management strategies consisted of increasing the power module cold plate performance (to decrease junction temperatures), mounting the capacitor on a cold plate(s), and cooling the bus bars that connect the power modules to the capacitors. Cooling the bus bars is predicted to be the most effective strategy for cooling the capacitors.

Introduction

This project will analyze and develop thermal management strategies for WBG-based automotive power electronics systems. A challenge with WBG devices is that although their losses in the form of heat are lower, the area of the devices is also reduced to increase power density and reduce costs, which results in higher device heat flux. Additionally, WBG's high junction temperatures will result in larger temperature gradients through the power module layers that will present reliability challenges and require high temperature bonding materials (e.g., high-temperature solder, sintered silver). Another challenge with WBG's higher junction temperatures is that they will expose other system components (e.g., capacitors and electrical boards) to higher temperatures that may exceed their allowable temperature limits. These challenges require system-level thermal management analysis and innovative thermal management solutions.

Approach

System-level (e.g., inverter scale) thermal management analyses were conducted to understand the effect of high-temperature WBG-based devices on the power electronics systems. There are currently no automotive power electronics systems that use WBG devices. Therefore, an automotive silicon-based inverter was modeled and used as the framework for the WBG analyses. The inverter thermal model included all the major inverter components including the power modules, electrical boards, capacitors, and associated electrical interconnects (e.g., bus bars) and assumed a heat dissipation for each component. The models were then used to evaluate various WBG-operating conditions and thermal management strategies. Below is a more detailed description of the project approach.

- Create and validate thermal computational fluid dynamics (CFD) and finite element analysis (FEA) models of an automotive power electronics system
- Use the models to evaluate the effects of incorporating high-temperature WBG devices into automotive power electronics systems
  - Compute system components (e.g., power module attach layers, capacitors, and electrical boards) temperatures when exposed to WBG junction temperatures of 175°C, 200°C, and 250°C
  - Determine the system components that will require additional thermal management to enable them to operate reliably under high-temperature WBG conditions
- Evaluate different vehicle (all-electric and hybrid-electric) under-hood environments and their effect on power electronic component temperatures
- Model various capacitor and electrical board cooling strategies. Determine the most effective and feasible cooling strategies for each component
- Select a few promising thermal management concepts identified in the modeling work. Conduct test to validate the select concepts.

Results and Discussion

WBG devices are currently not used in any commercially available automotive traction drive power electronics system (e.g., inverter). Therefore, a silicon-based inverter (2012 Nissan LEAF) was modeled and used to simulate the effect of high-temperature WBG devices on inverter components including the DC-link capacitors, electrical boards, and power module interface layers. Silicon-carbide (SiC) material properties were used for the transistor and diode to represent WBG devices. The reader is referred to the following reports by ORNL [1] and NREL [2] for detailed descriptions of the 2012 Nissan LEAF inverter electrical and thermal management systems.

In the Electric Drive Technologies Thermal Performance Benchmarking Project, CFD and FEA models of the 2012 LEAF power modules and cooling system were created. The model-predicted junction-to-coolant thermal resistance was validated using experimental data at various coolant flow rates [2]. For this project, the LEAF CFD and FEA models developed in the benchmarking project were expanded to include the DC-link capacitors, electrical boards (e.g., gate driver and control), electrical interconnects (e.g., bus bars), and inverter aluminum housing. The CFD modeled the air natural convection occurring within the inverter. The FEA models (steady-state and transient) did not model the air flow associated with natural convection, but instead used a simplified method to account for the air natural convection effects. A heat transfer coefficient boundary

condition was imposed at the exterior of the inverter enclosure to account for heat loss or gain from the under-hood environment to the inverter for both the CFD and FEA models. For both models, component heat was imposed as volumetric heat generation values. Temperature results between the CFD and FEA model were typically within ~ ±3°C for most components.

Computer aided design (CAD) drawings of the 2012 Nissan LEAF inverter, inverter capacitors, and power module-gate driver assembly are provided in Figure 3-51. The capacitor windings were modeled using anisotropic thermal conductivity varying according to a cylindrical coordinate system to account for the wound polypropylene-metallization film construction. Similarly, the gate driver boards were modeled using anisotropic properties to account for the board's metallization layers that increase the thermal conductivity in the board's in-plane directions. Table 3-2 and Table 3-3 provide thermal properties used for the various inverter components that were used in the thermal models. The geometries of the solder and thermal interface material (TIM) layers were not modeled but their thermal resistance effects were imposed as contact resistances.

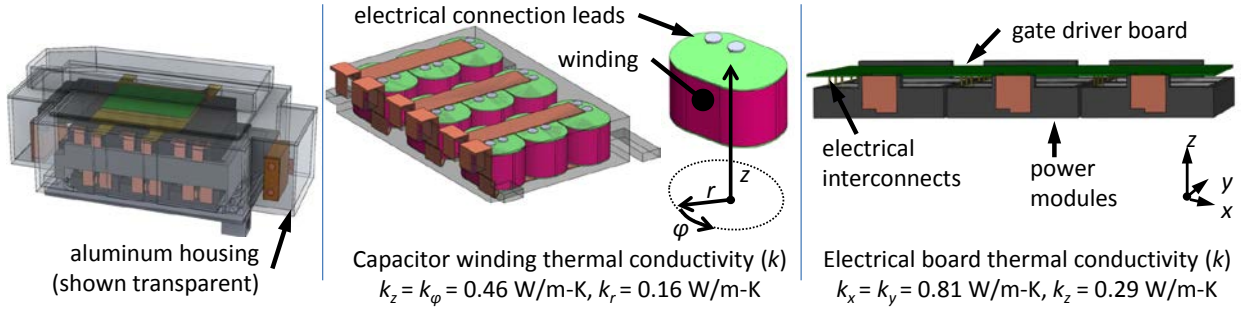

Figure 3-51: CAD drawing of 2012 LEAF inverter (left), DC-link capacitor (middle), and power module-gate driver assembly (right). Anisotropic thermal conductivity properties were used to model the thermal performance of the capacitor windings and gate driver board.

Comparing Model and Experimental Results

Before modeling WBG conditions, the results of the full-scale 2012 LEAF inverter thermal model were first compared with experimental results obtained by ORNL [1] for two operating conditions—80-kW steady-state and 50-kW transient operations at a motor speed of 7,000 revolutions per minute. The 80-kW and 50-kW power was assumed to be measured as the motor output. For these modeling validation efforts, silicon material properties were used for the devices (transistors and diodes). ORNL efficiency maps were used to obtain the efficiencies of the motor and inverter at the two operating conditions. The power output of the inverter was then calculated as the motor power output divided by the motor efficiency, and the power to the inverter (inverter input) was calculated as the motor power output divided by the product of the motor and inverter efficiencies. Heat losses from the inverter were then calculated as the difference between the input and the output inverter power.

Heat losses from the inverter were assumed to be generated at three components—bus bars (AC and DC sides), capacitors, and the devices (transistors and diodes). Bus bar heat for both the AC and DC sides was estimated assuming joule heating (I^2 Ω). The electrical resistance (Ω) was calculated using copper's electrical resistivity properties and the bus bar cross-section and length measurements. The current on the DC side was computed as the inverter input power divided by the battery voltage (375 VDC assumed). The current on the AC side was computed using the inverter output power and the equation $P_{out} = 3\, V_{RMS}\, I_{RMS}\, PF$ (three-phase AC system). V_{RMS} and $I_{RMS}$are the AC voltage and current, respectively. PF is the power factor and its value was assumed constant at 0.85. The capacitor heat was computed per the equation I_ripple^2 ESR where ESR is the equivalent series resistance of the capacitors and I_ripple is the ripple current. The device heat was then computed as the total inverter heat losses minus the heat from the bus bars and capacitors. The device heat accounted for most of the inverter heat losses. The device heat losses were distributed in a 3-to-1 transistor-to-diode heat loss ratio.

Table 3-2: Material properties for the inverter power module components. Materials that do not have a reference source were assumed values.

	SiC [3]	Die Solder	Substrate Solder	Copper-Moly (20-80) [4]	Copper [3]	Module Plastic [5]	Silicone [6]	Dielectric pad	TIM
Thermal Conductivity (W/m-K)	270	Contact resistance: R"th = 2 mm^2-K/W	Contact resistance: R"th = 1 mm^2-K/W	160	387	0.34	0.26	Contact resistance: R"th = 116 mm^2-K/W	Contact resistance: R"th = 55 mm^2-K/W
Density (kg/m3)	3,160			9,850	8,933	1,800	1,272		
Specific Heat (J/kg-K)	675			270	385	1,250	1,800		

Table 3-3: Material properties for the other inverter components. Materials that do not have a reference source were assumed values.

	Capacitor Encapsulant	Capacitor Windings	Copper Leads (Bus Bars) [3]	Housing Aluminum [9]	Electrical Boards [10]	Bus Bar Molding Plastic
Thermal Conductivity (W/m-K)	0.45 [7]	radial=0.16; angular, axial=0.46	387	167	in plane: 0.81: through plane: 0.29	0.34
Density (kg/m3)	1,200 [8]	900	8,933	2,00	1,900	1,800
Specific Heat (J/kg-K)	900 [8]	1,690	385	896	1,150	1,500

The results from the model comparison with ORNL results are provided in Figure 3-52. A temperature probe was placed within the capacitor models at a location that corresponded to the location of a thermistor that was embedded within the capacitor's encapsulating epoxy. This allowed for a direct comparison between experimental and model temperature results. The left plot in Figure 3-52 shows the CFD-predicted maximum insulated-gate bipolar transistor, capacitor, and gate driver board temperatures for the 80-kW steady-state condition. As shown, the model-predicted results of 75.2°C compared well with the measured temperature of 75°C. The right plot in Figure 3-52 plots experimental and transient FEA-predicted capacitor temperature versus time response for the 50 kW operating condition. The transient FEA model results were found to provide a reasonable match with experimental results. Only the capacitor temperatures were compared because this was the only inverter temperature measurement provided in ORNL's tests. As previously mentioned, the junction-to-coolant model results have been previously validated in an NREL report [2].

Modeling High-Temperature WBG Devices within an Automotive Inverter

The LEAF inverter thermal models were used to simulate high-temperature WBG devices within an automotive inverter. The effect of increasing the transistor (metal–oxide–semiconductor field-effect transistor [MOSFET]) temperatures to 175°C, 200°C, and 250°C on inverter component temperatures was computed via modeling. Of particular interest were the maximum temperatures of the capacitors, gate driver, and power module attach layers (i.e., solder) under elevated WBG-temperature conditions. SiC material properties imposed for the devices were used to simulate the WBG devices within the 2012 LEAF inverter. Maximum MOSFET temperatures of 175°C, 200°C, and 250°C were achieved by increasing the MOSFET heat (per device) to 223 W (99 W/cm^2), 273 W (121 W/cm^2), and 375 W (167 W/cm^2), respectively. Maintaining the 3-to-1, MOSFET-to-diode heat loss ratio resulted in total power module (three modules) heat dissipation of 5,350 W, 6,560 W, and 9,010 W for the 175°C, 200°C, and 250°C maximum junction temperature cases, respectively. Increasing the power module heat dissipation means that the inverter power also increases, assuming the inverter efficiency does not change. This increase in inverter power would require a redesign of the inverter including increasing the bus bars sizes and changing the number of capacitors to account for the higher current levels. Since the current model does not change the inverter geometry, three capacitors and bus bars heat dissipation cases were evaluated for the elevated device temperature conditions (Table 3-4). In Case 1, the bus bars and capacitors did not generate heat. In Case 2, the bus bar and capacitor

heat generation rates were computed for an 80 kW and 97% efficiency (pertaining to a maximum junction temperature of 125°C) condition and those values were used for all elevated junction temperatures evaluated. For Case 2, the assumption is that the bus bar size and number of capacitors would increase to accommodate the increased power, but the heat dissipated per component would remain the same. For Case 3, the bus bar and capacitor heat was taken as a percentage of the power module heat and that percentage was used to compute their heat generation rates at the elevated junction temperature conditions. The percentages of heat for the components were taken at the 80 kW 97% efficiency condition. Case 3 represents the most extreme heat dissipation condition.

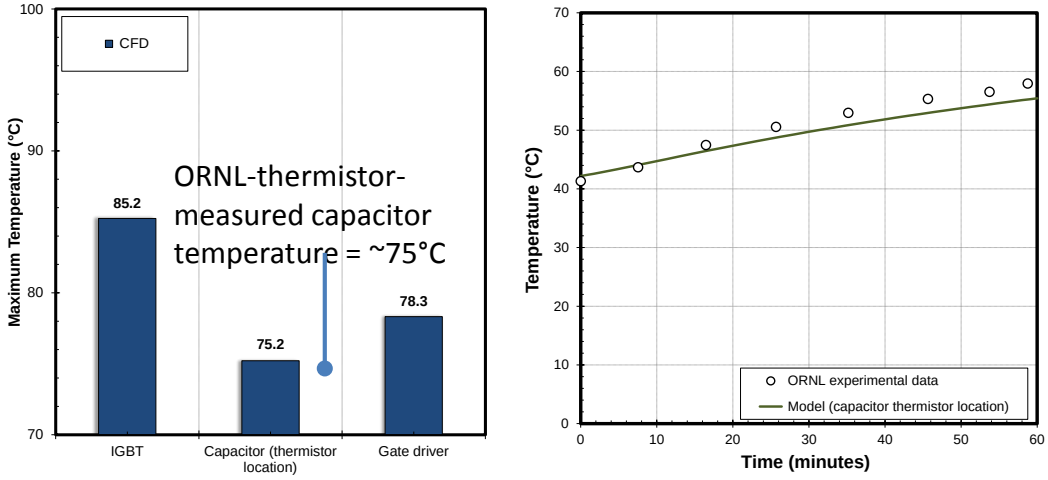

Figure 3-52: CFD-computed temperatures for the steady-state 80 kW operating condition (left) and transient FEA-generated capacitor temperature response for the 50 kW operating condition (right). Both the steady-state and transient model results compared well with experimentally obtained data from ORNL [1].

Table 3-4: Capacitor and bus bar (AC and DC sides) total heat dissipated for each case.

Case	Capacitors (Total)	Bus Bars (Total)
1	0	0
2	1.6 W	21.2 W
3	0.06% of module heat	0.72% of module heat

In addition to evaluating the effect of high-temperature WBG devices, the thermal models also evaluated three under-hood environment temperature conditions: 75°C, 125°C, and 140°C. The 75°C environment represents the under-hood conditions of an all-electric vehicle while the 125°C and 140°C environments represent under-hood conditions for hybrid electric vehicles. The hotter temperatures for the hybrid electric vehicles are associated with the heat generated by the internal-combustion engine. The more extreme under-hood case of 140°C represents a situation where the inverter is placed in close proximity to the combustion engine. The effect of the under-hood temperatures were imposed as heat transfer coefficient boundary conditions applied to the exterior of the inverter housing. A heat transfer coefficient of 10 W/m^2/K was used to simulate natural convection.

Figure 3-53 (left) provides the CFD-computed maximum capacitor temperatures for the 175°C, 200°C, and 250°C junction temperature cases at the three under-hood temperature environments (75°C, 125°C, and 140°C values shown in the figure legend). The maximum capacitor temperature was the maximum temperature found on any of the nine capacitor winding structures (see Figure 3-51). Results are provided for the three cases listed in Table 3-4. The values provided are the capacitor temperatures for Case 2. The error bar's lower and upper limits denote the temperatures for Cases 1 and 3, respectively. Results show that even for the lowest junction temperature case of 175°C, the capacitors are predicted to exceed the 85°C temperature limit (typical limit for polypropylene-film capacitors). For the 250°C junction temperature condition, capacitor temperatures approach 140°C. Several DOE projects are working to develop capacitors capable of operating at temperatures up to 140°C [11-13]. According to our analyses, the 140°C capacitor temperature rating is an appropriate target

for high-temperature WBG conditions. Increasing under-hood temperature from 75°C to 140°C results in a maximum capacitor temperature increase of about 7°C and thus the under-hood environment is not predicted to have a significant effect on capacitors temperatures. The aluminum housing with integrated cold plate is believed to create a somewhat sheltered temperature environment within the inverter as the heat on the invert housing is conducted through the housing walls to the cold plate and ultimately dissipated to the coolant. Figure 3-53 (right) shows the DC-side bus bar and capacitor winding temperature contours for the 175°C junction temperature case (75°C under-hood). These results show that the excessive capacitor temperatures are associated with heat from the power modules that is being conducted through the bus bars to the capacitors. Therefore, cooling the bus bars is a strategy to decrease capacitor temperatures.

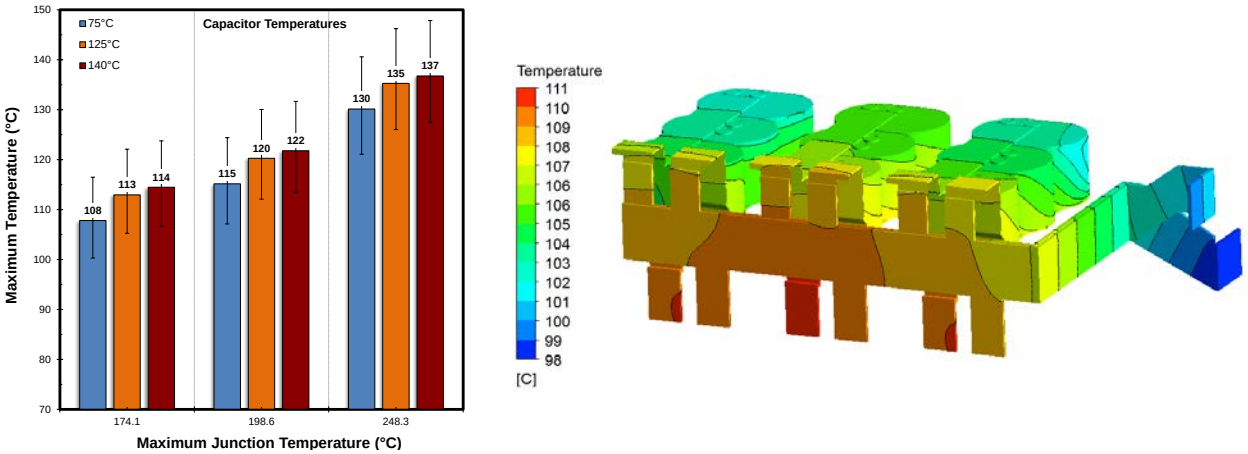

Figure 3-53: CFD-computed maximum capacitor winding temperatures for MOSFET temperatures of 175°C, 200°C, and 250°C (left). The under-hood temperatures are provided in the plot legend. CFD-computed DC bus bar and capacitor winding temperatures (right). Results demonstrate that heat is conducted from the power modules to the capacitors via the bus bars.

Figure 3-54 provides the CFD-computed maximum gate driver temperatures for the 175°C, 200°C, and 250°C junction temperature cases at the three under-hood temperature environments (75°C, 125°C, and 140°C values shown in the figure legend). The different operating conditions described as Cases 1–3 and shown in Table I-3 had no effect on gate driver temperatures. Therefore, only one gate driver temperature value is provided for each condition. As shown, varying the under-hood temperature has a negligible on the gate driver temperatures. This effect is associated with the proximity of the gate driver boards to the power modules, which makes them more sensitive to device temperatures and less sensitive to under-hood temperatures. Results show that even for the lowest junction temperature case of 175°C, the gate drivers are predicted to exceed the 125°C temperature limit (typical limit for electrical boards). At 250°C junction temperatures, the gate driver is predicted to reach a temperature of 183°C.These results indicate that either high-temperature gate drivers are required or thermal management solutions are needed to enable gate drivers to operate under high-temperature WBG conditions.

Figure 3-55 provides the estimated solder and TIM temperatures for the three junction cases. The device solder temperatures are essentially equal to the device temperatures. Results indicate that high-temperature solders are required for WBG temperatures. Additionally, high-temperature TIMs may also be required. TIM temperatures reach 223°C for the 250°C junction temperature case which is well above the limit for most TIMs. Figure 3-56 provides the power module and bus bar molding plastic maximum temperatures for the three junction temperature cases and for two under-hood temperature conditions (75°C and 140°C).

Transient FEA simulations were conducted to estimate the time that it takes for the capacitors and gate drivers to reach thermal equilibrium for the 250°C junction temperature condition (9,010 W power module heat in a 3-to-1 MOSFET-to-diode heat loss ratio and bus bar and capacitor temperatures defined as Case 2 and provided in Table 3-4). An initial temperature of 50°C was imposed for all inverter components. Figure 3-57 shows the temperature versus time response for the MOSFETs, gate driver board, and capacitors. As shown, the MOSFETs achieve temperature equilibrium within a few seconds while the gate driver and capacitors require several minutes to reach steady-state conditions. The results indicate that it is possible to operate at junction temperatures of 250°C for short periods of time without exceeding the typical gate driver board and capacitor temperature limits of 125°C and 85°C, respectively.

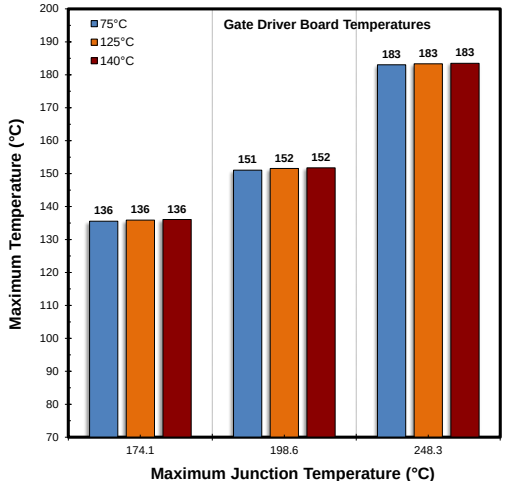

Figure 3-54: CFD-computed maximum gate driver temperatures for MOSFET temperatures of 175°C, 200°C, and 250°C. The under-hood temperatures are provided in the plot legend.

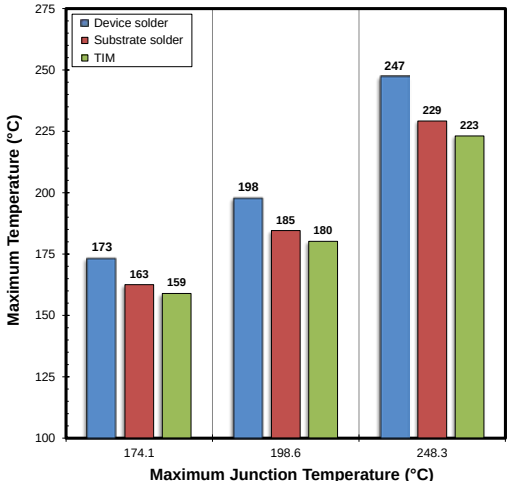

Figure 3-55: CFD-computed maximum solder and TIM temperatures for MOSFET temperatures of 175°C, 200°C, and 250°C.

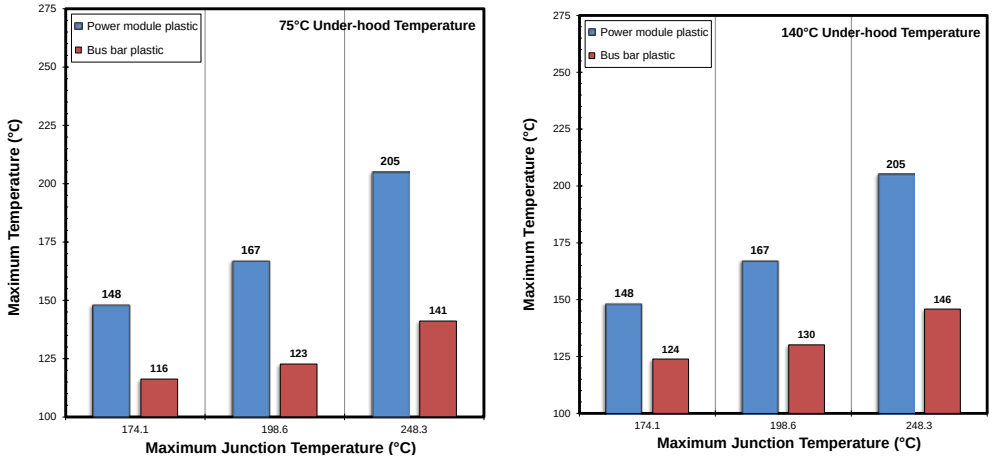

Figure 3-56: CFD-computed maximum power module and bus bar molding plastic temperatures for MOSFET temperatures of 175°C, 200°C, and 250°C. Results for under-hood ambient temperatures of 75°C (left) and 140°C (right) are provided.

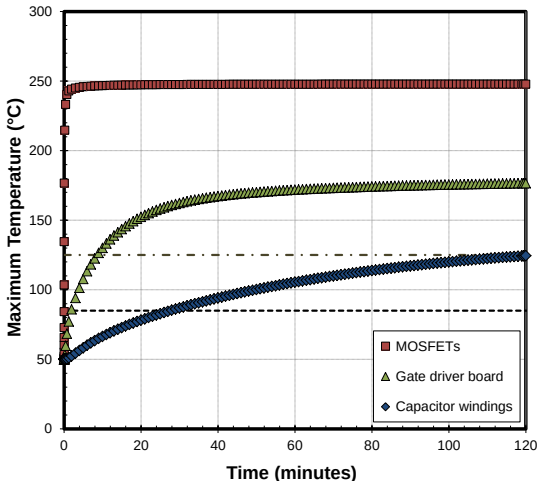

Figure 3-57: Transient FEA-estimated temperature response for the MOSFETs, gate driver board, and capacitors.

Evaluating Capacitor Cooling Strategies

A modified version of the LEAF inverter was used to evaluate the various capacitor cooling strategies. The modifications included placing the capacitors below the power modules as is shown in Figure 3-58. This configuration allows for the placement of a cold plate between the power modules, capacitors, and bus bars. This cold plate configuration enables cooling of the capacitors and bus bars in addition to the power modules. The modified model only included the capacitors, DC-side bus bars, and power modules because prior analysis indicated that capacitor excess temperatures were mostly associated with heat conduction through the bus bars. FEA was conducted to evaluate three capacitor cooling strategies: 1) improved cooling on the power modules to decrease junction temperatures, 2) directly cooling the capacitors using cold plates, and 3) cooling the DC-side bus bars using cold plates. The FEA only modeled one power module and one capacitor winding embedded within an epoxy encapsulant. Two bus bar configurations were evaluated (Figure 3-59). For bus bar Configuration A, the bus bars are placed side-by-side in a configuration that is typically used in inverters. For bus bar Configuration B, the bus bars are separate. Modeling the two configurations allows the effect of the bus bar design on the capacitor cooling strategies to be evaluated. Only the heat dissipated by the power modules was imposed in the models because capacitor temperatures are mostly dictated by the power module heat and not self-heating of the capacitors. Power module heat was imposed in a 3-to-1, MOSFET-to-diode heat loss ratio.

The effect of power module cooling performance on maximum capacitor temperatures is shown in Figure 3-60. A total of 1,784 W was dissipated by the devices, which produced a 175°C junction temperature for the baseline convective resistance case of 133 mm^2-K/W (convective resistance estimated for the LEAF cold plate at 10 liters per minute). As shown, reducing the convective resistance to 20 mm^2-K/W (85% reduction with respect to the baseline) reduces the junction temperature by 20°C and the capacitor temperature by 17°C. Therefore, improving the power module cold plate performance results in lower capacitor temperatures but the capacitor temperatures are still predicted to exceed 85°C for all cases evaluated. As expected, bus bar configuration has no effect on capacitor temperatures for this cooling strategy.

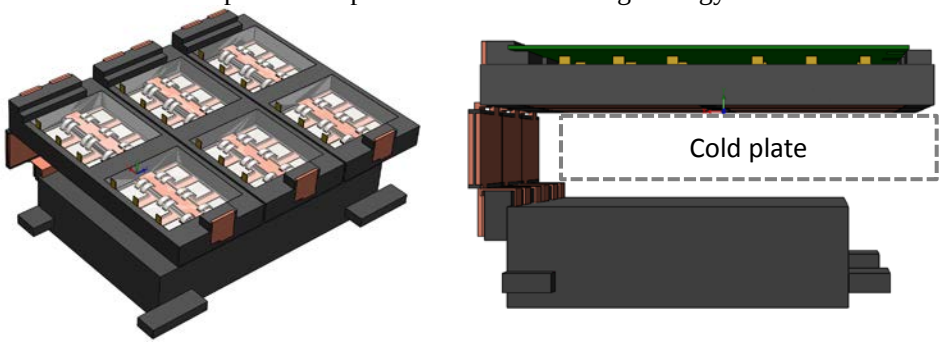

Figure 3-58: CAD drawing of the modified LEAF inverter used to evaluate various capacitor cooling strategies. This modified configuration would enable placing a cold plate between all components to aid in cooling the capacitors (right).

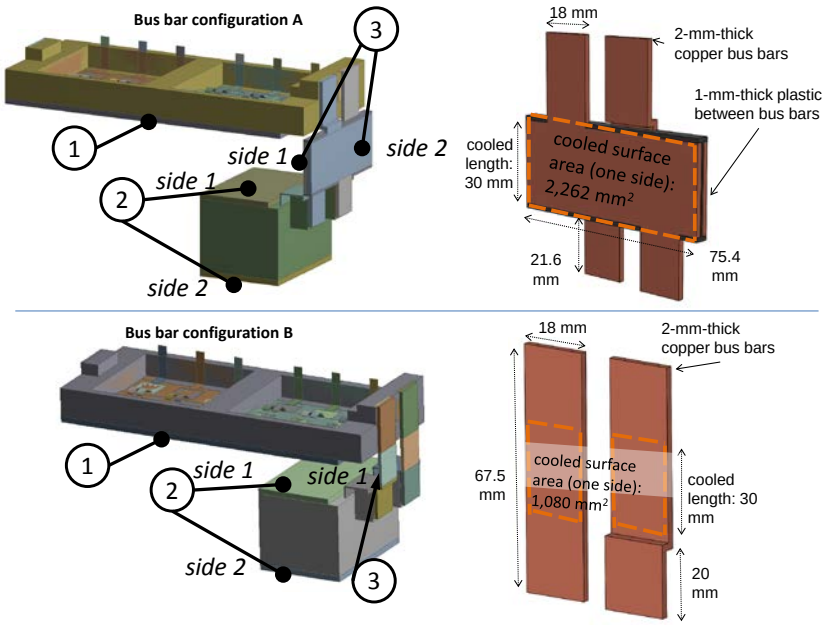

Figure 3-59: Bus bar Configurations A (top) and B (bottom). FEA was conducted to evaluate three capacitor cooling strategies: 1) increased cooling on the power module cold plate, 2) using cold plates on one or both sides of the capacitor, and 3) using cold plates on one or both sides of the DC bus bars.

The effects of using cold plates to cool the capacitors are shown in shown in Figure 3-61. Results are provided for the 175°C, 200°C, and 250°C junction temperature cases. A 3.25-mm-thick aluminum cold plate with a TIM thermal resistance of 55 mm^2-K/W at the cold plate-capacitor interface was used. Three capacitor cold plate strategies were evaluated: 1) cooling the capacitor's top surface (side 1 in Figure 3-59), 2) cooling the capacitor's lower-surface (side 2 in Figure 3-59), and 3) cooling both sides of the capacitor. Cooling one side of the capacitor provides slightly different capacitor temperatures for the two bus bar configurations—different thermal resistance through the bus bars for the two configurations is believed to be the reason for this effect. Additionally, cooling only one side of the capacitors does not enable capacitor temperatures <85°C. The capacitor electrical leads (hottest components) enter the capacitor encapsulant through the top and therefore cooling the top surface (side 1) is more effective as compared to cooling the lower surface. According to the analysis, a double-side cold plate cooling strategy would enable the capacitors to operate at temperatures below 85°C for junction temperatures up to 200°C. The double-side cold plate cooling solution does not provide sufficient capacitor cooling for the 250°C junction temperature case.

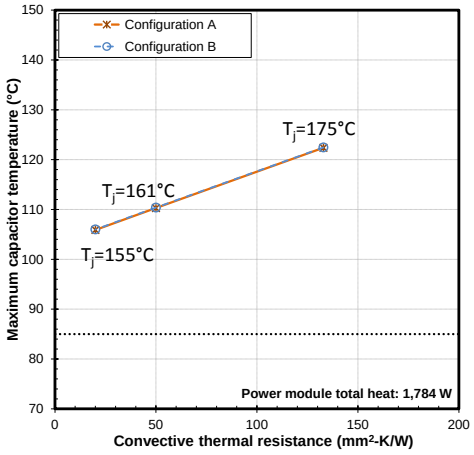

Figure 3-60: Maximum capacitor temperatures versus the power module cold plate convective resistance. Reducing the power module convective resistance from 133 mm^2-K/W to 20 mm2-K/W reduces the capacitor maximum temperature by ~17°C.

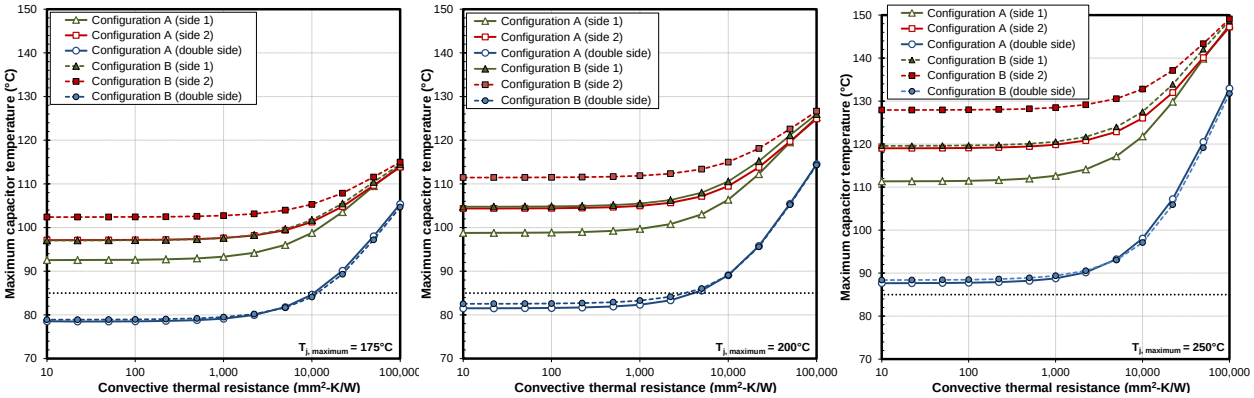

Figure 3-61: Maximum capacitor temperatures plotted versus the capacitor cold plate convective thermal resistance. The 175°C, 200°C, and 250°C junction temperature case results are provided. Results show that using two cold plates on the capacitor can enable the capacitor to operate below 85°C for junction temperatures up to 200°C.

The effects of using cold plates to cool the DC-side bus bars are shown in shown in Figure 3-62. Results are provided for the 175°C, 200°C, and 250°C junction temperature cases. Three bus bar cold plate strategies were evaluated for Configuration A—cooling the bus bar's front surface (side 1 in Figure 3-59), cooling the bus bar's back-surface (side 2 in Figure 3-59), and cooling both sides of the bus bars. Bus bar sides 1 and 2 are identical in surface area. The main difference between the two sides is that each side is connected to a different power module terminal (positive or negative). Due to the electrical lead layout with the power module, the different power module terminals operate at slightly different temperatures. Two bus bar cold plate strategies were evaluated for Configuration B—cooling the bus bar's front surface (side 1 in Figure 3-59) and cooling both sides of the bus bars. Only one side was cooled for Configuration B because its symmetric bus bar design meant that cooling the front side (side 1) was equivalent to cooling the back side. A heat transfer coefficient boundary condition was applied to the bus bar copper surface(s) to simulate cold plate cooling. Thermal resistances of magnitudes 181 mm^2-K/W and 19.5 mm^2-K/W were subtracted from the imposed convective resistance (inverse of the heat transfer coefficient) to account for the resistances associated with a dielectric pad and a 3.25-mm-thick aluminum cold plate. Therefore, the convective resistance values provided in Figure 3-62 are the resistances associated with the coolant and any area enhancement features (e.g., fins).

The results indicated that cooling the bus bars is an effective means to cool the capacitors. Cooling one or both sides of the bus bars enables the capacitor to operate at temperatures below 85°C even at the highest junction temperature of 250°C. Moreover, the bus bar cold plate convective thermal resistance values required to achieve capacitor temperatures below 85°C can be relatively high (~1,000 mm^2-K/W equivalent to an overall heat transfer coefficient of 1,000 W/m^2-K). Bus bar cooling for Configuration A initially provides lower capacitor temperature due to its larger cooled surface area as compared with Configuration B.

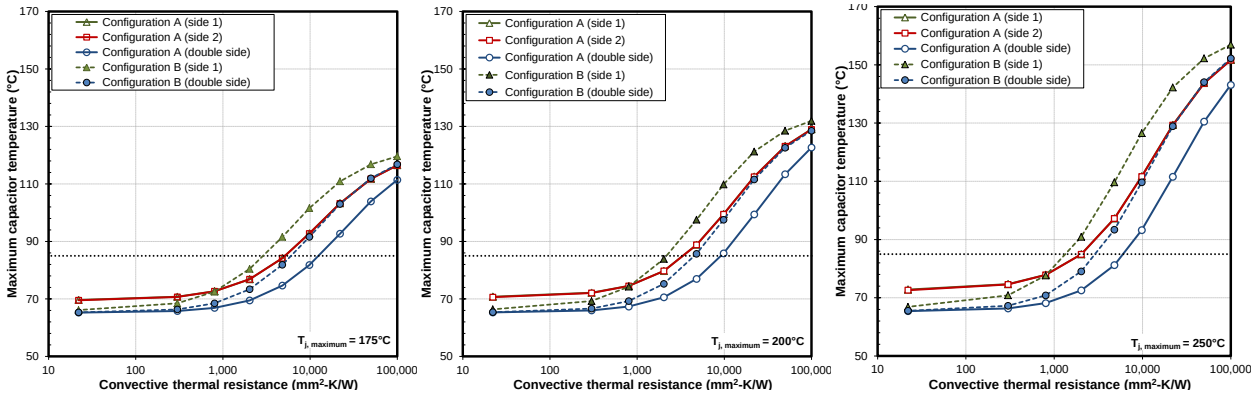

Figure 3-62: Maximum capacitor temperatures plotted versus the bus bar cold plate convective thermal resistance. The 175°C, 200°C, and 250°C junction temperature case results are provided. Results indicated that mounting cold plates to the bus bars enables capacitor temperature to operate below 85°C at all junction temperatures evaluated.

Figure 3-63 shows the effect of increasing the bus bar cooled surface area on capacitor temperatures. The cooled surface area was increased by increasing the cooled length dimension shown in Figure 3-59. Cooled lengths of 30 mm, 60 mm, and 90 mm were evaluated. The cooled surface areas for each configuration are provided in the figure legends. Results show that increasing the cooled surface area is more beneficial for higher convective resistance values (>1,000 mm^2-K/W).

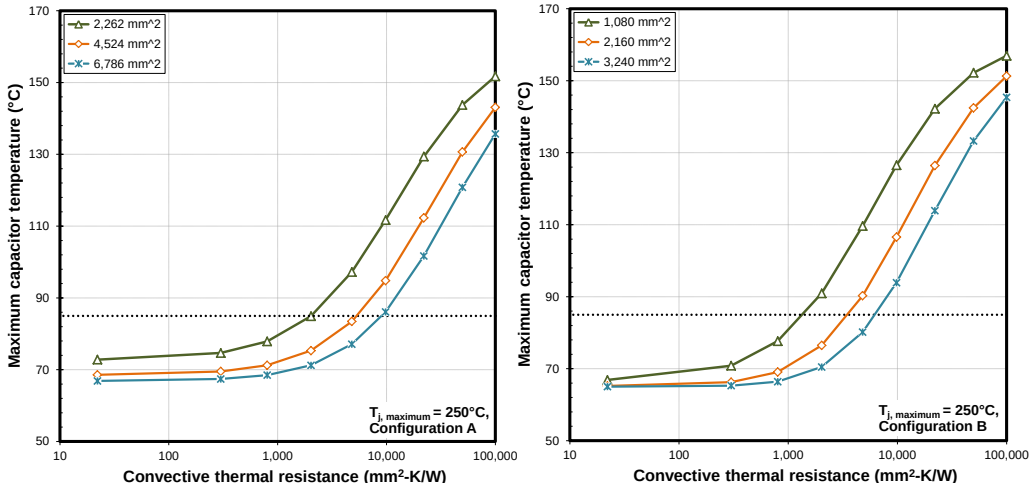

Figure 3-63: Maximum capacitor temperatures plotted versus the bus bar cold plate convective thermal resistance for the 250°C junction temperature case. The effect of increasing the bus bar cooled surface area (increasing the bus bar cooled length to 30 mm, 60 mm, and 90 mm, see Figure 3-59) on capacitor temperatures was evaluated. Cooling was only applied to one side of the bus bars. The figure legend provides the total cooled area.

Conclusions and Future Directions

Conclusions

- Modeling analyses indicate that capacitors and gate drivers are expected to exceed their typical temperature operating limits when exposed to high WBG temperatures (175°C, 200°C, and 250°C). The electrical interconnections (e.g., bus bars) are the primary thermal paths through which heat from the devices is conducted to the other components.
- Under-hood temperature environments are not predicted to have a significant effect on inverter component temperatures. The aluminum inverter enclosure provides a sheltered environment that limits the effect of under-hood temperature changes.
- Transient thermal simulations of an automotive inverter revealed that it may be possible to operate at 250°C junction temperatures, for short periods of time (several minutes), without exceeding the capacitor and gate driver typical temperature limits of 85°C and 125°C, respectively.
- Three capacitor cooling strategies were evaluated: 1) improving power module cold plate performance, 2) using cold plates on the capacitors, and 3) using cold plates on the bus bars. Using cold plates to cool the bus bars was the most effective strategy for cooling the capacitors. This cooling approach enables capacitor operating temperatures below 85°C at junction temperatures of 250°C. Moreover, a relatively low thermal performance cold plate placed on the bus bars can enable safe capacitor operation at high-temperature WBG conditions.

Future Directions

- Evaluate effect of module design on the various capacitor cooling strategies
- Evaluate gate driver cooling strategies
- Conduct experimental validation of key thermal concepts identified in the modeling work
- Evaluate motor-related inverter heating effects.

Nomenclature

I	electrical current
k	thermal conductivity
R"th	specific thermal resistance
T	temperature
Ω	electrical resistance

Subscripts

j	junction
RMS	root mean squared
r, z, φ	cylindrical system coordinates (radial, axial, and angular)
x, y, z	Cartesian system coordinates

FY 2016 Presentations/Publications/Patents

1. Bennion, K. "Power Electronics Thermal Management Research." 2016 DOE VTO Annual Merit Review, Washington, DC, June 2016.
2. Moreno, G. "Power Electronics Thermal Management Research." 2016 presentation to the DOE VTO Electrical and Electronics Technical Team, Southfield, MI, July 2016.

Acknowledgments

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References

1. Burress, T. "Benchmarking of Competitive Technologies." 2012 DOE VTO Annual Report, http://energy.gov/sites/prod/files/2014/03/f8/2012_apeem_report.pdf [Accessed: 2-Mar-2016].
2. Moreno, G. "Thermal Performance Benchmarking" 2015 DOE VTO Annual Report, http://energy.gov/sites/prod/files/2016/03/f30/FY%202015%20Electric%20Drive%20Technologies%20Annual%20Report.pdf [Accessed: 2-Sept-2016].
3. Lau, J.H., and Pao, Y.H. "Solder joint reliability of BGA, CSP, flip chip, and fine pitch SMT assemblies," 1997, NY McGraw-Hill.
4. Spectra-Mat, Inc. "Molybdenum-Copper Components" [Online]. Available: http://www.spectramat.com/pdf/PB-600-D%20Molybdenum%20Copper%20Components.pdf [Accessed: 18-Mar-2016].
5. MatWeb Material Property Data. "Overview of Materials for Polyphenylene Sulfide (PPS)" [Online]. Available: http://www.matweb.com/search/datasheet.aspx?matguid=301e3f904d6a43a7922601c9d11ded91 [Accessed: 18-Mar-2016].
6. MatWeb Material Property Data. "Overview of materials for Silicone, RTV, Encapsulation Grade" [Online]. Available: http://www.matweb.com/search/DataSheet.aspx?MatGUID=5660dbe1b55f4826809455e890cac682 [Accessed: 18-Mar-2016].
7. LORD Electronic Materials. "Circalok™ 6028/6029 Epoxy Encapsulant" [Online]. Available http://www.lord.com/products-and-solutions/electronic-materials/circalok-60286029-epoxy-encapsulant [Accessed: 20-Mar-2016].

8. MG Chemicals. “Thermally Conductive Epoxy Encapsulating & Potting Compound 832TC Technical Data Sheet” [Online]. Available: http://www.mgchemicals.com/downloads/tds/tds-832tc-2parts.pdf [Accessed: 20-Mar-2016].
9. MatWeb Material Property Data. “Aluminum 6061-T6; 6061-T651” [Online]. Available: http://www.matweb.com/search/datasheet.aspx?matguid=1b8c06d0ca7c456694c7777d9e10be5b [Accessed: 18-Mar-2016].
10. Azar, K., and Graebner, J.E. "Experimental determination of thermal conductivity of printed wiring boards." Semiconductor Thermal Measurement and Management Symposium, 1996. SEMI-THERM XII Proceedings. IEEE, 1996.
11. Balachandran, U. “Cost-Effective Fabrication of High-Temperature Ceramic Capacitors for Power Inverters.” 2014 DOE VTO Annual Report, http://energy.gov/sites/prod/files/2015/04/f21/FY14_EDT_Annual_Report.pdf [Accessed: 9-Sept-2016].
12. Yializis, A. “High Temperature DC Bus Capacitor Cost Reduction & Performance Improvements.” 2014 DOE VTO Annual Report, http://energy.gov/sites/prod/files/2015/04/f21/FY14_EDT_Annual_Report.pdf [Accessed: 9-Sept-2016].
13. Tan, D. “High Performance DC Bus Film Capacitor.” 2014 DOE VTO Annual Report, http://energy.gov/sites/prod/files/2015/04/f21/FY14_EDT_Annual_Report.pdf [Accessed: 9-Sept-2016].

3.5 Highly Integrated Wide Bandgap Power Module for Next Generation Plug-In Vehicles

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Contractor: General Motors Global Propulsion Systems
Subrecipients:
Cree Inc.
Virginia Polytechnic Institute and State University
Oak Ridge National Laboratory
Monolith Semiconductor Inc.

Contract No.: DE-EE0007285

Abstract/Executive Summary

- This annual report summarizes the first year's work of a three year collaborative to research, develop, and demonstrate a Highly Integrated Wide Bandgap (WBG) Power Module targeting GM's Next Generation Plug-In Vehicles.
  - Year one focus is technology evaluation, requirements definition, SiC MOSFET die development, die testing, die performance modeling, and power module concept design & analysis
    - Power module requirements are being derived from projected Plug-In Vehicle platforms launching in the 2022+ timeframe
  - Year two is SiC MOSFET power module detailed design, build, and testing
    - The power module will be functionally and mechanically optimized for use in GM's next generation traction inverter architecture
  - Year three is Inverter level integration, Testing and Manufacturing Process Development
    - Testing is planned to demonstrate efficiency and performance to meet or exceed DOE's specific power, power density and cost targets of 14.1 kW/kg, 13.4 kW/L and $3.3/kW

Accomplishments

- Excellent progress was made on Device Technology Assessments, Initial Power Module Design, and Top Side Metallization investigations.
- Issues concerning terms and conditions have delayed signing of ORNL CRADA, and the Cree sub recipient agreement.
  - The lack of agreements has delayed progress in die development specific to this project.
  - In spite of these obstacles, a analytically viable, Power Module design concept was developed.
- All work packages, except SiC MOSFET Die Development, are progressing as expected.
- WBG power module design concept was completed and analytical results were reviewed.

Introduction

This project will development a SiC MOSFET based automotive power module. The key goal is to establish a manufacturable WBG power module design, estimate power module production costs and integrate the power module into a target traction drive inverter design while making improvements in losses, mass, volume, and maintain automotive reliability/durability requirements. Highly efficient higher voltage traction inverters are key economic viability of high voltage electric traction drives.

Approach

Critical to implementing fast switching WBG devices, is reduction of DC loop inductance, effective control and protection of the SiC MOSFET switch.

GM is exploring improvement of the following components and features: gate drive circuitry, high bandwidth phase leg current measurement, fast over current protection, gate drive IC's with high common-mode transient immunity (CMTI), distributed DC link capacitors with a portion of DC link capacitors integrated with the power module; low inductance gate control interface, and potential for on die sensing.

The targeted maximum junction temperature is 200°C. To achieve this goal, GM will evaluate bonding, joining and thermal management technologies that can further reduce overall thermal impedance and improve high temperature reliability.

To achieve the aggressive power density target for the module level with high reliability requires:

- Minimize the number of paralleled dies through the use of larger size dies
- Potentially eliminate anti-parallel Schottky Barrier Diode die
- Use 900V SiC MOSFET die being developed by our partners
- Customize die topside metallization for high thermal and electrical conductivity
- Topside sintering
- Lower thermal resistance from die to substrate, to coolant channel
- Evaluate die characteristics at high junction temperatures to properly protect the power module.

SiC MOSFET's body diode and its channel, if turned on, can be used for commutation, thereby reducing or eliminating the need for separate anti-parallel Schottky Barrier Diodes (SBD), saving package space. GM and its partners will study the effects of SBD elimination on switching characteristics, losses, and thermal management without the anti-parallel Schottky Diodes.

Finally GM will verify the performance the resulted power module prototype using a selected set of GM production validation tests, including inverter level active load testing.

Results and Discussion

Technology Evaluation

Power Module Requirement Capture & Architecture Study

- A workbook has been developed to capture and cascade requirements
  - Contains: GM Inverter ratings, Power Module, Die Attachment, Capacitor, and Gate Drive Targets for future review with suppliers
  - Inverter Requirements have been cascaded from next vehicle applications
  - This task is at sufficient detail to continue with phase two tasks
  - If during the detailed design phase, additional requirements or changes are made, the document will be updated as needed

- Architectural modeling of a 3-phase hard switched inverter utilizing 3rd generation Cree SiC MOSFET die without paralleled diodes is complete
- Documented efficiency and range benefits given target design and architecture.

Key Findings: Project goal of "operate more efficiently" has been quantified through requirement capture and analysis. Detailed findings were presented during phase one Go/No-Go gate review.

WBG Device Technology Assessment

- Sub recipient, Virginia Tech (with confirmation testing performed in GM Labs):
  - Acquired static and dynamic performance data by testing supplier SiC MOSFET die samples assumed to be used in the project from Cree for modeling & analysis
  - Acquired static and dynamic performance data by testing Monolith SiC MOSFET die
  - Preparing and updated Cree Die MOSFET models in SPICE and SABER
  - Performed static and dynamic testing of other competitive pre-commercially released die that was not from sub recipients.
- Static Characterization
  - Characteristic curves of the target devices was performed at room temperature, 25°C and high temperature, 150°C. This includes transfer characteristics, output characteristics, RDSon, Vth, and device capacitances.

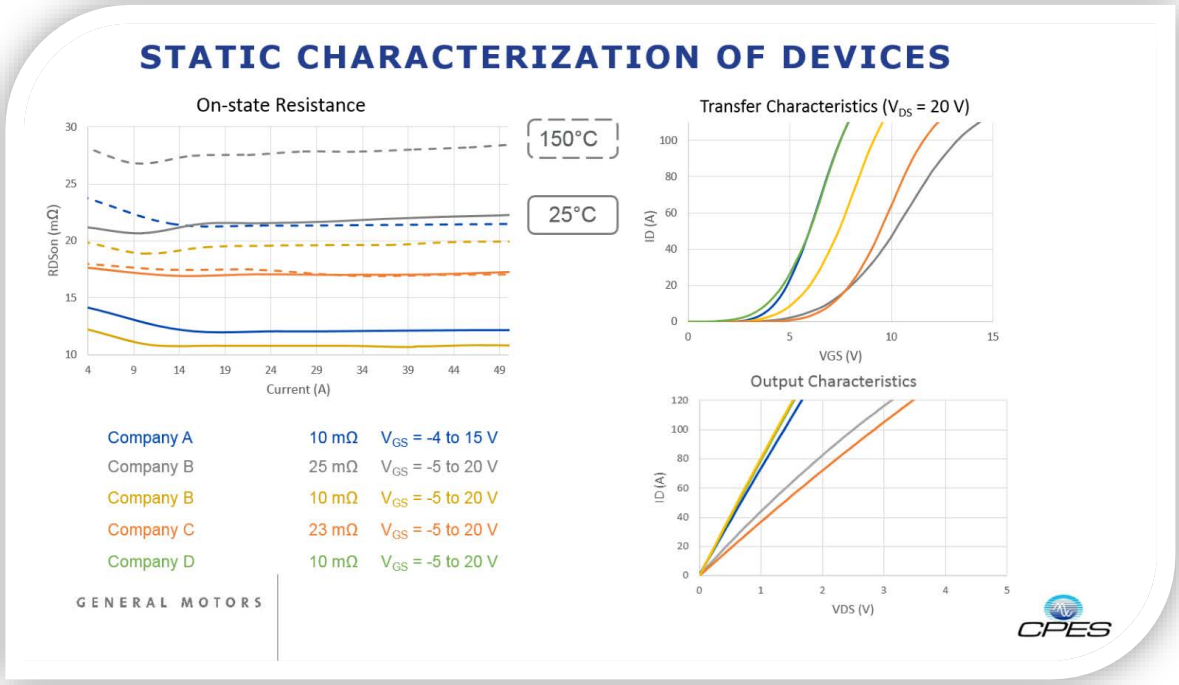

Figure 3-64: SiC MOSFET Static Characterization
Work performed by General Motors Subrecipient, Virginia Polytechnic Institute and State University, CPES

- Dynamic Characterization
  - Dynamic characterization of the target devices was performed at room temperature, 25°C.

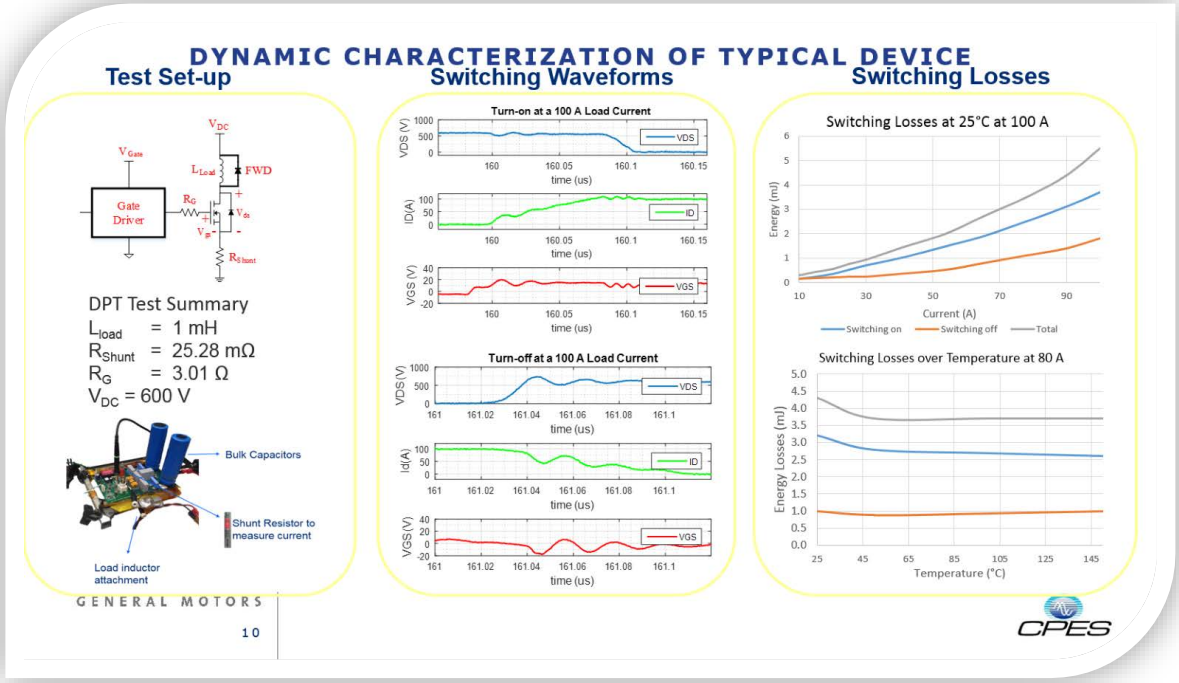

Figure 3-65: SiC MOSFET Dynamic Characterization
Work performed by General Motors Subrecipient, Virginia Polytechnic Institute and State University, CPES

- Schottky Barrier Diode (SBD) Effects on MOSFET Switching Energy

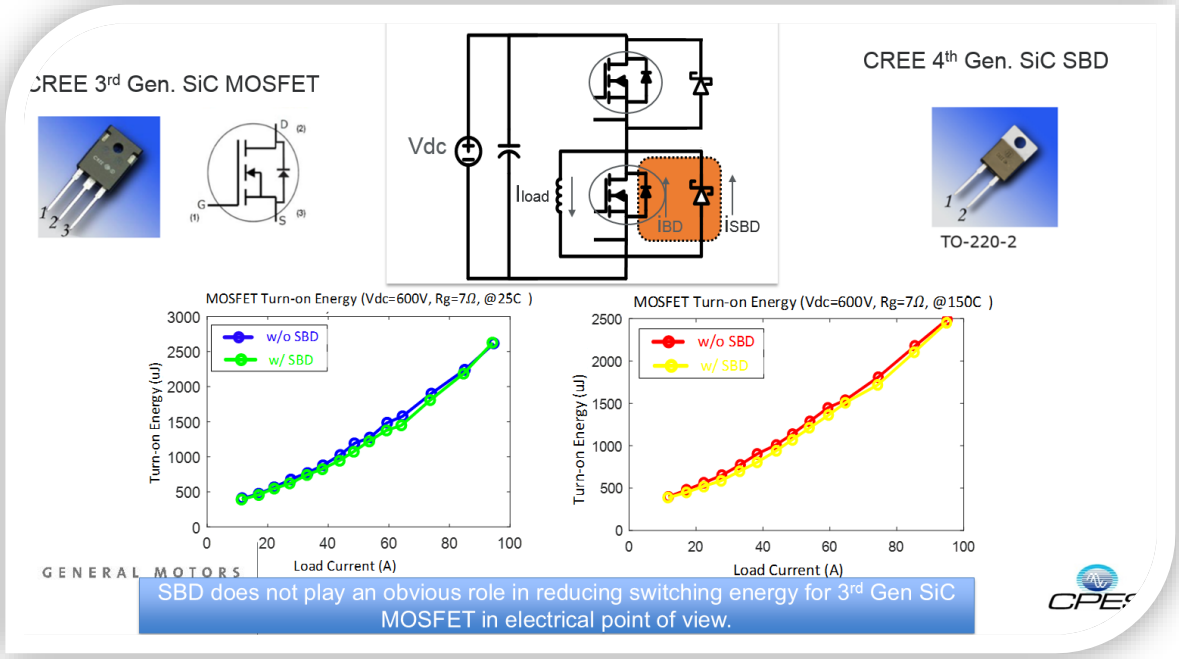

Figure 3-66: MOSFET Turn-on and Turn-off Energy with and without SBD at 25°C & 150°C
Work performed by General Motors Subrecipient, Virginia Polytechnic Institute and State University, CPES

Key Findings: (1) Die from subrecipients selected provide industry leading performance as compared to early SiC MOSFET samples tested. Detailed findings were presented during phase one Go/No-Go gate review. (2) SBD does not play an obvious role in reducing switching energy for 3rd Gen SiC MOSFET in electrical point of view. Project will move forward with plans to implement power module without SBD using subrecipient components.

WBG Device Modeling

- Based on device testing performed above, electrical performance models were developed to accurately reflect electrical performance.
- An equivalent circuit model was built using Q3D with inputs from:
  - High-temperature switching characterization
  - Double Pulse Test (DPT) board parasitics extracted via Q3D
  - Construction of a parasitic equivalent circuit using Saber® power MOSFET tool.

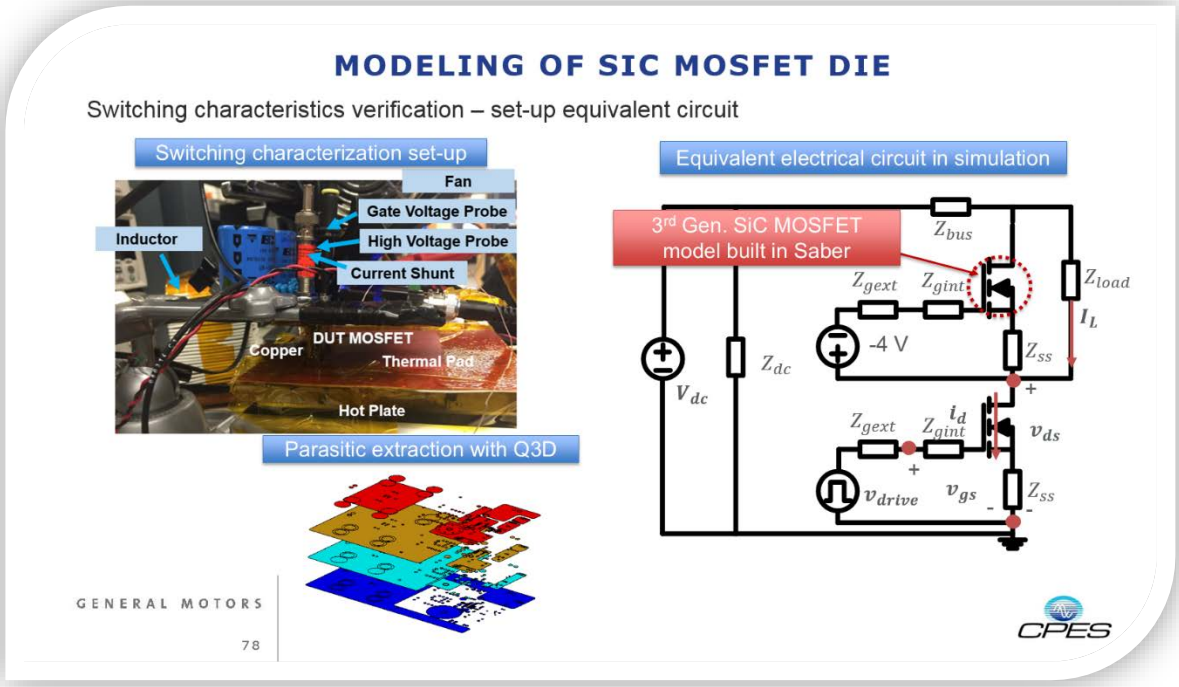

Figure 3-67: SiC MOSFET Modeling
Work performed by General Motors Subrecipient, Virginia Polytechnic Institute and State University, CPES

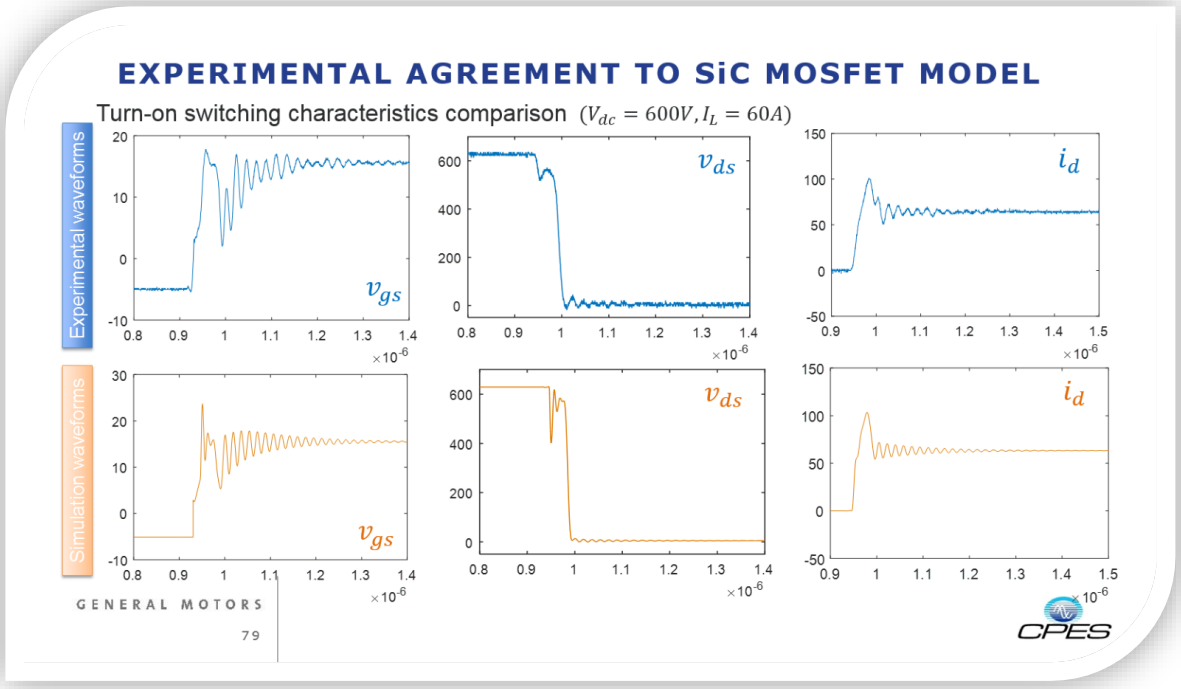

Figure 3-68: Experimental Agreement to SiC MOSFET Model
Work performed by General Motors Subrecipient, Virginia Polytechnic Institute and State University, CPES

Key Findings: Die modeling was successfully refined to have good agreement to experimental results.

WBG Device Modeling

- Based on device testing performed above, electrical performance models were developed to accurately reflect electrical performance

SiC MOSFET Die Development

Cree Die Development

- Provided MOSFET die in discrete packages to GM & Virginia Polytechnic University for evaluation
- Delayed project specific die development to budget period two

Monolith Die Development

- Completed pre-qualification on engineering samples
- Demonstrated state-of-art performance and reliability as compared to other manufacturer's devices
- Scaled MOSFET design to single die capable of currents to 150A, which were tested at CPES
- Provided MOSFET die in discrete packages to GM & Virginia Polytechnic University for evaluation
- Completed a 900V, 75A conceptual design to target requirements provided by GM
- Delivered a report on different approaches to implement sinterable top side metallization on die

Key Findings: Viable die from multiple sources are available for use on this project.

Integrated Power Module Technology & Design Concept Development

These key Power Module technology elements, were investigated during design concept development:

- Automotive specific power module design application duty cycles
- Hard switched SiC MOSFET 3-phase full-bridge in single package (6-Pack)
- Design features to reduce DC loop stray inductance
- Benefits of Distributed DC link capacitor in reducing DC loop inductance
- Distributed gate drive circuitry, particularly individual gate resistor on die
- Thermal impedance reduction junction coolant
- Sintered die attach, drain, source and gate connections without wire bonds

GM developed and modeled electrical and thermal performance, eight (8) design concepts utilizing target die. The leading concept summary is summarized below (patent application in process):

- Four(4) die per switch without anti-paralleling diode
- Power Loop inductance by Q3D analysis that meets target
- Signal loop inductance by Q3D analysis that meets target
- Footprint is half the size of industry leading silicon IGBT power modules
- Baseplate with a 3D Power Structure utilizing novel substrate integration techniques
- Pin fins on bottom for effective cooling.

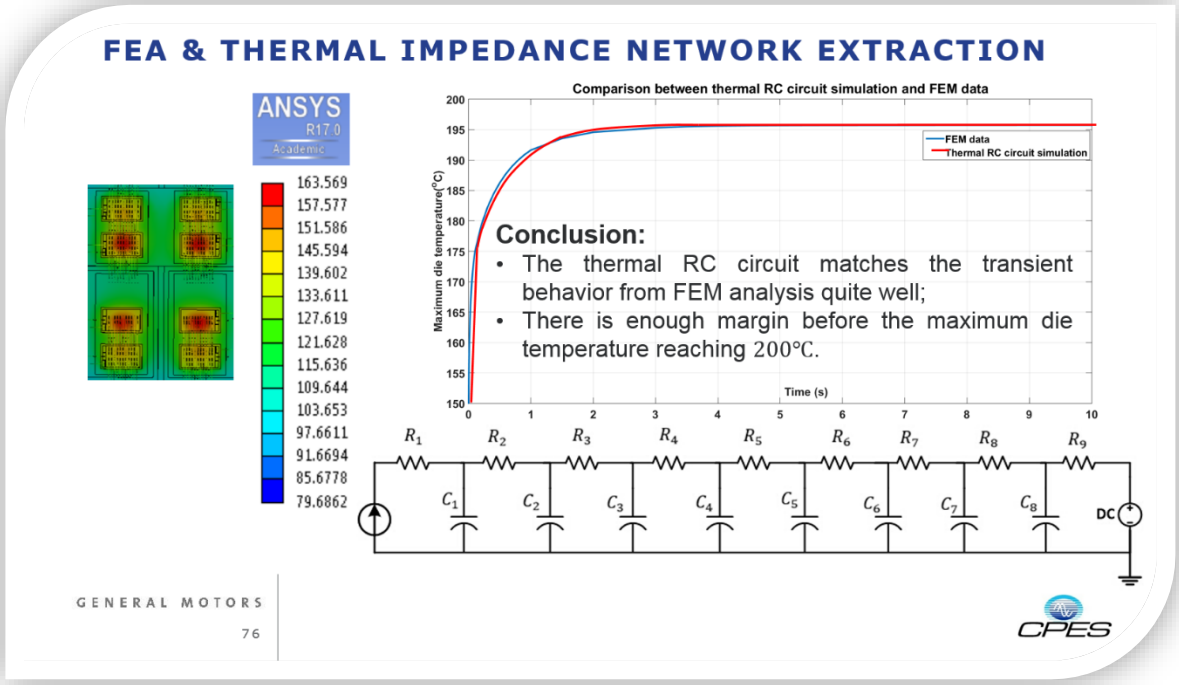

Figure 3-69: Power Module Concept design - FEA & Thermal impedance network extraction
Work performed jointly by General Motors & Subrecipient, Virginia Polytechnic Institute and State University, CPES

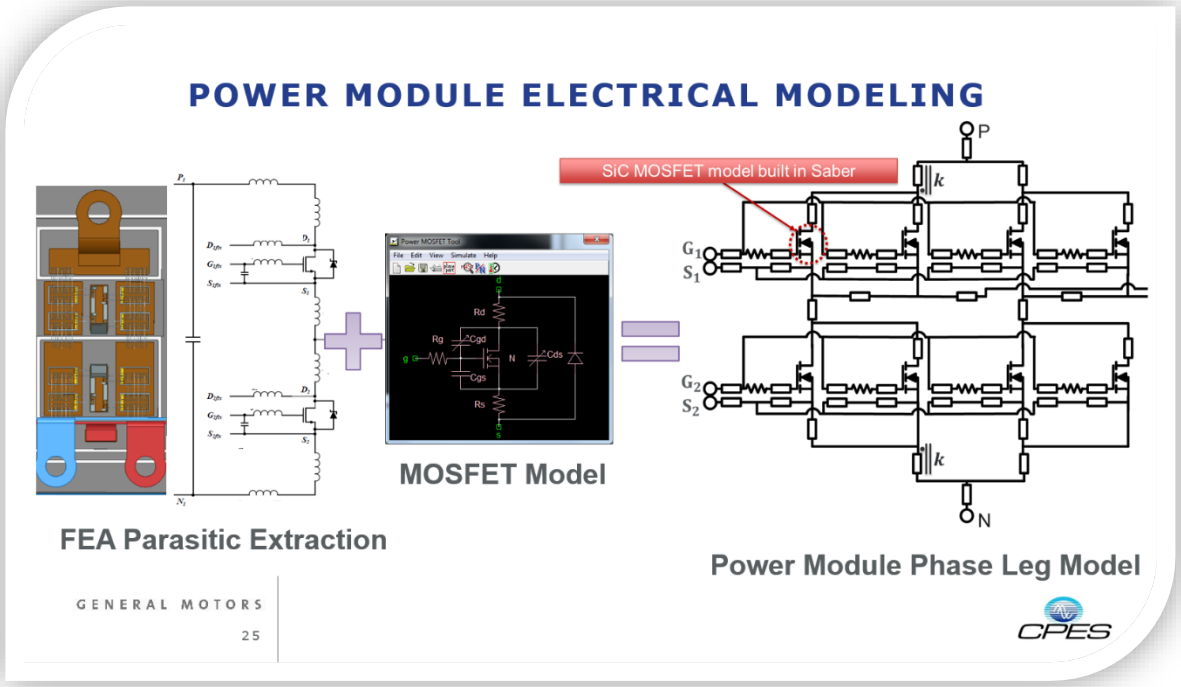

Figure 3-70: Power Module Concept design - Electrical Modeling
Work performed jointly by General Motors & Subrecipient, Virginia Polytechnic Institute and State University, CPES

Conclusions and Future Directions

Project goal of "operate more efficiently" has been quantified through requirement capture and analysis. Die from project subrecipients, demonstrated industry leading performance as compared to comparable early SiC MOSFET samples tested. The addition of an anti-paralleling SBD does not play an obvious role in reducing switching energy for 3rd Gen SiC MOSFET in electrical point of view. Die modeling was successfully refined to have good agreement to experimental results. Key performance parameters of package inductance, and size reduction have been accomplished. Although initial concepts were unable to keep the maximum die temperature below requirements, revised concepts have improved thermal performance.

Project will move forward with plans to implement power module without SBD using subrecipient components in phase two.

FY 2016 Presentations/Publications/Patents

Presentations

1. Power America Annual Meeting, 11 February 2016, "WBG Power Module Development"
2. ARPAe Switches Summit, 12 April 2016, "WBG Power Module Development"

Patent Applications

1. "Low Cost Dual Insulated Layer Substrate Power Module with Low Electrical Inductance" (P036622)
2. "Power Module Assembly With Reduced Inductance" (P036694)

3.6 88 Kilowatt Automotive Inverter with New 900 Volt Silicon Carbide MOSFET Technology

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Contractor: Cree, Inc.
Contract No.: DE-EE0006920

Abstract/Executive Summary for Budget Year Two

- Benchmark 900V 200A SiC MOSFET power module
  - At 20kHz operation, switching losses should be at least five times lower than Si IGBT modules
  - Estimated volume SiC die pricing should be < five times Si die costs, not necessarily amps per amps
- Qualify 900V, 10mΩ SiC MOSFET die and 900V, 200A SiC power module
  - Using minimum 1,000 die, 70 power modules assembled
  - Package die from three qual lots and use a mix of JEDEC and AEC-Q101 testing for qualification
  - Use >40 power modules for additional JEDEC and AEC-Q101 level tests
  - Power modules expected to have >1M hours MTTF
- Three Phase Traction Drive Demo
  - Three phase traction drive demo using 900V, 200A, 1/2 bridge power modules
  - Evaluate value proposition with automotive OEM or Tier One supplier

Accomplishments

- Benchmarked 900V, 350A SiC MOSFET power module with Ford Motor Company
  - Built 350A instead of 200A power modules based on OEM (including Ford) market feedback
  - Relative to 800V Si IGBT power modules, switching losses are up to 10X lower than Si IGBT power modules
  - Simulated EPA metro/highway drive cycle would result in 78% loss reduction in inverter for a pure EV, based on 90kW motor
  - Estimated volume die pricing of SiC is <5X of Si IGBT power die pricing.
- Began to qualify 900V, 10mΩ SiC MOSFET die and 900V, 350A SiC power module
  - Using 1,000 die, >39 of the 360A power modules assembled, which was equivalent amperage to 70 of the lower rated 200A power modules originally specified.
  - Three qual lots were used and a mix of JEDEC and AEC-Q101 qualification testing was performed. Die qualification tests have already successfully completed qualification at JEDEC level, 175°C.
  - Over 22 power modules have been assembled and used in qualification tests such as IOL, HTGB, HTRB. The quantity of 22 power modules at 360A, is approximately equivalent amps to the original milestone of 40 modules rated at 200A.

- Began Three Phase Traction Drive Demo
  - 900V, 350A, 2.5mΩ module measured at 25˚C are being used in the drive demo currently. Full results expected by end of contract in December, 2016.
  - Evaluation of measured module data with Tier One (Ford) resulted in 78% estimated inverter power savings when using these 900V power SiC MOSFET modules relative to 800V power Si IGBT modules. The primary power savings are in the city driving cycle.

Introduction

Present-day traction inverters are too expensive, too heavy, and too bulky to penetrate the mass consumer automotive market and hybrid vehicle sales are only about 3% of all vehicle sales. This effort seeks to revolutionize the electric vehicle traction drive industry through the optimization of the SiC device, power package, and traction drive systems to address the barriers listed. The main innovation thrust from the industry team will be on reducing system costs and extending reliability through inserting the newest break-through technology 900 V SiC MOSFET into advanced SiC-based power packaging and demonstrated traction drive technology. This new breakthrough SiC MOSFET based module is anticipated to reduce SiC die costs and switching losses in an 88 kW traction drive inverter modeled after the Ford Focus by 40% while increasing vehicle fuel economy, performance, and productivity (battery range, emissions reduction).

This effort brings together industrial teams which are leaders in products critical to HEV / EV drive trains. Cree is the leading supplier of SiC and GaN components, including SiC power MOSFETs and diodes. Cree is an automotive supplier of SiC diodes to HEV / EV platforms. APEI is a leading producer of high-temperature and low-inductance modules, which take full advantage of SiC power devices. APEI has also constructed automotive drive train prototype inverters in concert with other automotive OEMs on other efforts. Ford is the number one US producer of HEV / EV platforms, with a 13% market share in the US at the end of 2013.

Figure 3-71: This work brought together a team which is leading the market in SiC power device production (Cree), SiC power module technology (Cree Fayetteville, formerly APEI), and HEV/EV platforms in the US market (Ford). Cree is the leading supplier of SiC and GaN components, including SiC power MOSFETs and diodes, and is also an automotive supplier of SiC diodes to HEV / EV platforms. Cree-Fayetteville is a leading producer of high-temperature and low-inductance modules, which take full advantage of SiC power devices. Cree-Fayetteville has also constructed automotive drive train prototype inverters in concert with other automotive OEMs on other efforts. Ford is the number one US producer of HEV / EV platforms, with a 13% market share in the US at the end of 2013.

It is critical in this program is to use the best available SiC MOSFETs with 900V blocking (to handle up to 700V DC bus), low specific RDSON (cost), low RDSON over temperature, and low conduction losses. Working with a vehicle OEM (Ford), the team can determine if the improvement in drive-train efficiency would reduce battery costs enough to offset the extra cost of SiC. This team is uniquely positioned to develop the best available 900V SiC MOSFET, measure its performance in both discrete and module form, and bench mark it against other technologies in terms of cost and performance.

Approach

The approach here in the first year was to scale up the lowest RDSON, lowest RDSON per unit area, 900V SiC MOSFET possible, and optimize it for low conduction losses over temperature. This would produce the lowest RDSON MOFET of any technology known, with a blocking voltage capability >650V.

The system level advantage would be to produce a low RDSON power module which would enable dramatically lower conduction losses in the electric drive train. If the drive train inverter is responsible for approximately 4% of overall losses in an electric vehicle, cutting these losses in half would reduce vehicle losses by 2%, which is fairly dramatic impact to the cost of an electric vehicle.

The year two budget milestones are shown below, along with their status.

Table 3-5: Budget Year Two Milestones

	Type	Description	Status
900V 200A SiC MOSFET module benchmark summary	Technical	Summary comparison of data made from data collected in power module measurements and available comparable Si power modules. For 20 kHz operation, switching losses should be at least five times lower, and the estimated volume production of SiC die pricing should be less than a five times multiple of Si die costs. Comparisons may not be based on “Amps per Amps” comparisons, but instead on expected rated capabilities given the impact in different efficiency and thermal constraints.	Done
900V, ½ bridge power module QUAL assembly	Technical	Using 1,000 die minimum from the three QUAL wafer lots, 70 power modules (900V, 200A, ½ bridge configurations) will be assembled for extensive qualification and characterization.	Done* * built 39, 360A module instead of 70, 200A modules
Die level qualification of 900V, 10-20 mΩ, large-area MOSFET completed	Technical	Package die from all three qualification lots for die qualification testing. Generate die level qualification report using sufficient packaged die from each of the three qualification lots. A mix of JEDEC and AEC-Q101 testing will be done to prepare for commercial product release, and a quality report will be generated as a deliverable.	In process

	Type	Description	Status
Power module qualification of 900V, 200A, all-SiC, ½ bridge power module	Technical	A mix of JEDEC and AEC-Q101 tests will be performed on > 40 power modules. Results will be used to generate a qualification report for automotive customers. Power modules are expected to pass over one million hour's mean time to failure.	In process* * used >22, 360A module instead of >40, 200A modules * JEDEC & MTTF tests on die instead of modules for better statistics
Three Phase Traction Drive Demo	Go / No-Go	Perform three phase traction drive demo using 900V, 200A, ½ bridge power modules and evaluate impact of SiC performance on automotive traction drive system. Evaluate value proposition with automotive OEM or Tier 1 supplier as appropriate to determine if metrics (efficiency, reliability, costs) look reasonable to move forward. This is a system level decision based on cutting HEV cost premium through reduced inverter costs and/or extending battery range.	In process

Benchmark of 900V, 350A SiC MOSFET power module with Ford Motor Company

Continuing from year one, the 900V, 10mΩ SiC MOSFETs were fabricated with a total chip area of 32mm2, from many different lots, including three qualification lots (generating over 2,000 good die for qualification tests), and a delivery of 1,000 good die for module assembly in Fayetteville.

Thousands of the MOSFETs were assembled in TO247-4L packages for reliability testing, whilc over 1,000 MOSFETs were dedicated for module assembly in the 62mm, low-profile, 1/2 bridge power module described in last year's report. One difference is this year the isolation voltage was increased from 1.2kV to 3.5kV, and the modules were designated as "Rev B." The 900V Rev. B power module switching energy was re-measured as described below.

Table 3-6: 900V 10mOhm SiC MOSFET based module benchmark testing

Module 1 Benchmark	Module 2 Benchmark	Comments
FS200R12PT4P 6-pack configuration VCES = 1200V; ICnom = 200A 21.5 mJ; 4.9x higher @ 25°C 35 mJ; 8.0x higher @ 125°C 39 mJ; 9.0x higher @150°C	FF300R12ME4_B11 Dual configuration VCES = 1200V; ICnom = 300A Cies = 18.5 nF RGon = 1.3 Ω; RGoff = 1.3 Ω 34.9 mJ; 8.0x higher @ 25°C 54.5 mJ; 12.5x higher @ 125°C 61.5 mJ; 14.1x higher @150°C	Erec is ignored in both cases which skews data more favorably to Si IGBT. IGBT: Cies = 14.0 nF MOSFET: CISS = 3930 x 4 = 15.7 nF τ = RC are similar τ = 15.4 vs. 15.7 ns

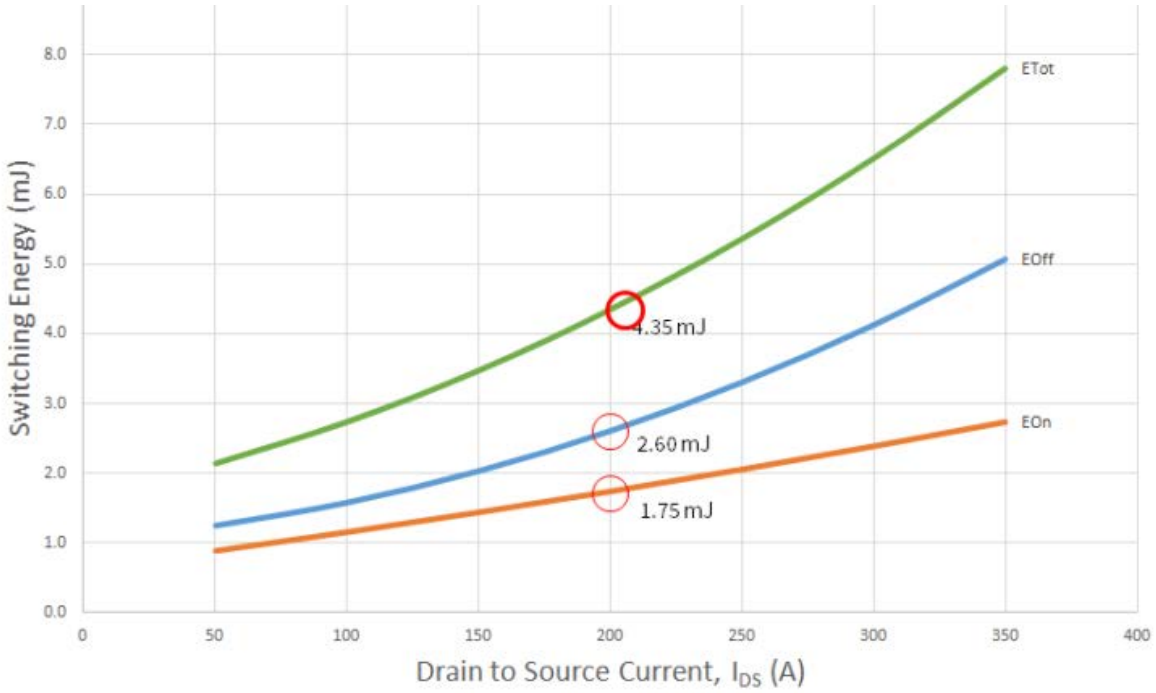

Figure 3-72: Comparison of measured switching energy for a 900V, 360A, 2.5 mΩ SiC half-bridge power module over drain current, with respect to data sheet values of Si IGBT based power modules. Measuring at 600V, 200A, total switching energy was 4.35mJ. Switching energy of the SiC based module are 5-14 times lower than benchmark Si based modules.

One of the important year two milestones was to benchmark the 900V, SiC MOSFET half-bridge power module relative to a Si IGBT half-bridge power module. In Figure 3-72, the measured switching energy is shown for a 900V, 360A, 2.5 mΩ SiC Rev. B half-bridge power module over drain current. Also shown are the data sheet switching energies for a Si IGBT based power module (FF300R12ME4_B11 and FS200R12PT4P), which are 5-14 times higher than the SiC MOSFET power module. This measured data meets the technical milestone for a minimum five times reduction in switching losses with SiC.

In addition to switching loss improvement, the SiC MOSFET has lower conduction losses than Si IGBT in two separate in two ways.

- First, for a 100A switch, the 900V, 10mΩ SiC MOSFET has dramatically lower forward voltage drop than the Si IGBT from 0-80 A. Only at ~100-120A depending on temperature, or "rated current", do the conduction losses actually match with an identical VF of approximately 1.8V.
- Second, since every IGBT has a "knee" voltage before turn-on, of around 0.5V, at light load conditions, which is where most automobiles are operated for the majority of the time, the VF cannot be reduced no matter how many IGBTs are placed in parallel. The SiC MOSFET on the other hand, can dramatically reduce its resistance even further when parts are put in parallel inside typical modules.

To look at the SiC impact at a system level, Ford measured the switching losses of an 800V Si IGBT power module used in their current BEV platform, and also measured the losses of a 900V, 2.5mΩ SiC power module provided by Cree under this program. The measurement set-up and details are shown in Figure 3-73. Only 127.2 mm2 of SiC was used per switch, whereas 400 mm2 of Si area was used per switch.

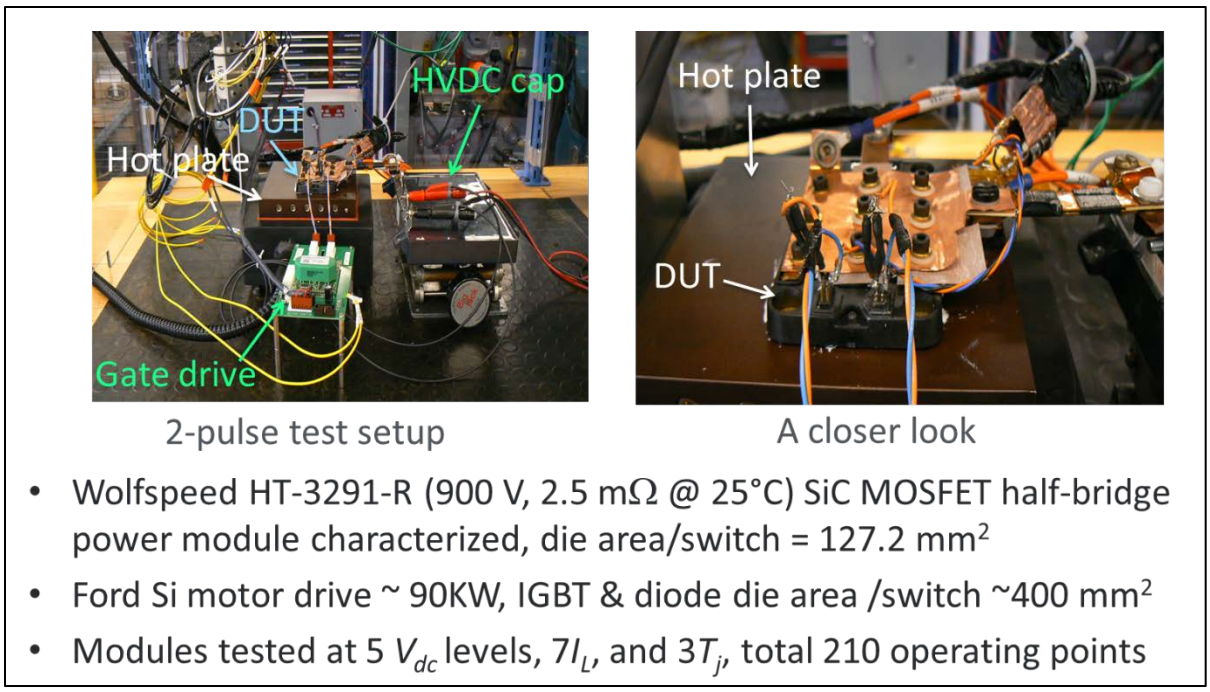

Figure 3-73: Double pulse test setup to measure switching energies of a 900V, 360A, 2.5 mΩ SiC half-bridge power module.

The measured data obtained in the set-up shown in Figure 3-73 was then used in a simulator, assuming a 90 kW electric motor assumed for the machine models, with synchronous rectification for SiC devices, and no added parallel diodes.

The results, shown in Figure 3-74, illustrate that compared to the Si one, SiC reduces inverter losses by ~78% in electric-only drive mode for EPA metro-highway cycle. The inverter loss comparison is shown in Figure 3-74 for both EPA drive cycle from city and highway driving. This result demonstrates the high-level value proposition for using SiC in a pure electric vehicle. In cutting the the inverter losses, the vehicle range can be extended for the same battery costs, or possibly battery costs could be reduced while maintaining range.

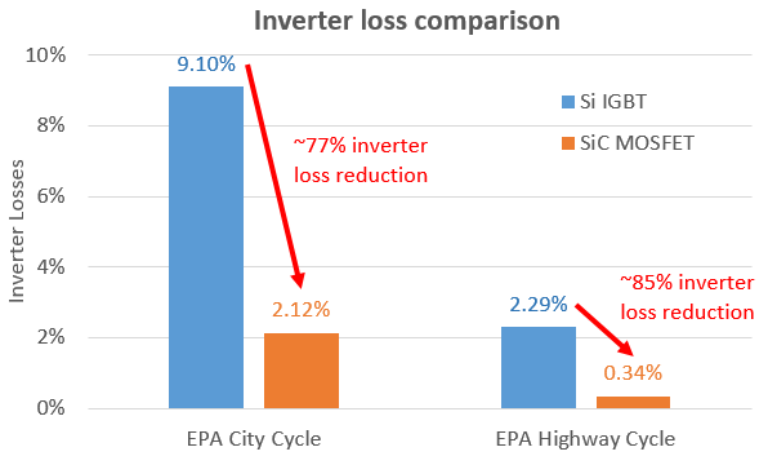

Figure 3-74: Circuit used for measurement comparison of switching characteristics of the 900V, 10 mΩ SiC MOSFET in a TO-247-3L package and a TO-247-4L (source Kelvin contact) package.

Module and Die Qualification

Another major milestone for this program in the second year was to package die from all three qualification lots for die qualification testing. The milestone was to then generate a die level qualification report using sufficient packaged die from each of the three qualification lots. A mix of JEDEC and AEC-Q101 testing is to be done to prepare for commercial product release, and a quality report will be generated as a deliverable.

Three qualification lots were fabricated, using the 900V, 10mΩ SiC MOSFET shown below in Figure 3-75. The cross-sectional cartoon is shown on the left, while the top-view is shown on the right inside a TO247-4L package. Connections to gate (G), drain (D), and source (S) are clearly marked in Figure 3-75 as well. The Kelvin Source (KS) contact is used to minimize gate-source voltage feedback (di/dt Lsource) during switching events.

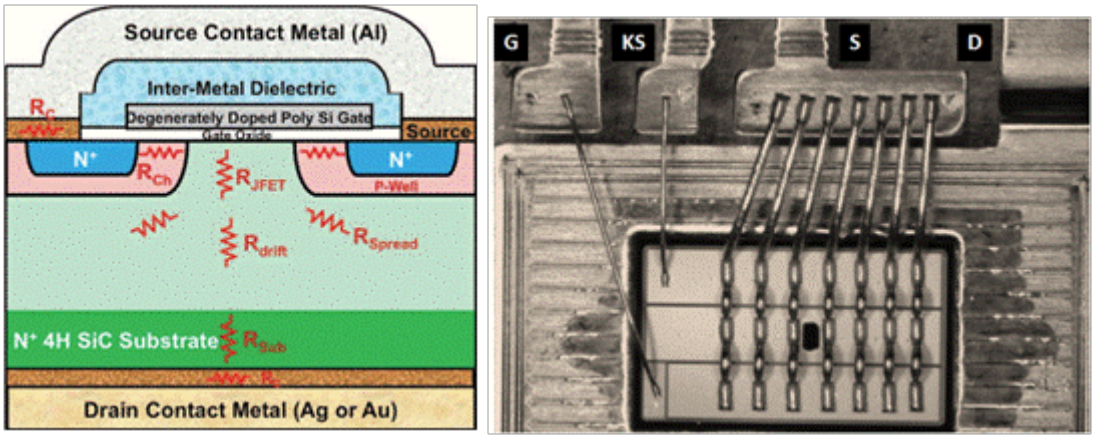

Figure 3-75: 900V, 10mΩ, 32mm2 SiC MOSFET shown in top view (left) and cross-section (right). The top photo illustrates the three source pads, gate pad, and Kelvin source contacts. The cross-section illustrates the planar DMOS cross-section of the MOSFET device.

The measured DC output characteristics of the MOSFETs are characterized in DC mode from -55°C to +175°C. Sample output characteristics are shown in Figure 3-76 at these conditions. Although the pulsed (200us) current exceeds 300A, thermally the MOSFET is practically limited to ~160A by the TO-247 terminals at 25°C, and a typical operating temperature of 100°C would result in a 117A rating. For modules, with different thermal surroundings and connection technology, different / higher amperage ratings are possible.

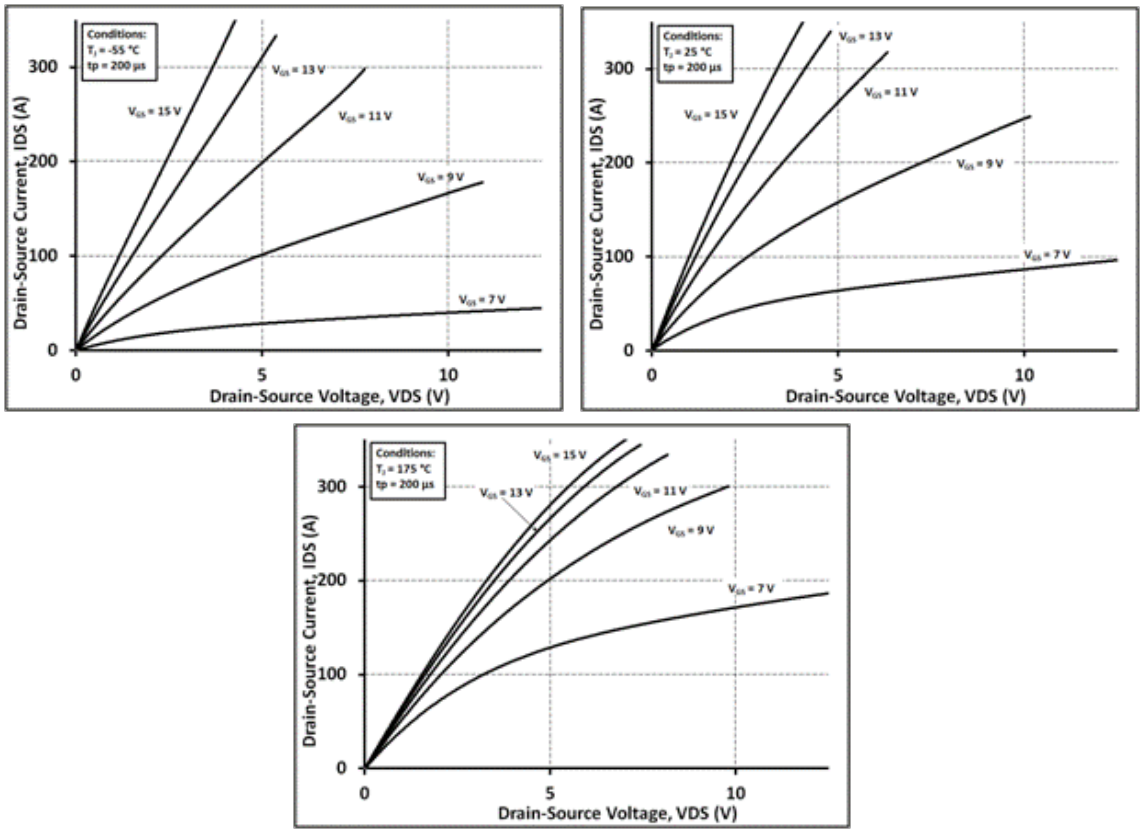

Figure 3-76: DC output characteristics of 900V, 10mΩ SiC MOSFET at -55°C (top left), 25°C (top right), and +175°C (bottom) temperature. The maximum DC operating point of the gate voltage is +15V, with a typical threshold voltage of 2.4V at 25°C.

For the 900V MOSFETs, it is also important that the product have significant overhead margin above 900V blocking capability under all temperature conditions. Examining a small population of the MOSFETs from the qualification lots, blocking voltage was measured from -55°C to +175°C. For a sample population of components, typical Breakdown Voltage from Drain-Source (VBRDSS) at the onset of avalanche voltage as a function of temperature from –55°C to 175°C was measured. Zero volts were applied to the gate terminal, and the typical VBRDSS ranged from 1150V to 1180V, with minimum VBRDSS >1100V over all temperatures measured for the 900V rated MOSFETs. The shaded region above and below the mean (typical) breakdown voltage below represents a standard deviation of the population measured.

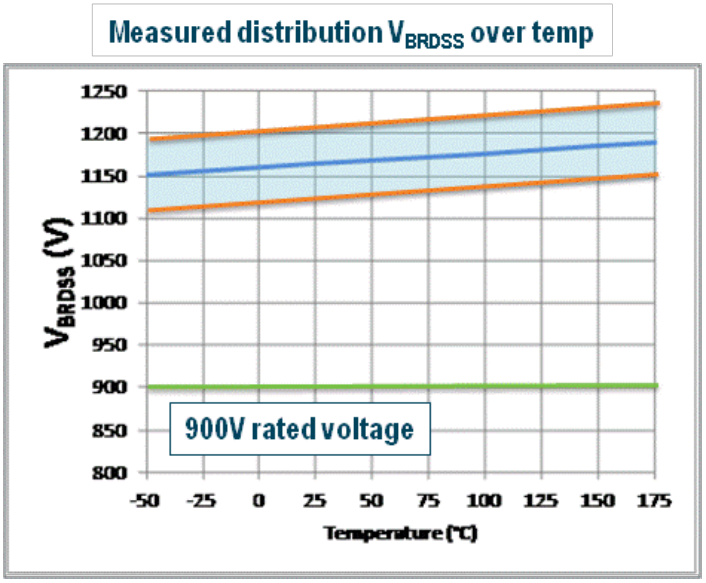

Figure 3-77: Typical VBRDSS ranges from 1150V at -55°C to 1180V at 175°C of the 900V, 10mΩ rated SiC MOSFET. Minimum VBRDSS of >1100V over all temperatures measured for sample distribution of parts.

The planar MOSFET structure here is detailed elsewhere, and is based on a rugged design which has been commercially available since 2011. The differences in this design are the total area is 20% larger than the largest commercial SiC MOSFET in the marketplace, and the design has been changed to lower peak electric fields in the drain. Being a planar structure, there are no sharp corners to be concerned with in the gate oxide which can crowd electric field.

This qualification plan is based on a compilation of the guidelines of AEC-Q101, Stress Test Qualification for Automotive Grade Semiconductors, and JEDEC document JESD47, Stress-Test-Driven Qualification of Integrated Circuits, and references therein. The die qualification is at TJ of 175°C, and qualification tests unique to plastic package parts were limited to 150°C as a precaution. As most die are intended for module use, the maximum die TJ rating is 175°C.

Table 3-7: 900V 10mOhm SiC MOSFET Qualification Tests

Qualification test	Stress Conditions	Lots	#/Lot	# Fails
High Humidity High Temperature Reverse Bias (H3TRB)	85°C, 85% Relative Humidity, 100V, 1000 hours	3	25	0
Thermal Shock (TS)	150°C/-55°C, 1000 cycles	3	25	0
High Temperature Reverse Bias (HTRB)	720V, 175°C, 1000 hours	3	25	0
High Temperature Gate Bias (HTGB)	15V, 175°C, 1000 hours	3	25	0
High Temperature Gate Bias (HTGB)	-4V, 175°C, 1000 hours	3	25	0
High Temperature Gate Switch (HTGS)	+19V/0V, 175°C, 10% DT for 100 hours	3	25	0

In Table 3-7, the qualification tests, stress conditions, number of lots tested, and number of devices per lot tested, are outlined. The die-related tests, H3TRB, HTRB, HTGB, and HTGS were all performed at 175°C. All of the die tests have been passed at the JEDEC level at 175°C. The AEC-Q101 testing is ongoing, and will be completed after the end of program.

Module reliability testing

For module level reliability testing, modules were assembled in half-bridge, 360A rating, 2.5mΩ configuration for reliability testing. Compared with last year's module, the structure was revised to "Rev B" which increased the isolation voltage from 1.2kV to 3.5kV.

Many of the same tests (HTRB, HTGB, etc.) were repeated from die level testing at the module level. For power cycle testing, which is unique to the package (module environment), successful results were obtained as shown in Figure 3-78, as the four modules tested all exceed 40,000 cycles (goal) before degradation. Failure analysis revealed lifted power bonds on the die as the failure mode for all high-side switch positions.

Module	# cycles	Failure Mode	TIM
199309	67,081	$V_f > 5\%$	Grease
199313	62,880	$V_f > 5\%$	Graphite
199314	73,374	$V_f > 5\%$	Grease
199315	79,659	$V_f > 5\%$	Graphite

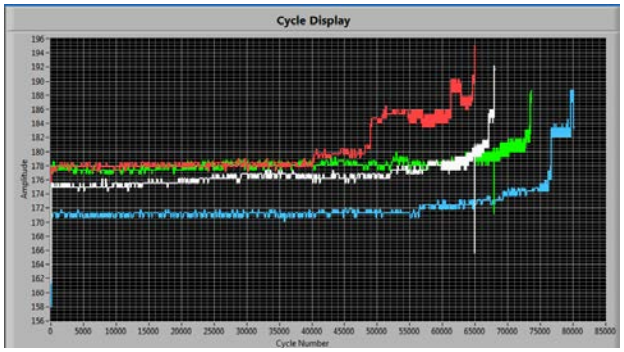

Figure 3-78: Switching Energy losses at 25°C for the 900V for 900V, 10 mΩ SiC MOSFET in TO-247-4 package (RG=5Ohm, VGS=-4V/+15V, VDD=600V)

Three Phase Traction Drive Demonstration

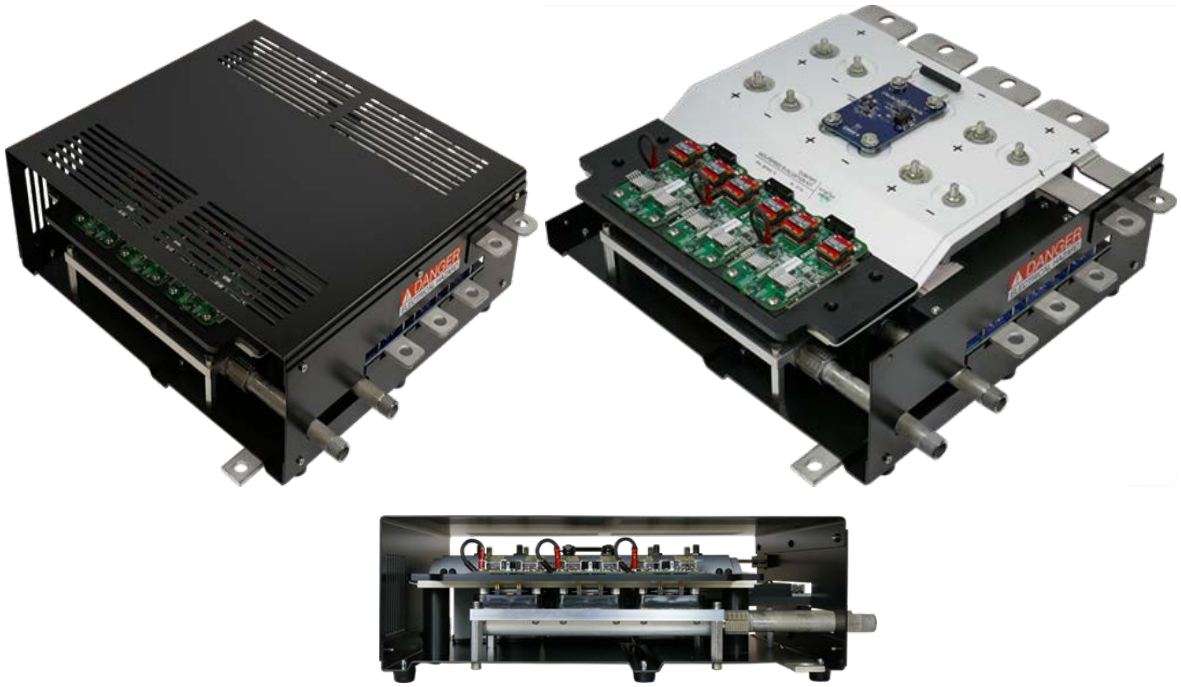

Figure 3-79: 900 V SiC-optimized high-power inverter for three phase evaluation.

Four (4) tests have been performed to date, with two (2) done with manual control and supervision to establish the safe operating areas at 200 and 400 V DC. Two (2) more tests were done using the auto-sequence at 200 V DC. The 20 kHz switching, this test ran fine without manual intervention. For 10 kHz switching, but it ran into some speed loop instability trying to reach 2000 RPM. The reasons for the instability are not yet determined but are under investigation.

Testing will continue through 12/14/2016.

The inverter build appears to operate as expected for the standard 20 kHz switching frequency. Although the 10 kHz switching data is incomplete, the part that overlaps the 20 kHz data shows a “better efficiency”. As more test data becomes available, these results will be compared to the 1200V SiC results. We expect to test over a range of switching frequencies to establish the trade-off between frequency and efficiency.

DC bus voltages will be tested at 200, 325, 450, and 575-600 volts. For testing beyond 200 A, a three-phase R-L load will be used

The SiC MOSFETs were placed in Cree Fayetteville 62 mm power modules in a half-bridge configuration, as described in last year's report. Four MOSFETs per switch position, or eight MOSFETs per module, were assembled in the low-inductance modules. Figure 3-80 below illustrates the placement of the MOSFETs in the module.

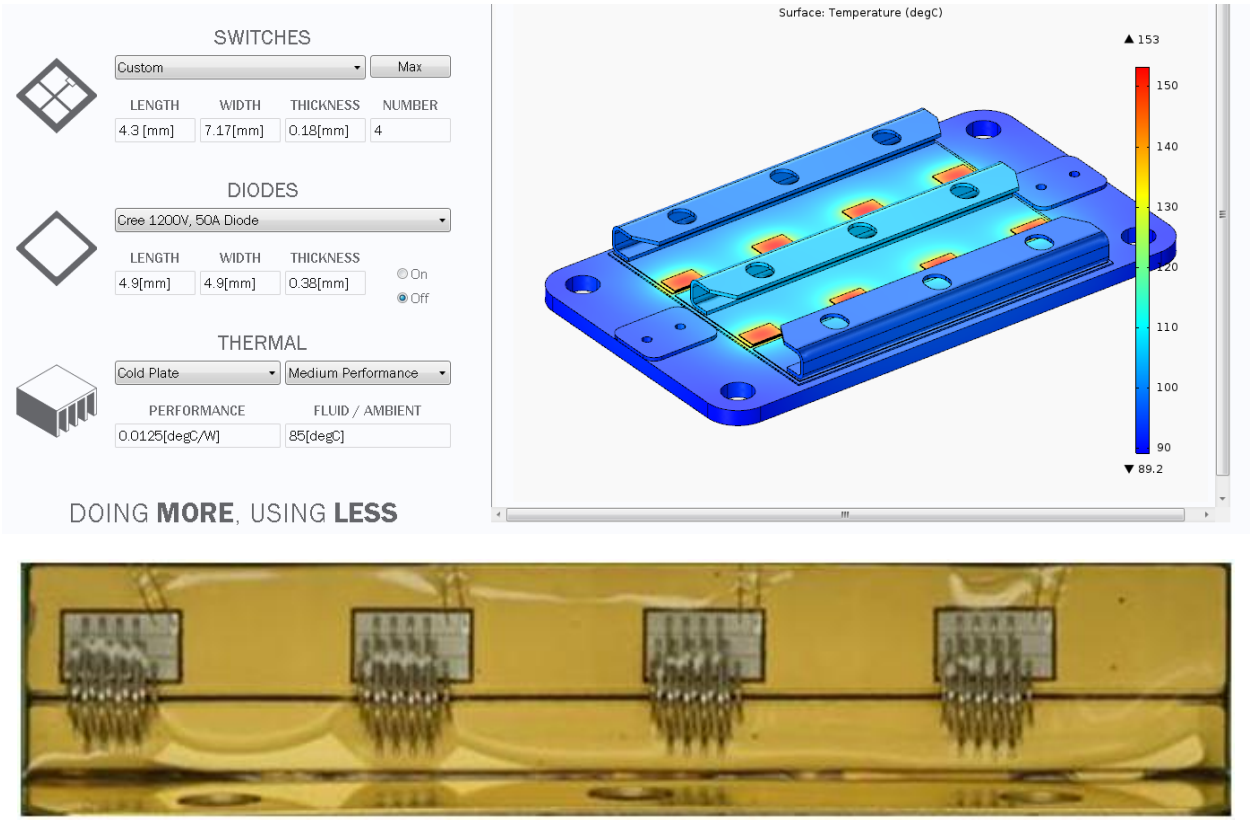

Figure 3-80: Four of eight die positions populated in the half-bridge power module with 900V, 10mΩ SiC MOSFETs. Upper image illustrates thermal simulation of all eight MOSFETs inside the power module, with peak temperature of 150°C on each die. Lower image illustrates a close-up of four MOSFETs in a single switch position inside the module.

Electrically, the power module switching energy losses were shown earlier in the report, but the conduction losses are of primary importance in the low-frequency drive-train application. As shown in Figure 3-81 below, measurements of the four die per switch result in ~2.5mΩ at 25°C, increasing to 4.25mΩ at 175°C. Relative to the Si IGBT, there is no knee voltage at low current, and the on-state resistance is fairly flat in the power module from 25A to 400A.

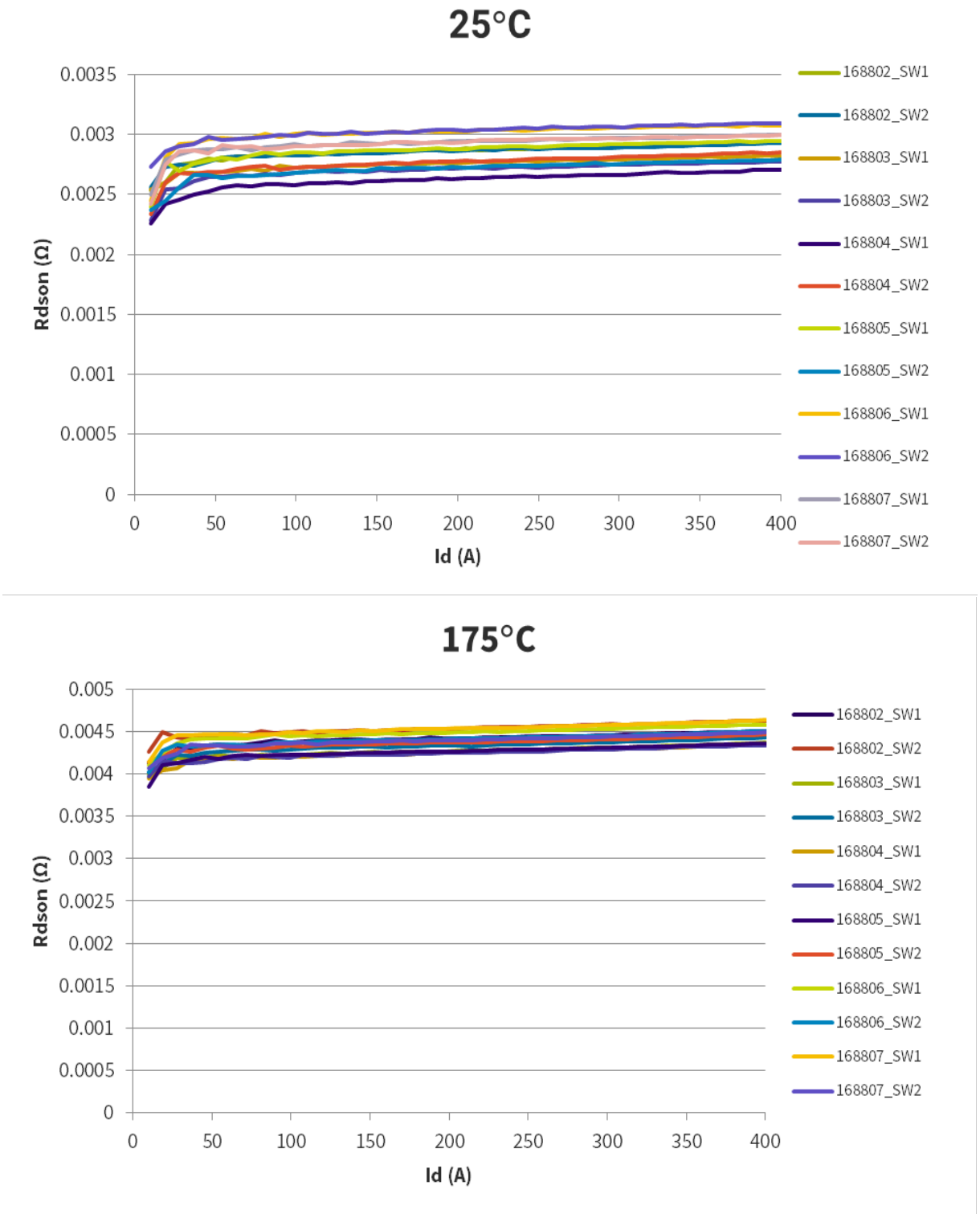

Figure 3-81: 900V, 2.5mΩ, half-bridge SiC power module on-state resistance as a function of drain-source current up to 400A; (top) 25˚C; (bottom) 175˚C.

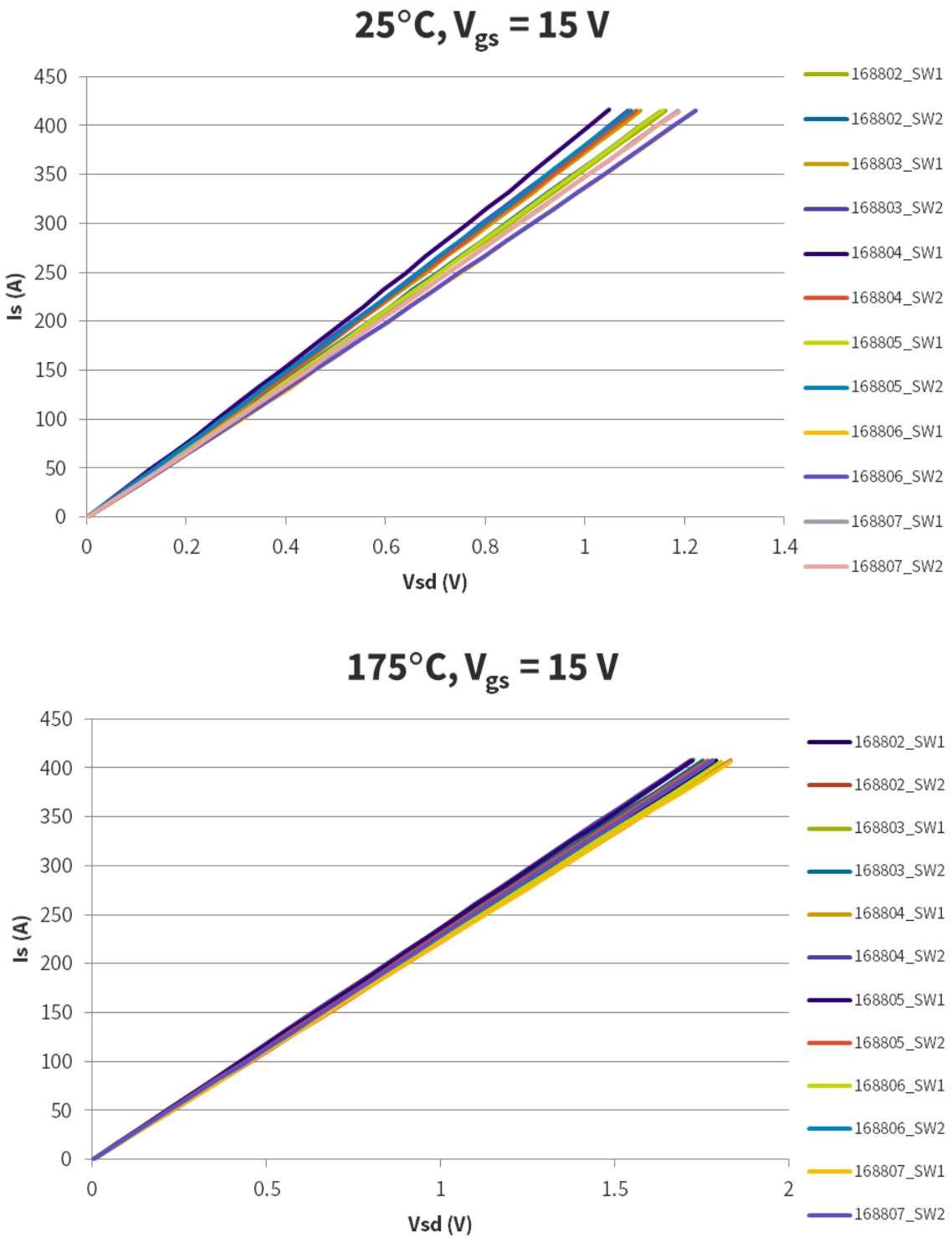

Figure 3-82. Qualification of the 900V, 10mΩ SiC MOSFET at die level has been undertaken at JEDEC level, with a maximum temperature of 175°C

The second year has been very successful in quantifying the value proposition and benchmarking the new record-low on-resistance (10mΩ) SiC MOSFET at 900V rating. Accomplishments include:

- Subcontractor Ford Motor Company found in EPA combined highway/metro driving, a 78% inverter loss reduction could be obtained using the 900V SiC MOSFET based power modules as opposed to 800V Si IGBT technology.

- Measured switching losses were 5-14X lower than Si IGBT power modules, which exceeded a milestone of 5X minimum switching loss reduction.
- Qualification of the 900V, 10mΩ SiC MOSFET at die level has been undertaken at JEDEC level, with a maximum junction temperature of 175°C. Over 2,000 die were assembled for these tests in TO247-4L packages. The die is approximately 20% larger than the largest commercial die in Cree's portfolio, and has passed all of the JEDEC tests for die qualification. Testing is continuing through contract end and afterward for larger sample sizes required for AEC-Q101.
- Over 1,000 die have been supplied for power module assembly. Instead of assembling 70 power modules with a 200A rating, approximately 40 power modules have been assembled with 360A current rating instead, which is equivalent to the total Amps required for assembly by the program milestone, and also is more congruent with market feedback for higher-amperage power modules.
- Measured results include 360A of current, 2.5mΩ on-resistance at room-temperature, and ~4.5mΩ of on resistance at 175˚C. In year two, the isolation of the power module was also increased from 1.2kV to 3.5kV based on feedback from Ford Motor and others.

A three phase inverter has been built using the 900V modules produced with these MOSFET chips and is being tested through the end of the program to contrast with other technologies to get full impact on cost and performance.

FY 2015-16 Presentations/Publications/Patents

1. V. Pala,et al, “900V Silicon Carbide MOSFETs for Breakthrough Power Supply Design,” in IEEE International Symposium on Power Semiconductor Devices and IC’s (ISPSD), 2015.
2. “Record-low 10mΩ SiC MOSFETs in TO-247, Rated at 900V,” in IEEE 2016 Applied Power Electronics Conference, 2016, pp. 979-982.
3. J. Casady, V. Pala, E. VanBrunt, B. Hull, S. Ryu, G. Wang, J. Richmond, S. Allen, D. Grider, J. Palmour, P. Killeen, B. McPherson, K. Olejniczak, B. Passmore, and D. Simco, “Ultra-low (1.25mΩ) On-Resistance 900V SiC 62mm Half-Bridge Power Modules Using New 10mΩ SiC MOSFETs,” in PCIM Europe 2016, 10-12 May 2016, pp. 34-41.
4. J. Mookken, “20KW Resonant Full Bridge LLC Converter using C3M MOSFETs for DC Fast Chargers,” Cree/Wolfspeed application note, http://www.paytongroup.com/webfiles/files/Wolfspeed%2020kW%20SiC%20EV%20charger%20solution%20dc-dc%20section%20Payton%20version%20.pdf, 2016.
5. M. Su and C. Chen, “Prospects for the Application of SiC Power Devices in Hybrid Electric Vehicle Drive Systems,” 4th IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 7-9 Nov 2016.
6. V. Iyer, et al, “A 6.6 kW bidirectional electric vehicle charger enabled by 900V SiC MOSFETs,” submitted to IEEE 2017 Applied Power Electronics Conference, 2017, under review.
7. J.B. Casady, B. Hull, J. Zhang, D. Gajewski, GangYao Wang, S. Allen, K. Olejniczak and J. Palmour, " First Automotive Reliability Assessment and Drive-train Performance of Large-area 900V, 10mOhm SiC MOSFETs," IEEE 2017 Applied Power Electronics Conference (APEC), Mar. 26-30, 2017.

References

1. Infineon 650V, 19mΩ MOSFET, part number IPZ65R019C7, http://www.infineon.com/dgdl/Infineon-IPZ65R019C7-DS-v02_00-en.pdf.
2. Infineon 650V 100 A IGBT, Part No. IGZ100N65H5, http://www.infineon.com/dgdl/Infineon-IGZ100N65H5-DS-v02_01-EN.pdf.

3.7 A Disruptive Approach to Electric Vehicle Power Electronics

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Contract No.: EE0006921

Objectives

This project includes development of two power electronics drivetrain demonstrations: a silicon 30 kW system, and a SiC 30 kW system. Both will meet aggressive efficiency and capacitor size targets, while the SiC demonstration will additionally meet power density targets and will provide an objective comparison of how SiC technology affects system optimization to improve cost and power density performance. Hence the objectives are: (a) Develop, design, and demonstrate a new EV power electronics architecture that reduces average loss over the US06 drive cycle by a factor of 2-4 and film capacitor size by a factor of two, using Si devices, and (b) Develop, design, and demonstrate a SiC version meeting the above goals, that further improves efficiency and cost, and that meets DOE power density goals.

Technical Barriers

- In electric vehicle drivetrains containing boost dc-dc converters, such as those employed by Ford [1], Toyota [2-4], Honda [5], and others, the efficiency of the boost dc-dc converter dominates the power electronics system efficiency, and exhibits poor efficiency at partial power. This leads to a substantial additional average power loss over standard drive cycles, with typical power converter system average efficiencies of 92.5% for US06 and 90.4% for UDDS. Reduction of the average loss could lead to reduction of the cooling system size and cost.
- The film capacitors of these systems are bulky and expensive, with a specific energy of 9 J/kW in recent commercial designs. Capacitor size is generally constrained by rms current and applied voltage [5]; hence, increase of switching frequency does not reduce capacitor size and other approaches must be found for reduction of capacitor size and cost.

Technical Targets

APEEM 2020 Goal	Goals of this Project
Traction drive system (power electronics plus machines): Efficiency > 94%	Power electronics US06 average efficiency improved from 92.5% to 97.5%: 30 kW drivetrain demonstration
Power electronics density > 13.4 kW/L	SiC high density demonstration: > 13.4 kW/L
Power electronics specific weight > 14.1 kW/kg	SiC high density demonstration: > 14.1 kW/kg
Power electronics cost < $3.3/kW	Reduced film capacitor requirements: capacitor specific energy reduced from 9J/kW to < 5J/kW Reduced cooling system requirements: *Pout*/*Ploss* improved from 10 to over 40

DOE PHEV Charger 2022 Targets	Goals of this Project
On-board charger meeting 3.3 kW, 3.5 kg, 0.943 kW/kg	Integrated Level 2 charger: Added mass 1.6 kg, add-on specific weight 4 kW/kg

Accomplishments

- Composite boost dc-dc converter system design, for non-incremental improvement of boost plus inverter drivetrain architecture
  - Demonstration of Si MOSFET prototype at 30 kW
    - Measured boost efficiency of 98% at 250 V : 650 V over 30:1 range of powers
    - Computed reductions in loss by 2x to 4x over EPA drive cycles
    - Commensurate improvements in cost and size of cooling system, MPGe, and cost
    - Reduction of film capacitor requirements by 2x through fundamental improvements in converter topology.
  - Demonstration of 30 kW boost employing SiC 900 V MOSFETs
    - High density boost system (240 kHz, 23 kW/L) has been fabricated and is under test
    - Similar efficiency
    - Laboratory demonstration of planar ferrite magnetics at 240 kHz.
- 800 V SiC inverter prototype
  - Improved CAFE average efficiency from 95.6% to 98.4% (2.5x reduction in average loss)
  - Fabricated inverter prototype and controller have been fabricated and are under test
  - Demonstrated experimental operation over US 06 drive cycle at partial power.
- Control of composite converter system
  - Development of detailed Simulink models
  - Development of control algorithms
    - Demonstrated fast response and seamless transitions between modes
    - Extension to negative-incremental resistance loads is underway
  - Experimental demonstration of control of composite boost system at full power and voltage is complete for resistive load
- Add-on integrated Stage 2 charger
  - Re-use of composite converter modules for charging configuration
    - Existing DCX module provides isolation, and existing buck module controls battery current
    - Additional bridgeless boost module required for ac line current shaping
    - Projected added weight for SiC charger modules: 4 kW/kg for 6.6 kW on-board charger, exceeds PHEV 2022 target power density by factor of four
    - Prototype SiC 6.6 kW power stage and microcontroller PCBs are under test

Introduction

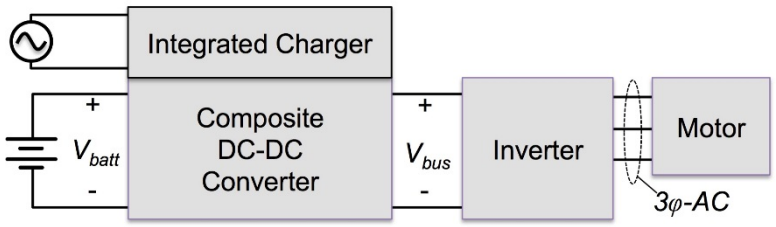

Figure 3-82: Composite converter powertrain approach with integrated charger

A high-level block diagram of the power electronics system is illustrated in Figure 3-82. The system includes a voltage boost function, as is found in some hybrid vehicles such as the Toyota Prius or Ford Focus. The boost function is performed by the new Composite DC-DC converter approach, in which several partial-power converter modules are combined to perform the boost function with higher performance. An intermediate dc bus with voltage *Vbus* supplies a boosted voltage of up to 800 V peak to an inverter. The inverter is a conventional three-phase bridge that drives a high-speed permanent-magnet ac machine. An integrated charger reuses some of the composite converter modules to achieve level 2 charging in an on-board charger having substantially lower weight than that of a discrete charger.

The conventional approach to realizing the DC-DC boost function is illustrated in Figure 3-83. Multiple 1200 V silicon IGBT dice are connected in parallel in a multichip power semiconductor module. A typical switching frequency is 10 kHz, which then determines the inductor size and loss. The efficiency of the DC-DC boost converter dominates the system efficiency; the dominant loss mechanisms are inductor ac and dc losses, and IGBT switching losses. When boosting by a high voltage ratio, the boost converter must operate with a high duty cycle where the efficiency is relatively low. The partial-power efficiency is also poor, because of ac losses (switching loss and ac magnetics loss) that depend on voltage but are nearly independent of current. At high duty cycles, the rms current applied to the bus capacitor is also quite high; this impacts the size and cost of this capacitor.

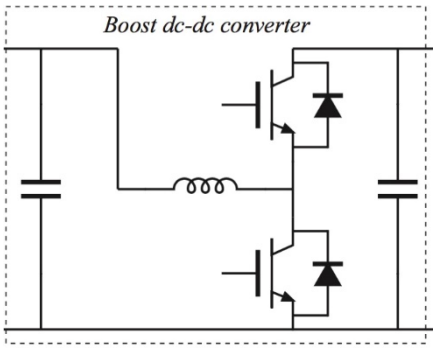

Figure 3-83: Conventional boost converter power stage

Approach

We have proposed the new composite boost converter architecture illustrated in Figure 3-84. With this approach, we employ the same semiconductor area as the conventional boost converter. However, instead of the brute-force parallel connection of semiconductor die, we connect the devices in a better way that allows better optimization and reduced requirements for the reactive elements. The particular configuration of Figure 3-84 employs three partial-power dc-dc converter modules in an architecture that is optimized to minimize loss for standard drive cycles. Efficiency is improved by reduction of switching loss and magnetics ac loss, through use of passthrough modes and reduced module voltages. RMS capacitor currents are minimized because the duty cycles of the DC-DC boost and buck modules are restricted to ranges where these currents are inherently low. Thus, the composite converter approach leads to fundamental improvements in performance arising from a new superior converter architecture.

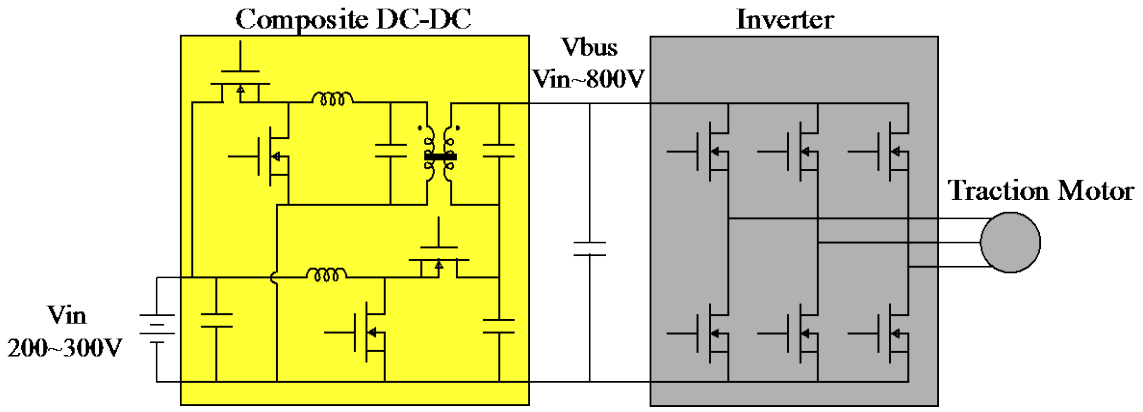

Figure 3-84: Power electronics architecture for this project, including a DC-DC composite boost converter and an inverter.

Figure 3-85 illustrates the computed and measured improvements in efficiency for the proposed composite converter architecture, relative to the conventional boost topology. Efficiency curves are plotted for a battery voltage of 250 V, and DC bus voltage of 650 V, and a rated power of 30 kW. This result was obtained using a detailed loss model that includes semiconductor switching and conduction loss, as well as magnetics dc and ac losses (dc and ac copper losses, core losses, and copper loss induced by fringing flux). This figure includes measured laboratory data from our 30 kW Si composite boost converter experiment.

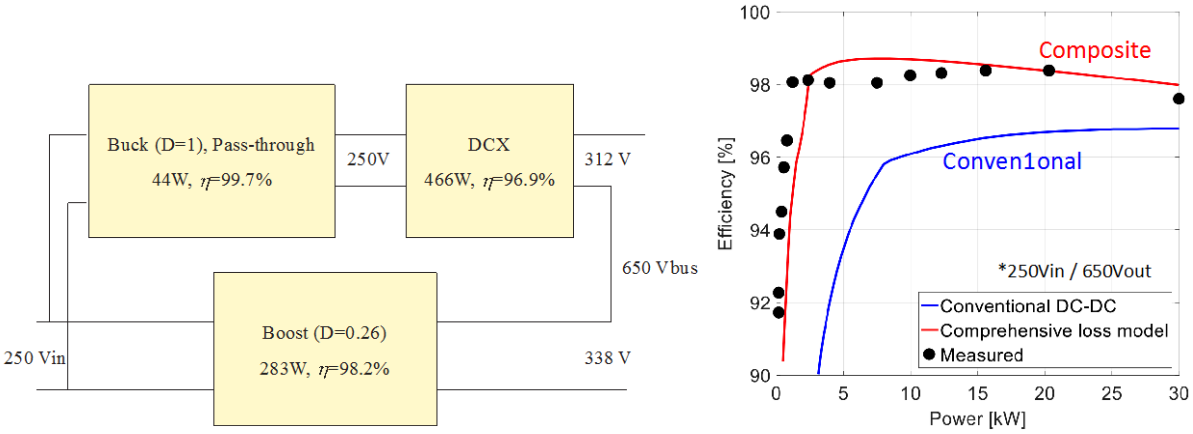

Figure 3-85: Achieving high efficiency at high boost ratio in the composite architecture. Left: module operating points and losses at 250V : 650V, 30 kW. Right: comparison of efficiency curves of conventional boost converter with composite design, at 250V : 650V.

Results and Discussion

Vehicle and Power Electronics System Modeling

A vehicle system model was developed and was employed to identify the key loss mechanisms of the electric vehicle powertrain system. This model was based on the Chevy Volt 2015, and scaled to 30 kW maximum power. The motor is modeled based on the Toyota Prius 2010, and scaled to the 30 kW power level as well. A detailed converter loss model has also been developed, based on data from pilot-scale prototypes in our laboratory for systems containing a boost dc-dc function. The vehicle model has been simulated using these standard driving profiles US06 and UDDS, and the required power and bus voltage profiles were calculated. Based on this data, the US06 average driving efficiency can be calculated. Extensive loss modeling and system optimizations were performed [5,6], to minimize average US06 drive cycle loss. Figure 3-86 contains plots of the converter loss components and operating points for the US06 driving test, for the optimized design.

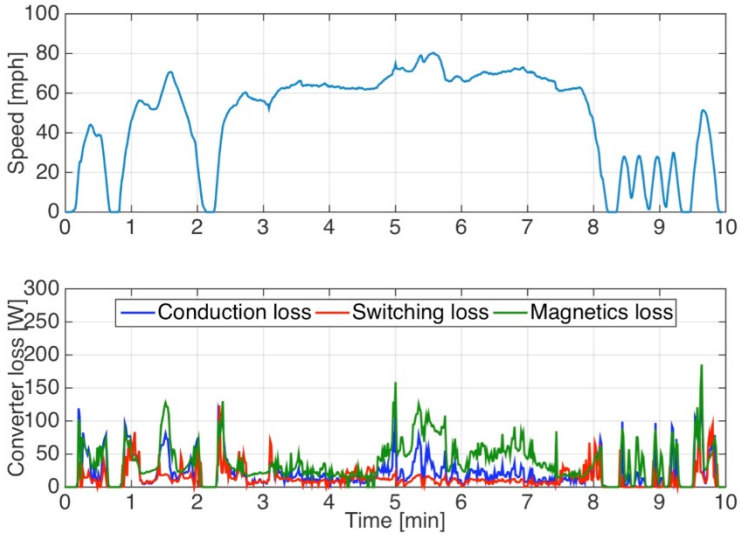

Figure 3-86: Modeled loss mechanisms over the US06 drive cycle for the Si composite boost converter. Top: US06 speed profile. Bottom: total semiconductor conduction loss, switching loss, and dc+ac magnetics losses.

Based on the detailed loss models, multiple composite system architectures were modeled, and a candidate approach was found to be suitable for our project goals. A composite boost converter architecture (Figure 3-84) was selected, consisting of 650 V Si MOSFET DC-DC converter modules and a 1200 V SiC MOSFET inverter. Additionally, a similar system employing 900 V SiC MOSFETs in the DC-DC converter modules has been selected. The projected average US06 efficiencies for these approaches, as well as for a conventional commercial architecture, is summarized in Table 3-8. The proposed composite architecture can meet the goal of > 97.5% US06 average efficiency. Relative to the existing conventional approach employed in commercial products, the composte architecture achieves a reduction in US06 average loss of a factor of approximately four. Similar gains are projected for the all SiC version; use of SiC MOSFETs allows an increase in switching frequency of almost one order of magnitude, with corresponding gains in magnetics size.

Table 3-8: Comparison of Projected 30 kW US06 Performance

	Conventional	Composite
DC-DC Converter	Si IGBT 1200 V 94.9%	Si MOSFET 650 V 98.8%
Inverter	Si IGBT 1200 V 97.4%	SiC MOSFET 1200 V 99.2%
System Average Efficiency, US06	92.5%	98.0%
Q = Pout/Ploss	12.3	49.0

We have run similar simulations and calculations for both Si and SiC designs, calibrated using experimental test data, with US06, UDDS, and HWFET driving profiles. For the UDDS profile, the conventional boost converter is predicted to exhibit an average efficiency of 90.4% with Q = 9.4, as compared to 98.1% efficiency and Q = 51.6 for the composite approach. Again, the major improvements in *Q = Pout/Ploss* suggest substantial potential improvements in cost, power density, MPGe, and cooling system requirements via the composite converter approach.

Silicon Prototype Construction

A silicon-based prototype composite boost converter system has been designed, assembled, and tested. The module designs, DCX turns ratio, and magnetics designs each were optimized at the operating points where impact on the US06 average efficiency is greatest. This 30 kW system employs 650 V Si superjunction MOSFETs. A photograph of the laboratory prototype is illustrated in Figure 3-87. This top view shows the gate driver PCB (blue solder mask) attached to the top side of the power interconnect PCB (having a green solder mask). The power MOSFETs are attached underneath the PCB, and the heat exchanger with water

cooling is also underneath the PCB. The gate driver PCB is a four layer board with 2 oz copper that can accommodate SOIC pin spacings. The power interconnect PCB is a two-layer board with 9 oz copper that can conduct the required currents. A laser-cut spacer having cutouts for the needed interconnects is placed between the driver and power PCBs, to provide isolation between PCBs. This approach leads to low-inductance interconnects between the power semiconductors, film capacitors, and gate drivers, with minimal ringing and overshoot of switch node and bus voltage waveforms. This silicon system is intended as an electrical testbed and is not packaged for high power density.

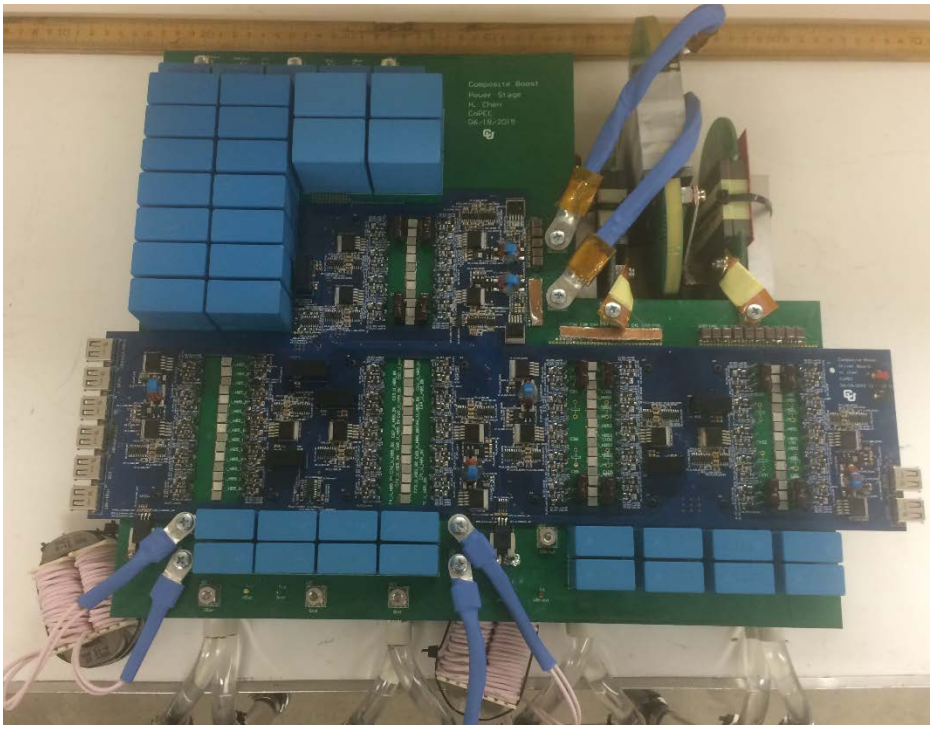

Figure 3-87: Photograph of assembled silicon prototype.

The ferrite planar magnetics of the 33 kHz DCX module can be seen in the upper right corner of the prototype. The filter inductors for the 20 kHz buck and boost modules employ metglass cores, and are visible on the lower side of the photograph. The film capacitors for the various modules are the blue rectangular elements.

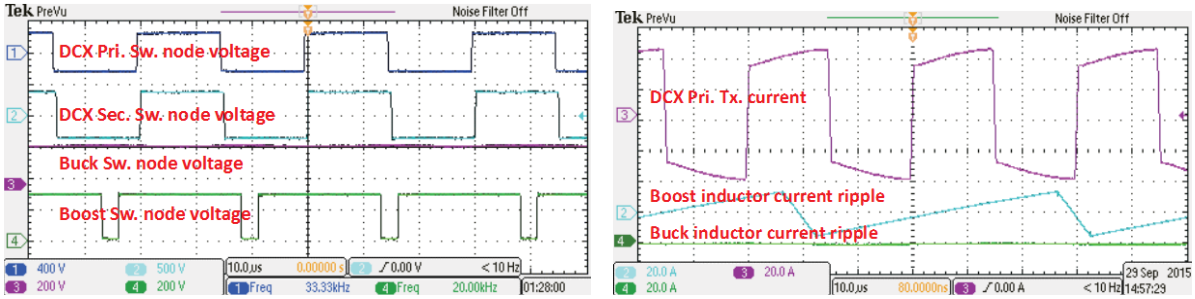

Figure 3-88: Prototype measured waveforms, operating at 250 V battery voltage, 650 V dc bus voltage, and 50% of rated power (15 kW). Left oscilloscope figure waveforms, from top to bottom: DCX primary switch node voltage, DCX secondary switch node voltage, buck module switch node voltage, boost module switch node voltage. Right oscilloscope figure waveforms, from top to bottom: DCX primary transformer current, boost inductor current, buck inductor current. At this operating point, the buck module operates in passthrough mode.

The 30 kW Si composite boost converter has now been tested and debugged at all operating points with output dc bus voltages over the range 250 V to 800 V and with power over the range 0 to 30 kW. Sample operating waveforms are documented in Figure 3-88. Based on experimental data, a loss model has been developed and calibrated. Figure 3-89 shows efficiency contours of the composite boost converter operating with an input battery voltage of 250 V, for various output bus voltages and powers. The superimposed blue lines are trajectories of power and bus voltage for the US06 drive cycle, in which the dc bus voltage is proportional to

vehicle speed, and the power is based on a vehicle model scaled to a maximum 30 kW. The composite converter system achieves 98.6% peak efficiency at 15 kW and 650 V, and maintains high efficiency over a remarkably wide range of operating points. Based on this data, the average composite boost efficiency is computed to be 98.4% over the US06 drive cycle.

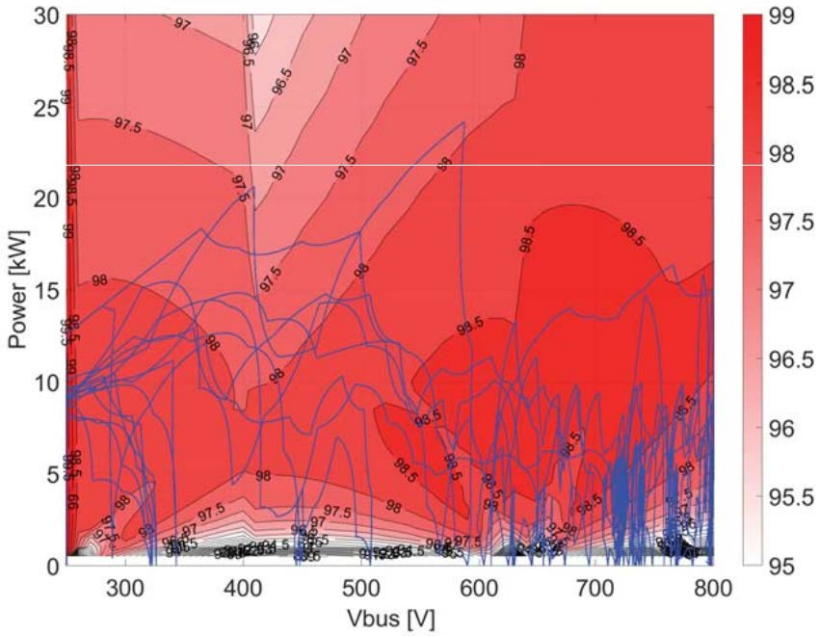

Figure 3-89: Efficiency contours of the Si composite boost converter system, with superimposed US06 operating points.

Table 3-9 compares the average efficiencies of the conventional and composite boost approaches for the US06, UDDS, and HWFET drive cycles. The CAFE weighted efficiency (55% UDDS plus 45% HWFET) is also compared. It can be seen that the composite approach leads to substantially higher efficiency in all cases; for example, the improvement in CAFE efficiency represents a reduction in average loss by a factor of approximately four.

Table 3-9: Comparison of Average Efficiencies over EPA Drive Cycles

Driving Cycle	Conventional Boost Converter	Composite Boost Approach
US06	93.3%	98.4%
UDDS	97.1%	99.0%
HWFET	91.8%	98.1%
CAFE	94.7%	98.6%

Table 3-10 contains a summary of the Si composite boost design. This system includes three partial-power converter modules, each incorporating superjunction Si MOSFETs.

Table 3-10: Summary of Si Composite Boost Design

	Boost module	Buck module	DCX module
Number of Si MOSFET die	10	10	28
MOSFET part	IPW65R041CFD2	IPW65R041CFD2	IPW65R041CFD2
Switching frequency	20 kHz	20 kHz	33 kHz
Magnetics	60 µH inductor	48 µH inductor	8:12 planar transformer 4.5 µH planar tank inductor
Core material	Amorphous alloy	Amorphous alloy	Ferrite

SiC Composite Boost High-Density Demonstration

A SiC version of the composite boost system has been developed, assembled, and is under test. This system will be completed by the conclusion of the project. Details of the design are given in [3,6,9]; selected key results are highlighted here.

H-bridge modules containing 900 V 10 mΩ SiC MOSFETs with antiparallel 1200 V SiC schottky diodes were developed and delivered by subcontractor APEI/Wolfspeed. These devices have now been assembled into a high-density composite boost prototype system rated 30 kW average, 39 kW peak. The volume of the packaged system is 1.6 Liters and its weight is 2.5 kg. Hence the power density is 21 kW/L. Figure 3-90 contains CAD drawings illustrating the mechanical design, and photographs of the laboratory prototype are included in Figure 3-91.

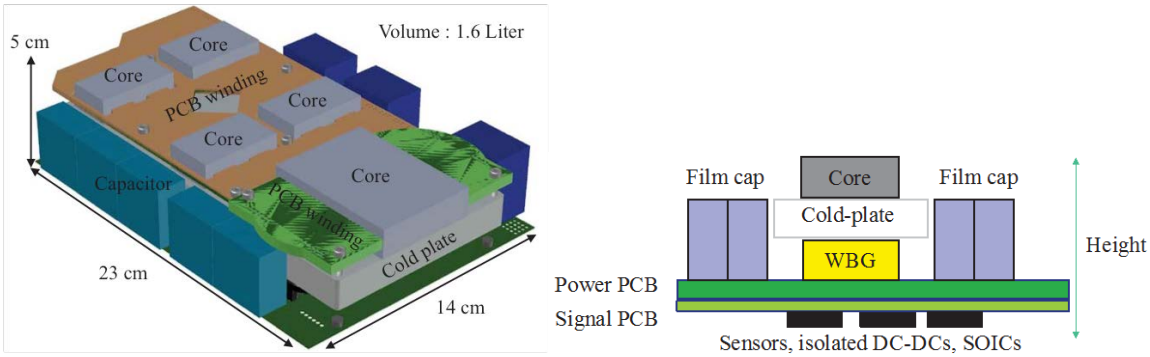

Figure 3-90: High-density composite boost mechanical design. Left: CAD drawing of assembled unit. Right: Side view of mechanical layout. An off-the-shelf cold plate provides water cooling, with ferrite cores mounted on top side and wide bandgap semiconductors mounted on bottom side. A PCB with high-weight copper provides power interconnects, and a PCB with conventional copper provides gate driver and signal interconnects.

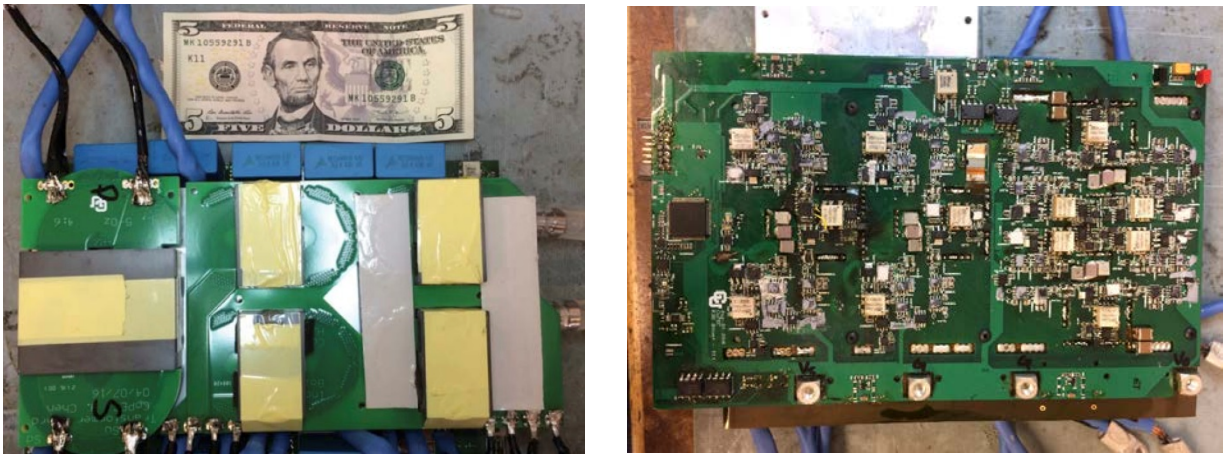

Figure 3-91: Assembled high-density composite boost converter laboratory prototype. Left: top side, with planar magnetics visible. Right: bottom side, with signal PCB visible.

Figure 3-92 illustrates the predicted loss curves for the SiC composite boost converter design, with a nominal battery voltage of 250 V and with junction temperatures of 100˚C. The superimposed red dots are sampled operating points over the US06 drive cycle. The highest density of operating points occurs in the vicinity of 650 V and 5 kW; high efficiency of approximately 98.5% occurs for most of these points.

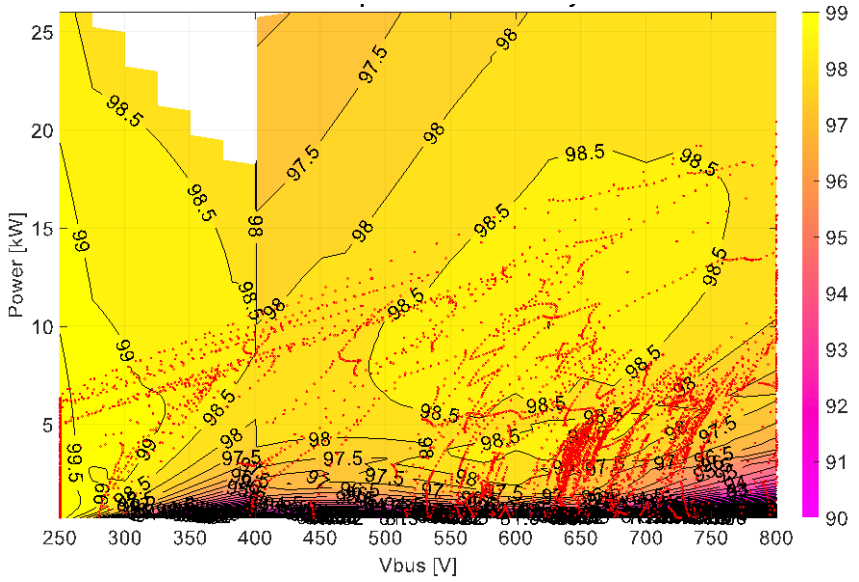

Figure 3-92: Predicted efficiency contours of the SiC composite dc-dc converter system at Vbatt = 250 V and with 100˚C junction temperature. The red dots represent superimposed operating points during the US06 drive cycle.

Table 3-11 compares the projected performances of boost converter technologies. The silicon composite boost approach reduces the US06 average loss by a factor of 3.2 relative to the conventional Si boost approach, with film capacitor size reduced by a factor of over 2. Relative to the conventional Si boost approach, the SiC composite boost reduces the US06 average loss by a factor of 4, again with the film capacitor size reduced by a factor of over 2. The SiC composite boost also reduces magnetics volume by a factor of approximately 10, commensurate with its increased switching frequency.

Table 3-11: Projected Performances of Boost Technologies

	Conventional Si Boost	Composite Si Boost	Composite SiC Boost
Switching frequency	10 kHz	20 kHz	240 kHz
Efficiency at 50% of rated power at 250V : 650 V	96.4%	98.6%	98.8%
US06 average system efficiency	92.5%	97.5%	98.0%
Pout/Ploss	12.3	39	49
Power density of magnetics: core volume [L/kW]	12.7 mL/kW	10 mL/kW	1.2 mL/kW
Capacitor specific energy [J/kW]	9 J/kW	4 J/kW	4 J/kW

Ferrite Planar Magnetics

We have demonstrated ferrite planar magnetics designs for the SiC composite boost converter design, optimized to minimize loss over the US06 drive cycle, with the buck and boost modules switching at 240 kHz and the DCX module switching at 480 kHz. Core loss was estimated using the iGSE method, and was experimentally verified in the laboratory prototypes. AC winding losses were computed using Dowell's equations, with additional verification using finite element analysis and laboratory measurements.

Table 3-12 summarizes the improvement gained by increase of switching frequency from 20 kHz (Si MOSFET prototype, AMCC50 Metglass core) to 240 kHz (SiC MOSFET prototype, Ferrite N87 core) for the example of a boost module operating at Vin = 250 V, Vout = 275 V, P = 7 kW. The total loss of 13 W can be maintained while the core volume is decreased from 82.2 cm3 to 11.5 cm3.

Table 3-12: Reduction in Magnetics Volume of SiC Composite Boost Converter

	Switching Frequency 20 kHz		Switching Frequency 240 kHz	
Core material	Metglass	Ferrite N87	Metglass	Ferrite N87
Core size	AMCC50	PM114/93	AMCC4	EILP43
Core volume [cm3]	82.2	344	13.4	11.5
Core loss [W]	5	3	46	3
Winding loss [W]	8	5	11	10

A weighted loss optimization was performed, to minimize average loss over the US06 drive cycle including multiple options in ferrite core size, switching frequency, PCB copper weight and turns, and interleaving options. The results are summarized in Table 3-13.

Table 3-13: Summary of Optimized SiC Composite Boost Design

	Buck (interleaved)	Boost (interleaved)	DCX
Switching frequency	220 kHz	220 kHz	440 kHz
Ferrite core	ELP 43 (2 total), N49	ELP 43 (2 total), N49	ELP 64, N49
Inductance	5.2 µH	3.4 µH	-
Turns	6, 5 oz Cu	4, 5 oz Cu	4:6, 5 oz Cu
Film capacitors	450 V, 6.8 µF (2 total)	450 V, 6.8 µF (2 total)	450 V, 5 µF (2 total) 630 V, 3.3 µF (3 total)

Figure 3-93 illustrates finite element modeling of the final 440 kHz DCX planar transformer design. This transformer employs a single EILP 64 planar ferrite core using Epcos N49 material. The PCB contains eight layers of 5 oz copper, and the turns ratio is 4:6. Similar optimization and modeling has been carried out for the inductors of the boost and buck modules; results for the planar boost inductor are illustrated in Figure 3-94.

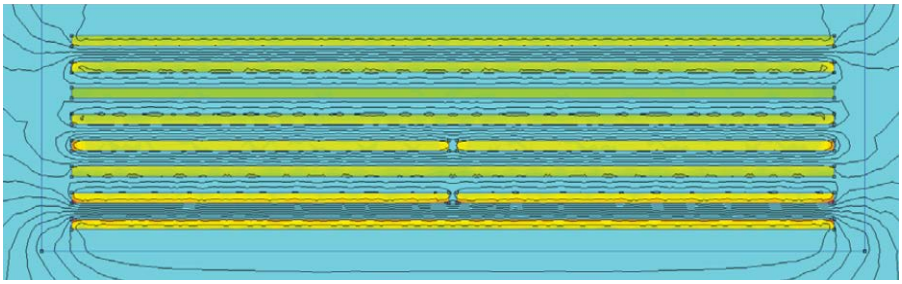

Figure 3-93: Two-dimensional finite element modeling of the DCX planar transformer. The eight-layer PCB employs primary and secondary windings interleaved as follows: -1/1/-1/1/-2/1/-2/1. Negative numbers denote secondary layers.

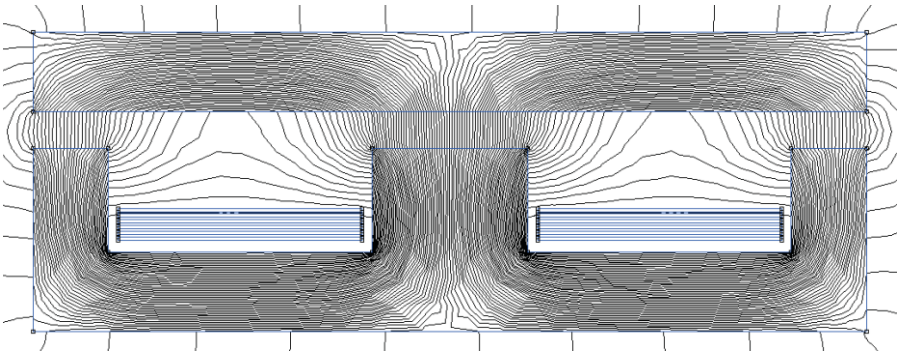

Figure 3-94: Two-dimensional finite element modeling of the boost module planar inductor. The six-layer PCB employs six turns, with one turn per layer and 5 oz copper.

Improvement of Inverter Efficiency Achievable with SiC MOSFETs

We have employed our calibrated converter loss models to assess the potential impact of SiC MOSFETs on inverter average efficiency over standard drive cycles. Details of the inverter models, experimental validation, and calcuations are given in [6,7]. Figure 3-95 illustrates the efficiency contours of an 80 kW inverter employing 600 V IGBTs (Infineon IKW75N60T die) with a 350 V battery and with vehicle parameters based on the Nissan Leaf. Operating points of the UDDS, HWFET, and US06 drive cycles are superimposed.

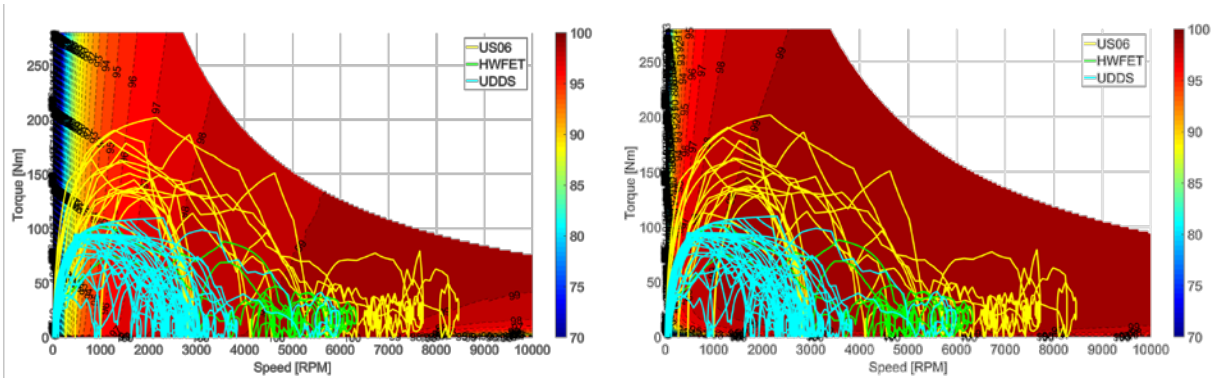

Figure 3-95: Inverter efficiency contours, with superimposed EPA drive cycle operating points. Left: 600 V Si IGBT inverter. Right: 1200 V SiC MOSFET inverter.

Based on this data, the performance of Si and SiC inverters can be compared for standard EPA drive cycles. Table 3-14 summarizes the impact of increasing DC input voltage and of switching from Si IGBT devices to SiC MOSFET devices. The listed drive cycle efficiencies are averaged over the complete drive cycles. The

CAFE efficiencies are weighted averages of UDDS and HWFET efficiencies. The *Q* factors are the ratio of total throughput energy to total loss energy. It can be observed that increase of operating voltage can impact the average efficiency, even when Si IGBTs are employed. A more substantial increase is achieved through use of SiC MOSFETs, with an increase of *Q* by a factor of four.

Table 3-14: Comparison of Si and SiC Inverter Performance

	600 V Si IGBT	1200 V Si IGBT	1200 V SiC MOSFET
Switching frequency	5 kHz	5 kHz	5 kHz
DC input voltage	350 V	800 V	800 V
US06 avg efficiency	98.6%	98.9%	99.7%
CAFE avg efficiency	98.2%	98.7%	99.5%
CAFE *Q*	54.8	73.7	215.7
Peak loss	2.2 kW	1.5 kW	0.8 kW

Control of Composite Boost System

Our control system work for this project has two goals: (1) in view of the required mode switching, demonstrate how the composite converter system can be effectively controlled; (2) implement control as needed to demonstrate average efficiency claims for the US06 and other drive cycles.

Digital control of the composite boost converter has now been experimentally demonstrated, using a TMS3200 microcontroller. Figure 3-96 illustrates closed-loop control, in which the bus reference is adjusted in steps from 340 V to 770 V and back to 340 V, for a constant battery voltage of 270 V. It can be seen that the bus voltage steps as commanded, without significant overshoot or ringing and with a fast response. Individual module gate drive signals are also shown.

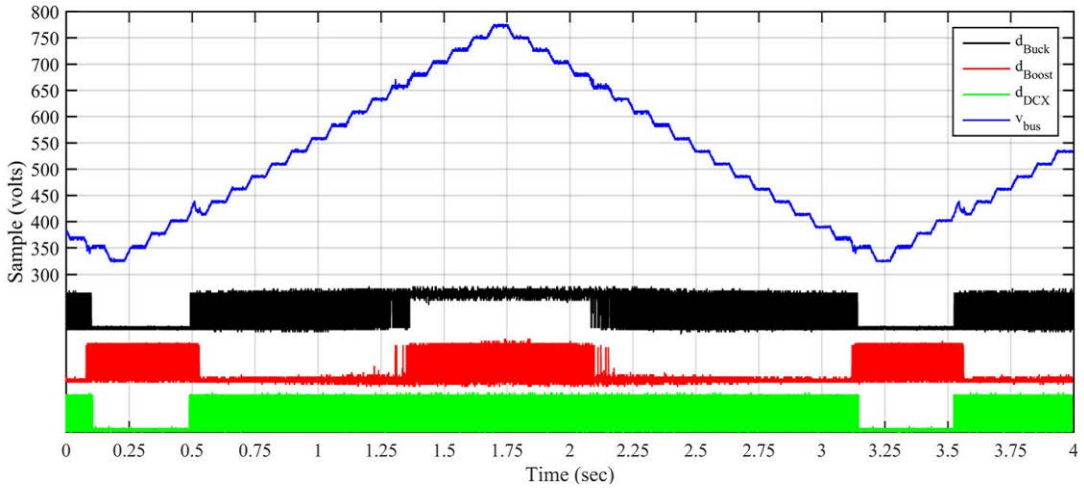

Figure 3-96: Simulink model of controller algorithms for composite boost system with 250 V battery input. The commanded bus voltage is stepped from 300 V to 800 V and back. The system automatically switches modes as necessary, and the transient response is well behaved.

There is near-seamless transition between modes. For 0.1 s < *t* < 0.5 s, the system operates in boost only mode, with the DCX and buck modules shut down. For 0.55 s < *t* < 1.3 s, the system operates in DCX + buck mode, with the boost converter operating in passthrough mode. For 1.3 s < *t* < 2.1 s, the system operates in DCX + boost mode, with the buck converter operating in passthrough mode. No converter terminal voltage ever exceeds 415 V, and hence all 650 V Si MOSFETs are operated at no more than 67% of their rated voltage. The mode transitions employ a new DZAM control techniques that maintains a monotonic control characteristic across the boundaries without increasing switching loss.

Integrated Charger Prototype

The modular nature of the composite boost converter approach admits reuse of modules for battery charging while the vehicle is stationary. In this project, an onboard integrated charger is being developed that uses the buck and DCX modules of the composite boost system during charging operations. An additional bridgeless boost converter module is added, which performs ac line current waveshaping. Figure 3-97 illustrates how this additional circuitry integrates into the boost composite system. In this project, level 2 charging at 6.6 kW is achieved while minimizing the added weight and volume; higher power would be achievable if desired.

A 6.6 kW SiC bridgeless boost module has now been designed, constructed, and tested, along with the necessary sensor and control circuitry. Figure 3-98 illustrates measured waveforms of this module operating at 5 kW. This module employs the same 900 V SiC MOSFET modules that are used in the SiC composite boost prototype; this design switches at 120 kHz and employs ferrite planar magnetics. The efficiency at 6.6 kW is approximately 96%. Potentially this approach could process reactive power, and could allow V2G and G2V operation, although that functionality has not been incorporated into the current controller prototype. Details regarding control of this module are documented in [8].

With this design, the added mass required to achieve this functionality is 1.9 kg, leading to an add-on specific weight of 3.5 kW/kg. This substantially exceeds the DOE PHEV charger 2022 target of approximately 1 kW/kg.

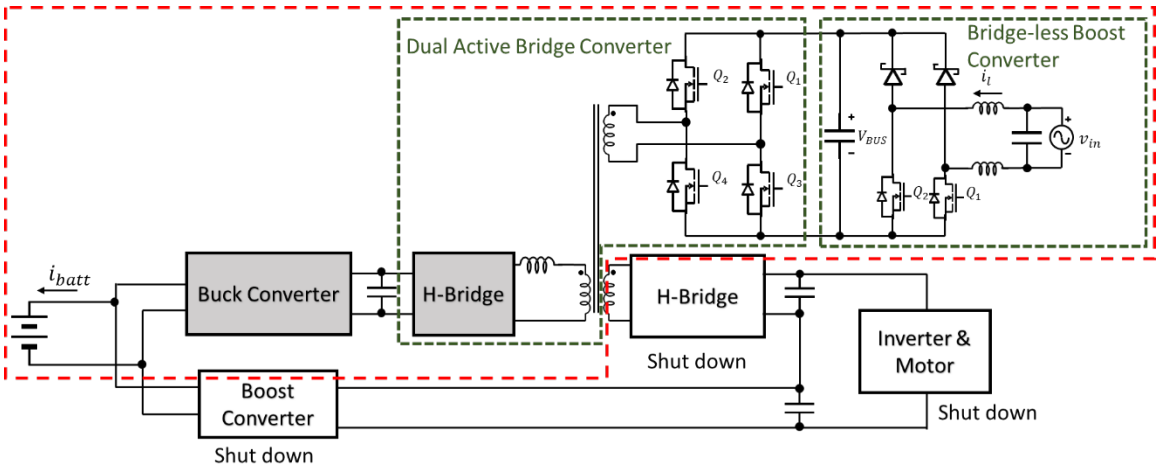

Figure 3-97: Integrating an on-board charger into the composite boost architecture. Add additional output is added to the DCX (DAB) and a bridgeless boost converter is added for power factor correction.

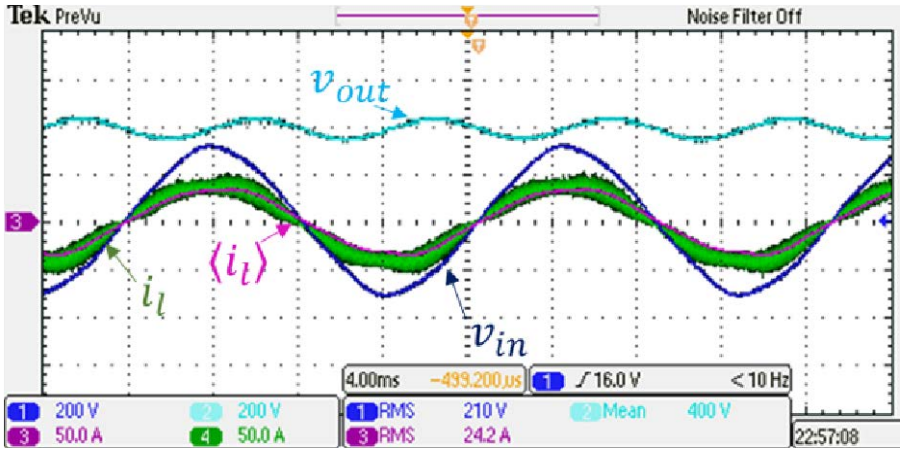

Figure 3-98: Measured waveforms of power factor correction module (bridgeless boost) prototype: ac line voltage (purple), inductor current (green), and dc output voltage (blue), operating at 210 Vrms input, 400 Vdc output, and 5 kW power.

Conclusions and Future Directions

The power electronics of electric vehicles are loss-limited. Hence, the ratio of output power to loss power is the key metric governing power density, cost of cooling system, and the impact of the power electronics on MPGe. It is shown here that it is possible to reduce $Q = Pout/Ploss$ by a factor of four or more through use of a new composite converter approach. Further, average loss over typical drive cycles is substantially impacted by the low-power efficiencies of the power electronics. Improvement of the low-power and high boost-ratio efficiencies can significantly impact the net power loss.

Total film capacitor size and cost significantly impacts the system power density and cost, and is driven by the rms currents imposed on the capacitors by the power converters. Merely increasing the switching frequency does not affect the magnitude of the rms capacitor currents. The composite converter approach leads to significant reductions in capacitor currents, through fundamental improvements in conversion mechanisms. We have demonstrated that the capacitor size can be reduced by a factor of approximately two.

Use of SiC 900 V MOSFETs can lead to an order of magnitude increase in switching frequency with a reduction in magnetics size and cost. We have constructed a high density prototype based on these devices; this prototype is currently under test. This prototype will demonstrate a power density of 21 kW/L in a composite boost converter system, and incorporates high-density planar magnetics.

The composite converter approach employs approximately the same amount of semiconductor area, but with somewhat more complex interconnections. There is significant ongoing research in power electronics packaging and interconnects; it is expected that this research could enable the practical deployment of more complex converter structures. Indeed, the substantial performance gains demonstrated by this work can justify further packaging and interconnect research.

The use of SiC MOSFETs in the inverter stage can also reduce the inverter loss over standard drive cycles by a factor of 2-4, because of the substantial improvement in light-load efficiency. An inverter driven by an 800 VDC bus has been designed and fabricated using 1200 V SiC MOSFET modules and is currently under test.

Extensive design, firmware development, and testing of the digital control system has been undertaken. Control of the Si composite boost system has been experimentally demonstrated with a resistive load, including extensive testing. Modeling and design of the control system for constant power loads (closed-loop inverter) and for reversal of power flow (regenerative braking) has also been performed and is under test.

The modular nature of the composite converter approach also affords new opportunities for onboard charger integration. We have demonstrated an onboard level 2 charger system that repurposes composite converter modules to perform the charging functions of isolation and regulation of battery current. This reduces the add-on module requirement to a PFC rectifier stage plus a tertiary DCX winding and circuit. A 120 kHz 6.6 kW PFC module has been realized using 900 V SiC MOSFETs, achieving add-on gravimetric power density of over 4 kW/kg. This approach is suitable for on-board chargers with ratings of up to approximately half of the power rating of the composite boost converter, with V2G and G2V capability.

FY 2016 Presentations/Publications/Patents

1. H. Chen, K. Sabi, H. Kim, T. Harada, R. Erickson, and D. Maksimovic, “A 98.7% Efficient Composite Converter Architecture with Application-Tailored Efficiency Characteristic,” *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 101-110, Jan. 2016.
2. H. Chen, H. Kim, R. Erickson and D. Maksimovic, “Electrified Automotive Powertrain Architecture Using Composite DC-DC Converters,” *IEEE Transactions on Power Electronics*: accepted, to appear.
3. Hua Chen, “Advanced Electrified Automotive Powertrain with Composite DC-DC Converter,” Ph.D. thesis, University of Colorado, April 2016.
4. U. Anwar, H. Jin, H. Chen, R. Erickson, D. Maksimovic, and K. Afridi, “High Power Density Drivetrain-Integrated Electric Vehicle Charger,” *IEEE Energy Conversion Congress and Exposition*, Sept. 2016.
5. H. Kim, H. Chen, D. Maksimovic, and R. Erickson, “Composite Converter Design Based on Drive Cycle Weighted Losses in Electric Vehcile Powertrain Applications,” *IEEE Energy Conversion Congress and Exposition*, Sept. 2016.
6. Hyeokjin Kim, “98% CAFE EV power conversion system design,” Ph.D. thesis, University of Colorado, November 2016.

7. H. Kim, H. Chen, J. Zhu, D. Maksimovic, and R. Erickson, "98.4% CAFE Efficiency SiC-MOSFET EV Traction Inverter," *IEEE Workshop on Wide Bandgap Power Devices and Applications*, Nov. 2016.
8. U. Anwar, R. Erickson, D. Maksimovic, and K. Afridi, "A Control Architecture for Low Current Distortion in Bridgeless Boost Power Factor Correction Rectifiers," *IEEE Applied Power Electronics Conference*: accepted, to appear Feb. 2017.
9. H. Kim, H. Chen, D. Maksimovic, R. Erickson, Z. Cole, B. Passmore, and K. Oejniczak, "SiC MOSFET Composite Boost Converter with 22 kW/L Power Density for Electric Vehicle Application," *IEEE Applied Power Electronics Conference*: accepted, to appear Feb. 2017.

4 Benchmarking, Testing, and Analysis

4.1 Benchmarking Electric Vehicles and Hybrid Electric Vehicles

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Contract No.: DE-AC05-00OR22725

Abstract/Executive Summary

This benchmarking project provides vital information about the status and developmental trends of electric vehicle/hybrid electric vehicle (EV/HEV) components to DOE VTO for strategic planning of state-of-the-art technologies projects. ORNL's detailed benchmarking reports have received tremendous positive feedback from researchers in academia and industry, as well as other individuals with an interest in EV/HEV technologies. This information serves as a valuable educational resource on EV/HEV architectures, yields a track of lessons learned, prevents reinventing/duplication of advancements, and promotes leap-frog/competitive development. FY 2016 efforts include design assessments and comprehensive dynamometer testing of the electric machine and drive inverter from the 2016 BMW i3 electric vehicle.

Accomplishments

- Designed, fabricated, and assembled the hardware necessary to adapt the 2016 BMW i3 transmission to the dynamometer test cell.
- Successfully integrated ORNL controls with the 2016 BMW i3 motor inverter.
- Conducted comprehensive dynamometer testing of the 2016 BMW inverter and motor to obtain efficiency maps, peak torque, peak power, and many other performance metrics.
- Confirmed published peak torque and power specifications for the 2016 BMW i3 inverter and motor.

Introduction

The 2016 BMW i3 is an electric vehicle that includes a motor with a published power rating of 125 kW and a torque rating of 250 Nm. The 2016 i3 is sold in the battery-only option with a published range of 80 miles, and the range extender (with small combustion engine) option, with a published range of 160 miles. This first generation vehicle includes a 360 Vdc, 22 kWh lithium-ion battery. The second generation, beginning in model year 2017, includes the option for a 33 kWh battery with a 114-mile battery-only range, and the range extender option with a 180-mile range. This report reviews results from the disassembly of the motor and inverter unit and discusses detailed findings from teardown analyses. Comprehensive dynamometer testing was conducted, and the performance, efficiency, and other operational results are summarized herein.

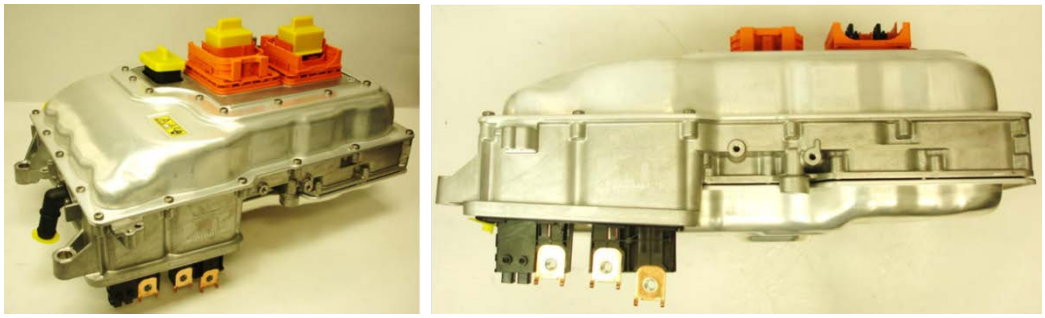
Approach

Automotive manufacturers do not typically publish details about the design, functionality, and operation of EV/HEV technologies, and even published details and specifications must be verified and clarified. For example, single-value power ratings for motors and inverters are often published, but they do not include information about the power capability throughout the operation range (e.g., versus speed), the duration for which this power can be maintained, the efficiency throughout the operation region, and many other important characteristics. Therefore, ORNL performs teardown assessments to obtain comprehensive information on design, functionality, and subcomponent characteristics. Furthermore, components are completely instrumented and tested in a dynamometer test cell to determine operational characteristics such as performance and efficiency. These activities provide the information needed for DOE to warrant a robust program and provide DOE partners and other researchers with valuable information on state-of-the-art EV/HEV technologies.

Results and Discussion

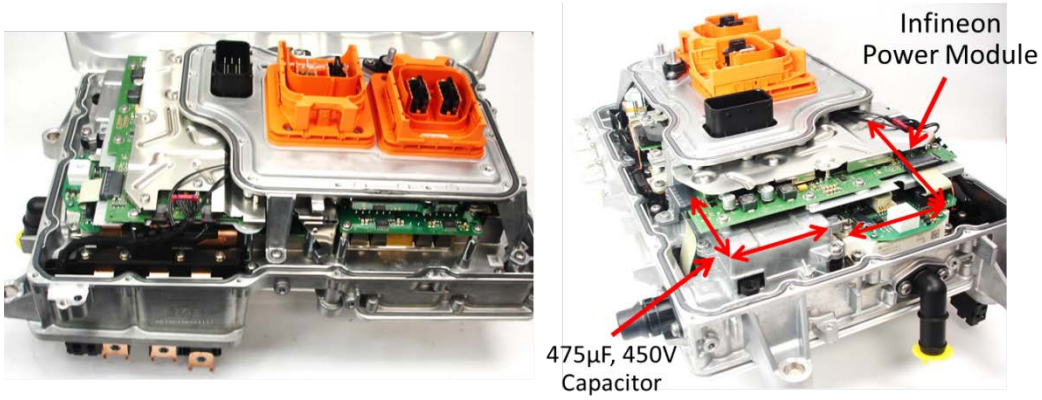
2016 BMW i3 Inverter Design and Functionality Assessments

The BMW i3 inverter assembly shown in Figure 4-1 contains the motor inverter, dc/dc converter (~360 V to 12 V), and a 3.7 kW battery charger. The mass of the inverter as received was 19 kg. Visible electrical connectors in this figure include two large dc voltage connectors and a small connector for low voltage power supply, communication, and other low voltage signals. After the top cover is removed as shown in Figure 4-2, key components of the assembly are visible. Circuitry for the 3.3 kW charger is located in the top compartment along with all components of the main inverter, including the power module, a driver board, control board, dc link capacitor, three current transducers, and ac bars.



(a) (b)

Figure 4-1: 2016 BMW i3 inverter assembly: (a) isometric view and (b) side view.



(a) (b)

Figure 4-2: 2016 BMW i3 inverter assembly with top cover removed: (a) front and (b) side.

After the control board, interface connectors, and other components are removed, the driver board, power module, and dc link are visible, as shown on the left in Figure 4-3. The right portion in the assembly shown in Figure 4-3 contains the passive components and electronics of the 3.3 kW charger. A 475 µF, 450 V capacitor is shown in the top left of Figure 4-3. The size of this capacitor is much smaller than other systems with comparable power ratings. This is being investigated further. It may be possible that a capacitor is installed on the dc link in the other 3.3 kW charger or perhaps (but not likely) at another location on the vehicle. A detailed examination of the control board components was conducted, and the key items are indicated in Figure 4-4. Two TriCore Infineon DSPs are noticed, as well as an Altera MAX II EPM570 CPLD chip. Additionally, an AD2S1210 resolver-to-digital (R2D) converter chip was identified. This is the first benchmarked system that does not use a Tamagawa R2D product.

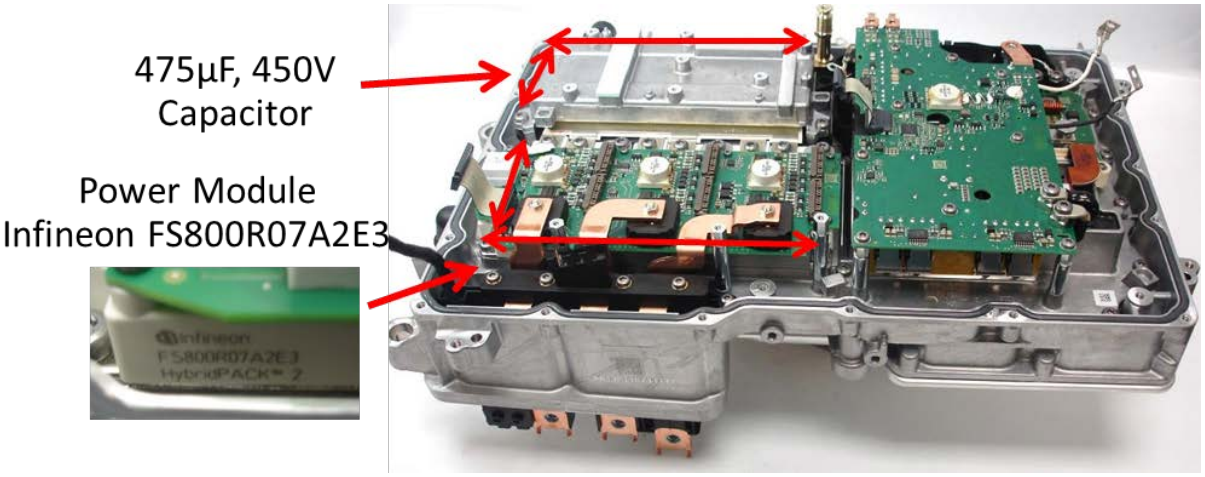


Figure 4-3: Location of inverter components in 2016 BMW i3 inverter assembly.

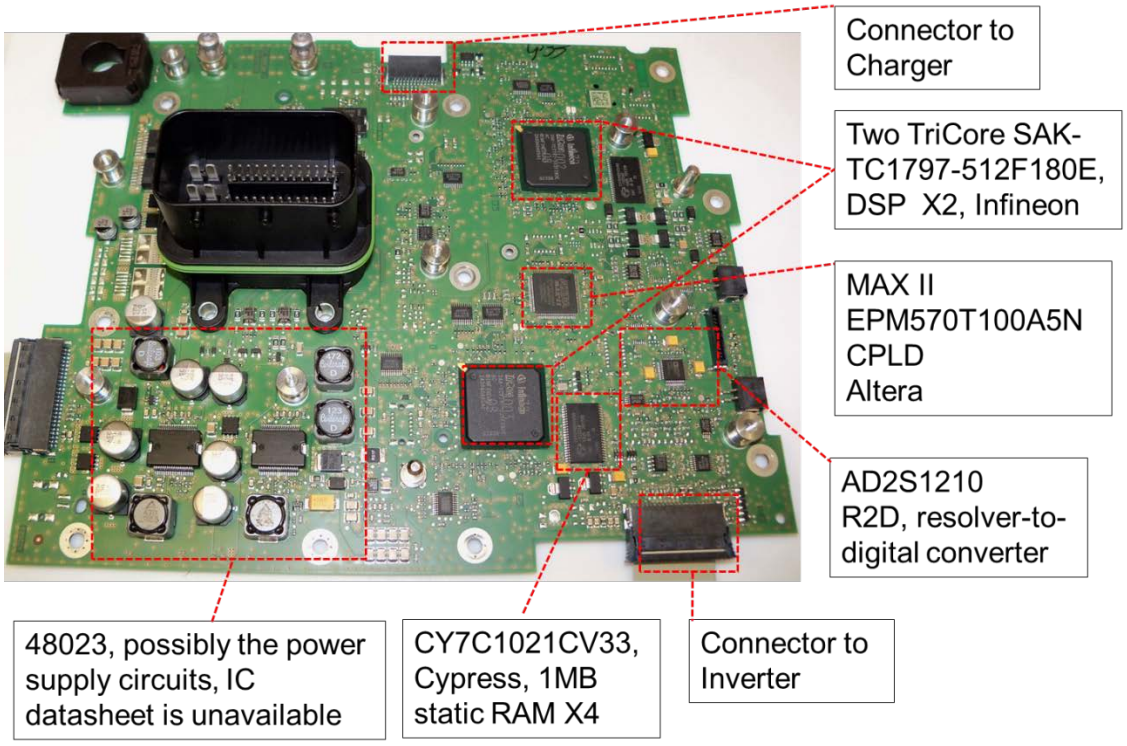


Figure 4-4: Key components on control board in 2016 BMW i3 inverter assembly.

Detailed component analysis of the driver board for the Infineon FS800R07A2E3 power module was conducted, and key components are shown in Figure 4-5. The module has a rating of 650 Vdc and 800 A/1600 A peak. It appears that a transformer is included for power isolation on each phase, and three 700 A LEM HC5F700 current sensors are located on the driver board. Six 2.2 Ω resistors are used for gate drive resistance at the 851 and 951 totem pole output.

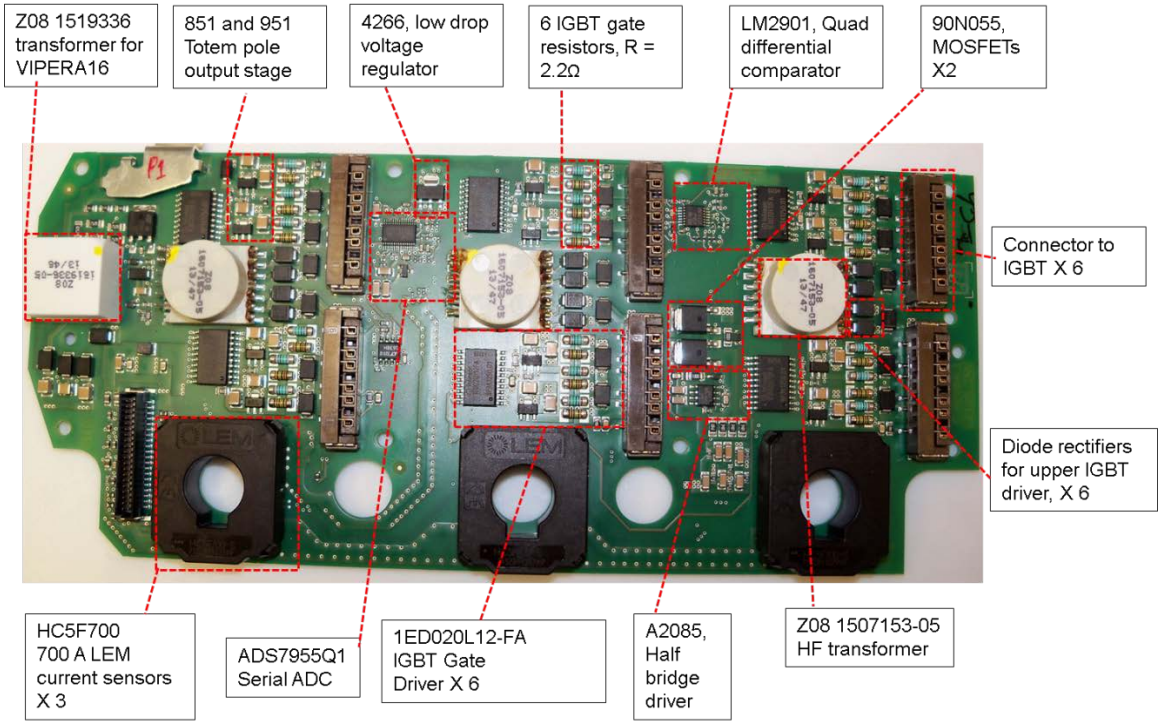


Figure 4-5: Key components on driver board in 2016 BMW i3 inverter power module.

After removing the gate driver board and plastic power module cover plate, the power electronics devices are visible in Figure 4-6. It is seen that four insulated-gate bipolar transistors (IGBTs) and four diodes are arranged in a parallel configuration for each switch. As with other Infineon modules, only one gate drive pin and trace is used to drive all four IGBTs in parallel. All connections from the devices to the dc link and ac output are accomplished with wire bonds. The dc bus bars from the capacitor attach to two terminals for each phase, as seen in the lower portion of Figure 4-6, and ac output terminals are visible in the top portion of Figure 4-6.

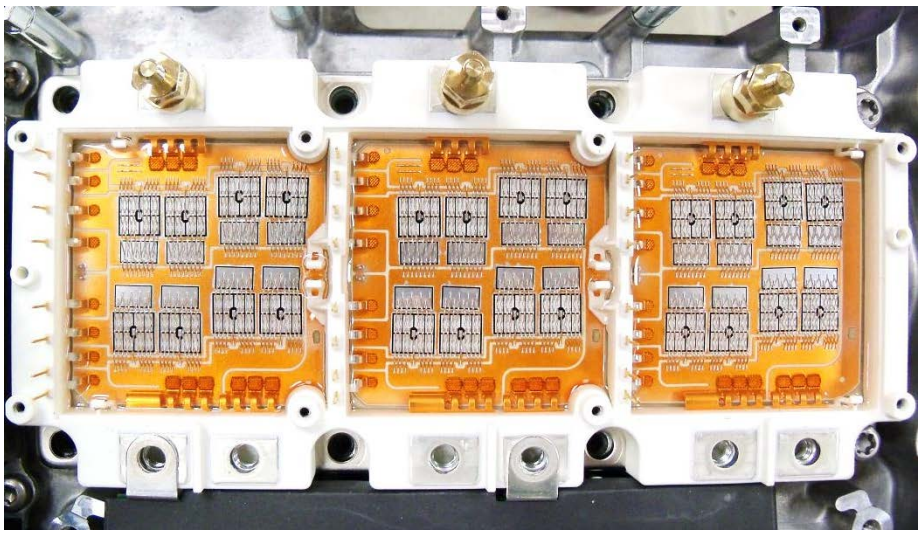


Figure 4-6: 2016 BMW i3 Infineon three-phase inverter power module with cover removed.

A close-up image of two IGBTs and two diodes is shown in Figure 4-7. Each IGBT has a cross section of 9.6 mm by 10.3 mm, and each diode has a cross section of 5.4 mm by 9.15 mm.

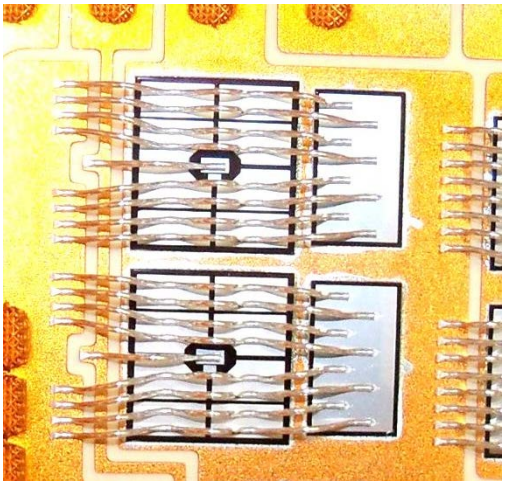


Figure 4-7: IGBTs and diodes in 2016 BMW i3 Infineon inverter power module.

2016 BMW i3 Motor Design and Functionality Assessments

The BMW i3 motor is contained in its own assembly, as shown in Figure 4-8(a), and is separately packaged from other power train components. The motor assembly has an overall mass of 42 kg, a published power rating of 125 kW, and torque rating of 250 Nm. An aluminum sheath is shrink-fitted onto the outer diameter of the stator, and the outer surface of the sheath has a spiral channel to form a circulating cooling path with the outer housing. The stator-sheath unit slides relatively easily out of the outer housing and includes large O-rings on each end to form a seal for the water-ethylene glycol coolant. The other housing, which includes one bearing, has a mass of 6.9 kg, and the sheath/flange has a mass of 4.6 kg. The stator steel core, copper, paper, insulation, and thread have combined a mass of 20.8 kg.

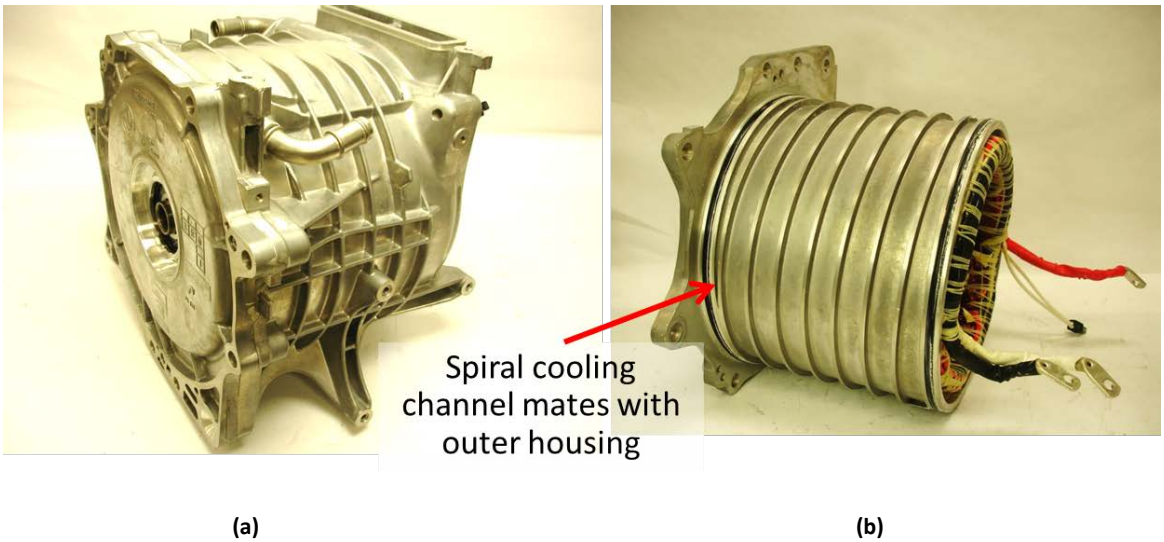
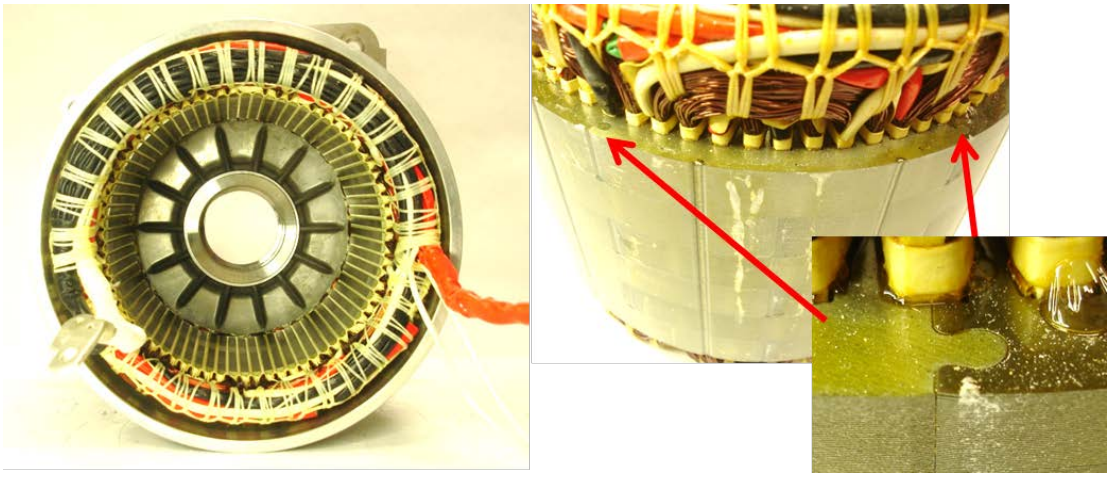


Figure 4-8: 2016 BMW i3 motor assembly (a) and motor assembly with outer case removed (b).

Figure 4-9 shows the stator winding and lamination in more detail. With 72 stator teeth, the machine has 12 poles and six slots per pole. The winding is full pitch and concentrically wound with 12 wires (21 AWG) in hand. Each pole is wired in parallel, giving six parallel paths and nine turns per slot. Two temperature sensors are mounted in the assembly, with one placed on the end turns and one placed near the rotor bearing. In Figure 4-9(b), it can be seen that the stator laminations are actually composed of six separate sections around the stator joined by what resembles a puzzle piece. This technique can greatly reduce manufacturing waste, as conventional full cylindrical stampings have considerable waste both outside and inside the cylinder,

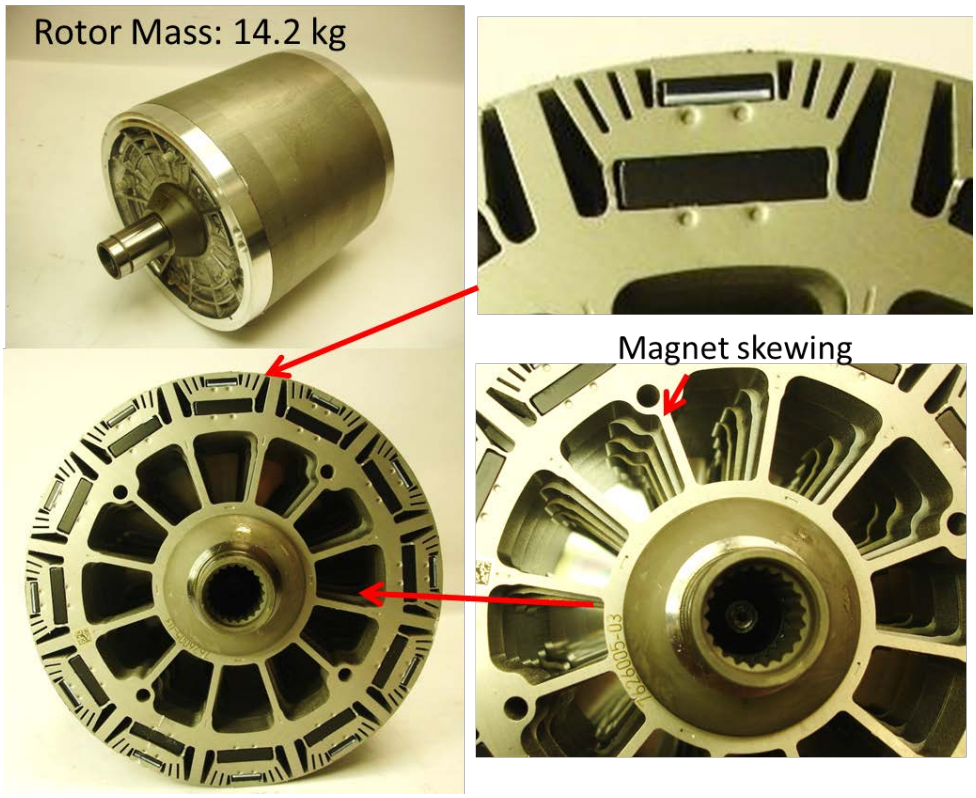
whereas the segmented stator pieces can be stamped in any orientation. The seam at which the puzzle-like interface occurs is alternated in six sections throughout the stack, which is likely to distribute the negative magnetic impacts of the seams across multiple phases and poles. The overall core length is 132.3 mm with an OD of 242.1 mm.



(a) (b)

Figure 4-9: 2016 BMW i3 motor stator front view (a) and stator windings/laminations (b).

The rotor, shown in Figure 4-10(a), has a total mass of 14.2 kg, which includes the rotor shaft, end plates, end plate bolts, laminations, and magnets. With an outer diameter of 178.60 mm, the lamination design resembles a synchronous reluctance rotor but has one small and one large neodymium iron boron magnet per pole. Incremental magnet skewing, visible in 10(b), is implemented six times throughout the stack, which is likely to mitigate cogging torque and torque ripple during operation. A summary of motor design specifications is provided in Table 4-1.



(a) (b)

Figure 4-10: 2016 BMW i3 motor rotor (a) and rotor magnets (b).

Table 4-1: Motor design specifications

Parameter	BMW i3
Stator OD, cm	24.2
Stator ID, cm	18.0
Stator stack length, cm	13.2
Stator mass, kg	20.2
Stator core mass, kg	13.7
Stator copper mass, kg	7.1
Number of stator slots	72
Stator turns per coil	9
Parallel circuits per phase	6
Coils in series per phase	1 per leg
Number of wires in parallel	12
Wire size, AWG	21
Winding notes	Full pitch, concentrically wound

Dynamometer Evaluation of the 2016 BMW i3 Motor and Inverter

For detailed component testing at ORNL, designs were developed to provide access to the electric motor shaft while maintaining the cooling and lubrication functionality used in the original form. This integration requires special attention to detail because high speed and power levels are involved. A custom plate was designed with high tolerance alignment features and considerations for lubrication. A unique adapter shaft also was designed to adapt the motor shaft to ORNL's dynamometer as shown in Figure 4-11.

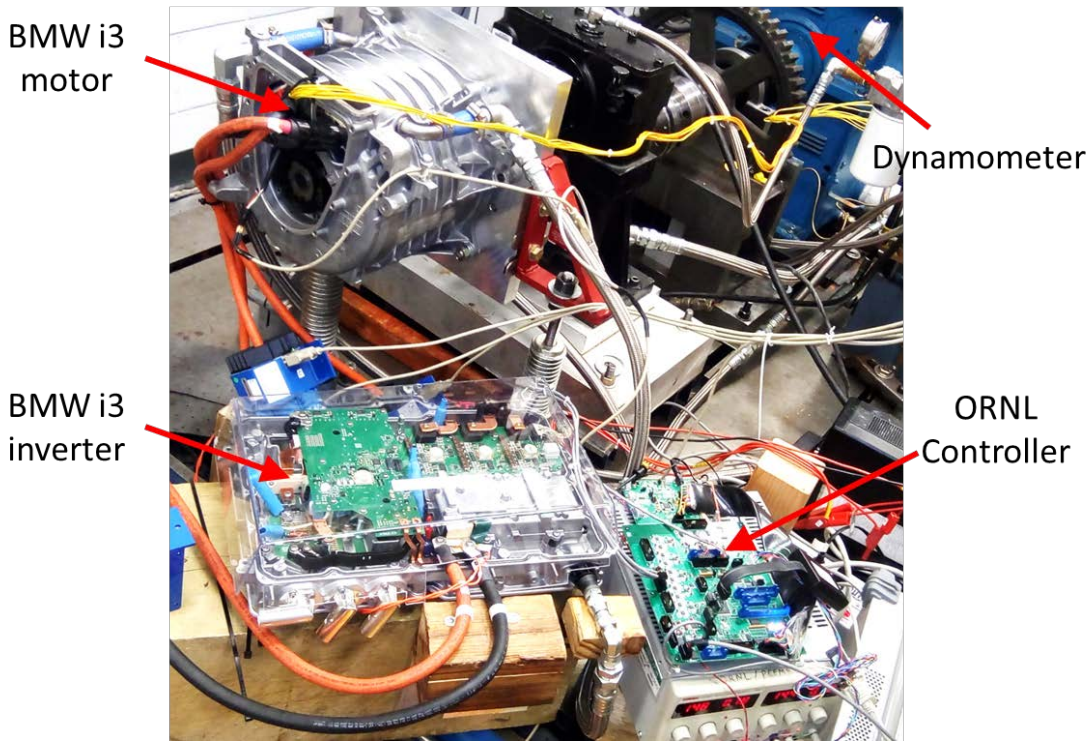


Figure 4-11: 2016 BMW i3 motor and inverter installed in ORNL dynamometer test cell.

Locked Rotor Tests

The graph in Figure 4-12 shows locked rotor torque measurements for various positions and applied current. Test results indicate that a peak current of ~530 Adc is required to produce the published peak torque of 250 Nm. Overall, the torque behavior versus position is very smooth, with maximum torque at high currents occurring at about 135 degrees. Linear behavior in the plot of peak locked rotor torque (of all positions) versus current shown in Figure 4-13 indicates that very little if any magnetic saturation is encountered, even at the published peak torque of 250 Nm.

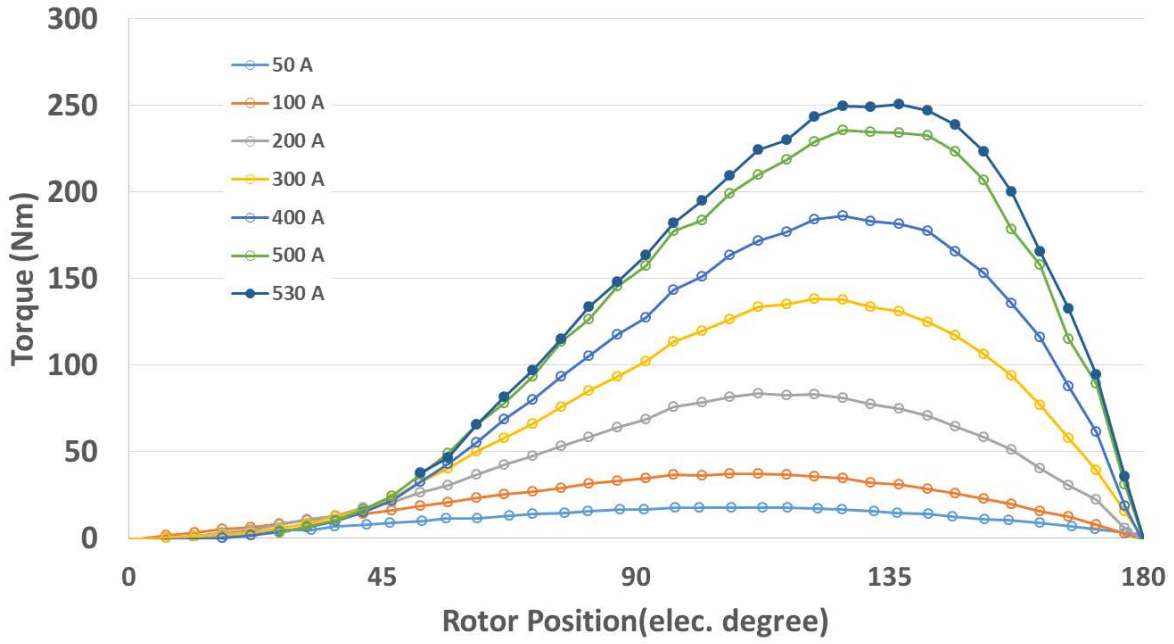


Figure 4-12: 2016 BMW i3 motor locked rotor torque versus position for various dc levels.

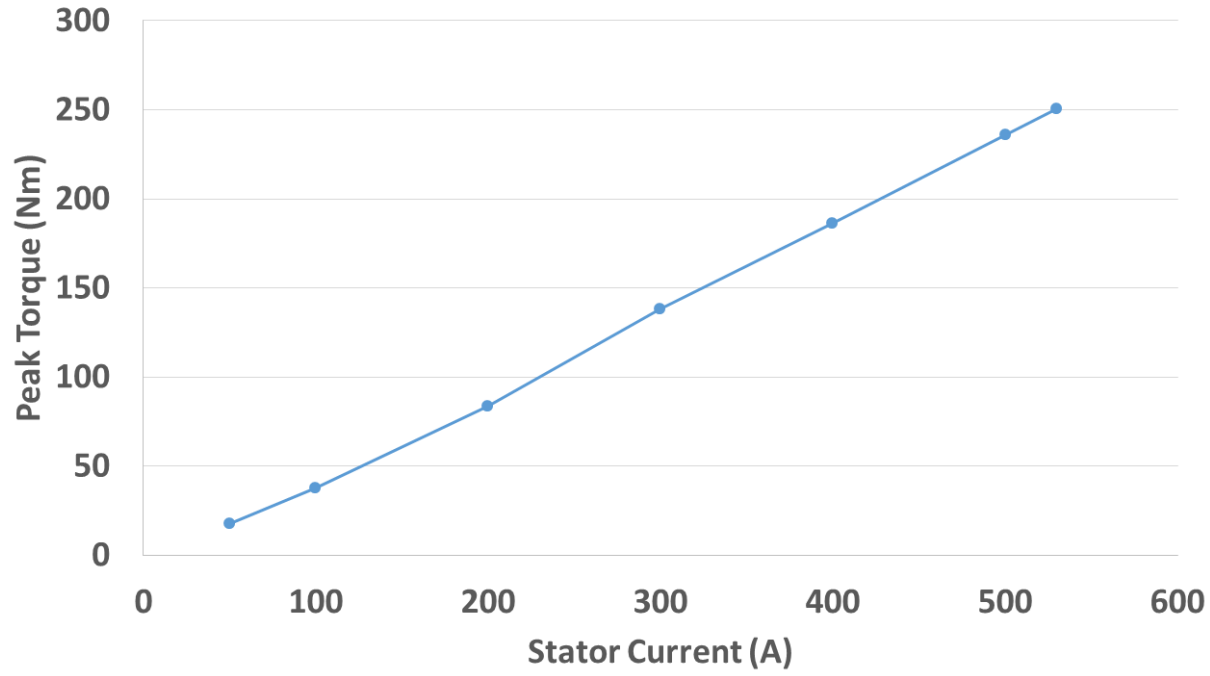


Figure 4-13: 2016 BMW i3 motor peak locked rotor torque versus position.

Efficiency Mapping, Performance, and Continuous Testing

Performance testing and efficiency mapping for the 2016 BMW i3 was conducted at various torques and speeds for a dc link voltage level of about 360 Vdc. During these tests, the BMW i3 inverter and motor were operated together, as optimal operation at each point was ensured. The inverter was cooled directly with standard automotive 50% water/50% ethylene glycol coolant flowing at a rate of 10 L/min with an inlet temperature of 65°C. Figure 4-14 shows motor efficiency contours exceeding 94% between ~2,500 and 9,000 rpm at most torques above 125 Nm. Figure 4-15 shows inverter efficiency contours, with efficiencies ranging from ~88% to 99% as speed increases. As shown in the combined efficiency map in Figure 4-16, combined motor and inverter efficiencies exceed 90% when the motor operates above torque levels of ~50 Nm at speeds greater than 5,000 rpm. During these tests, the published rated torque of 250 Nm was confirmed at up to a speed of 4,000 rpm. Tests also confirmed that the motor is capable of producing the published peak power of 125 kW at speeds between ~5,000 rpm and the maximum speed rating of 11,400 rpm.

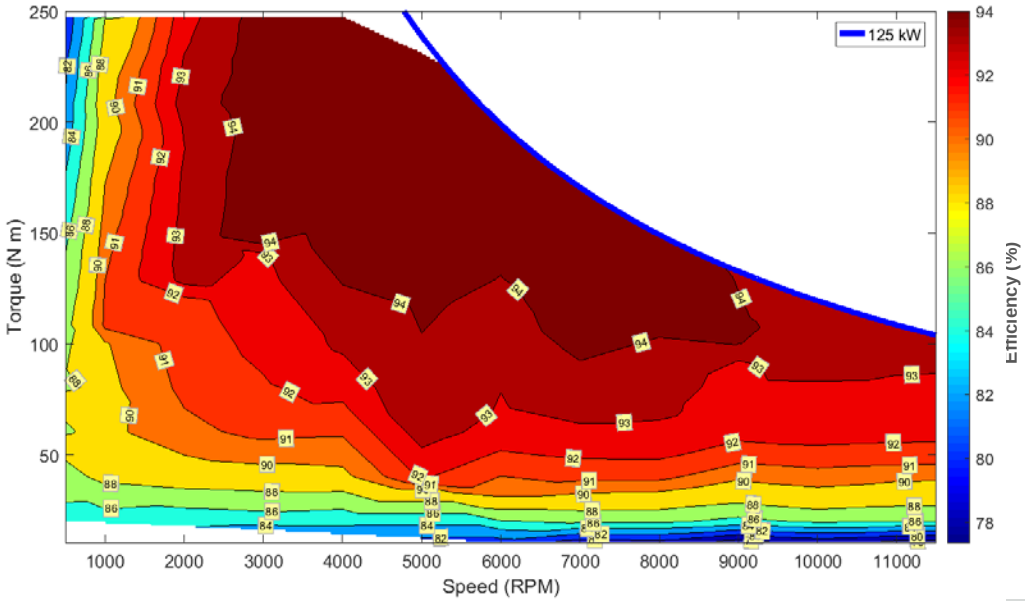


Figure 4-14: 2016 BMW i3 motor efficiency map.

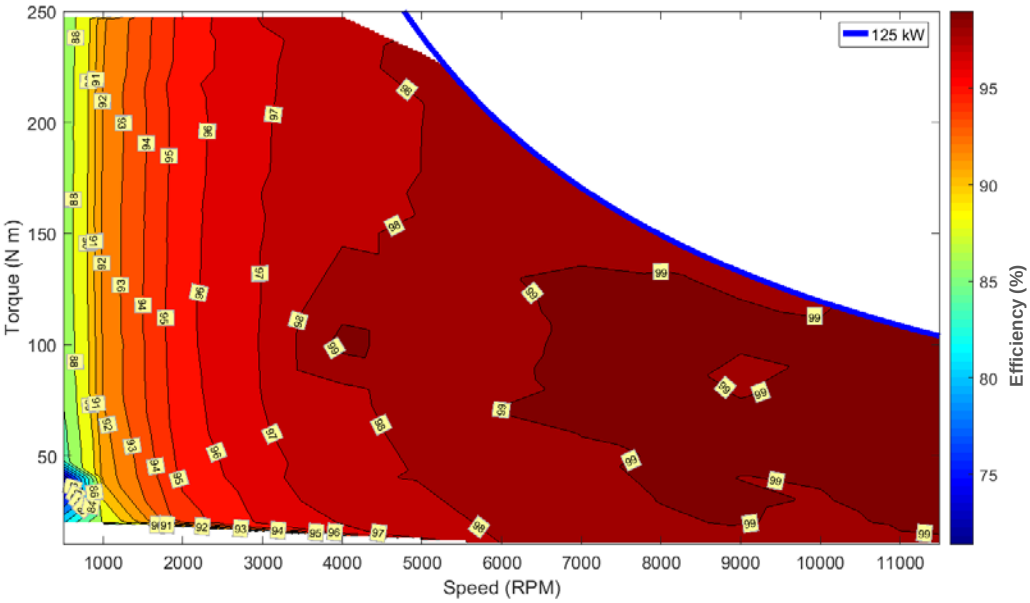


Figure 4-15: 2016 BMW i3 inverter efficiency map.

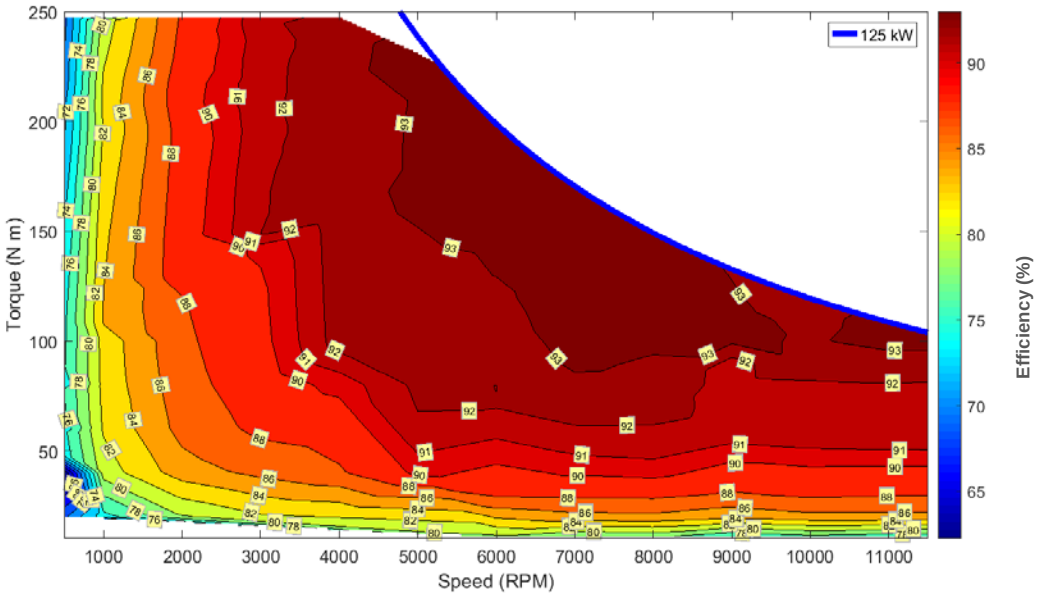


Figure 4-16: 2016 BMW i3 motor/inverter combined efficiency map.

When possible, continuous tests were conducted at 5,000, 7,000, and 9,000 rpm at power levels of 25, 50, and 75 kW. The plot in Figure 4-17 indicates the power level and motor winding temperature versus time for continuous tests at 7,000 rpm and 25, 50, and 75 kW. After operation at 25 kW for a half hour, the motor temperature reached about 85°C. Then the power was increased to 50 kW for a half hour, and the motor temperature was relatively stable at ~95°C. Furthermore, the power was increased to 75 kW, and temperatures remained below 110°C. As shown in Figure 4-18, for continuous operation at 5,000 rpm, motor temperatures stabilized at about 100°C after a half hour of operation at 50 kW.

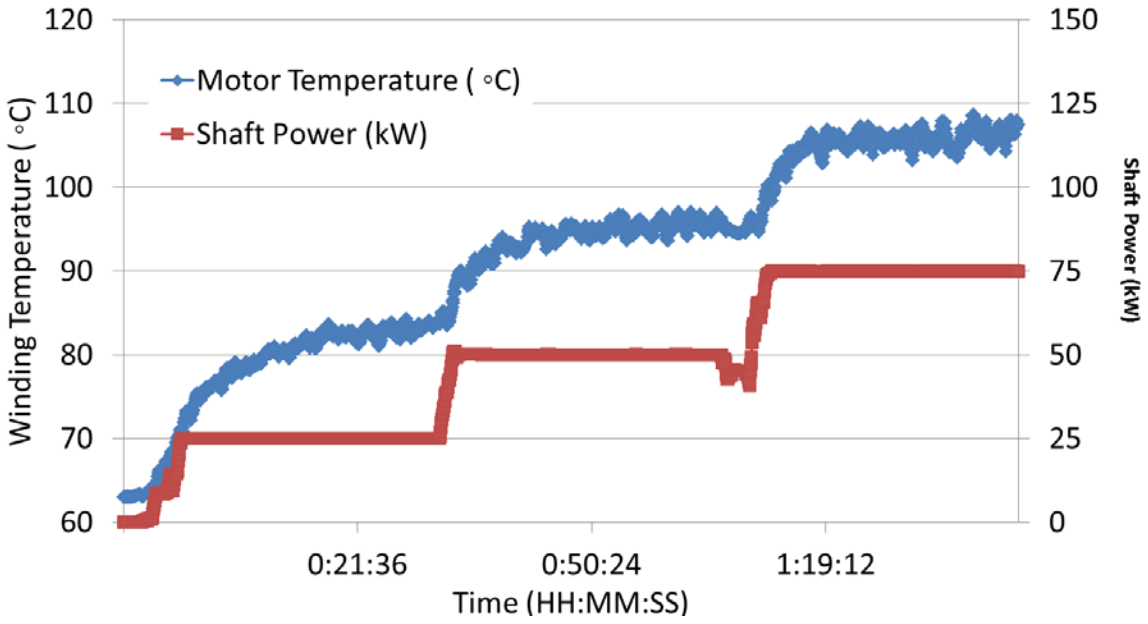


Figure 4-17: Continuous tests of 2016 BMW i3 motor and inverter at 7,000 rpm and various power levels.

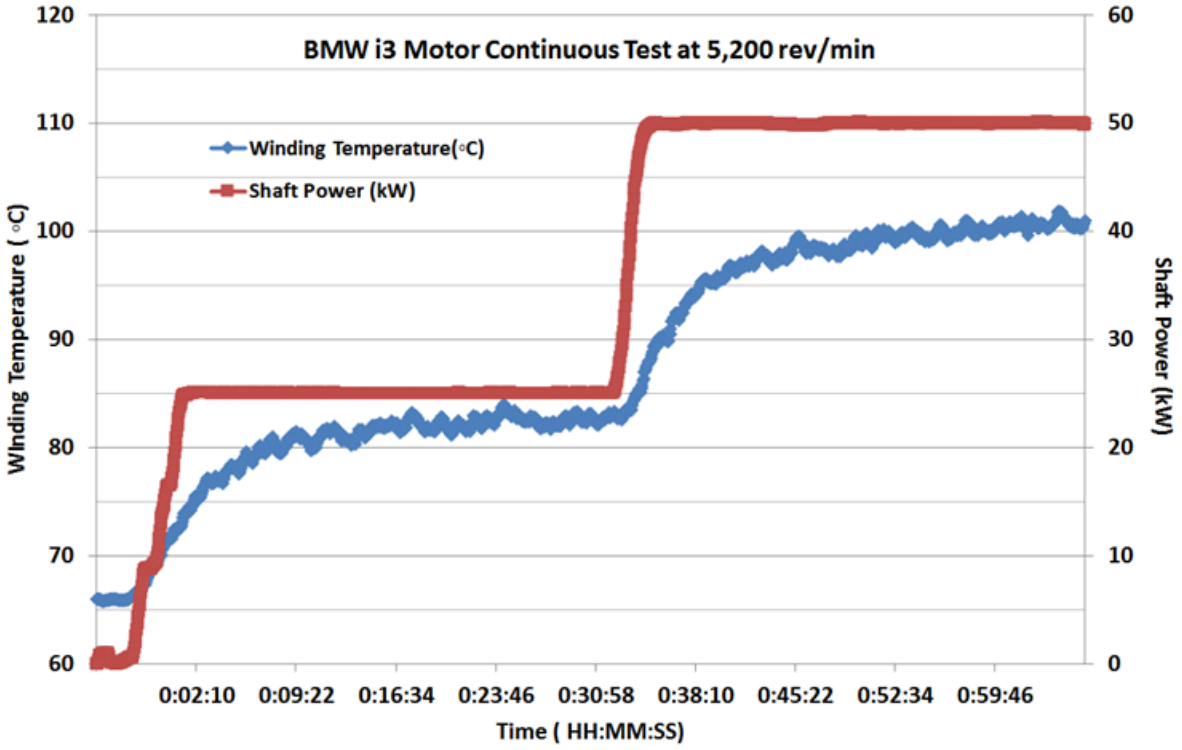


Figure 4-18: Continuous tests of 2016 BMW i3 motor and inverter at 5,000 rpm and various power levels.

Conclusions and Future Directions

Detailed disassembly and analysis of the BMW i3 inverter assembly revealed key design features, including a commercially available Infineon power module rated for 650 Vdc and 800 A/1,600 A-peak. The 450 Vdc, 475 µF capacitor is very small for the given power rating of the drive system; it is likely that either another capacitor is attached to the dc link or ripple mitigation switching methods are used.

Electric motor teardown analyses yielded many interesting design features, including a shrink-fit water jacket with spiraling cooling channels. A unique approach was taken with the stator laminations to reduce manufacturing waste, as separate pieces were stamped and pieced together with seams that resemble puzzle piece interfaces. The rotor design closely resembles a synchronous reluctance pattern but includes one small and one large neodymium iron boron magnet per pole. There are six magnet segments along the axial length of the rotor that are likely to mitigate cogging torque and torque ripple.

Locked rotor torque tests indicate very smooth behavior of torque versus speed, and it can be concluded that very little or no magnetic saturation occurs, even for the published peak torque rating of 250 Nm. Operation at published peak torque was confirmed up to 3,000 rpm, and peak power of 125 kW was confirmed between ~5,500 rpm and the maximum published speed of 11,400 rpm. Peak motor efficiencies reached 94% for a very wide range of operation, and inverter-motor efficiencies reached 94% for a small region of operation near 4,000 and 5,000 rpm and for torque above 150 Nm. Continuous tests indicated that the system is capable of operating continuously at 75 kW and 7,000 rpm, and the motor temperature remained below 110°C after 30 minutes of operation. During testing at 5,000 rpm and 50 kW, temperatures reached above 100°C after 30 minutes of operation.

Components for the 2017 Toyota Prius will be the focus of FY 2017 efforts. Comprehensive benchmarking of a Toyota product has not been conducted since the 2010 Prius, and there is a high level of interest in these components of this hybrid drive system.

FY 2016 Presentations/Publications/Patents

1. T. Burress, et al., "Status and trends of electric drive technologies," presented at the DOE Vehicle Technologies Program Electric Drive Technologies Electrical and Electronics Technical Team meeting, December 2016, Southfield, Michigan.
2. T. Burress, et al., "Benchmarking EV and HEV technologies," presented at the DOE Vehicle Technologies Office 2016 Annual Merit Review, June 2016, Washington, DC.

4.2 Thermal Performance Benchmarking

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Abstract/Executive Summary

The goal for this project is to thoroughly characterize the performance of state-of-the-art (SOA) in-production automotive power electronics and electric motor thermal management systems. Information obtained from these studies will be used to:

- Evaluate advantages and disadvantages of different thermal management strategies
- Establish baseline metrics for the thermal management systems
- Identify methods of improvement to advance the SOA
- Increase the publicly available information related to automotive traction-drive thermal management systems
- Help guide future electric-drive technologies (EDT) research and development efforts.

The performance results combined with component efficiency and heat generation information obtained by Oak Ridge National Laboratory (ORNL) may then be used to determine the operating temperatures for the EDT components under drive-cycle conditions. In FY16, the 2014 Honda Accord Hybrid power electronics thermal management system was benchmarked. Characterization of the 2015 BMW i3 power electronics thermal management system started in FY16, and the results will be reported in FY17.

The focus of this project is to benchmark the thermal aspects of the power electronics system. ORNL's benchmarking reports of electric and hybrid electric vehicle technology provide detailed descriptions of the electrical and packaging aspects of these automotive systems [1, 2].

Accomplishments

- Experimentally characterized the thermal performance of the 2014 Honda Accord Hybrid power electronics thermal management systems.
- Developed and validated both steady-state and transient thermal models of the 2014 Honda Accord power electronics systems. The models were used to identify the thermal bottlenecks within each system. Solutions to improve the thermal performance were proposed.
- Compared the thermal performance of the 2014 Honda Accord power electronics and 2012 Nissan LEAF power electronics systems to understand the advantage and disadvantage of different designs from cost and performance perspectives.

- Working to understand heat loss distributions within each system. Heat loss information will be used as inputs into the transient models and used to compute component temperatures under drive-cycle operations.
- We initiated benchmarking of the 2015 BMW i3 power electronics and electric motor thermal management systems and completed the experimental measurements of the power electronics system.

Introduction

This project will seek out SOA power electronics and electric motor technologies to benchmark their thermal performance. Benchmarking will focus on the thermal aspects of the system. System metrics, including the junction-to-liquid thermal resistance, winding-to-liquid thermal resistance, and the parasitic power consumption of the heat exchangers, will be measured. The type of heat exchanger (i.e., channel flow, brazed, folded-fin) and any enhancement features will be identified and evaluated to understand their effect on performance. Additionally, the thermal resistance/conductivity of select power module and motor components will also be measured. The research conducted will allow insight into the various cooling strategies to understand which heat exchangers are most effective in terms of thermal performance and efficiency. Modeling analysis will also be carried out to better understand the heat transfer and fluid dynamics of the systems. The research conducted will allow insight into the various cooling strategies to understand the current SOA in thermal management for automotive power electronics and electric motors.

Approach

Hardware testing and modeling analyses were conducted to benchmark the performance of the power electronics and electric motor thermal management systems. The project approach is outlined below.

- Collaborate with industry and ORNL to identify the vehicle system to benchmark
  - The 2014 Honda Accord Hybrid power electronics thermal management system was benchmarked in FY16. Tests were initiated to measure the thermal performance of the 2015 BMW i3 power electronics thermal management system.
- Experimentally measure the performance of the thermal management systems
  - Measure the power electronics junction-to-liquid thermal resistances
  - Measure the thermal properties of the system components (e.g., thermal pads, stator laminations, motor windings)
  - Measure heat exchanger thermal resistance, pressure drop, volume, and weight.
- Create thermal models of the thermal management systems
  - Validate the models using experimental results
  - Compute thermal resistances that cannot be experimentally measured
  - Create transient thermal models and use them to estimate component temperatures under various drive-cycles.
- Analyze and report data
  - Identify thermal bottlenecks in the system and provide solutions to improve the SOA
  - Establish baseline metrics for the thermal management systems
  - Share results with industry and research institutions
  - Support other EDT projects (power electronics thermal management research, electric motor thermal management research, benchmarking electric vehicle and hybrid electric vehicle technologies [ORNL]).

Results and Discussion

In FY16, the 2014 Honda Accord Hybrid power electronics thermal management systems were benchmarked. Experimental testing of the hardware was first completed to measure thermal resistance values of the systems. The laboratory tests were intended to provide an accurate means of measuring thermal performance of the systems and were not intended to simulate actual automotive operating conditions. Steady-state and transient models were then created and validated against the experimental data. The validated thermal models were used

to further understand the heat transfer mechanisms within the systems. The goal is to use the models to compute component temperatures under drive-cycle conditions. Efforts to benchmark the 2015 BMW i3 power electronics thermal management system also started in FY16.

2014 Honda Accord Power Electronics (Inverter) Thermal Management System

Figure 4-19 shows pictures of the Honda Accord power electronics and cooling system. The Accord power electronics system consists of two inverters for the two electric machines (motor and generator) in the vehicle and one DC-to-DC boost converter. The Accord inverter does not use a "brick" style power module design, but instead uses a number of insulated gate bipolar transistor (IGBTs) and diodes soldered onto a direct-bond copper (DBC) substrate to create the two inverters and boost converter. The same size (footprint) IGBTs and diodes are used throughout the entire system [3]. It is also shown in Figure 4-19 that intricate finned structures are fabricated on the cold plate surface to augment cooling. Figure 4-20 shows the power module model created using a computer-aided-design (CAD) tool, and the cross-sectional view of the stack module structure (thermal path) of the Accord. Unlike the 2012 LEAF, the Accord does not utilize grease as a thermal interface material (TIM) between the layers, but still uses the conventional metalized-ceramic substrate.

Figure 4-19: Pictures of the 2014 Honda Accord inverter. The left image shows the entire power electronics system and the middle image presents the cold plate cooling channels. The image on the right shows the intricate fins directly fabricated on the cold plate.
Photo Credit: Gilbert Moreno (NREL)

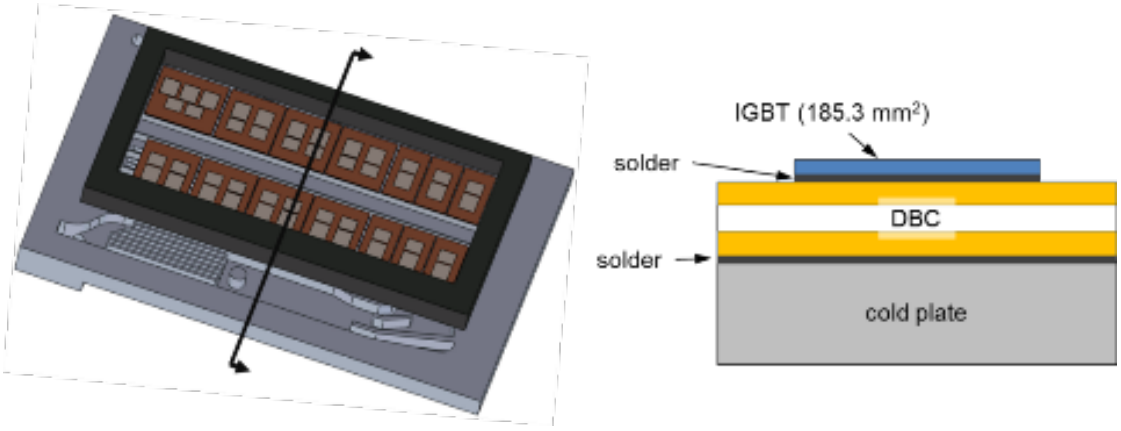

Figure 4-20: CAD model of the Honda Accord power module (left). The various power module layers are shown in the cross-section view on the right.

Experiments were conducted to measure the junction-to-liquid resistance of the power modules. For the experiments, the module was connected to the water-ethylene glycol (WEG) flow test bench. The test bench circulated WEG (50%/50% water and ethylene glycol by volume) at a 65°C inlet temperature through the inverter cold plate at various flow rates. The experiments were repeated to ensure repeatable results. A transient thermal tester (T3ster) system was used to power/heat and measure the temperature of one IGBT. A total of 50 A were provided to power one IGBT (approximately 55 W of heat). Measuring temperatures required calibrating the voltage drop through the IGBT to its temperature. Temperature calibration was carried out within a temperature-controlled chamber. Two calibrated K-type thermocouples were mounted onto the power modules (placed near the IGBT that was to be tested) and used to obtain the temperature versus IGBT voltage drop relationship while supplying a 1-milliamp sense current through the device. Ten volts were used

to gate the IGBT. The entire system was insulated with thick layers of insulation to minimize thermal losses to the surrounding environment. Then the specific thermal resistance was defined per Equation 1:

$$R"_{th,\ j-l} = \frac{(\overline{T_j} - \overline{T_l})}{Q_{IGBT}} \times A_{IGBT} \qquad \text{Equation 1}$$

where $\overline{T_j}$ is the average junction temperature, $\overline{T_l}$ is the average WEG temperature, Q_{IGBT} is the total heat dissipated through the IGBT, and A_{IGBT} is the area of the IGBT. Following the experimental procedure, the thermal performance of the 2014 Honda Accord power electronics system was characterized. Figure 4-21 shows the junction-to-liquid specific thermal resistance values at various flow rates. The 2014 Accord system provides thermal resistance values that are lower than the values from the 2012 Nissan LEAF that was characterized in FY15. The results also indicate that the passive stack thermal resistance is significantly larger than convective resistance (at the flow rates tested). At the typical automotive power electronic flow rates (~10 Lpm), the junction-to-liquid specific thermal resistance is about 44 mm^2·K/W, nearly 50% lower than that of the Nissan LEAF. The Accord's lack of TIM layers is the likely reason for its superior thermal performance. The lack of a TIM layer in the Accord reduces its passive-stack thermal resistance, which makes it more sensitive to increasing convective heat transfer (i.e., increasing flow rates) as compared with the LEAF.

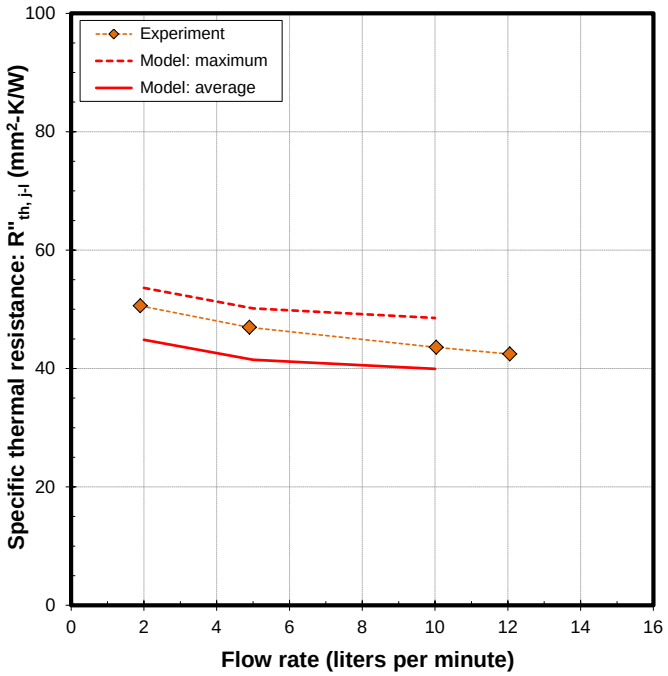

Figure 4-21: Experimentally measured and model-predicted IGBT thermal resistance values for the 2014 Honda Accord inverter.

The laboratory tests were intended to provide an accurate means of measuring thermal resistance of power electronics systems and were not intended to simulate actual automotive operating conditions or environments. The experimental results were used to validate the thermal models which were then to be utilized to understand the thermal performance of the systems under various working conditions. Both computational fluid dynamics (CFD) and finite element analysis (FEA) were applied to simulate the Accord power electronics thermal management systems to better understand the heat transfer within inverter. Table 4-2 lists the properties of the various power module components that were used in the models. Temperature-dependent thermal conductivity properties were used for silicon and copper. The thermal conductivities of the other components were obtained from literature. CFD-computed wetted-surface average heat transfer coefficients at various flow rates are provided in Table 4-3. The streamlines of the liquid and also the temperature profile on the cold plate surface calculated from the CFD simulation are presented in Figure 4-22. In the left graph of Figure 4-22, it clearly shows that the coolant flows through the finned structure and the temperature profile in the right graph also suggests where the hot spot locates.

The computed heat transfer coefficient values were imposed as boundary conditions in the FEA model. The FEA model replicated the experimental conditions (dissipate approximately 55 W through one IGBT). Once the models were validated by the experimental results, they are then applied to predict the steady-state and transient thermal resistance values under various conditions. The transient thermal resistance or thermal impedance (Z''_{th}) was computed using Equation 2.

$$Z''_{th,\ j-f} = \frac{\left(T_{j,max}(t) - T_f\right)}{Q_{IGBT}} \times A_{IGBT} \qquad \text{Equation 2}$$

where $T_{j,max}(t)$ is the maximum junction temperature, T_f is the WEG temperature, Q_{IGBT} is the total heat dissipated through the IGBT, A_{IGBT} is the area of the IGBT, and t is time.

Figure 4-21 also provides the model-estimated maximum (computed using the maximum junction temperature) and average (computed using the average junction temperature) thermal resistance values. As shown, the model-predicted results provide a good match with the experimental data (maximum ~6% difference between model and experimental results). The FEA model was then used to generate a temperature profile from the IGBT to the liquid to identify the largest thermal bottlenecks in the system, with about 100 W of heat generated on the IGBT. The temperature profile is shown in Figure 4-23 and clearly shows that the passive stack provides the largest thermal bottleneck within the system. The silicon nitride layer is found to provide the largest resistance within the passive stack.

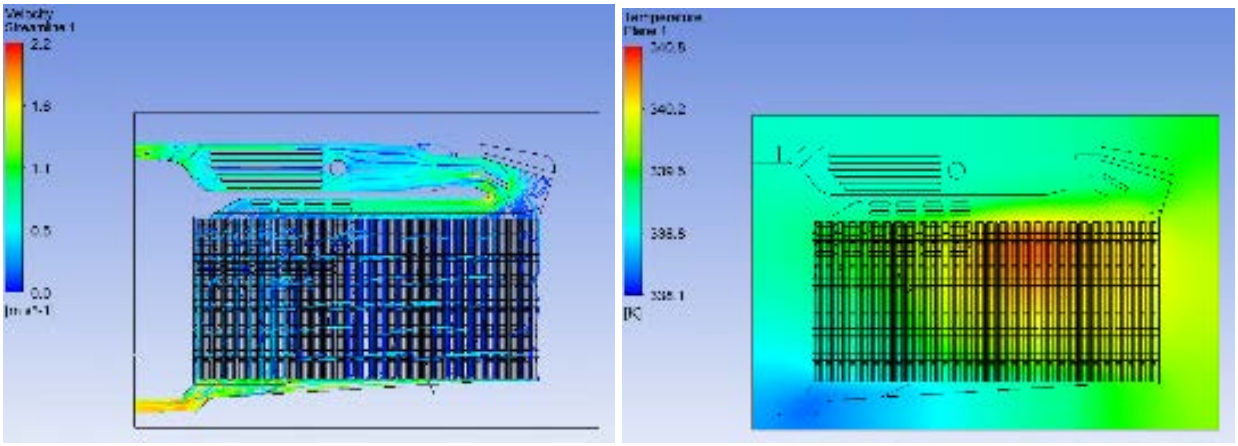

Figure 4-22: CFD-generated plot showing the liquid velocity streamlines at a flow rate of 10 Lpm (left iamge) and the temperature distribution (right image) on the cold plate surface.

Table 4-2: Thermal conductivity and thickness values used in the Honda Accord inverter thermal models

	Silicon[4]	Copper [4]	Silicon Nitride [5]	Aluminum [6]	Molding plastic [7]
Thermal conductivity (W/m·K)	Temperature-dependent	Temperature-dependent	20	200	0.34

Table 4-3: CFD-predicted average heat transfer coefficient values for the Honda Accord inverter cold plate

Flow rate (Lpm)	Heat transfer coefficent (W/m^2·K)
2.0	992
5.1	1793
9.8	2518

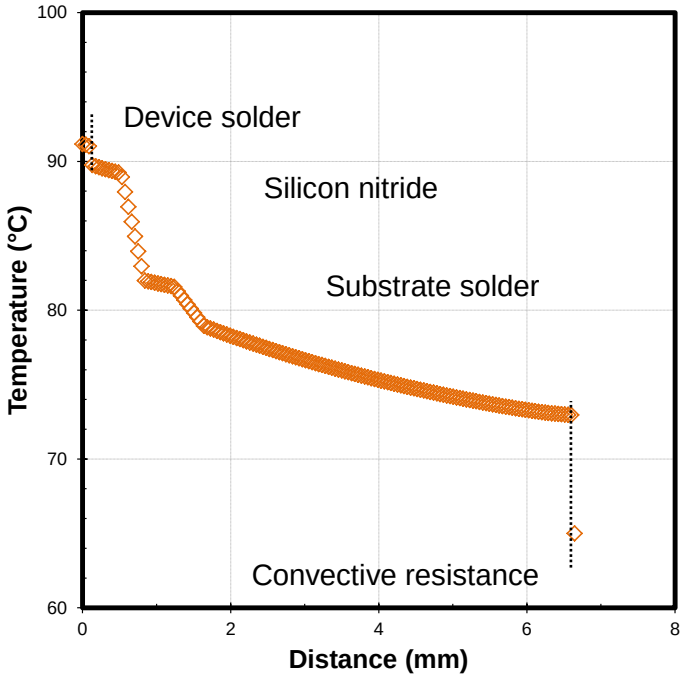

Figure 4-23 : Temperature profile through the Accord inverter depicting the thermal path from the IGBT to the liquid. The silicon nitride layer constitutes a significant thermal resistance in the power modules.

With the validated FEA model, simulations were conducted to analyze the steady-state thermal resistance of various power modules at a wide range of convective thermal resistance values (i.e., convective heat transfer coefficient values). The thermal performances of the LEAF and Accord systems were compared with the performance of a more conventional module design, which uses a metalized-ceramic substrate and a TIM layer between the module and the cold plate. Two conventional power module designs were studied. One design was achieved by replacing the copper-molybdenum plates and the dielectric pad with a DBC substrate. The DBC substrate has an alumina sheet of 0.38-mm thickness and two 0.25-mm-thick copper layers on both sides. The second conventional design was a Semikron SKM power module that also has an alumina DBC substrate. In both designs, a TIM layer is applied between the modules and an aluminum cold plate.

In the FEA models used to simulate the power module systems, only one power module was modeled and a three-to-one (IGBT-to-diode) heat loss ratio was used in the simulations. Because the Accord's power electronics does not use brick-type module design, only one half-bridge segment that consisted of two IGBT-diode pairs per switch was studied. The total power dissipated through the modules was adjusted so that the maximum junction temperatures reach 200°C, which is high for typical silicon-based devices. However, the 200°C junction temperature was applied here to simulate the high-temperature wide-bandgap devices. The liquid temperature was set to be 70°C. In these analyses, the finned structures on the cold plate surface were not modeled, and the convective thermal resistance was applied as a heat transfer coefficient boundary condition on the lower surface of the cold plate.

Figure 4-24 shows the specific thermal resistance versus the convective thermal resistance for the four power module systems introduced above. The thermal resistance was calculated using Equation 1 by applying the maximum junction temperature for $\overline{T}_J$. As presented in Figure 4-24, the LEAF (standard) power module has greater specific thermal resistance than that of the DBC-modified LEAF module. At 100 mm^2·K/W convective thermal resistance, the Accord module's thermal resistance is about 38% and 12% lower than the LEAF and DBC-modified LEAF power modules, respectively. In addition, the Accord's module thermal resistance decreases at a faster rate with decreasing convective thermal resistance. This indicates that the Accord module has the lowest stack thermal resistance among the four systems characterized. It needs to be pointed out that the cooled surface area where the convective boundary condition is applied is different for the four designs and is the smallest for the Accord power module.

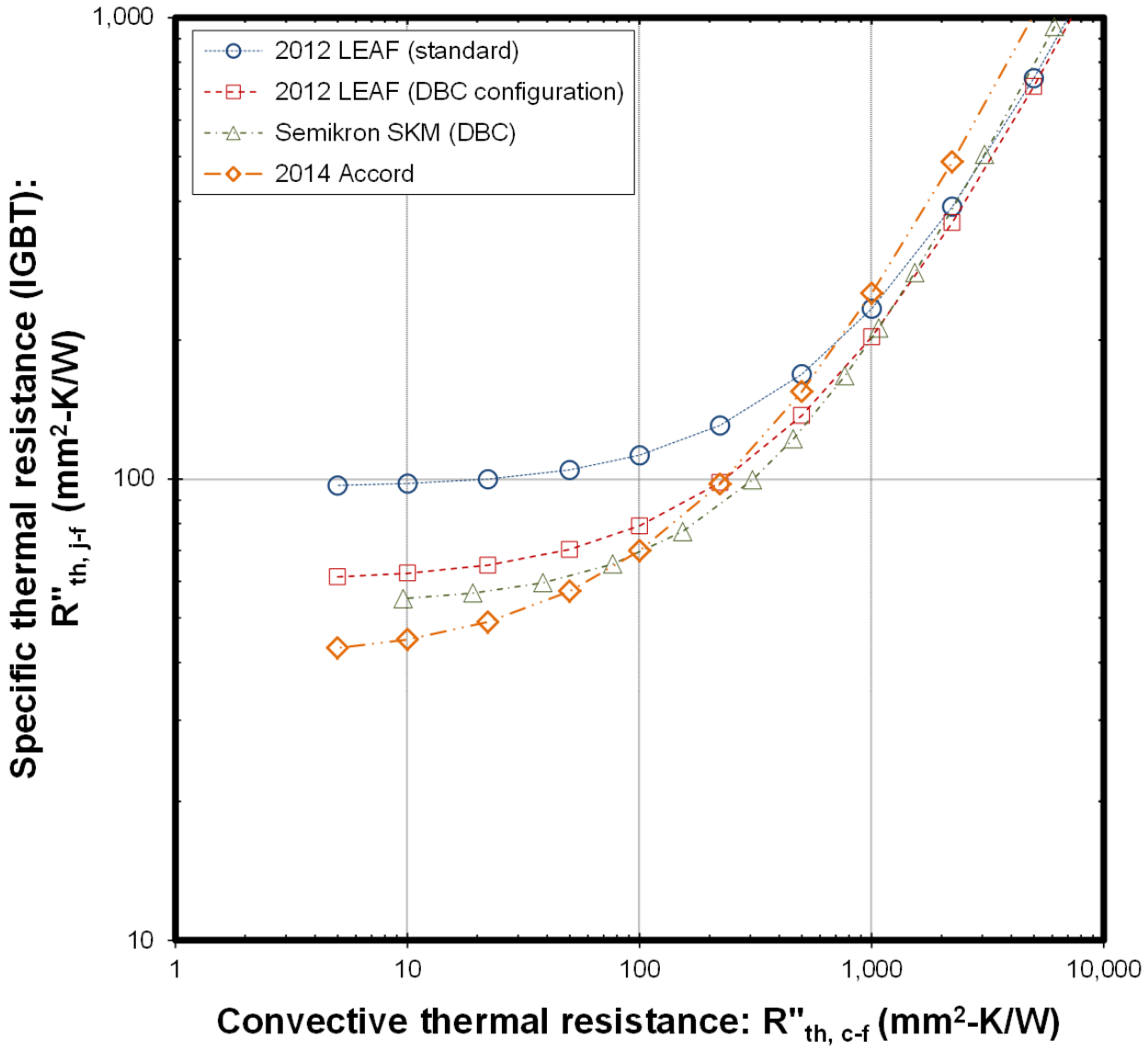

Figure 4-24: Specific (junction-to-liquid) thermal resistance versus the convective thermal resistance for the standard LEAF, DBC-modified LEAF, the Accord, and Semikron modules. The Semikron data were from Bennion and Moreno [8].

FEA simulations were also conducted to study the transient thermal performance of three power modules. In Figure 4-25, the thermal impedances of the LEAF, DBC-modified LEAF and the Accord are shown. In the study, the power modules were initially at a uniform temperature of 70°C, and power to the devices was turned on (i.e., increasing temperature condition). The total heat applied on the power modules was 2,084 W, 2,956 W, and 1,865 W for the LEAF, DBC-modified LEAF, and Accord, respectively. The total heat was adjusted so that the maximum junction temperature reaches 200°C. Although the Accord has the lowest thermal resistance, it also has fewer IGBTs as compared to other modules and thus it dissipated the least amount of heat. A three-

to-one IGBT-to-diode heat loss ratio and a convective thermal resistance of 100 mm^2·K/W were applied in the simulation.

The impedance of the standard LEAF power module was found to be the lowest at a time of less than one second. This is probably due to the placement of a highly conductive copper-molybdenum plate directly below the IGBT and moving the low thermally conductive layer farther away from the IGBT-diode pair. In contrast, the DBC-modified LEAF module has a relatively low thermally conductive DBC plate close to the heat source, which limits the initial heat transfer. Additionally, the thermal mass of the copper-molybdenum layer increases the heat capacitance near the devices. When the time is larger than one second, the thermal impedance of the standard LEAF becomes larger than that of the DBC-modified LEAF and the Accord modules, as it gradually approaches steady state. These trends indicate that the standard LEAF configuration may offer an advantage at transient conditions. Compared with the Accord power module design, the LEAF system also shows cost and reliability advantages. In the LEAF system, dielectric pads were sued for insulation instead of metalized-ceramic substrates and the modules were directly mounted onto cast-aluminum cold plates instead of precesely machines plates.

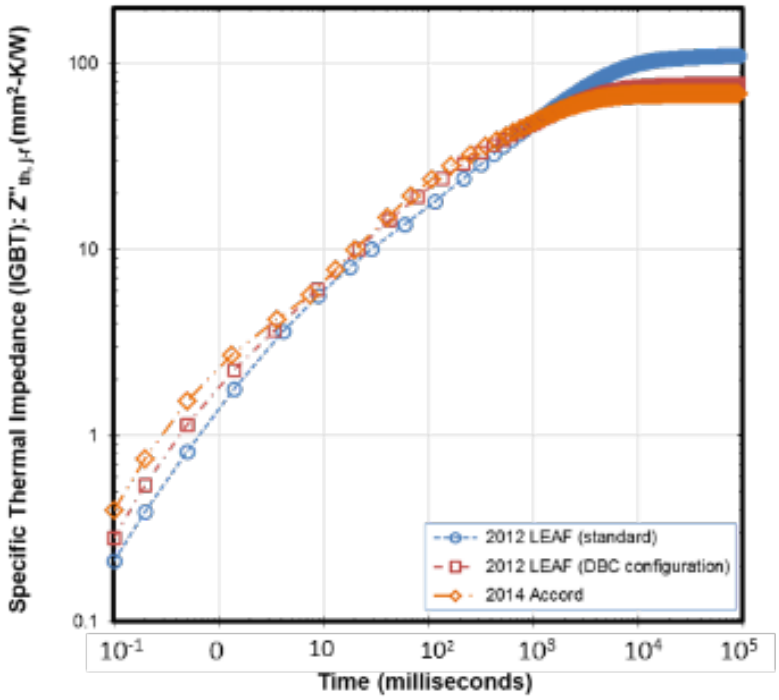

Figure 4-25: Transient junction-to-liquid thermal impedance plotted versus time.

2015 BMW i3 power electronics (inverter) thermal management system

Benchmarking of the 2015 BMW i3 power electronics thermal management system also started in 2016. Figure 4-26 shows the images of the 2015 BMW i3 electrical machine electronics (EME), which serves as control electronics for the electrical machine. The electrical machine electronics fulfill the task of converting the DC voltage from the high-voltage battery into a three-phase AC voltage for operating the electric motor. It can also work as an alternator to convert the three-phase AC voltage from the electrical machine to a DC voltage to charge the high-voltage battery. Figure 4-26 also shows the cold plate and the drive board mounted on the power module. The power block is an Infineon HybridPACK 2 which was developed for hybrid-and electric vehicles. This module accommodates a three-phase six-pack configuration of Trench-Field-Stop IGBT 3 and matching emitter- controlled diodes, as shown in the right image in Figure 4-24. The power module also comes with an integrated pin-fin baseplate for direct cooling that significantly enhances heat removal from the chips. The cross-section view of the stack structure of the power module is shown in Figure 4-27. Detailed investigation of each layer's thermal property is in progress.

Figure 4-26: Pictures of the 2015 BMW i3 inverter. The left image is the top view of the i3 EME system. The middle image shows the cold plate cooling channels. The image on the right shows the power block mounted on the cold plate.
Photo Credit: Xuhui Feng (NREL)

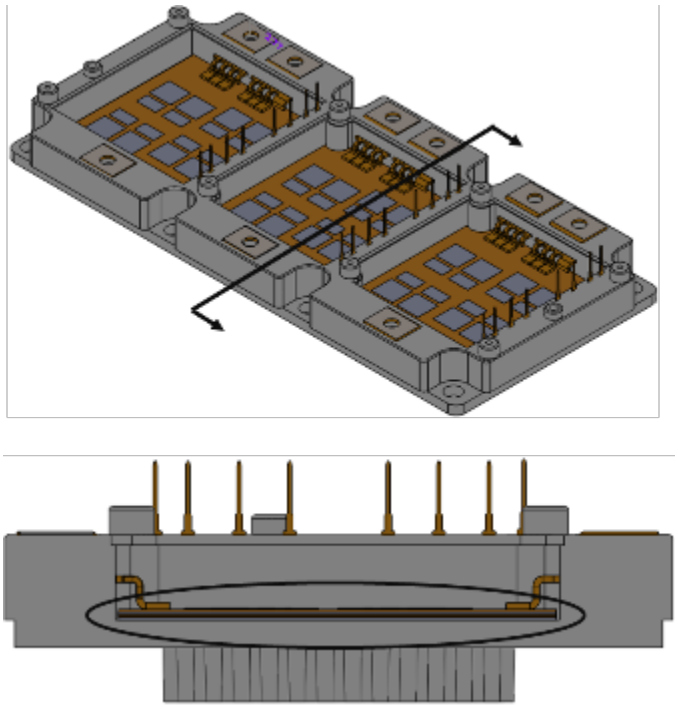

Figure 4-27: CAD model of the BMW i3 power module (top). The various power module layers are circled out in the lower cross-section view.

Following the procedure adopted for the Accord power electronics, measurements of thermal resistance were also performed for the BMW i3 IGBT module. Figure 4-28 displays the junction-to-liquid thermal resistance versus various flow rates for the BMW i3 power module, along with that of the 2012 LEAF and 2014 Accord power modules. Experiments were conducted at flow rate, temperature, and input power values similar to those used for the Leaf and Honda power electronics systems. The BMW i3 system provided the thermal resistance in the range of 12–14 mm^2·K/W, lower than the values from both the Leaf and Honda systems. At 12 Lpm, the i3 power module has a low junction-to-liquid thermal resistance of only 12 mm^2·K/W, compared to 78 mm^2·K/W for the LEAF and 42 mm^2·K/W for the Accord. A possible reason for the significant improvement in the i3's specific thermal resistance is that the module incorporates higher thermally conductive materials and reduces the IGBT size. In-depth study of the materials and the properties within the stack module needs to be conducted to better understand the improved thermal performance. In addition, the junction-to-liquid thermal resistance shows minimal variation with the flow rates, suggesting that the stack thermal resistance is significantly larger than the convective resistance (at the flow rates tested).

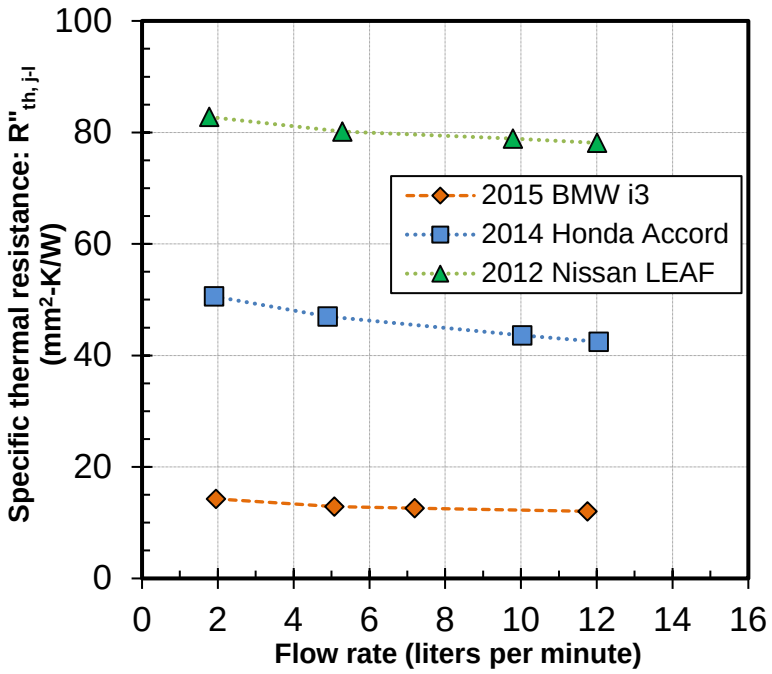

Figure 4-28: Specific (junction-to-liquid) thermal resistance plotted versus the convective thermal resistance for the 2012 LEAF, 2014 Accord and 2015 BMW i3 power electronics systems.

Conclusions and Future Directions

In FY16, we benchmarked the thermal performance of the 2014 Honda Accord Hybrid power electronics thermal management systems. Both experiments and numerical simulation were utilized to thoroughly study the thermal resistances and temperature distribution in the power module.

- Experimental results obtained from the WEG tests provided the junction-to-liquid thermal resistance. The FEA and CFD models were found to yield a good match with experimental results. Both experimental and modeling results demonstrate that the passive stack is the dominant thermal resistance for both the motor and power electronics systems.
- The 2014 Accord power electronics systems yield steady-state thermal resistance values around 42–50 mm^2·K/W, depending on the flow rates. At a typical flow rate of 10 Lpm, the thermal resistance of the Accord system was found to be about 44% lower than that of the 2012 Nissan LEAF system that was benchmarked in FY15. The main reason for the difference is that the Accord power module utilizes a metalized-ceramic substrate and the TIM layers are eliminated in the Accord module.
- FEA models were developed to study the transient performance of 2012 Nissan LEAF, 2014 Accord and two other systems that incorporate a conventional power module design. The simulation results indicate that the 2012 LEAF power module has lowest thermal impedance at a time scale less than one second. This is probably due to the moving of low thermally-conductive materials further away from the heat source and enhancement of the heat spreading effect from the copper-molybdenum plate close to the IGBTs. When approaching steady-state, the Honda system shows lower thermal impedance.
- Thermal Measurement results from the 2015 BMW i3 power electronic system indicate that the i3 IGBT module has significantly lower junction-to-liquid thermal resistance as compared to the other systems. At a flow rate of 12 Lpm, the thermal resistance of the i3 system is only 30% of the Accord system and 15% of the LEAF system.

Nomenclature

A	area
k	thermal conductivity
Q	heat
R"th	specific thermal resistance
Z"th	thermal impedance
T	temperature

Subscripts

j	junction
l	liquid

FY 2016 Presentations/Publications/Patents

1. Moreno, G., Bennion, K., King, C., and Narumanchi, S. "Evaluation of Performance and Opportunities for Improvements in Automotive Power Electronics Systems." The Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, Las Vegas, Nevada, May 2016.
2. Feng, X., Moreno, G., and Bennion, K. "Thermal Performance Benchmarking." 2016 DOE VTO Annual Merit Review, Washington, D.C., June 2016.

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References

1. Burress, T. "Benchmarking of Competitive Technologies." 2012. DOE VTO Annual Merit Review, Washington D.C., May 2012.
2. Burress, T. "Benchmarking EV and HEV Technologies." 2015. DOE VTO Annual Merit Review, Crystal City, VA, June 2015.
3. Burress, T. "Benchmarking EV and HEV Technologies." Oak Ridge National Laboratory, 2014 VTO EDT Annual Report, 2014.
4. Lau, J. H., and Pao, Y. "Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies, 1997." NY McGraw-Hill.
5. MatWeb. "CeramTec SL200B Silicon Nitride." http://www.matweb.com/search/DataSheet.aspx?MatGUID=50f707073d0149218469a887fb0bbf31.
6. MatWeb. "Aleris 55HX Aluminum (5005-h14)." http://www.matweb.com/search/DataSheet.aspx?MatGUID=b8de580814574dda958c8b2a4aebe710.
7. MatWeb. "Overview of Materials for Polyphenylene Sulfide (PPS) with 40% Glass Fiber Filler." http://www.matweb.com/search/datasheet.aspx?matguid=301e3f904d6a43a7922601c9d11ded91
8. Bennion, K., and Moreno, G. "Thermal Management of Power Semiconductor Packages-Matching Cooling Technology with Packaging Technologies." Second Advanced Technology Workshop on Automotive Microelectronics and Packaging, Dearborn, MI, April 2010.

5 Packaging Technologies Research and Development

5.1 Advanced Packaging Technologies and Designs

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Contract No.: DE-AC05-00OR22725

Abstract/Executive Summary

- The project was focused on the development and implementation of advanced packaging technologies for wide bandgap (WBG) semiconductor power modules to accelerate the application of WBG power semiconductor devices in the automotive industry.
- Specific packaging technologies were designed and developed for in-house manufacture of the WBG power modules for automotive inverters and converters, using the latest industrial WBG devices and integrating electrical, thermal, and mechanical functions in a high-density package.
- Innovative packaging technologies and designs were developed for using superior attributes of the WBG devices. The simulations and experimental analyses were performed and validated the advances of the design and technologies. The packaging process development leads to improved manufacturability and high reliability. The in-house-fabricated prototypes successfully demonstrated the advances of the WBG power electronics packages.
- Commercial state-of-the-art silicon carbide (SiC) power modules were analyzed and their limitations examined.
- Working jointly with other projects within the program for development of the systemic power electronics packaging, prototypes for thermal analysis were made and delivered.
- New bond materials and processes were developed and implemented in the SiC modules for advancing power electronics materials research.
- One patent application and one invention disclosure were filed in addition to five publications.

Accomplishments

- Developed a packaging approach of multiple chip-scale packaged gallium nitride (GaN) devices for high mechanical flatness, enabling three-dimensional (3-D) high density assembly. Fabricated and delivered GaN modules for building a 6.6 kW GaN isolation converter in project EDT 054.
- Performed electromagnetic simulation and experimental evaluation of state-of-the-art commercial power modules. Electrical performance limitations of the module packaging have been identified. Technical aspects for further improvements have been suggested.

- Designed and fabricated record-low switching ringing SiC modules. A feature inductance of 1.46 nH in a SiC power module has been realized for the first time. This will allow converter/inverter operation at higher frequencies and low electromagnetic interference (EMI) and, in turn, lower cost and high power density.
- Developed large area bonding process technologies for high reliability SiC modules. New materials and processes push SiC operating temperatures higher and increase the reliability by 3 times.
- Fabricated and delivered SiC planar-bond-all modules to the National Renewable Energy Laboratory team for thermal evaluation. The double-sided larger area bonds increase the area of the thermal path by 40%, allowing reduction of thermal resistance and reduction in cost and increase in power density.
- Established a power cycling method and test bed for power cycling tests of WBG module packaging.

Introduction

Existing automotive inverter designs with silicon power semiconductor modules will likely not meet the DOE EDT 2022 cost, size, and efficiency targets. State-of-the-art power inverters and converters in electric vehicles (EVs) are manufactured by using conventional packaging technologies; however, the electrical, thermal, and thermomechanical performance of these inverters, as well as their manufacturability, is limited. These limitations cause large power losses, low semiconductor operational temperatures (limited to 150°C), high thermal resistance (0.6 $cm^2 \cdot °C/W$), and poor power thermal/temperature cycling capabilities, resulting in low efficiency and high costs.

WBG semiconductors such as SiC and GaN permit devices to operate at much higher temperatures, currents/voltages, and frequencies—making power electronic systems using these materials significantly more powerful and energy efficient than ones made of silicon. They also offer greater efficiency in converting electrical power and operating electric traction drives.

The objective of this project is to address the challenges and barriers to use of WBG technologies for automotive electric drives. This research will develop WBG automotive power modules in inverters/converters through advanced packaging to accelerate their adoption in traction drive systems and achieve the potential superior attributes of WBG power semiconductors: high current density and low losses, fast switching, high temperature operation, etc.

This research will lead to all-inclusive improvements in the performance and manufacturing of power modules for use in inverters/converters as a result of transitioning from silicon to WBG power semiconductors and of innovations in packaging materials, structure, and processing. These comprehensive advances can directly affect the cost, efficiency, reliability, and density of power electronics systems in the electric drives of EVs. The goal of a 40% cost reduction and 60% power density increase in the power module supports DOE EDT 2022 power electronics targets of $3.3/kW and 14.1kW/kg, respectively.

Approach

- Realize the targets of cost reduction, power density increase, and power efficiency improvement through leapfrogging barriers of the existing industrial baseline and bringing innovative, systemic development by advancing technologies that improve technical metrics: thermal resistance (θja), parasitic electrical impedance (Lp, Rp, Cp), thermal expansion coefficient mismatch (ΔCTE), and manufacturability.
- Evaluate state-of-the-art power module packaging technologies through simulation and experimental measurement to examine limitations of the performance of the module packaging and identify technical aspects for further improvements.
- Fabricate prototypes of the all-WBG power modules for automotive inverters and converters by adopting the latest industrial WBG power semiconductor devices in custom designs to take advantage of the superior attributes of WBG power semiconductors.

- Develop innovative power packaging techniques featuring optimized electrical interconnections, highly efficient heat transfer, multifunctional structural integration, high reliability at high temperature operation, and low cost manufacturing.
- Deliver advanced packaging solutions: optimal packaging designs, data on state-of-the-art packaging technologies, and novel processes for cost-effective manufacture of integrated WBG power electronics systems.

Results and Discussion

The development and evaluation of advanced WBG packaging technologies are summarized in the following four sections: GaN power module packaging for charger inverter, evaluation of state-of-the-art power module packaging, ultralow inductance SiC power module packaging, and high reliability packaging technologies. Performance improvements were determined mostly through experimental measurements and simulations, and efficiency, cost, and reliability benefits to power electronics systems were evaluated.

A. Gallium Nitride Power Module Packaging for Charger Inverter

A customized GaN power module was developed as part of another project, EDT 054 (WBG chargers R&D). This all-GaN power module is composed of the latest GaN metal oxide semiconductor field-effect transistors (MOSFETs). The switch units consist of up to three paralleled MOSFETs, and the two coupled H-bridge modules include a maximum 24 devices. The selected GaN MOSFET is chip-scale packaged (the MOSFET die is embedded in the plastic resin case with double-sided metal pads on the planar surfaces). A thermal pad is on the top surface while electrodes [source (S), gate (G), and drain (D)] are all on the bottom side. The dimensions of the package are 9.00 mm (L) × 7.65 mm (W) × 0.54 mm (H). In the packaging design of this all-GaN power converter module, two printed circuit boards (PCBs) are used to bear all the GaN MOSFETs and provide electrical interconnections. Solder bonds join the devices to the board underneath each electrode pad. The other surfaces of the PCBs are designed for assembly of other electronic components. Then the two boards are attached to a liquid-cooled heatsink through tight contacted thermal interface material.

The challenges for packaging of the GaN MOSFETS on board include (1) flip-chip soldering of multiple chip-scale device attachments on the circuitry, (2) alignment of multiple devices to pads on the PCBs, (3) flatness of the multiple devices for attachment to the cold plate, and (4) uniformity in electrical performance of paralleled devices.

For better paralleling, the devices have been sorted based on their electrical performance using a special fixture made in house. Figure 5-1, a photo of the final assembly of multiple devices and PCB board on a hot plate for reflow soldering, displays some of the techniques taken to overcome the difficulties mentioned above. A special mask was designed and fabricated for alignment of multiple devices and pads on the PCBs; it also withstands the soldering temperature (240ºC) and allows placement of a flat cover and weight on top of these thin devices during solder reflow. The assembly is located on the hot plate in an environment-controlled oven to avoid solder defects. A number of GaN power modules for charger converters have been fabricated at the ORNL packaging laboratory with these measures. Figure 5-2 shows two packaged GaN power units (eight MOSFETs each). The power devices are packaged separately on two PCB boards for the upper unit and lower unit in converter assembly. The packages, which meet the design specifications, have been delivered for further testing in the GaN charger prototypes.

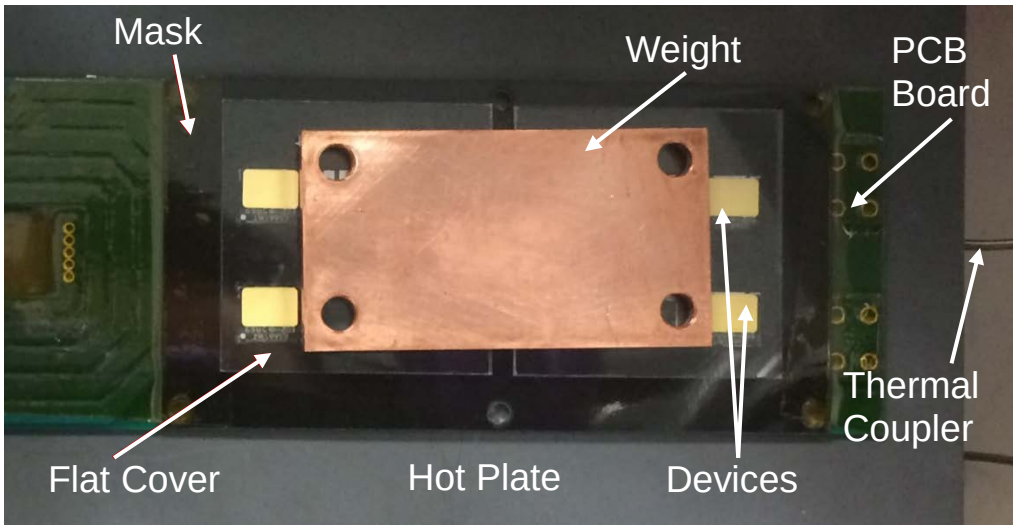


Figure 5-1: Photo of the final assembly of all parts for soldering multiple GaN MOSFETS (devices) on a PCB board on a hot plate in a solder reflow oven to form a power module.

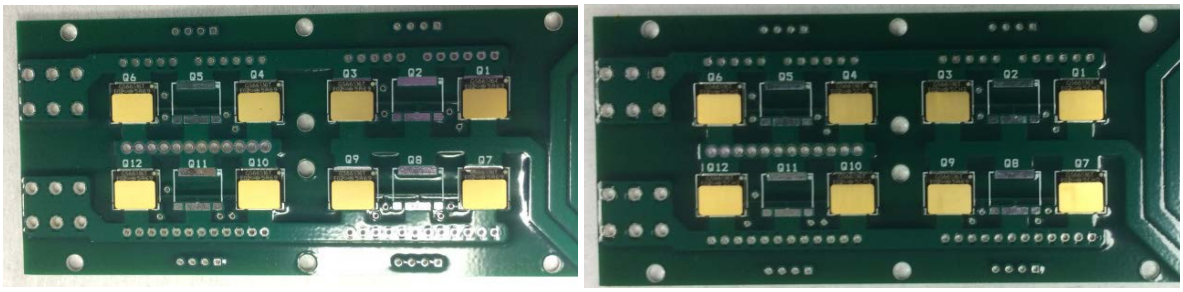


Figure 5-2: Two packaged GaN MOSFET power phase legs (eight MOSFETS each) for assembly of a GaN charger converter (project EDT 054).

B. Evaluation of State-of-the-Art Power Module Packaging

The power converters and inverters are made in different topologies through electrical interconnection of multiple power semiconductor devices by packaging processes. These interconnections, made of electrical conductive materials, bring parasitic electric impedance to the pure semiconductor circuits. The parasitic components have severe effects on switching performance of the power semiconductor devices, leading to large, high-frequency electric spike and ringing during switching transitions. The electric parasitic parameters are among the critical technical metrics used to evaluate and compare packaging technologies. For this study, the power module in a 2013 Toyota Camry Hybrid electric drive system was examined. Figure 5-3(a) is a photo of the unit modules (paralleled insulated gate bipolar transistor and diode) that, when assembled, make a half-bridge, like overlaid electric diagrams. Multiple half-bridge assemblies, which are double-sided cooled by stacked coolers, are electrically interconnected through a bulky copper frame, as shown in Figure 5-3(b). Figure 5-3Figure 5-3(c) illustrates the 3-D model of the modules and interconnections in the assembly. The parasitic impedance is modeled as a lumped element associated with each interconnection section, shown as the electric diagram in Figure 5-3(d). The values of each element were calculated based on the geometry of the electrical interconnection and material properties using electromagnetic simulation software (Ansys Q3D Extractor). It is well known that the inductances, along with the major power commutation loops, CL1 and CL2 in Figure 5-3(d), are the most critical ones for power conversion performance of the inverters and converters. The calculated commutation loop inductance is about 63 nH. It is worth noting that the planar modules themselves offer very small inductance; however, the complex terminals produce much larger inductances (Lp and Ln) than conventional wire bond modules (generally around 35 nH). This can be concluded as one of the major drawbacks of such packages.

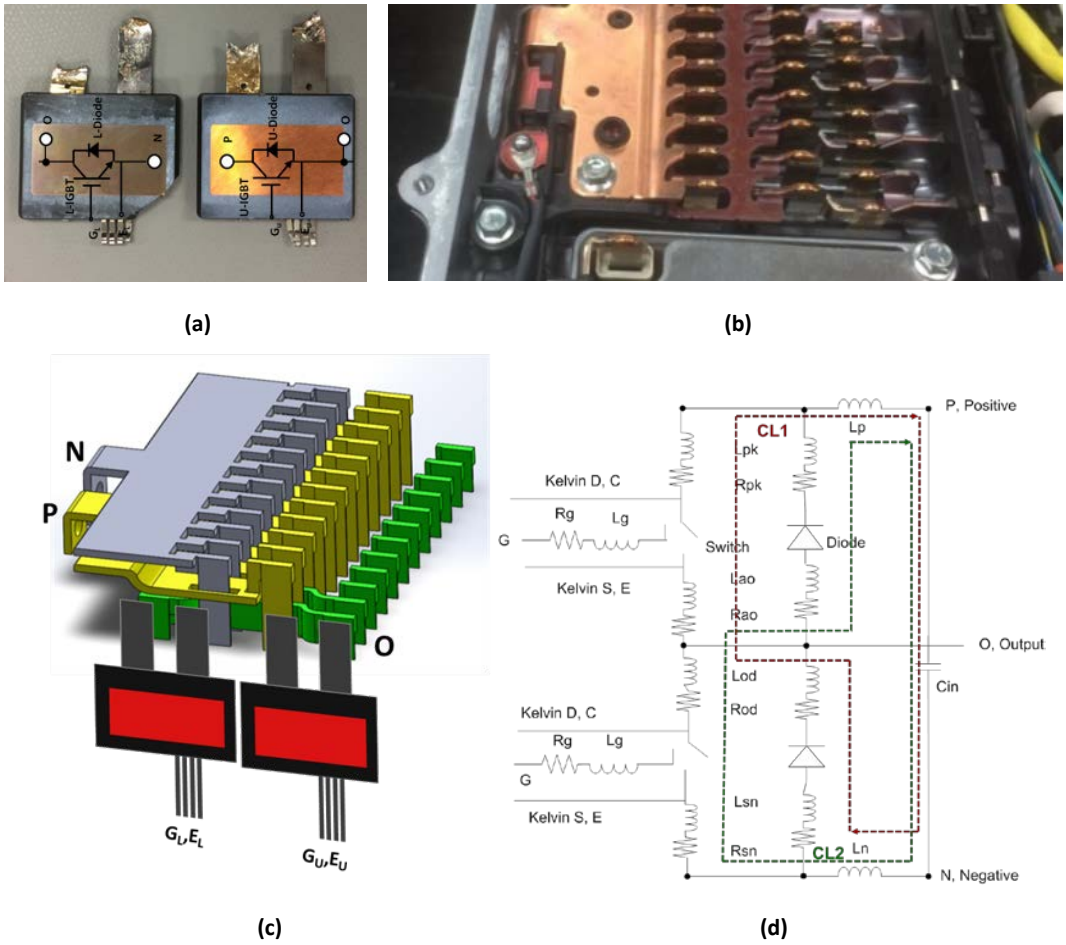


Figure 5-3: Analysis of parasitic inductance in the 2013 Toyota Camry inverter: (a) planar power modules with overlaid electric diagrams, (b) photo of partial inverter with copper terminals, (c) 3-D model of the electrical interconnection in inverter module, and (d) lumped element model of parasitic electric components with illustrated major power commutation loops.

Another evaluation was performed experimentally on a state-of-the-art SiC module, as shown in Figure 5-4. An all-SiC half-bridge module made of CREE's C2M MOSFET (1.2 kV, 13 mΩ) and Z-Rec Diode, is assembled on a specifically designed and fabricated test bed optimized with electrical interconnection and with specific instrumented current sensor and voltage test points. A specific gate drive board is also made to closely connect the module with variable gate resistance. The module is mounted onto a hot plate to elevate its temperature.

The MOSFETs' turn-on and turn-off switching were tested under different operation conditions: the bus bar voltage is fixed at 600 V while the current is from 30 to 100 A; the gate resistor (Rg) is from 0 to 20 Ω (with steps of 5 Ω); temperature is from 25°C to 150°C (at 25°C steps). Figure 5-5 (a) and (b) show the waveforms of the current Id, voltages Vds, Vgs at Tj = 150°C with the gate resistance varying from 0 to 20 ohms. The switching parameters such as rising time (tr), falling time (tf), delay times (tds), dV/dt, dI/dt, as well as their dependence on the test conditions can be extracted. Figure 5-5 (c) presents the dV/dt dependences on both Rg and operation temperature. All these data have been collected and represent the characteristics of this SiC product. Extensive comparisons and further analyses of the data have been performed.

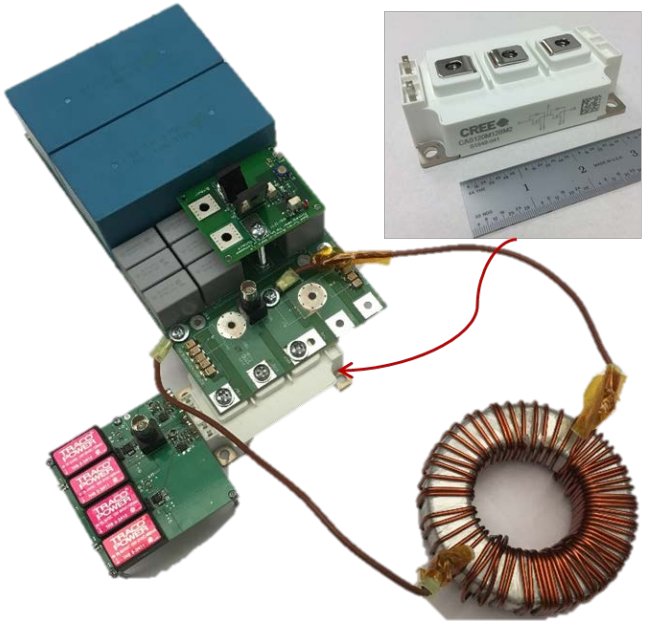
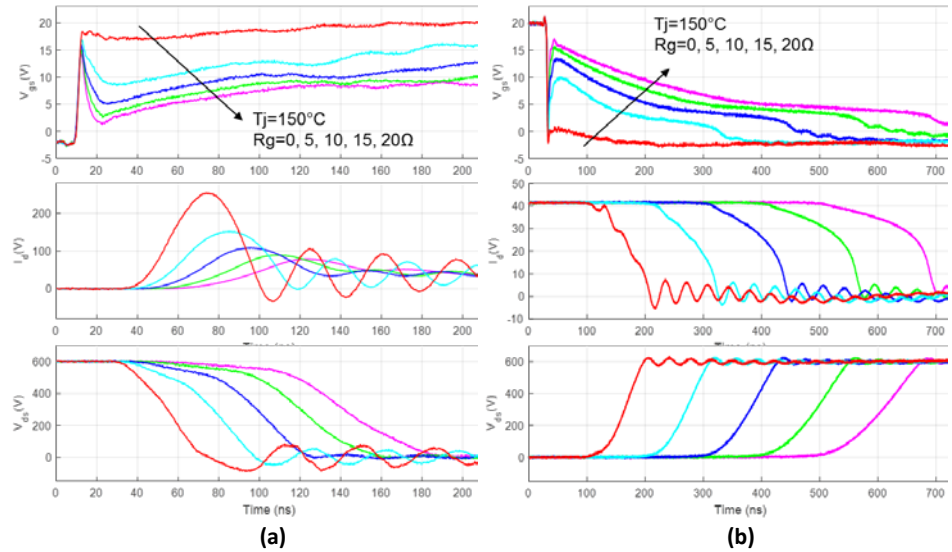


Figure 5-4: The test setup for evaluation of switching performance of a SiC module: CREE's CAS120M12BM2 (upper right corner).



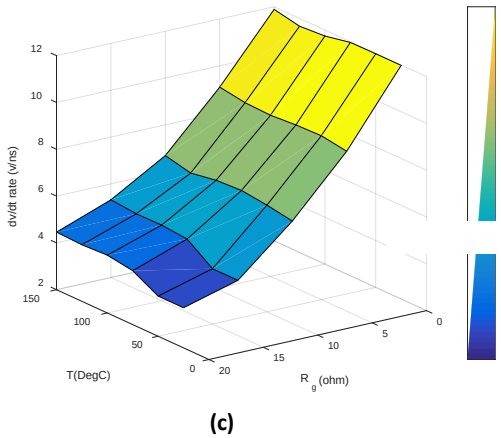


Figure 5-5: Measured switching performance of Cree SiC MOSFET in module CAS120M12BM2: waveforms of the current Id, voltages Vds, Vgs at Tj = 150°C with the gate resistance varying from 0 to 20 Ω [(a) and (b)]; dV/dt dependences on both Rg and operation temperature (c).

C. Ultralow Inductance SiC Power Module Packaging

As discussed above, the parasitic inductances within the module package more severely affect the switching performance of fast devices such SiC and GaN. Therefore, it is important to develop packages for the WBG modules with smaller moderate parasitic inductance, thus ensuring high performance, safe operation of these devices.

Figure 5-6 presents the design and development of an all-SiC half-bridge power module with ultralow inductance. Figure 5-6Figure 5-6(a) shows its electric diagram, with two SiC MOSFET dies and two SiC diode dies paralleled as a switch unit to form a 100 A, 1,200 V SiC phase-leg. Except for power connectors, P, O, and N terminators, the so called Kelvin gate, source and drain pins are added for separation of power loops and drive (signal) loops, which will greatly reduce the electric coupling between them. Figure 5-6(b) presents an aerial view of the designed package with the planar interconnection configuration. Between two direct bond copper (DBC) substrates, the two upper MOSFETs and two lower diodes are arranged on the left lower half of the package and two lower MOSFETs and two upper diodes are placed on another half of the substrate so that the commutation loops CL1 and CL2 are located in a smaller space with the shortest distance, as depicted in Figure 5-6(a).

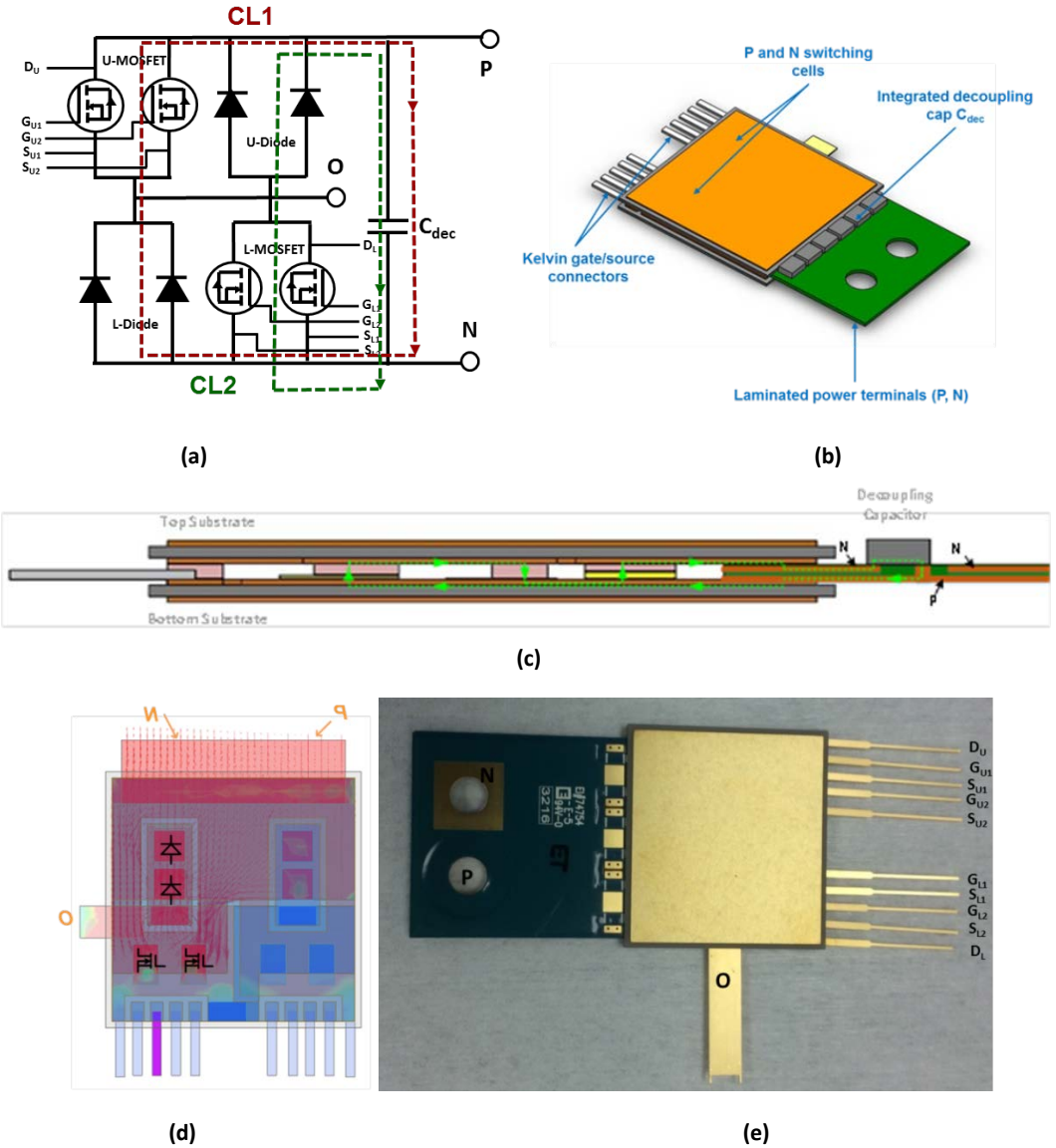


Figure 5-6: Design of an ultralow inductance SiC phase-leg module: (a) electric diagram with regrouped switches; (b) aerial view of the planar package; (c) cross-sectional view of the interconnections and current in commutation loop; (d) current density distribution in the package along a commutation loop; and (e) photo of laminated planar-bond-all package of a 100 A, 1,200 V SiC MOSFET/JBS diode phase-leg power module.

In the package all dies are directly bonded onto the top and bottom substrate by solders. The top and bottom substrates have patterns (such as copper traces) on their inner surfaces for electrical interconnection. The metal shims (spacers) are used to connect the pads on the top and bottom substrates. The signal pins (Ss, Ds, Gs), are arranged on the left side with bond wire connections with the MOSFETs, while the power terminals (P, N) are made of laminated two-layer copper conductors and can be directly mounted between the top and bottom substrates and bonded onto their inner surfaces. The power output pin O is also bonded on the bottom substrate. The laminated P and N terminals provide a "friendly" interface for connection to the capacitor tank of the inverter, leading to tremendous reduction of the stay inductance with the power bus bar compared to that in Figure 5-3(b). The so-called decoupling caps are integrated (mounted) on the P and N terminals, which are designed to compensate for the inductive effects and effectively constrain electric ringing during device switching.

Figure 5-6(c) illustrates the cross-sectional view of a commutation loop. It can be seen that the power terminals P and N are fully and closely laminated. This laminated electric conduction configuration not only shortens the power flowing distance in the package, but also makes use of the electromagnetic cancellation effect to reduce parasitic inductance along the loop. In addition, the decoupling caps are so closely mounted to the devices that the CL1 and CL2 loops can be very small.

Figure 5-6(d) shows the current density distribution during electric power flow along the CL1 loop. It can be seen that the gap between current paths in different directions will offer strong coupling. The final extracted parasitic inductance, by Ansys Q3D Extractor, is 1.46 nH, much smaller than the 35 nH of conventional wire bond modules.

Figure 5-6(e) is a photo of the 100 A, 1,200 V SiC phase leg power module prototype fabricated from this design. All eight SiC dies were bonded between two DBC substrates by solder from both the top and bottom surfaces [see Figure 5-6(c)]. At the same time, the laminated power terminals P and N (on the left side) and O (on the bottom side) and signal pins Gs, Ss, Ds, are also mounted onto the DBC substrates. A soldering process was used to form the planar bonds. It offers high electrical conductivity and easy processing. The final package dimension is 40 × 37 × 2 mm, excluding the terminals and pins.

The parasitic inductance was measured using a specially built power switching test system to experimentally test electrical performance of the devices in the package. Figure 5-7Figure 5-7(a) is a photo of the experimental setup with the module connected to the power stage and gate drive board. Figure 5-7Figure 5-7(b) illustrates the electric diagram of this test circuit. With fixed bus bar voltage, the gate drive supplies two continuous pulses (from −2 V to 15 V) to the MOSFET, adjusts the widths of the pulse to the power inductor, and controls the current going through it (load current). Thus, the current and voltage variations during turn-on and turn-off can be picked up through current sensor (shunt) and voltage test points (Bayonet Neill-Concelman connectors) instrumented in the modules and test boards. The parasitic inductance can be extracted simply by the ratio of the overshoot voltage over the current slope (dI_d/dt). Note that the overshoot voltage at different test points is dependent on the sectional inductances included in the test loop. For example, in the graph of Figure 5-7(c), the overshoot voltage (ΔVpn) of the Vpn (blue) is caused by parasitic inductances Lstray 1 and Lstray 2 [Figure 5-7Figure 5-7(b)], while the voltage Vds (between Kelvin D and S terminals) overshoot (ΔVds) is caused by all elements in the loop, Ld, La, Lk, Lp, Ls, and Ln, in addition to Lstray 1 and Lstray 2. Thus, the module's total internal inductance can be calculated based on the difference between Vds and Vpn. Specifically, the extracted value based on the test in Figure 5-7(c), is 3 nH. Furthermore, the designed decoupling caps are mounted on the laminated terminals as shown in Figure 5-6Figure 5-6(b), and the voltages Vpn and Vds change greatly as illustrated by the waveforms shown in Figure 5-7(d). The ringing of Vpn has been completely eliminated. The ringing of Vds has been reduced to only half magnitude. The reason is that the commutation loop has been shrunk to the path formed by internal devices and the decoupling caps (Cdec), excluding effectively the Lp and Ln associated with power terminals. The internal inductance calculated based on this measurement is 1.5 nH, in good agreement with the simulation. This is a record-low value compared to other counterparts.

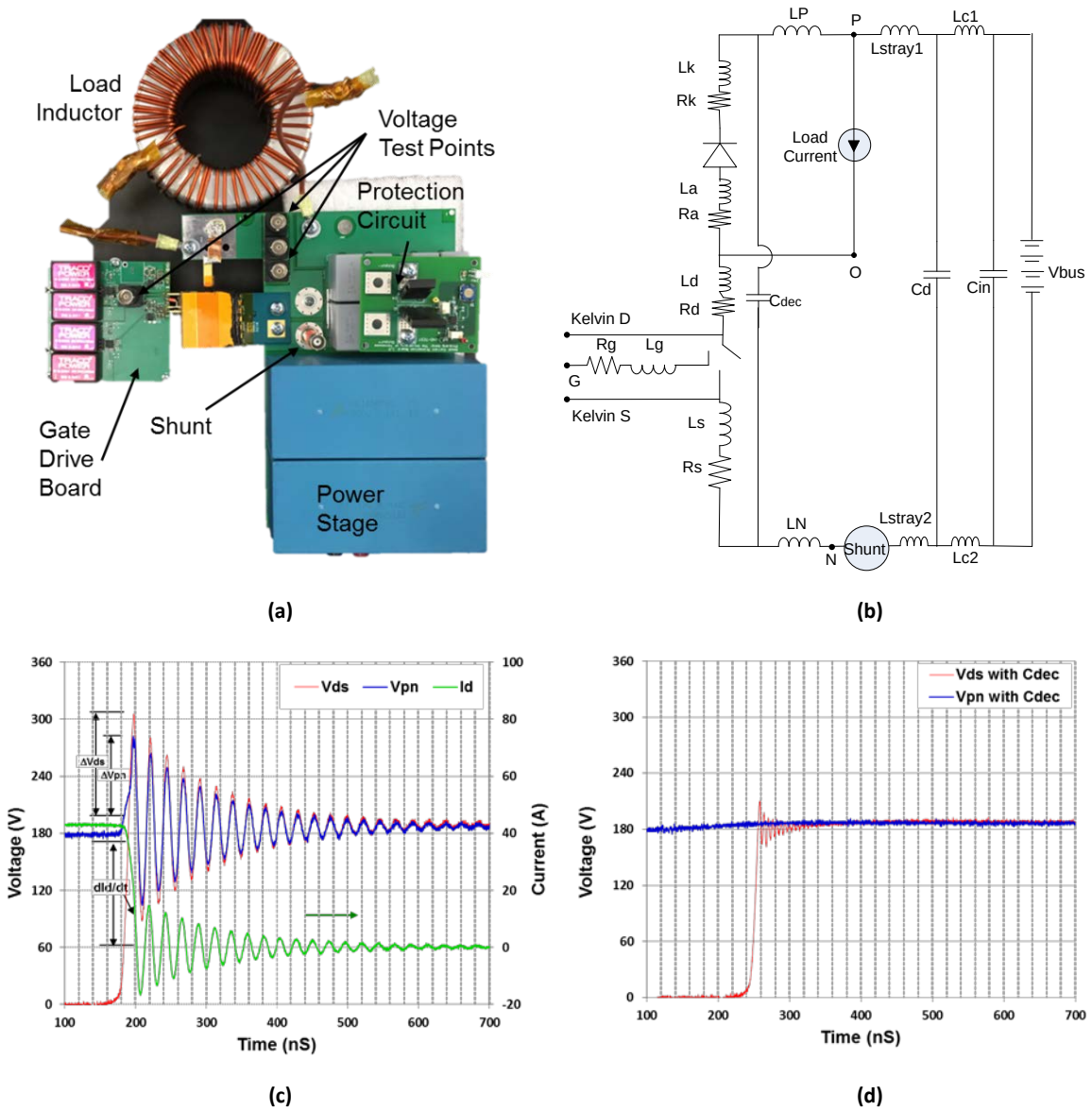
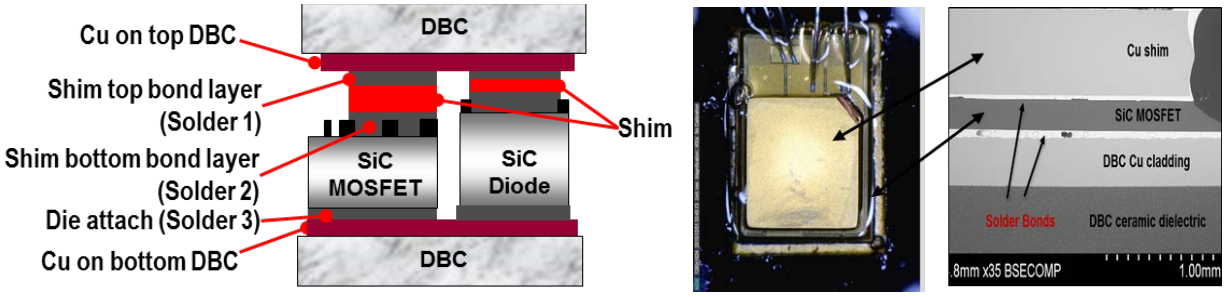


Figure 5-7: Test of the electrical performance of packaged modules: (a) experiment setup; (b) electric diagram of the test circuit (c) typical waveforms of switch turning off; and (d) waveforms with added decoupling caps.

D. High Reliability Packaging Technologies

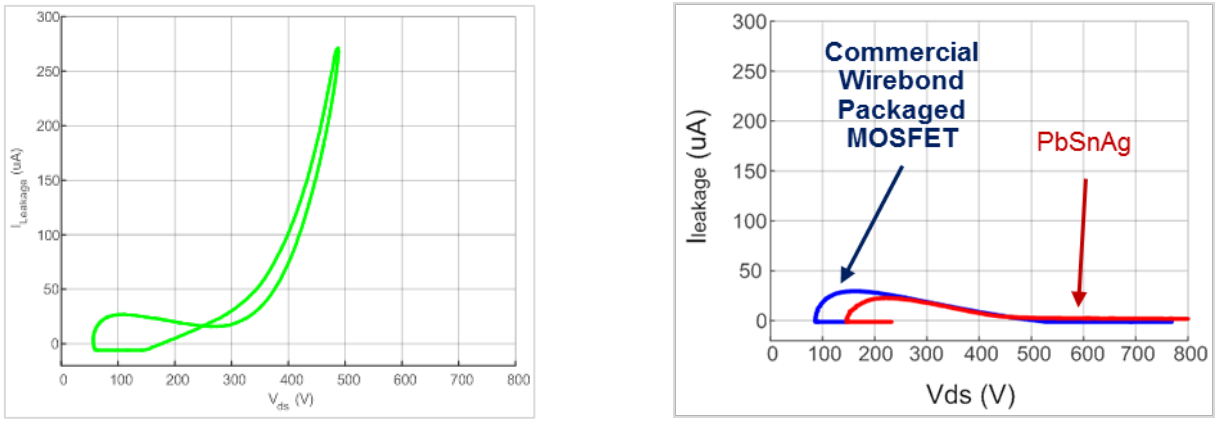
The planar bonding packaging implies that both the tops and bottoms of the device dies are attached to the metal pads (electrically conductive) on the power substrates such as DBCs. Figure 5-8(a) is a cross-sectional diagram of a SiC MOSFET and a diode in parallel in such a package, where the shims on each die with different thickness are inserted between the top surface and the top substrate, and the whole package is joined together by three-layer solders. The shims compensate for the thickness mismatch among different devices. Figure 5-8(b) shows photos of a SiC MOSFET die attached on a DBC substrate with a shim bonded on top, while the tiny wires are bonded onto the small gate and source pads for Kelvin connectors.



(a) (b)

Figure 5-8: Planar bond of SiC dies in package: (a) Cross-sectional view of a SiC die bonded onto a DBC substrate through shims; (b) photos of a shim bonded on SiC MOSFET.

To facilitate the high-temperature operation capability (>200ºC) of the SiC devices, higher melting point solders were chosen for the three-layer bonding. The first tested solder was gold-tin (AuSn), a eutectic alloy with a melting point of 280ºC. However, an unexpected higher leakage current of the SiC MOSFET (at high voltage blocking state) when a copper shim is bonded on top as shown in Figure 5-9(a), was observed. The normal leakage current of this device is shown in Figure 5-9Figure 5-9(b), which depicts a commercial wire bond packaged MOSFET. This degradation in leakage current was briefly attributed to the residual mechanical stress induced during cooling down of solder reflow due to the large difference in the coefficient of thermal expansion (CTE) between copper and SiC. This conclusion has been indirectly proven by additional experiments. First, a thinner copper shim was used, and the degradation was very minor. Second, the AuSn solder was replaced by a lead-tin-silver (PbSnAg) solder (noneutectic, melting points 287°C–296°C). The leakage current measurement is shown in Figure 5-9(b), which corresponds well with the wire-bonded one. The reason is that this solder has a modulus of elasticity (Young's modulus) of 13.8 GPa, smaller than the 74 GPa of the AuSn solder; thus it releases the residual stress through its deformation in the final stack. Furthermore, a new alloy (with close CTE, 7 ppm/C to SiC) was used to replace the copper ones in the AuSn solder bonding package, and the degradation of the leakage current was eliminated.



(a) (b)

Figure 5-9: Leakage current of SiC MOSFET in different packages: (a) AuSn soldered copper shim; (b) wire-bonded package and PbSnAg soldered shim.

As discussed above, although the impacts of the larger area metal attachment on electrical performance were eliminated by changing the materials in the package, the mechanisms behind these phenomena have not been intensively investigated. Further studies on this topic are necessary to fully understand fundamentals related to the reliability of newly developed WBG devices.

Sintered silver layers are well known to be a superior die attachment (bonding) compared to solder layers for WBG power module packaging. It offers much better electrical; thermal; and, especially, thermomechanical properties.

In recent years, intensive research has been conducted on the process technologies for in situ sintering of nano-silver pastes for SiC device packaging. Figure 5-10 presents some results of this research. Figure 5-10(a) shows a cross-sectional view photo of a SiC diode die attached to a DBC substrate. A good bond layer was formed between die and substrate by using optimized processing parameters. However, silver outflow from the bond layer was observed. It was the result of a little pressure on the die when it was placed on the wet silver paste before sintering. For improving the accuracy of the die attachment and preventing any potential electrical defaults, a special pro-bake processing was developed that ensures maintaining the printed geometry and realizing successful no-pressure sintering. Figure 5-10(b) shows a broken interface at the bond layer. Uniform sintered silver residues can be seen on both substrate and die surfaces. Furthermore, as shown in Figure 5-10(c), three silver layers replace all solder layers [shown in Figure 5-8Figure 5-8(a)] to form a planar package with the SiC diode. Figure 5-10(d) is a photo of the sheared off shim bottom bond layer (sintered Ag 2) from one of these three-silver-layer bonded packages.

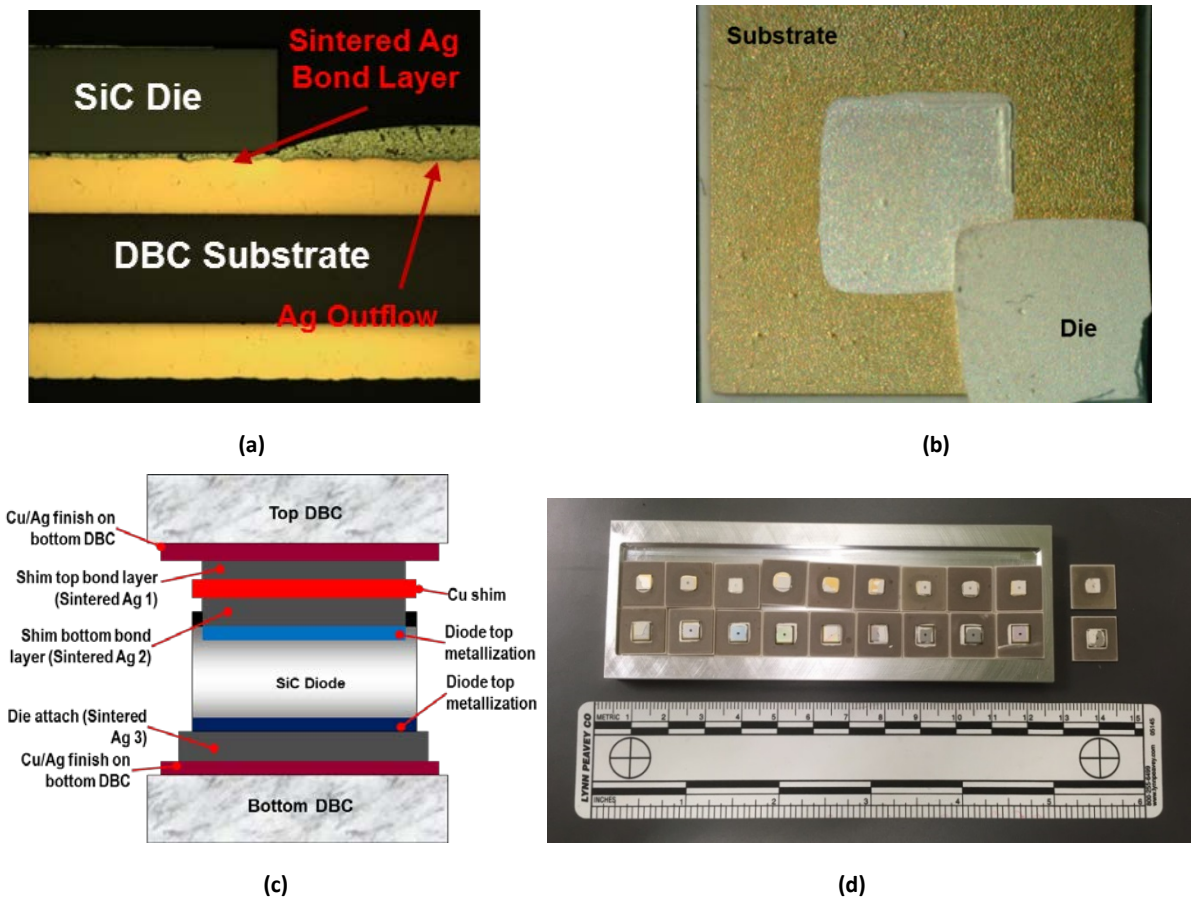


Figure 5-10: Experimental studies of silver sintered die bonds: (a) cross-sectional view of sintered silver bond of SiC die on DBS, (b) broken interface of bonded die on DBC, (c) three bond layers in planar package, and (d) photo of sheared off samples.

In experiments, the shear strength to break off the bond layers was measured and is summarized in Figure 5-11. It indicates that the die attach (sintered Ag 3) is the strongest bond with more than 50 MPa of shear strength. The shim top bonds (sintered Ag 1) are in the range of 15 to 25 MPa, while the shim bottom bonds (sintered Ag 2) are mainly in the 10 to 20 MPa range. The difference is attributed to the finishing metallization on each bonding surface. The finishing metallization is silver on the substrate; gold on all surfaces of the shim; and aluminum on the top of the SiC diode die, with silver on the bottom of it. Thus the sintered Ag 3 layer bonds both surfaces with silver finishing. The sintered Ag 2 bonds surfaces with silver and gold, while the sintered Ag 1 bonds surfaces with silver and gold. From these experiments, a conclusion can be drawn that silver metallization produces the strongest sintered silver bond, gold metallization produces acceptable bonds, and aluminum produces poor bonds.

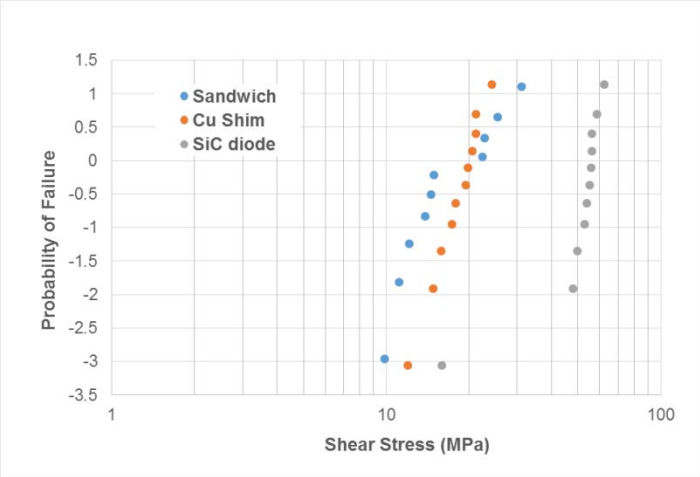


Figure 5-11: Shear strength of three bond layers.

Conclusions and Future Directions

Focusing on achieving a 40% cost reduction and 60% power density increase to facilitate DOE EDT 2022 power electronics targets ($3.3/kW, 14.1 kW/kg, 13.4 kW/L), the R&D on advanced packaging design and technology demonstrates the following.

- Specially designed packaging technologies for fabrication of multiple device GaN power modules will allow an increase of 30% in the power density of a charger converter.
- Limitations of state-of-the-art industrial packages would prevent achievement of the superior performance of WBG devices.
- Ultralow inductance designs and prototypes demonstrated a record-low switching ringing SiC module that will greatly enhance the advantages of using WBG in inverters and converters.
- Optimized area bonding technologies significantly improved the high-temperature reliability of SiC packaging for WBG power modules.

The achievements fulfill greatly the project objectives and the developed WBG packaging technologies result in leapfrogging barriers of existing industrial baseline and bring innovative, systemic development to electric drive systems

Future works include integration of these advanced packaging designs and technologies into building up of WBG systems and work together with industry to transfer them to manufacturers.

FY 2016 Presentations/Publications/Patents

Presentations/Publications

1. Zhiqiang Wang, Xiaojie Shi, Leon M. Tolbert, Fred Wang, Zhenxian Liang, Daniel Costinett, and Benjamin J. Blalock, “Temperature-dependent short-circuit capability of silicon carbide power MOSFETs,” *IEEE Transactions on Power Electronics*, **31**(2), pp.1555–1566 February 2016.
2. Fei Yang, Zhenxian Liang, Zhiqiang Wang, and Fred Wang, “Parasitic inductance extraction and verification for 3D planar bond all module,” presented at the International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM), June 13–15, 2016, Raleigh, North Carolina.
3. Zhenxian Liang, “Integrated double sided cooling packaging of planar SiC power modules,” presented at the Seventh Annual IEEE Energy Conversion Congress and Exposition (ECCE 2015), September 20–24, 2015, Montreal, Canada.

4. Zhenxian Liang, “Survey of high density power electronics packaging technologies,” presented at the United States Council for Automotive Research LLC, U.S. DRIVE Electrical and Electronics Technical Team meeting, July 21, 2016.
5. Zhenxian Liang, “Advanced packaging technologies and designs,” presented at the DOE Vehicle Technologies Office 2016 Annual Merit Review, June 7, 2016, Washington, DC.
6. Zhenxian Liang, “Advanced packaging technologies and designs,” presented at the United States Council for Automotive Research LLC, U.S. DRIVE Electrical and Electronics Technical Team meeting, April 26, 2016.
7. Zhenxian Liang, “Power packaging reliability test plan,” presented at the United States Council for Automotive Research LLC, U.S. DRIVE Electrical and Electronics Technical Team meeting, February 25, 2016.
8. Zhenxian Liang, “Integrated packaging of SiC power modules,” presented at the 3rd IEEE Workshop on Wide Bandgap Devices and Applications (WiPDA), November 2–5, 2015, Blacksburg, Virginia (panelist presentation).

Patents and Invention Disclosures

1. Zhenxian Liang, “Integrated packaging of multiple double sided cooling planar bond power modules,” US Patent Application 62/167,371, filed for ID-3211, May 20, 2016.
2. Zhenxian Liang, Fei Yang, and Fei Wang, “Ultra-low parasitic inductance planar power module packaging,” Invention disclosure 201603720, DOE S-138,365, August 15, 2016.

5.2 Performance and Reliability of Bonded Interfaces for High-Temperature Packaging

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Abstract/Executive Summary

Current generation automotive power electronics packages utilize silicon devices and lead-free solder alloys. To meet stringent technical targets for 2020 and beyond (for cost, power density, specific power, efficiency, and reliability), wide-bandgap devices are being considered because they offer advantages such as operation at higher frequencies, voltages, and temperatures. Traditional power electronics packages must be redesigned to utilize the full potential of wide-bandgap devices, and the die- and substrate-attach layers are key areas where new material development and validation is required. Present solder alloys do not meet the performance requirements for these new package designs while also meeting cost and hazardous substance restrictions.

Sintered silver (Ag) promises to meet the needs for die- and substrate-attach interfaces but synthesis optimization and reliability evaluations must be completed. Sintered Ag material was proposed as an alternative solution in power electronics packages almost 20 years ago. However, synthesis pressure requirements up to 40 MPa caused a higher complexity in the production process and more stringent flatness specifications for the substrates. Recently, several manufacturers have developed sintered Ag materials that require lower (3–5 MPa) or even no bonding pressures.

Degradation mechanisms for these sintered Ag materials are not well known and need to be addressed. We are addressing these aspects to some extent in this project. We are developing generalized (i.e., independent of geometry) J-Integral versus cycles-to-failure relations for sintered Ag. Because sintered Ag is a relatively new material for automotive power electronics, the industry currently does not have a good understanding of recommended synthesis parameters or expected reliability under prescribed conditions. It is an important deliverable of this project to transfer findings to industry to eliminate barriers to using sintered Ag as a viable and commercialized die- and substrate-attach material. Only a few manufacturers produce sintered Ag pastes and may consider some processing conditions as proprietary. It is the goal of this project to openly explore and define best practices in order to impact the maximum number of power electronics module manufacturers and suppliers.

Accomplishments

- Modeled strain energy density and J-Integral values for sintered coupons with round and 50-mm x 50-mm geometries under thermal cycling conditions.
- Synthesized and shear tested initial samples for mechanical characterization of sintered Ag. Material properties gathered are replacing bulk silver material properties to more accurately model the interface structure.

Introduction

Standard packaging technologies have limited the advancement of automotive power electronics modules toward designs that promise higher performance and reliability. The drive toward reduced cost, weight, and volume of components in electric-drive vehicles has led to increased performance demands on power electronics modules. Increased power densities and larger temperature extremes reduce lifetimes for traditional power electronics packages and require new materials and manufacturing processes to be utilized. Before new technologies can be introduced into commercial products, their reliability must be evaluated and quantified.

Current power electronics packages utilize silicon devices and lead-free solder alloys within their construction. As package designs transition to wide-bandgap devices, interface materials must improve to fully utilize the capabilities of these new devices [1-6]. Current solder alloys exhibit creep effects when subjected to elevated temperatures and cannot operate at temperatures as high as 200°C. The operating ranges of several currently used interface materials are shown in Figure 5-12.

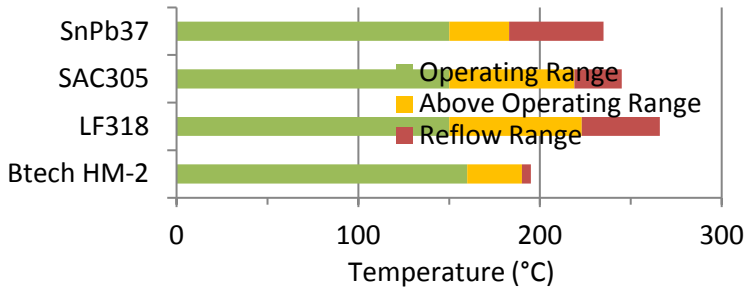

Figure 5-12: Operating range of common interface materials.

Research efforts for high-temperature bonded interface materials can be roughly classified into three categories: Ag sintering, high-temperature soldering, and transient liquid phase (TLP) sintering. The advantages and disadvantages to these processing technologies are summarized in Table 5-1.

Table 5-1: Emerging die- and substrate-attach processes

Process	Advantages	Disadvantages
Ag sintering	High thermal conductivity, highest operating temperature	High processing pressure, material cost
High-temperature soldering	Similar to current soldering procedures	High processing temperature, higher residual stresses, material cost
TLP sintering	Minimal bonding pressure	Processing time, navigating phase diagrams

Some solder alloys have been developed for high-temperature operation, but face cost limitations (e.g., gold alloys) or do not meet Restriction of Hazardous Substances standards (e.g., high-lead alloys). Additionally, solder alloys must always be processed at temperatures higher than their desired operating temperature because their reflow temperatures are equivalent to their processing temperature. This imparts higher residual stresses onto the devices and insulating substrates during processing. Some power electronics module suppliers are evaluating high-temperature solders as a “drop-in” replacement to previously used solder alloys and acknowledge the higher associated material costs.

TLP sintering involves an assembly or paste of low- and high-melt materials. Processing occurs at low temperatures (250°C–300°C) where the low-melt component material diffuses into the high-melt material to form intermetallic compounds. These intermetallic compounds will only re-melt at temperatures much higher

than the processing conditions (400°C–600°C). Toyota Research Institute of North America has several publications on the development of nickel-tin (Ni-Sn) TLP bonding for automotive power electronics. The University of Maryland's Center for Advanced Life Cycle Engineering is working to develop Ni-Sn and copper-tin (Cu-Sn) TLP bonding systems while Ames Laboratory has developed a Cu-Ni TLP process.

Sintered Ag material was proposed as an alternative solution in power electronics packages as far back as 20 years ago. To reduce synthesis temperatures to below 300°C, the concurrent application of pressure up to 40 MPa onto the package or sintered Ag bonded interface material was originally advocated. However, this caused a higher complexity in the production process and more stringent flatness specifications for the substrates. Recently, several manufacturers have developed sintered Ag materials that require lower (3–5 MPa) or even no bonding pressures. Virginia Tech, Heraeus, Henkel, and Kyocera have developed these materials. Semikron currently has production power electronics using sintered Ag as the die-attach layer. Large-area substrate attachment, as well as low-pressure synthesis, requires additional research and development for power electronics module suppliers to transition to sintered Ag. Prior work at NREL and Oak Ridge National Laboratory has demonstrated the promise of the processing technology, but a comprehensive evaluation of all processing variables is needed to demonstrate best practices to industry.

Approach

Finite element simulations in ANSYS were conducted to obtain the desired modeling parameters to develop a predictive lifetime model for sintered Ag. The two parameters of interest are strain energy density and J-integral. Strain energy density is calculated as the time integral of product of stresses and incremental strains at any given node, and has been identified as a suitable parameter for predictive lifetime models [7].

In the previous year, J-integral [8] was identified as the fracture mechanics parameter to be computed using finite element analysis. J-integral, a contour integral around the crack tip, is a convenient parameter for crack tip studies mainly because of its path-independent nature. However, it has to be noted that the path independence of J-integral for elastic-plastic materials holds only under certain circumstances, such as when the material behavior can be described based on deformation theory of plasticity or when the material is subjected to purely monotonic loading. Under such circumstances, elastic-plastic materials can be idealized as non-linear elastic materials and the J-integral effectively characterizes the crack tip field parameters. A few researchers have proved that the incremental theory of plasticity mimics the deformation theory of plasticity, but only when the loading is proportional. Nevertheless, under the incremental theory of plasticity, the path-dependent nature of J-integral becomes less pronounced with successive contours around a crack tip and exhibits a converging trend [9]. This converged value can be considered as a valid parameter that defines the crack tip field. The relevance of parameters computed numerically can be justified only after developing a model fit with experimental results, and determining the accuracy of that fit in predicting lifetime of sintered Ag samples tested under different loading conditions.

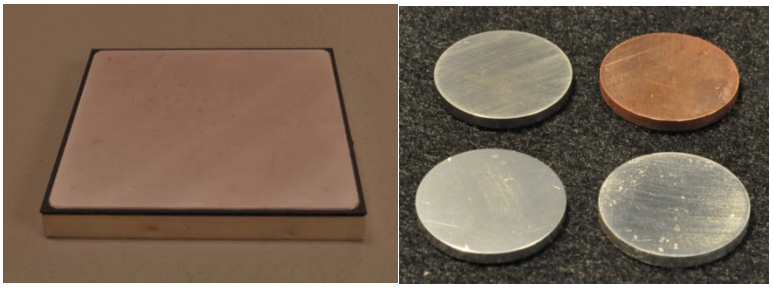

Figure 5-13: A) 50-mm x 50-mm sample (left), and B) copper and Invar coupons (right)

Simulations were performed on both 50-mm x 50-mm samples and round coupons shown in Figure 5-13A and Figure 5-13B, respectively. For a given configuration, multiple simulations with decreasing bond pad areas were run to simulate crack propagation. Thermal cycle temperature loads for round coupons were -40°C and 170°C, whereas the 50-mm x 50-mm samples were subjected to a thermal cycle between -40°C and 150°C. Strain energy density results were volume-averaged over the entire circular bond pad region of round coupons to avoid singularity issues. For 50-mm x 50-mm sample simulations with crack feature inserted into the model, it was found that J-integral results converged to within 5% after six contours around the crack front.

Round Coupons

The round coupon samples were of three different types—copper-Invar, copper-copper, and Invar-Invar—all with sintered Ag as the joint. Figure 5-14 shows a plot of strain energy density per cycle values of copper-Invar samples with varying bond pad diameters. A red triangle dot indicates that the result corresponds to an actual sample that was tested experimentally. Reading the graph from right to left, it can be inferred that a reduction in the bond pad diameter results in higher values of strain energy density per cycle, but only up to a certain diameter. Beyond that point, strain energy density decreases slightly. For any bond pad diameter, strain energy density is more concentrated on the outer regions and decreases toward the center. Also, a detailed analysis shows that strain energy density is predominant in the out-of-plane shear planes, as shown in Figure 5-15.

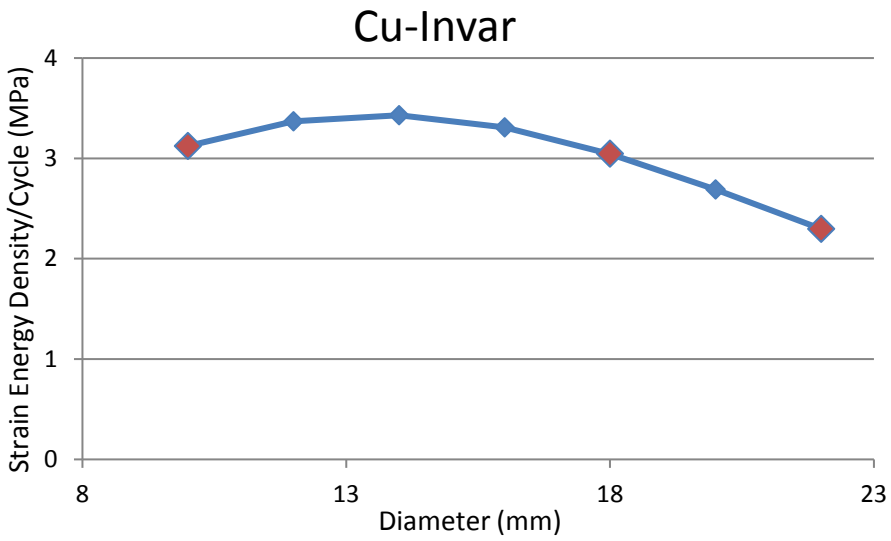

Figure 5-14: Strain energy density per cycle results of copper-Invar samples

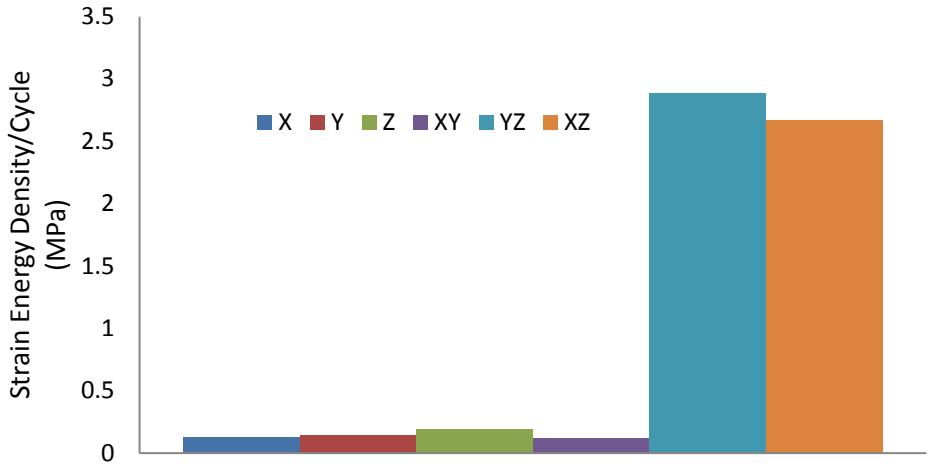

Figure 5-15: Strain energy density per cycle components of an element split in six directions

Figure 5-16 shows a plot of strain energy density per cycle values of copper-copper and Invar-Invar bonded samples with varying bond pad diameters. Although not as severe as the global coefficient of thermal expansion (CTE) mismatch between the adherend coupons, the local CTE mismatch between Invar and sintered Ag results in a higher strain energy density for Invar-Invar samples than copper-copper samples. As compared to copper-Invar samples, bond pad diameter variation does not have any impact on the strain energy

density of sintered Ag due to little CTE mismatch in the out-of-plane directions. Hence, changing an in-plane dimension of the joint will not affect the strain energy density.

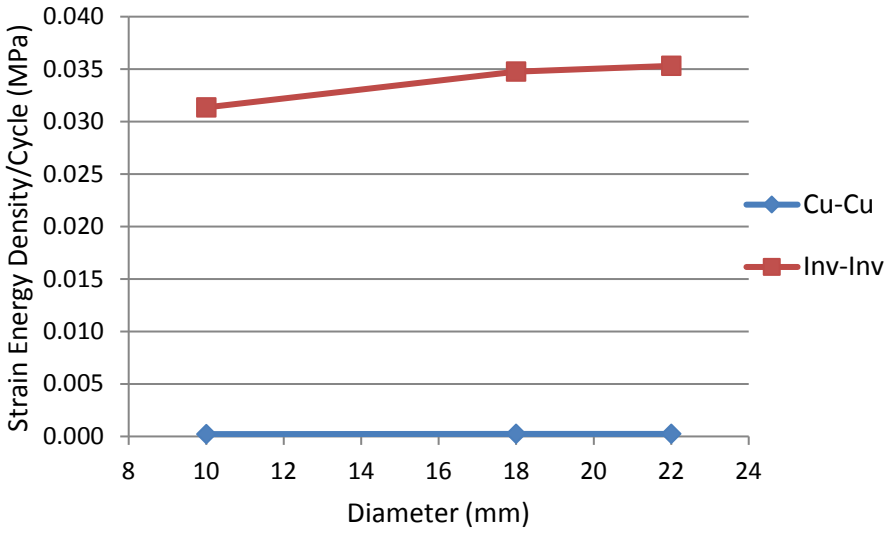

Figure 5-16: Strain energy density per cycle results of copper-copper and Invar-Invar samples

50-mm x 50-mm

Samples measuring 50 mm x 50 mm were also included in the modeling study as C-mode scanning acoustic microscopy images of the sintered Ag interface within the sample were already available from a previous project. A non-linear finite element method analysis showed that higher values of strain energy density occur at the corner regions of the sintered Ag joint and is where cracks are likely to initiate. A meshed model of the geometry with crack feature (not visible) inserted in the corner region is shown in Figure 5-17a. A higher mesh density is implemented in the corner regions around the crack front to adequately capture the effect of crack front on the stress and displacement fields. The focus was mainly on calculating the J-integral values with these samples. Six concentric contours were created around the crack front (red line) for evaluating the J-integral values as shown in Figure 5-17b. The Anand model was used as the material constitutive model and the model parameters were obtained from the literature [10]. Multiple simulations with reduced bonded areas were conducted as an indirect way of simulating crack propagation, as shown in Figure 5-18.

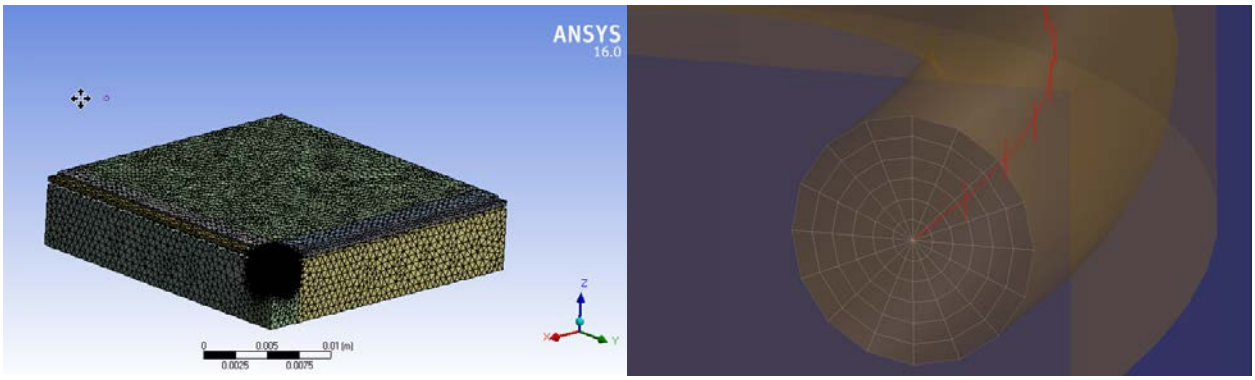

Figure 5-17: Quarter-symmetric model of 50-mm x 50-mm sample with a) tetrahedral mesh (left), and b) J-Integral contours shown (right)

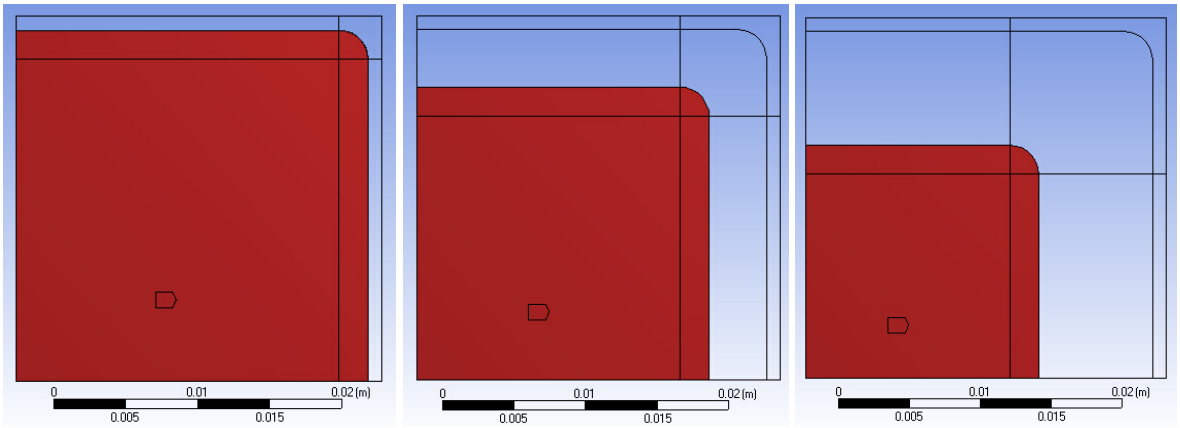

Figure 5-18: Samples measured 50 mm x 50 mm with reduced bonded areas shown by the red region, where joint area is a) 48.4-mm x 48.4-mm (left), b) 40.4-mm x 40.4-mm (center), and c) 32.4-mm x 32.4-mm (right)

Thermal cyclic loading was repeated for four cycles before the results converged. After solution, a contour plot of J-integral along the crack front was obtained in the post processing phase. Analysis of J-integral values at the crack front nodes from each contour show that path dependence becomes less pronounced with each successive contour and is within 5% to 6% after six contours. In order to avoid any singularity issues, J-integral values from the sixth contour were then averaged along the crack front nodes. Also, J-integral, being a cumulative value, keeps increasing with each thermal cycle. Hence, J-integral over a thermal cycle range was obtained and taken as the final output. Figure 5-19 shows a plot of J-integral along the crack front.

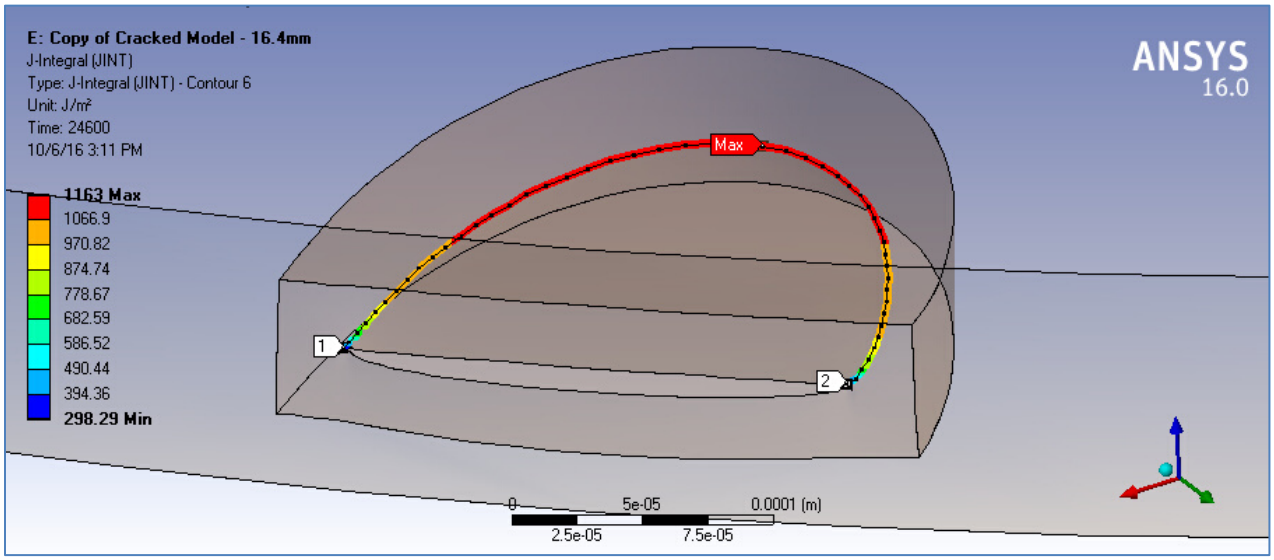

Figure 5-19: J-integral plot

The obtained values of the J-integral along the crack contour are compiled in Table 5-2.

Table 5-2: J-integral/cycle for 50-mm x 50-mm samples

Bond Pad Area	J-Integral/Cycle (J/m^2)
48.4 x 48.4	114.1
40.4 x 40.4	188.7
32.4 x 32.4	222.2

Strain energy density per cycle results were also calculated for the 50-mm x 50-mm samples. Simulations were performed without the crack feature for different bond areas, and strain energy density results were volume-averaged over the corner fillet region. These results are plotted in Figure 5-20, shown below.

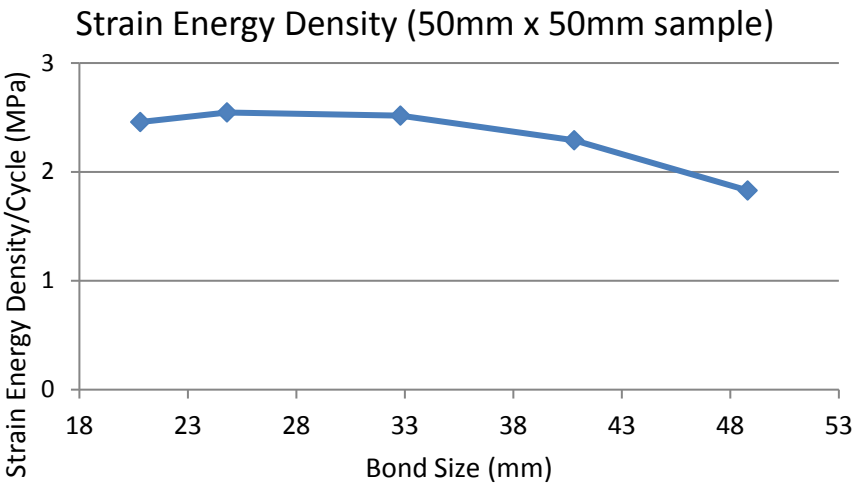

Figure 5-20: Strain energy density results for 50-mm x 50-mm samples

Mechanical Testing

Prior testing found that poor bonding of the Cu-Invar round samples due to the intended CTE mismatch quickly led to separation of the test coupons [6]. This was consistently shown for 10-, 18-, and 22-mm bond pad diameter samples, with no samples reaching 500 cycles. Several Invar-Invar samples also failed, with two of the three failures occurring in the samples that were sintered for a longer duration. New samples were sintered for shear testing in the hopes that improved shear strength will lead to stronger round coupons. While the mechanical properties of bulk Ag are well known, variations in paste manufacture, drying procedure, and sintering method can all lead to significant differences in properties for sintered Ag. To obtain the needed material properties for accurate modeling of the interface, shear testing of the material was completed. Three Cu coupons comprise the shear test sample, all 12.7-mm x 12.7-mm square. The middle coupon is 5-mm thick while the outer coupons are 1.8-mm thick. The desired bonded interface material is used to adhere the three coupons together into a test sample. This sample is placed in a shear test fixture that supports the outer coupons while applying a load to the middle coupon. The symmetry of the test samples allows for the interface layers to be loaded in a pure shear fashion. A test sample and the shear fixture are shown in Figure 5-21. The shear fixture is placed within an Instron 5966 dual column testing system that can be configured with 100 N and 10 kN load cells. The environmental chamber has a temperature range from -100°C to 350°C for capturing temperature-dependent material properties. A noncontact video extensometer is used for strain measurements. The Instron mechanical testing system is shown in Figure 5-21.

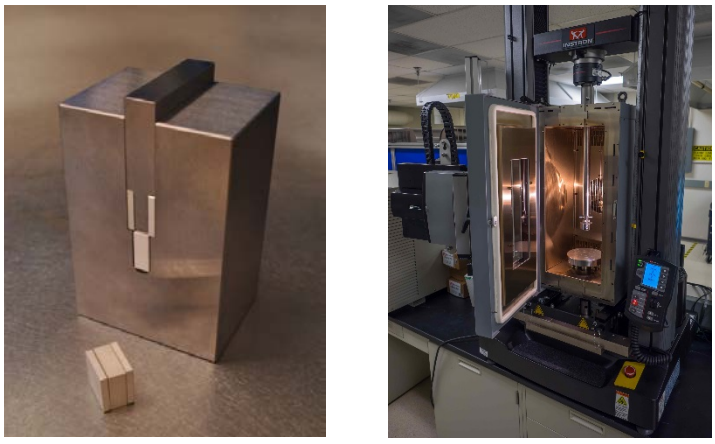

Figure 5-21: Test sample and shear test fixture (left) and Instron mechanical testing system (right)

To validate the shear testing procedure, $Sn_{63}Pb_{37}$ solder was used to synthesize several samples. Solder preforms were placed between the test coupons along with a few glass beads to ensure planarity of the bond line. After a solder reflow process was completed, the bond layers were inspected by acoustic microscopy. Only samples with minimal voiding were selected for shear testing. After screening, samples were placed within the shear test fixture and sheared at a strain rate of 0.02. The video extensometer measured displacement change of the fixture and the testing system recorded the compressive loading. Shear stress was calculated by dividing the compressive loading force by the bonded area of the test coupons. The acoustic images revised the bonded area by subtracting voided areas. A compilation of stress-strain curves of five $Sn_{63}Pb_{37}$ solder samples is shown in Figure 5-22.

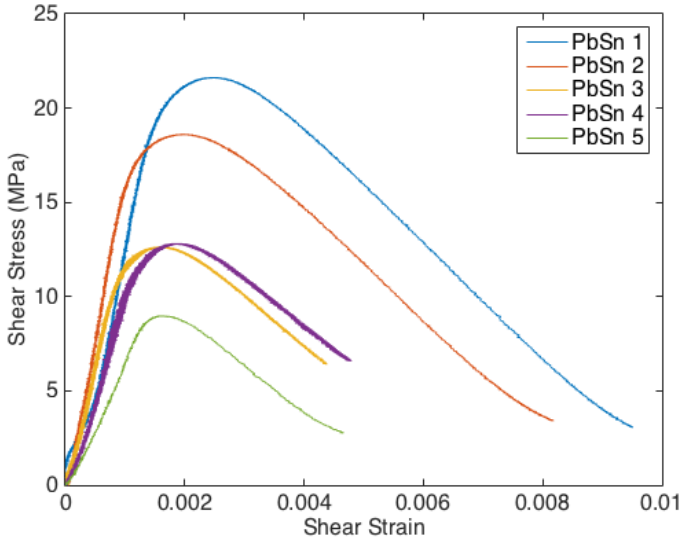

Figure 5-22: Solder stress-strain curves

Maximum shear stress values varied among samples between eight and 22 MPa. Shear testing was repeated with sintered Ag samples. Stress-strain curves of eight samples are shown in Figure 5-23.

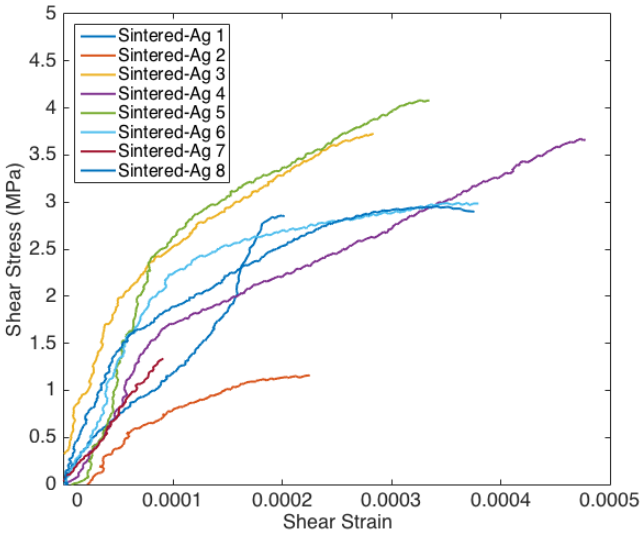

Figure 5-23: Sintered Ag stress-strain curves

When compared to the $Sn_{63}Pb_{37}$ solder samples, it was found that sintered Ag samples reached their ultimate strength with very little displacement, confirming that creep effects are minimal within the material. Variation in ultimate strength varied more from sample to sample and may be due to the synthesis variations between samples. The maximum shear stress values for sintered Ag are also significantly lower than measurements of $Sn_{63}Pb_{37}$ solder samples, indicating that additional synthesis optimization for sintered Ag is required.

Conclusions and Future Directions

As maximum device temperatures approach 200°C continuous operation, sintered Ag materials promise to maintain bonds at these high temperatures without excessive degradation rates. Recent work has modeled strain energy density and J-Integral values for sintered coupons with round and 50-mm x 50-mm geometries under thermal cycling conditions. Sintered Ag samples were synthesized and shear tested for mechanical characterization. Material properties gathered are replacing bulk silver material properties to more accurately model the interface structure. Working in close collaboration with Kyocera and Virginia Tech, a detailed characterization of the thermal performance and reliability of sintered Ag materials and processes has been initiated for the next year.

Future steps in crack modeling include efforts to simulate crack propagation directly using the extended finite element method (X-FEM). X-FEM is a numerical technique that uses partition of unity method for modeling discontinuities such as cracks in a system. The biggest advantage of X-FEM is that crack propagation can be modeled without re-meshing. Also, we will investigate the application of cohesive zone models, which employ traction-separation laws, in an X-FEM framework to simulate cohesive crack growth.

Development of lifetime estimation tools will allow the reliability of sintered Ag to be predicted (similar to the reliability prediction of solder materials), and enable a time- and cost-effective design process. Performance and reliability of novel/emerging techniques such as atomic-level bonding (in collaboration with industry) will also be investigated as a longer-term development goal.

FY 2016 Presentations/ Publications/ Patents

1. P. Paret, D. DeVoto, and S. Narumanchi. 2016. “Reliability of Emerging Bonded Interface Materials for Large-Area Attachments.” *IEEE Transactions on Components, Packaging and Manufacturing Technology* Vol. 6, No. 1, pp. 40-49.
2. A.A. Wereszczak, M.C. Modugno, S.B. Waters, D.J. DeVoto, and P.P. Paret. 2016. “Method to Determine Maximum Allowable Sinterable Silver Interconnect Size.” IMAPS High Temperature Electronics (HiTEC), Albuquerque, NM.

Acknowledgments

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References

1. A.A. Wereszczak, Z. Liang, M.K. Ferber, and L.D. Marlino. 2014. “Uniqueness and Challenges of Sintered Silver as a Bonded Interface Material.” International Conference on High Temperature Electronics (HiTEC), Albuquerque, NM.
2. R.W. Chuang and C.C. Lee. 2002. “Silver-Indium Joints Produced at Low Temperature for High Temperature Devices.” *IEEE Transactions on Components and Packaging Technologies* Vol. 25, No. 3, pp. 453–458.
3. K. Sow. 2014. “Are Sintered Silver Joints Ready for Use as Interconnect Material in Microelectronic Packaging?” *Journal of Electronic Materials* Vol. 43, No. 4, pp. 947–961.
4. S.W. Yoon, K. Shiozaki, S. Yasuda, and M.D. Glover. 2012. “Highly Reliable Nickel-Tin Transient Liquid Phase Bonding Technology for High Temperature Operational Power Electronics in Electrified Vehicles.” Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 478–482.
5. H. Greve and F.P. McCluskey. 2014. “LT-TLPS Die.” *Journal of Microelectronics and Electronic Packaging* Vol. 11, No. 1, pp. 7–15.

6. D.J. DeVoto, A.A. Wereszczak, and P.P. Paret. 2014. “Stress Intensity of Delamination in a Sintered-Silver Interconnection.” IMAPS High Temperature Electronics (HiTEC), Albuquerque, NM.
7. P. Paret, D. DeVoto, and S. Narumanchi. 2016. “Reliability of Emerging Bonded Interface Materials for Large-Area Attachments.” IEEE Transactions on Components, Packaging and Manufacturing Technology, Vol. 6, No. 1, pp. 40–49.
8. J.R. Rice. 1968. “A Path Independent Integral and Approximate Analysis of Strain Concentration by Notches and Cracks.” ASME Journal of Applied Mechanics, Vol. 35, pp. 379–386.
9. W. Brocks and I. Scheider. 2001. “Numerical Aspects of the Path-Dependence of the J-Integral in Incremental Plasticity.” Technical Note GKSS/WMS/01/08.
10. X. Chen, R. Li, K. Qi, and G.Q. Lu. 2008. “Tensile behaviors and Ratcheting Effects of Partially Sintered Chip-Attachment Films of a Nanoscale Silver Paste.” *Journal of Electronic Materials* Vol. 37, No. 10.

6 Electric Drive Technologies Materials Research and Development

6.1 Power Electronics and Electric Motor Materials Support (Joint with VTO Propulsion Materials)

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Contract No.: DE-AC05-00OR22725

Abstract/Executive Summary

Materials research and development (R&D) support is provided to both power electronics (PE) and electric motor (EM) research efforts under way at NTRC via joint funding from the VTO Propulsion Materials and EDT Programs.

- PE materials support: The FY 2016 effort involved applied R&D of sinterable silver (Ag) as a candidate interconnect for PE devices and attempts to hasten the more confident adoption of sintered-Ag technology and consequent improvement in the reliability of automotive PE devices. Other EDT-sponsored PE packaging efforts at NTRC were supported and an ORNL-led collaborative effort with the National Renewable Energy Laboratory (NREL) occurred as well.
- EM materials support: Two primary R&D efforts occurred in FY 2016. The first effort involved investigation of new candidate potting compounds that could have better thermal transfer characteristics and higher- temperature capability and that are economically competitive. The second effort involved a fundamental study and measurement of the directional thermal transfer in copper (Cu) windings used in EMs, and involved an ORNL-led collaboration with NREL.

Accomplishments

- PE materials support (FY 2016 focus—sintered-silver interconnects)
  - Quantified achievable maximum strength
  - Showed asymmetric residual stress can limit mechanical reliability
  - Developed a proof test to identify the largest achievable interconnect size
  - Showed shear strength was insensitive to the choice of plating, processing, and printing methods
  - Showed sintered-Ag interconnects can be fatigue resistant
  - Identified failure locations (weakest areas) in different sintered-Ag interconnect systems
  - Used Weibull analysis and postmortem to identify failure exclusivity and parasitics.

- EM materials support (FY 2016 focus—materials to promote thermal transfer in Cu windings)
  - Showed significant apparent thermal conductivity anisotropy of packed Cu wire.
  - Contrasted thermal conductivity test methods using Cu winding samples.
  - Used percolation theory to interpret thermal conductivity trends at higher wire-packing fractions.

Introduction

For future PE devices, the potential use of sintered-Ag interconnection technology has several advantages over conventionally used solder-based interconnection technology (e.g., better electrical and thermal conductivity, microstructural equilibrium, potential for much better reliability). However, its adoption has been slow because it is a relatively new technology and the PE community is relatively conservative. This VTO Propulsion Materials–EDT jointly funded effort seeks to hasten the more confident adoption of sintered-Ag by identifying the achievable strength characteristics of such interconnect systems, which are relatively complex (Figure 6-1Figure 6-1). This effort will guide future sintered-Ag design for PE and improve the PE community's receptiveness to adopting sintered-Ag technology.

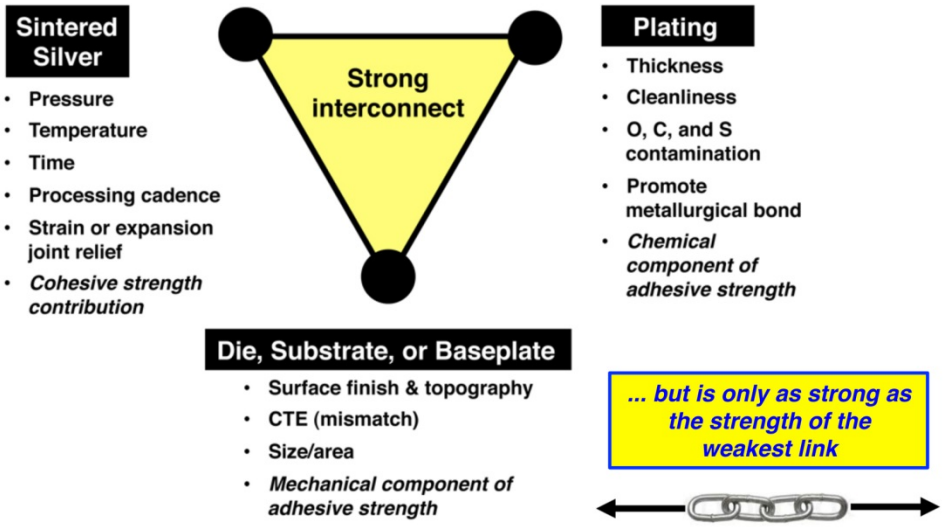

Figure 6-1: The strength and reliability of a sintered-Ag interconnect is a function of many parameters.

Minimizing the service temperature in Cu windings in EM slot liners will promote greater efficiency and enable EM size and weight reductions. Such wires in slot liners are shown in Figure 6-2. Two ways to achieve minimization are by using more thermally conductive materials in EMs and by improving the understanding of the anisotropic thermal transfer within those Cu windings. New potting and molding compounds that have better thermal transfer characteristics and higher temperature capability are attractive candidates for this purpose, provided they are cost competitive and do not introduce performance compromises. Greater understanding of the thermal transfer characteristics starts with the fundamental study and measurement of the directional thermal transfer in Cu windings used in EMs; however, specimens that represent how these Cu windings thermally respond in service must be developed and thermally measured.

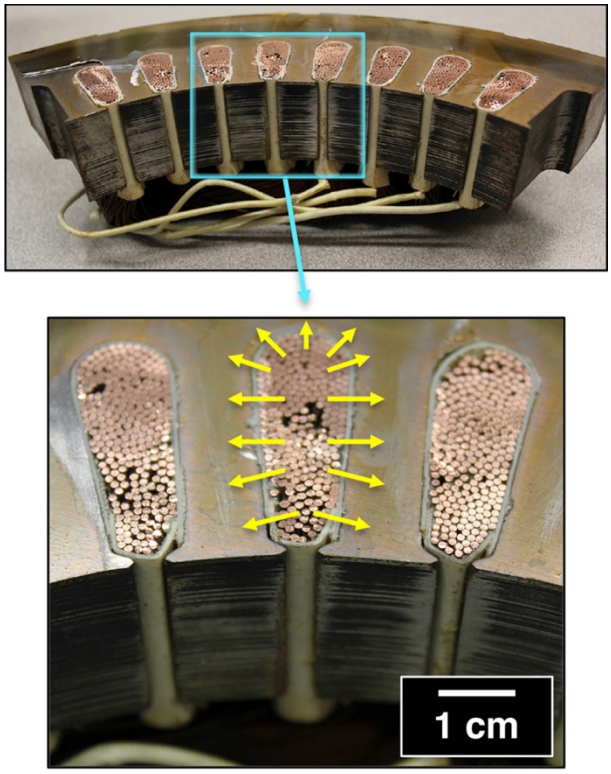

Figure 6-2: Sectioned view showing Cu-wire packing within slot liners. Yellow arrows represent the direction of potential heat transfer from the Cu wires.

Approach

PE Materials Support

- Fabricate sintered-Ag test coupons that enable the measurement of a critical dependent parameter associated with interconnect reliability and shear strength, and measure it as a function of the plating material [Ag vs. gold (Au)], drying method, and printing method (screen vs. stencil).
  - Perform postmortem failure analysis to identify failure location and failure type.
  - Publish results and interpretations.
- Coordinate and lead a sintered-Ag thermomechanical reliability study with NREL.
  - Examine the effect of coefficient-of-thermal-expansion (CTE) –induced residual stress on sintered-Ag printed pad size and the onset of delamination of the interconnect.
  - Fabricate all specimens and provide materials characterization analysis.
  - Publish results and interpretations.

EM Materials Support

- Fabricate Cu-wire-wound test coupons with filler materials that will promote greater thermal conductivity perpendicular to the wires.
  - Publish results and interpretations.
- Coordinate and lead a collaboration with NREL to better understand the directional thermal response of Cu-wound structures.
  - Fabricate test specimens that facilitate the valid measurement of thermal diffusivity and thermal conductivity as a function of wire orientation.
  - Use different methods of thermal property measurement to enable comparisons, and validate the legitimacy of the results.
  - Publish results and interpretations.

PE Materials Support

Maximum Size

A simple and inexpensive approach was developed to identify the largest achievable interconnect size with sinterable Ag. That size is an outcome of all the cumulative effects of numerous independent parameters that each affects that achievable size. The method can be viewed as a proof test. The method involves making geometrically simple test coupons whose materials have CTEs that match or mimic those of materials used in PE devices and that are bonded by an interconnect material whose bond size is likely to exceed that used in that device. Figure 6-3Figure 6-3 is a schematic of the geometries and materials used in this study.

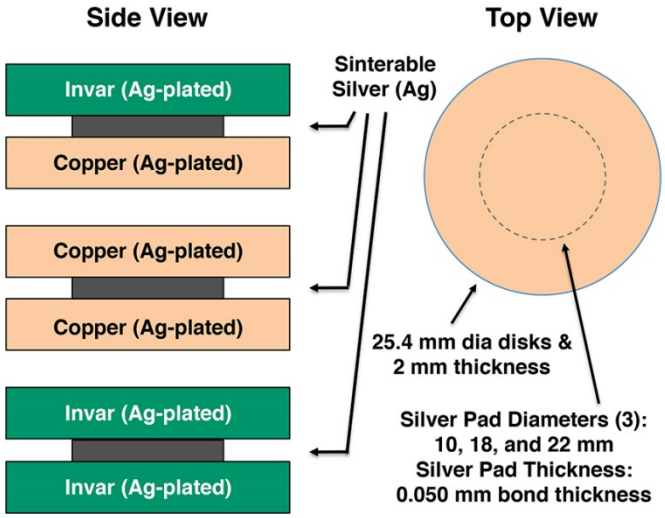

Figure 6-3: Schematic showing how CTE-induced residual stress was purposely varied through choice of disk materials and bonding size.

Delamination occurred simply from the cooldown to room temperature from the 250°C bonding process for the Cu-invar couple when they were bonded with 18 and 22 mm diameter sintered-Ag pads. Delamination did not occur in this stage for this couple when 10 mm diameter sintered-Ag pads bonded the Cu and invar.

A large differential in the CTE mismatch relative to the sintered-Ag would cause delamination for larger bonded areas (i.e., the Ag-bonded invar-invar couples); however, an asymmetric CTE across (or perpendicular to the interconnect plane of) the sintered-Ag interconnect is more apt to promote the onset of delamination. Such across-the-interconnect CTE asymmetry superimposes in-plane and out-of-plane shear stress resulting in an overall higher (equivalent) stress that is more likely to reach the interconnect system's shear strength and cause the onset of delamination. Examples of delaminations as a function of size for the Cu-invar couple are shown in Figure 6-4 and Figure 6-5.

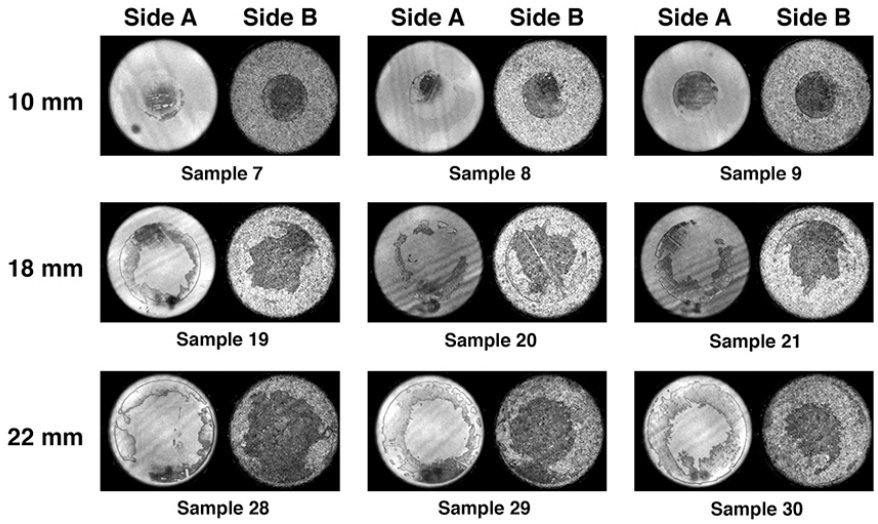

Figure 6-4: Acoustic microscopy images of the as-processed Cu-invar couples bonded with Ag. Each of the nine pairings consists of images captured through opposite directions. Disks are 25 mm in diameter.

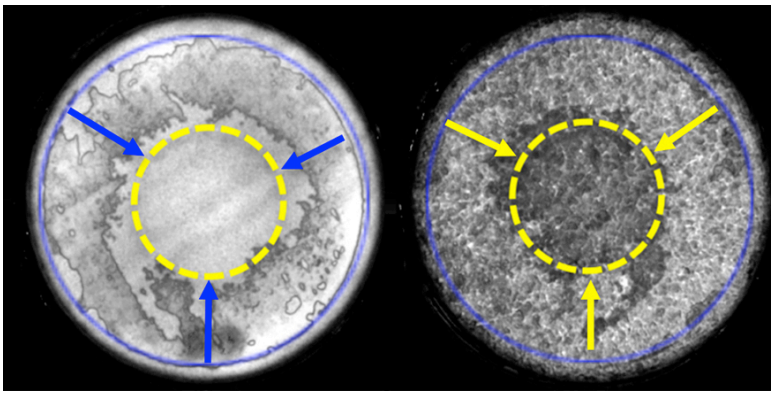

Figure 6-5: Example of superimposed (dashed) circles on a Cu-invar couple used in the analysis of the sustained sintered-Ag bond shape. The arrows show the radial ingress from the original printed diameter. Disks are 25 mm in diameter.

Thermal cycling (entire coupon at an isothermal temperature for any given temperature of that cycling) caused mortality of all the Cu-invar couples by 400 cycles (Figure 6-6). This suggests that subjecting such an interconnect system to a relatively low number of thermal cycles could serve as an effective proof test. Such thermal cycling did not cause failure for Cu-Cu or invar-invar couples bonded by sintered-Ag (up to 22 mm diameter print pads); this further illustrates the deleterious influence of an asymmetric CTE mismatch across the sintered-Ag interconnect.

Interpretation of the tracking of the delamination of the thermal-cycling-induced failures suggests that the sintered-Ag process used here produced a relatively fatigue-resistant interconnect. That statement is based on the absence of identifiable continuous delamination up to failure of the interconnect system (i.e., catastrophic delamination must have initiated and entirely occurred in less than 100 cycles); this is an indicator of a relatively high fatigue exponent.

A sintered-Ag interconnect having a diameter of at least 22 mm can bond Cu to Cu, and a sintered-Ag interconnect of at least 10 mm can bond invar to invar. A 10 mm diameter sintered-Ag interconnect will fail in thermal cycling if it bonds Cu to invar. Sintered-Ag bondability with other material pairings [e.g., silicon, aluminum, molybdenum, and direct bond copper (DBC) substrates] based on the respective CTEs of the materials has also been considered.

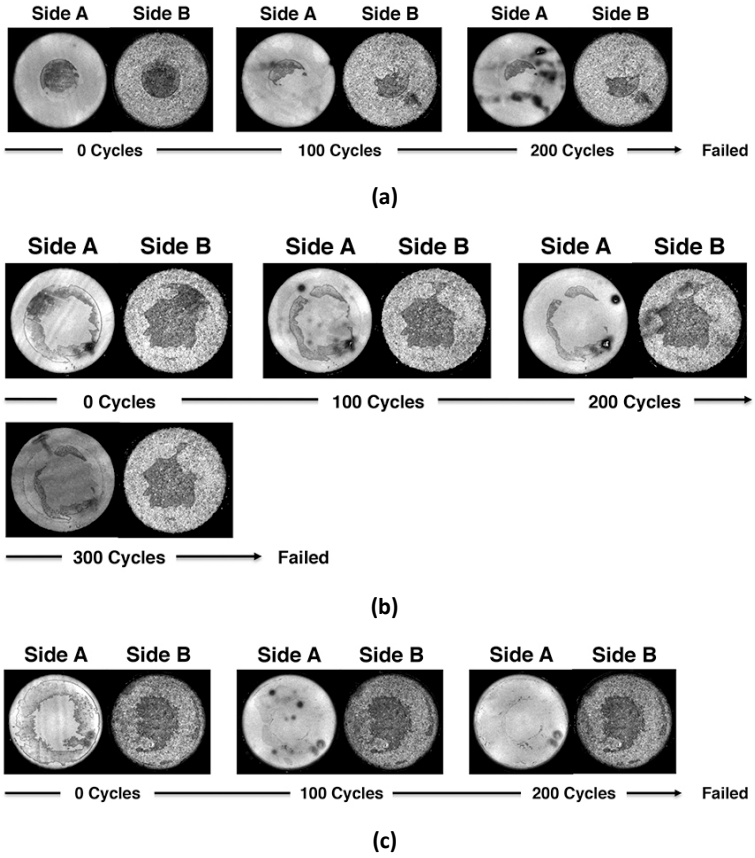

Figure 6-6: Tracked acoustic microscopy images of (a) 10 mm diameter, (b) 18 mm diameter, and (c) 22 mm diameter bonded Cu-invar couples. All failed in less than 400 thermal cycles.

Plating, Processing, and Failure Interpretation

Shear strength of the explored sintered-Ag interconnect system was insensitive to the choice of Au or Ag as plating material, processing method (predrying vs. wet-surface-consolidation), and printing method. Sintered-Ag interconnect systems should be able to withstand shear stresses of ~30 MPa if consistent processing (i.e., no exclusive flaw types) is used (Figure 6-7). They will fail if service shear stresses exceed ~ 60 MPa.

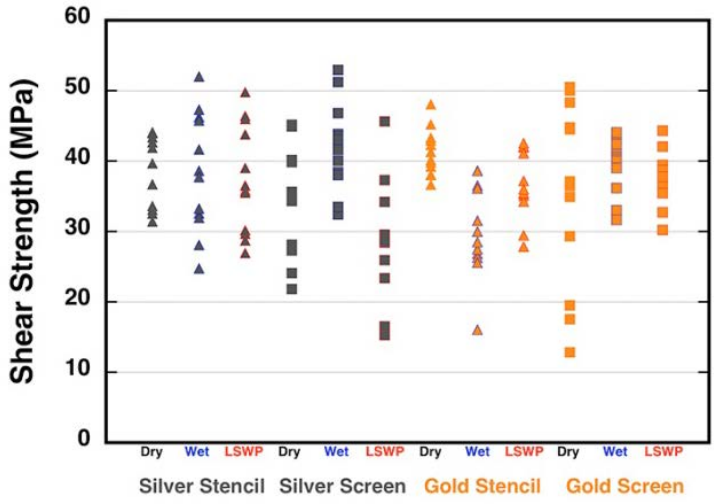

Figure 6-7: With the exception of some low-strength outliers, the majority of shear strengths were greater than 25–30 MPa.

Despite shear strength being insensitive to the processing method, compromised print-pad structure can be introduced with predried, screen-printed, and wet-processed sintered-Ag, and that can manifest itself in

relatively low shear strength of the interconnects. Because sintered-Ag is still undergoing process development, the use of combined Weibull and failure analyses can be useful in identifying exclusivity and parasitics associated with its process development and testing. The change-in-slope at lower strength values in the Weibull plot (Figure 6-8) is an illustration of such compromise.

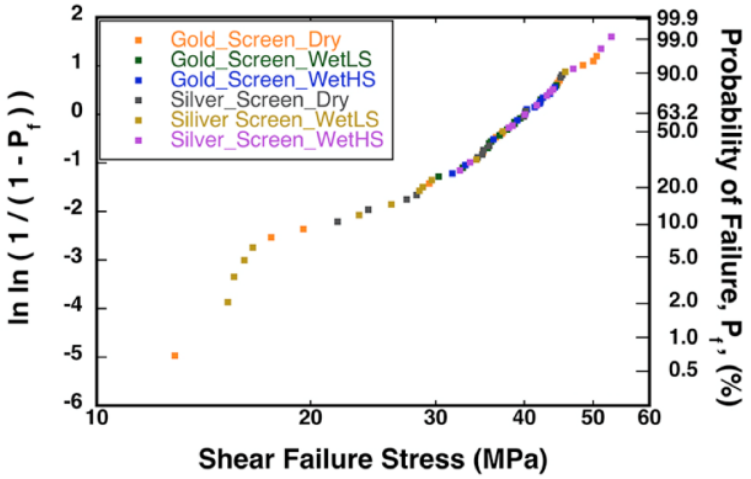

Figure 6-8: Change in slope at failure stresses < 20 MPa is an indication of operative exclusive flaw types.

Ag-plated DBC sandwiches tended to adhesively fail between the Ag plating and DBC cladding. Gold-plated DBC sandwiches tended to fail in a hybrid manner, with the majority of failure resulting from cohesive failure of the sintered-Ag bond with additional adhesive failure between the Au plating and the nickel-phosphorus (Ni-P) sublayer.

EM Materials Support

EM materials support included investigating materials to promote thermal transfer in Cu windings. The anisotropic apparent thermal conductivity of packed Cu wire can be satisfactorily estimated with appropriate specimen preparation and use of the laser flash and transmittance test methods. The transient hot disk method did not consistently produce trustworthy and defendable apparent thermal conductivity results for the Cu wire specimens and their architecture. Test specimens and methods are shown in Figure 6-9Figure 6-9.

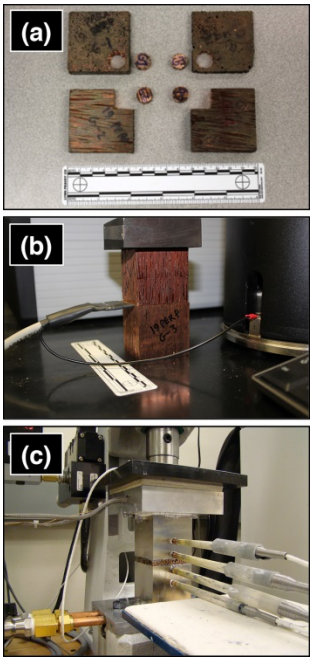

Figure 6-9: Test specimen harvesting for (a) laser flash testing and test setups for (b) transient plane source and (c) thermal transmission testing.

The apparent thermal conductivity of the packed Cu wire was about 2 orders of magnitude higher in the direction parallel to the wires than perpendicular to them. The former was more than 200 W/mK while the latter was only 0.5 to 1 W/mK for a wire packing efficiency of about 50%. Results are shown in Table 6-1.

Table 6-1: Measured thermal conductivities as a function of test method

Material	Apparent Thermal Conductivity κ_app (W/mK)		
	Laser Flash E1461	Transient Plane Source ISO 22007-2	Thermal Transmittance ASTM D5470
Cu-Wire & Varnish, Parallel or Longitudinal, 19-Ga	238	[a]	
Cu-Wire & Varnish, Perpendicular or Transverse, 19-Ga	0.55	[a]	1.0–1.2
Cu-Wire & Varnish, Parallel or Longitudinal, 22-Ga	212	[a]	
Cu-Wire & Varnish, Perpendicular or Transverse, 22-Ga	0.52	[a]	1.0–1.2
Varnish[b]		0.19	

[a]Technique unfavorable for highly anisotropic materials.
[b]Actual κ measured (not κ_app).

The measured apparent thermal conductivity responses of the packed Cu wires consisting of either 670 or 925 µm diameter wires did not exhibit significant differences in the direction perpendicular to the wires at a packing efficiency of ~ 50%. The Kanzaki model's prediction of apparent thermal conductivity differences for their combinations also indicates an equivalence [1]. However, the apparent thermal conductivity parallel to the wires for the 925 µm diameter wires was nearly 10% higher than that for the wire packs containing the 670 µm diameter wires.

For the transmittance test method, the average apparent thermal conductivity perpendicular to the wires and the amount of scatter were insensitive to specimen thickness for thicknesses from 3.2 to 6.4 mm. This is illustrated in Figure 6-10. It is believed this thickness range constitutes a size smaller than the representative volume element for these packed Cu wire systems; therefore, the amount of scatter in the measured apparent thermal conductivity could be greater or less as the thickness gets smaller or larger.

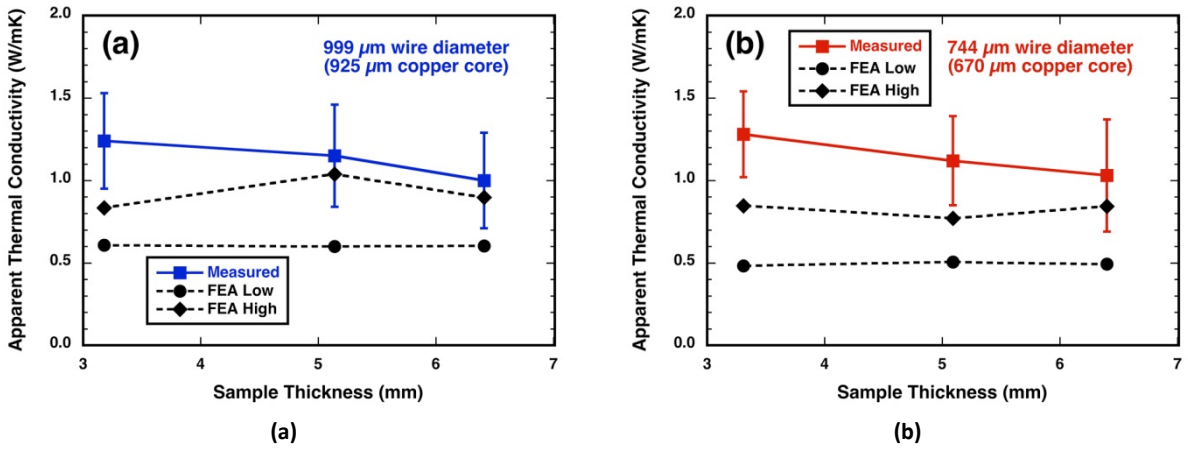

Figure 6-10: Apparent thermal conductivity perpendicular to wires as a function of sample thickness using transmittance test method for (a) 925 µm diameter or 19 Ga and (b) 670 µm diameter or 22 Ga Cu core wires. Indicated bars on the measurements represent 95% confidence bands. Finite element analysis (FEA) low and high bounds represent fill factors from density and image analysis estimations, respectively.

Percolation channels (Figure 6-11), representing localized pathways having relatively high concentrations of Cu, likely caused the packed Cu wire to have a slightly higher apparent thermal conductivity than that predicted by finite element analysis (FEA).

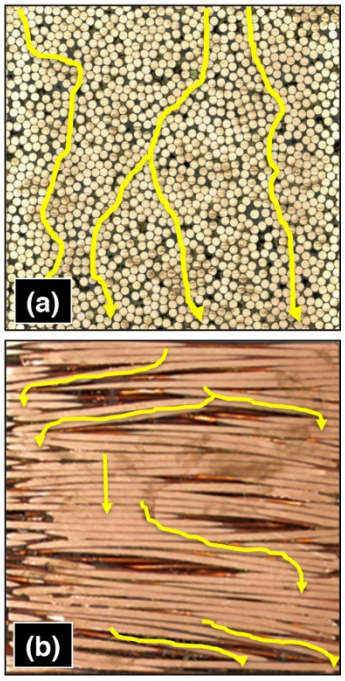

Figure 6-11: Percolation pathways (yellow) that potentially provide localized preferential thermal conduction. Potential pathways are illustrated for two mutually orthogonal sections of packed Cu wire [(a) and (b)].

The Kanzaki model (with FEA confirmation) provides a satisfactory numerical estimation of the apparent thermal conductivity of the packed Cu wire in the direction perpendicular to the oriented wires. This estimation takes into account the wire diameter and its thermal conductivity, the wire insulation coating thickness and its thermal conductivity, and the packing factor and the thermal conductivity of the interstices material. The model supports the expectations that increasing the thermal conductivity of both the wire insulating coating material and the material in the interstices can significantly increase the apparent thermal conductivity perpendicular to the wire orientation in packs of aligned Cu wire. This is illustrated in Figure 6-12.

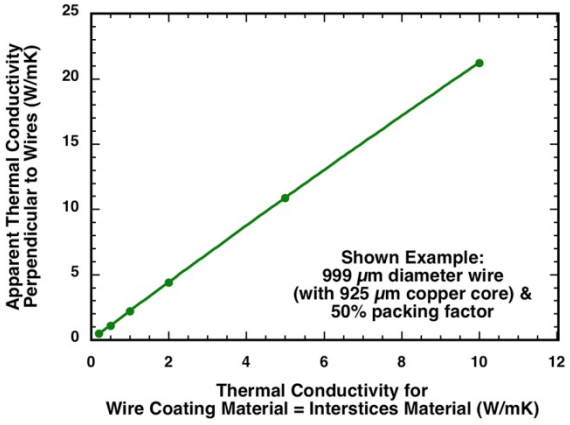

Figure 6-12: Calculated apparent thermal conductivity perpendicular to the wires as a function of thermal conductivity of the wire coating material and interstices material (after [1]). The thermal conductivities of the wire coating material and interstices material are set equal in this example.

Conclusions and Future Directions

Conclusions

- PE materials
  - Maximum strength: Sintered-Ag interconnect systems should be able to withstand shear stresses of ~30 MPa if consistent processing is used. They will fail if service stresses exceed ~ 60 MPa.
  - Asymmetric residual stress: Asymmetric CTE across (or perpendicular to) an interconnect's plane is more apt to promote the onset of delamination. Such an oriented stress state superimposes in-plane and out-of-plane shear stress resulting in higher (equivalent) stress that is more likely to reach the interconnect system's shear strength and cause the onset of delamination.
  - Proof testing: A simple and inexpensive approach was developed to identify the largest achievable interconnect size with sintered-Ag. The method can be considered as a proof test.
  - Shear-strength insensitivity: Shear strength of the explored sintered-Ag interconnect system was insensitive to the choice of Au or Ag as plating material, processing method (predrying vs. wet-surface-consolidation), and printing method (screen vs. stencil).
  - Fatigue resistance: Sintered-Ag was determined to be a relatively fatigue-resistant interconnect. There was no identifiable continuous delamination occurring up to failure of the interconnect system; this is an indicator of a relatively high fatigue exponent.
  - Failure location: Silver-plated DBC sandwiches tended to adhesively fail between the Ag plating and DBC cladding whereas Au-plated DBC sandwiches tended to fail in a hybrid manner, with the majority of failures resulting from cohesive failure of the sintered-Ag bond with additional adhesive failure between the Au plating and the Ni-P sublayer.
  - Failure analysis: The use of combined Weibull and postmortem failure analyses can be useful in identifying exclusivity and parasitics associated with sintered-Ag process development and testing or both.

- EM materials
  - Anisotropy: Identified that the apparent thermal conductivity of packed Cu wire was about 2 orders of magnitude higher in the direction parallel to the wires than perpendicular to them. The former was more than 200 W/mK while the latter was only 0.5 to 1 W/mK for a wire packing efficiency of about 50%.
  - Test methods: The anisotropic apparent thermal conductivity of packed Cu wire can be satisfactorily estimated with appropriate specimen preparation and use with the laser flash and transmittance test methods. The transient hot disk method did not consistently produce trustworthy and defendable apparent thermal conductivity results for these specimens and their architecture.
  - Specimen size: The average apparent thermal conductivity perpendicular to the wires and the amount of scatter were insensitive to specimen thickness (for thicknesses 3.2 to 6.4 mm) for the transmittance test method. It is believed this thickness range constitutes a size smaller than the representative volume element for these packed Cu wire systems; therefore, the amount of scatter in the measured apparent thermal conductivity could be greater or less as the thickness gets smaller or larger.
  - Percolation: Percolation channels, representing localized pathways having relatively high concentrations of Cu, likely cause packed Cu wire to have a slightly higher apparent thermal conductivity than that predicted by FEA.

Future Directions

- Paste drying: Refine new ORNL-developed method to dry sinterable-Ag paste. It enables strong interconnect bonding without the need for concurrent pressure and the use of reflow oven processing.
- Sintering with reflow oven: Refine sintered-Ag interconnect processing method using reflow oven processing technology.
- Shear and tension: Complete study and mechanical test method development to examine how shear or tension stress states or both affect strength of sintered-Ag interconnects.

- Fracture toughness: Complete study and mechanical test method to estimate the apparent fracture toughness of sintered-Ag interconnects.
- Silver plating: Examine mechanical integrity of Ag plating used with sintered-Ag interconnects.
- Thermally conductive fill: Complete study on candidate thermally conductive fill materials.

FY 2016 Presentations/Publications/Patents

1. A. A. Wereszczak, J. E. Cousineau, K. Bennion, H. Wang, R. H. Wiles, T. B. Burress, and T. Wu, "Anisotropic thermal response of packed copper wire," in review, *Journal of Thermal Science and Engineering Applications*, 2016.
2. A. A. Wereszczak, M. C. Modugno, S. B. Waters, D. J. DeVoto, and P. P. Paret, "Method to determine maximum allowable sinterable silver interconnect size," in *IMAPS HiTEC 2016*, Paper WP23, May 10–12, 2016, Albuquerque, New Mexico, pp. 207–215.
3. M. C. Modugno, A. A. Wereszczak, and S. B. Waters, "Toward interpreting failure in sintered-silver interconnection systems," in *IMAPS HiTEC 2016*, Paper WP26, May 10–12, 2016, Albuquerque, New Mexico, pp. 234–241.
4. T. Wu, A. A. Wereszczak, H. Wang, B. Ozpineci, and C. Ayers, "Thermal response of an additive manufactured aluminum," presented at the *International Symposium on 3D Power Electronics Integration and Manufacturing*, June 13–15, 2016, Raleigh, North Carolina.
5. "Method to Determine Maximum Allowable Sinterable Silver Interconnect Size," presented at *IMAPS HiTEC 2016*, May 10–12, 2016, Albuquerque, New Mexico,.
6. "Sintered silver R&D at ORNL," presented at the United States Council for Automotive Research LLC, U.S. DRIVE Electrical and Electronics Technical Team meeting, March 17, 2016, Southfield, Michigan.
7. "Materials introspections," presented at the EDT Research Industry Engagement Meeting, October 28, 2015, Knoxville, Tennessee.

References

1. H. Kanzaki, K. Sato, and M. Kumagai, "A Study of a Technique to Predict the Equivalent Thermal Conductivity of an Electric Coil," *Transactions of the Japan Society of Mechanical Engineers, Series B*, **56**(526) pp. 1753–58, 1990.

6.2 Development of Radically Enhanced alnico Magnets (DREaM) for Traction Drive Motors

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Subcontractors: University Nebraska-Lincoln, ORNL, Arnold Magnetic Technologies, Inc.
Contract No.: U.S. Department of Energy Contract No. DE-AC02-07CH11358, Ames Laboratory

Abstract/Executive Summary

- New alnico magnets are being developed that do not contain RE elements; instead the main alloy components are Al, Ni, Co, and Fe, with minor additions (e.g., Cu, Nb and Ti), which are all abundant and readily available around the world from multiple sources (including recycling) and can be obtained in a sustainable manner.
- New formulations will address reducing the Co content without sacrificing coercivity.
- Alnico magnets retain a temperature dependence of their magnetic flux that is far superior to RE-based magnet alloys, i.e., essentially without any significant change through the planned vehicle drive motor operating range of -55˚C to 180-200˚C.
- Of key importance for PM drive motors, the new magnets are being developed to have superior coercivity (up to 2X) compared to current alnico magnets and must retain high levels of magnetization to enable high performance operation of advanced PM motors. The magnets also must be developed with a highly aligned structure for enhanced remanence and magnetic anisotropy to satisfy motor load line designs that make full use of the enhanced coercivity that is being pursued.
- The improved alnico magnet alloys and innovative processing methods also are intended to enable production of bulk magnets with reduced cost and greatly improved mechanical properties. The powder processing method that is being developed will permit mass production of final-shaped alnico magnets in quantities of millions with far less scrap from machining of castings and from breakage during handling/motor assembly than the current special casting/machining process.

Accomplishments

- Combined atom probe tomography (APT) and scanning transmission electron microscopy (STEM) has elucidated the chemical ordering during magnetic annealing and subsequent draw processing.
- Demonstrated that the spinodal spacing and its uniformity is very sensitive to the temperature of the magnetic annealing. The optimal temperature is compositionally dependent. It is this stage where the coercivity is determined.
- Developing protocols to establish draw time and temperature for a range of alnico alloys, which is key to the full development of coercivity.

- Atomistic modeling and micromagnetic modeling are providing key insights into the chemical ordering and the needed topology to enhance coercivity. Numerical micromagnetic simulations have been used to investigate the magnetic properties and the detailed mechanisms of magnetization reversal in alnico giving critical insight into the desired nanostructuring of the Fe-Co magnetic phase needed to enhance coercivity.
- Reduced the Co content significantly while increasing coercivity in bulk alnico samples made by chill casting. Disclosure and provisional patent has been filed and a utility patent application is being pursued.
- Achieved sufficient progress to file a provisional patent on a solid state (abnormal) grain growth approach that uses uni-axial stress biasing or temperature gradient/grain seeding to promote the desired grain alignment direction in bulk alnico magnet samples. Full development of this alignment approach will permit the maximum remanence and energy product to be achieved for enhanced magnetic energy density.
- Sintered magnets of alnico 8H were tested at NREL and showed superior (2X) mechanical (bend) strength over the test temperature range (-40˚C to 150˚C) and lower thermal conductivity than commercial alnio 8H or 9.
- Half-scale magnets based on UQM's motor design demonstrated that the powder processing route will produce superior magnetics with improved mechanical properties for traction drive motors.

Introduction

Broad expansion of electric drive vehicles and the global economic competitiveness of the domestic automotive industry are tied to establishing key technology advances that provide them with superior permanent magnets that do not contain rare earth (RE) elements. This project utilizes a DOE National Lab-lead effort and a demonstrated science-based process to design and synthesize a high energy product permanent magnet of the alnico type in bulk final shapes without RE elements that will be competitive with existing commercial RE-based magnets on a cost per MGOe per kg basis and will have a more sustainable long term supply and cost outlook. This work utilizes a combination of researcher capabilities centered in a National Laboratory, Ames Lab, and partnerships with Univ. of Nebraska-Lincoln, NREL, ORNL, and with a commercial magnet manufacturer, Arnold Magnetic Technologies, to leverage critical capabilities for permanent magnet development. We are also working in concert with a motor design teams at Unique Mobility and ORNL. The project harnesses the power of fundamental science, modern instrumentation for detailed characterization, and the most advanced processing methods that respond to concerns expressed by industry partners for scale up to full-scale manufacturing capability. New alnico magnets being developed do not contain RE elements; instead the main alloy components are Al, Ni, Co, and Fe, which are all abundant and readily available around the world from multiple sources (including recycling) and can be obtained in a sustainable manner. The alnico magnets have superior temperature dependence of their magnetic flux compared to RE-based magnet alloys, i.e., essentially without any significant change through the planned operating range of -55˚C to 180-200˚C. Of key importance for PM drive motors, the new magnets should have superior coercivity (up to 2X) compared to current alnico magnets and retain high levels of magnetization and remanence to enable high performance operation of advanced PM motors. The magnets also must meet expectations for magnetic anisotropy to satisfy motor load line designs that make full use of their enhanced coercivity. Improved alnico magnet alloys and innovative processing methods should enable production of bulk magnets with reduced cost, compared to current RE-based magnets. More specifically, the powder processing method that is being developed will permit mass production of final-shaped magnets in quantities of millions with far less machining and scrap material and in a cost efficient manner.

Co-lean alnico

Co facilitates better coercivity and thermal stability in many permanent magnets. In commercial alnico alloys, the Co content can be as high as ~34-35 at.% in high coercivity grades such as alnico 8 and 9. However, Co is also a strategic element that is subject to price and supply instabilities. Reduction of Co without degrading magnetic and thermodynamic properties of alnico system is a significant challenge in the development of new advanced alnico magnets. Our previous work on the chemical ordering of the alnico during spinodal formation has enabled precise guidelines to devise substitution of the Co content by Fe and Ni in a systematic way. This

becomes possible by the application of the Rigid Band Approximation approach that assumes that structure of electron bands of the alloy remain rigid even after specific chemical modifications. This is most effective if the applied chemical adjustments do not significantly change the total electron concentration of that alloy, i.e. still abide by the *Hume-Rothery Rule*. New knowledge of the chemistry and phase relationships enables design of several alnico grades with lower Co content without loss of coercivity as compared to their commercial counterpart. For example, the total Co content of Co-rich alnico 8 alloys has been reduced by up to 40%.

Optimized processing and chemistry to enhance coercivity

Over the decades, the various classes of alnico underwent extensive optimization of the magnetic annealing and subsequent heat treatments. Very careful control of times and temperatures were found to be necessary to achieve the best magnetic performance. Quantifying this very sensitive relationship of processing to performance will enable a direct connection of the modelling efforts to the chemical and microstructural evolution. Using a prototypical alnico 8 alloy, we quenched samples at various points along the rather complex optimized annealing schedule. Extensive characterization of the microstructures, their chemistries and magnetic properties revealed very enlightening insight into the enhancement of coercivity.

Micromagnetics: Noninteracting needles

As will be demonstrated below, the phase evolution and the chemistry of the alnico is quite complex. Currently processing protocols for each of the nearly two dozen alnico alloys have been optimized by trial and error. Changes in the alloy chemistry affect the Curie temperature which in turn alters the optimal temperature for the magnetic annealing. How the various spinodal phases evolve is dependent also on the details of the time and temperature for the draw cycles. The objective of the multi-scale modeling is to short-circuit the Edisonian trial-and-error approach typically used in optimization of alloy and magneto-thermal processing.

Approach

Co-lean alnico

The ingots were produced in an inert (Ar) atmosphere. Cylindrical ~3 mm (dia.) by ~8 mm (length) samples were cut from the buttons for heat treatments, followed by microstructural analyses and magnetic measurement. A typical heat treatment process for these Co-lean alnico alloys is quite complex, but necessary as described below. Each experimental alloy starts with arc-melting/chill casting and high temperature solutionizing at 1165 -1170ºC for 20 min to form a single-phase solid solution that is then quenched. The initial phase separation 'template' is set by the magnetic annealing (MA) at 1.2 Tesla field and temperatures ranging from 842 to 847°C for ~ 10 min. followed by air cool. Lower temperature anneals (without external magnetic field) known as "draw cycles" are performed at lower temperatures, typically at 650°C for 5h followed by furnace cool and 580°C for 15h followed by another furnace cool. We also discovered that additional "draw" cycles at even lower temperatures of 500 – 520ºC for 3 – 5 days facilitates further improvement of the coercivity of the Co-lean alnico grades. The reason for each of these annealing selections is described below.

Optimized processing and chemistry to enhance coercivity

Cylinders of ~ 3mm in diameter and 10 mm in length were prepared from the same alnico 8H sample (14.2Al-11.7Ni-34.0Co-30.5Fe-2.5Cu-7.1Ti, in at.%), which was made from gas atomized powder that was hot iso-statically pressed at 1250˚C to full density. These samples were interrupted during strategic points of the processing: as-solutionized for 30 min. at 1250˚C and oil quenched (Sample 1), quenched during 840°C magnetic anneal, after 30s, 90s, 5 min. and 10 min., (Samples 2 to 5) and quenched during the 650°C draw, after 1, 3 and 5h, (Samples 6 to 8). Our previous work demonstrated that the formation of the spinodal is very sensitive to the direction of the applied magnetic field relative to the crystallographic orientation. To insure that each of the samples for atom probe tomography (APT) had the same crystallographic orientation relative to the magnetic anneal, we first preformed electron backscattered electron diffraction to identify the grains with the proper orientation (Figure 6-13). The focused ion beam (FIB) was then used to make the APT samples. The FIB and APT was carried out at Center for Nanophase Materials Sciences, Oak Ridge National Laboratory.

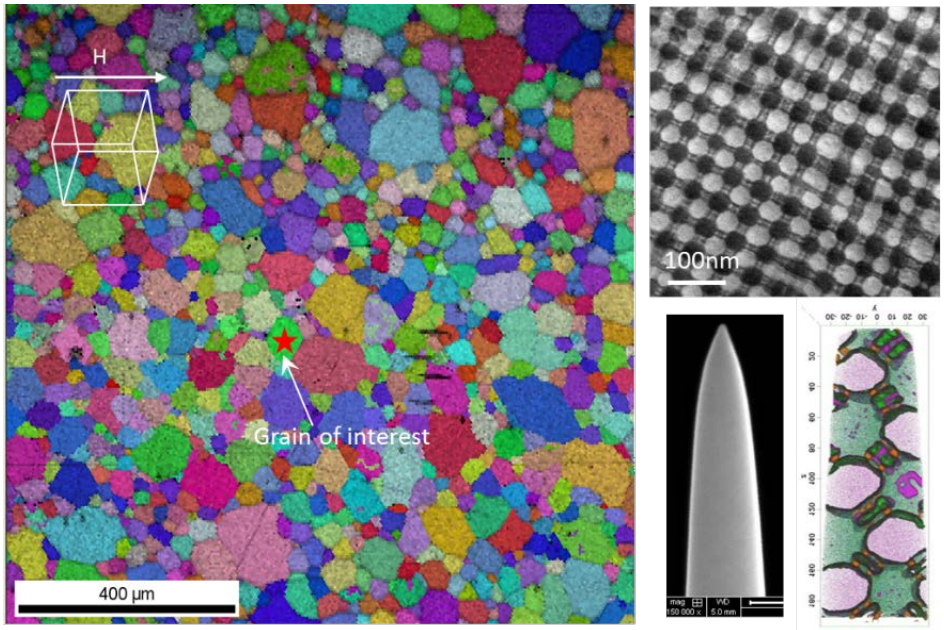

Figure 6-13: EBSD map of one of the alnico 8 samples. The starred grain is one that has the proper orientation for APT which is confirmed by TEM of that same region. The APT map shows the chemical distributions in the spinodally decomposed phases.

Micromagnetics: Noninteracting Needles

Numerical micro-magnetic simulations have been used to investigate the magnetic properties and the detailed mechanisms of magnetization reversal in Alnico. The calculated coercivity is in the same range as experimental values, which are much lower than the estimation from the Stoner-Wohlfarth model due to alnico's tendency toward magnetization curling rather than coherent rotation.

Results and Discussion

Co-lean alnico

Equi-electronic substitution of Co by Fe and Ni showed that nearly ~40% of Co can be reduced in alnico 8H without significantly compromising magnetic properties (Figure 6-14). In fact, magnetic properties of Co-lean alnico increase significantly and can surpass the commercial values in cases with small Co reduction, e.g., of up to ~15%. (Figure 6-15). The XRD and SEM-TEM analyses showed that there is a complex interplay between chemistry and thermodynamics which cause the latter phenomenon. Both the Co amount and amounts of the "minor components" like Ti, Nb, Al and Cu influence the incremental evolution of magnetic coercivity. The effect of equi-electronic reduction of Co by itself is practically "linear", i.e., less Co reduction – better coercivity, in contrast to the accepted 'lore'. This is more or less obvious from our simple comparison of H_{ci} values of both present examples i.e., $Fe_{35.0}Co_{21.5}Ni_{19.0}Al_{15.0}Ti_{7.5}Nb_{0.5}Cu_{1.5}$ (~37% Co reduction) H_{ci} = 1850 Oe, B_r = 0.78 T, $(BH)_{max}$ = 4.7 MGOe and $Fe_{29.1}Co_{29.0}Ni_{14.7}Al_{15.4}Ti_{8.7}Nb_{0.6}Cu_{2.5}$ (~15% Co reduction) H_{ci} = 2558 Oe, B_r = 0.68 T, $(BH)_{max}$ = 4.8 MGOe,

Surprisingly, the small compositional variations/optimizations in Ti, Nb, Al and Cu add more "non-linearity" to the optimization of the chemistry. For example, slight increases in Al, Ti, Nb and Cu in our second example allow for significant enhancement of coercivities above commercial alnico 8H to nearly ~2200 Oe. We attribute this to the crucial role that these "minor components" are playing in defining optimal volume fraction of the magnetic B2'(Fe-Co) needles and non-magnetic $L2_1$ phase. In contrast to the well-faceted microstructure of typical alnico 8H, the microstructure of Co-lean alnico is not that well defined and regular. Instead the "composition refinements" of both spinodal components occur during all stages of heat treatment.

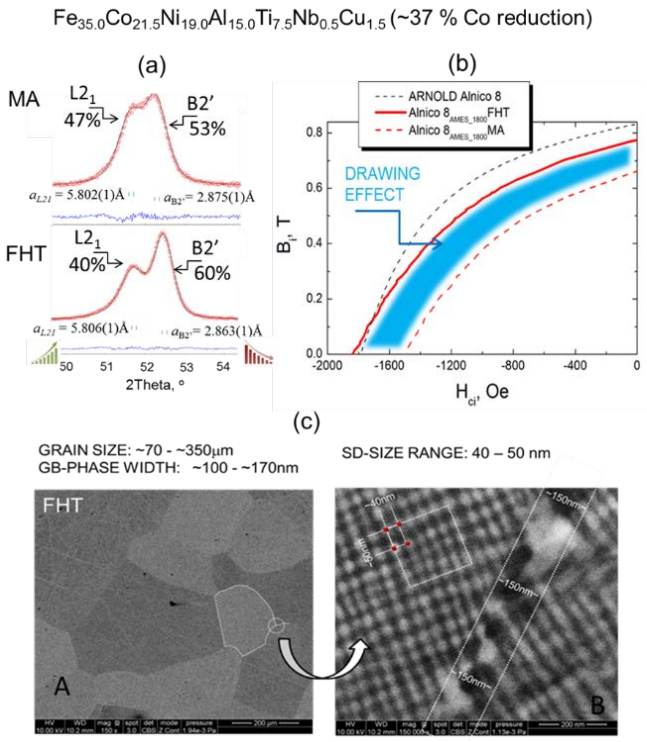

Figure 6-14: Characterization results of Co-lean alnico with ~37% of Co reduction. (a) XRD patter showing the evolution of $L2_1$(Ni/Al) and B2′(Fe/Co) spinodal components by comparison and evaluation of the intensities of [220] and [110] Bragg reflections from $L2_1$ and B2′, respectively; (b) the demagnetization curves of the Co-lean alnico in comparison to Alnico 8; (c) SEM images of grain structure and spinodal structure of Co-lean alnico.

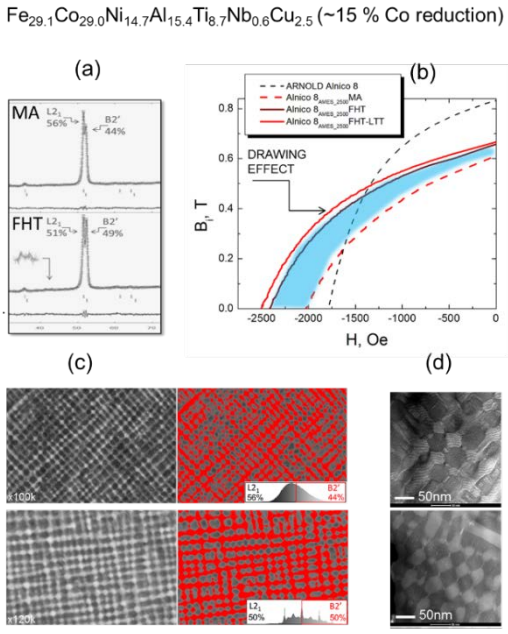

Figure 6-15: Characterization results of Co-lean alnico with ~15% of Co reduction. (a) XRD patter showing the evolution of $L2_1$(Ni/Al) and B2′(Fe/Co) spinodal components by comparison and evaluation of the intensities of [220] and [110] Bragg reflections from $L2_1$ and B2′, respectively; (b) the demagnetization curves of the Co-lean alnico in comparison to Alnico 8; (c) SEM images of grain structure and spinodal structure of Co-lean alnico after magnetic annealing (upper part) and after full heat treatment (lower part); (d) TEM images of Co-lean alnico after magnetic annealing (upper part) and after full heat treatment (lower part).

Optimized processing and chemistry to enhance coercivity

The change in the coercivity and APT maps along various key points during the optimized processing schedule for the alnico 8 alloy is shown in Figure 6-16. Note that the quenched sample right after 1250°C solutionizing has no coercivity yet chemical segregations has already begun. After only 30s of the magnetic annealing, most of the coercivity imparted from this step is observed even though the APT shows further chemical segregation up to the full 10 minutes to which samples typically are subjected. The 650°C draw (Figure 6-17) has a remarkable effect on both the coercivity and refinement of the chemistry between the magnetic bcc phase and the $L2_1$ phase. Note how the 1 hour draw (sample 6) forms very well faceted and isolated bcc regions and a continuous $L2_1$ matrix with a coercivity that more than doubles. From 1 to 5 hours (sample 8) of the draw, coercivity increases almost another 50%. Here the largest change seems to be the development of the copper rods, shown here as orange colored features between the pink bcc phase and the light green $L2_1$ matrix. Not shown is that the saturation magnetization shows a very slight drop over this sequence of steps, most likely due to some unwanted grain boundary phase formation. The remanence plateaus between 30 and 90s magnetic anneal. The key to optimization of the magnetic properties lies clearly in controlling the magnetic annealing which sets the template (spacing and anisotropy) for the Fe-Co spinodal phase, locking in remanence. Apparently, the draw process is responsible for the finer-scale microstructural and chemical ordering which controls coercivity.

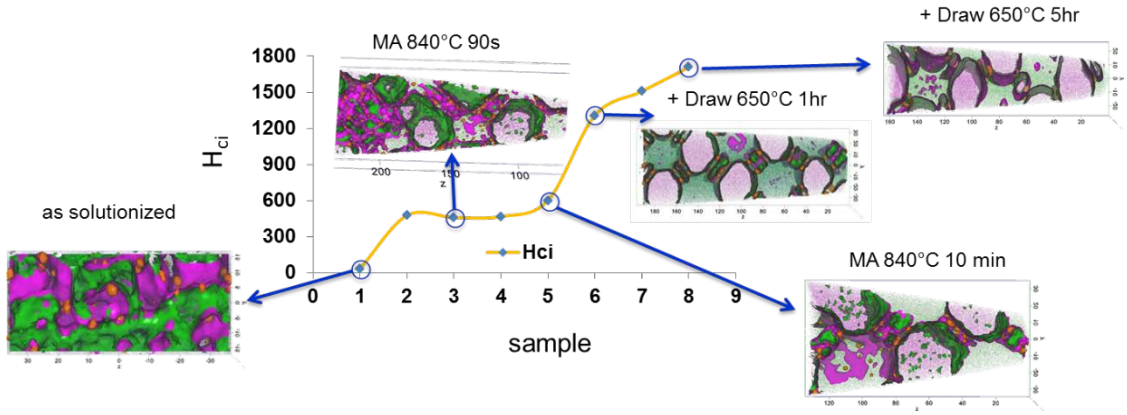

Figure 6-16: The actual measured coercivity for each samples and representative APT maps.

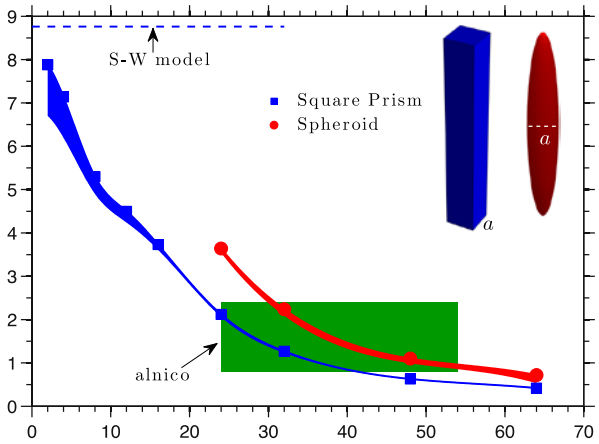

Figure 6-17: Shape and size dependence of the FeCo rods on coercivity. The blue dashed line denotes the cuboidal rod's HC value predicted using Stoner-Wohlfarth model while the solid lines are for rods of various diamters for the two different shapes.

The APT results combined with detailed TEM and magnetization measurements provided a clear picture of relationship between the phase evolution and the development of magnetic properties. The sequence of the

phase evolution and the chemical ordering observed in the APT is consistent with the KMC modeling that has been performed. What is clearly lacking to complete the picture is a complete 3-D imaging of the full extent of the needle morphology. This information on the Fe-Co needle phase is useful because the micro-magnetic modeling shows that the size, shape (anisotropy), and connecting ("bridge") points between the needles (see below) control the coercivity.

Micromagnetics: Noninteracting Needles

Coercivity is dependent on the size of the rod and their geometries. The aspect ratios of the rods were fixed at based on the TEM characterization. Coercivity quickly decreases with increasing rod diameter consistent with previous experiments and simulations. As indicated by the shaded region in Figure 6-17, H_C is ~about 1-2 kOe. The calculated H_C values generally agree with the reported experimental values, both of which are much smaller than predicted by the Stoner-Wohlfarth (SW) theory. The deviation from SW is due to the fact that magnetization reversal occurs by curling instead of coherent rotation, which only becomes dominant when the rod radius R is small. The calculated H_C from micro-magnetics only approaches the SW predictions if the rod size is very small and coherent rotation dominates during reversal.

Figure 6-18 shows the initial developments of curling, a non-coherent reversal mechanism, before magnetization reversal in isolated cuboidal and ellipsoidal magnetic rods. For the square prism, the curling starts from the ends of the rod near the short edges then spreads along the middle of the long faces. The magnetization at the long edges and center of the rod changes the least before reversal. This is consistent with previous studies. For the ellipsoid, which is closer to the actual shapes based on 3D imaging, the curling starts from the middle of the rod where the radius is the largest. The details of the reversal mechanism become quite important when optimizing particle assemblies.

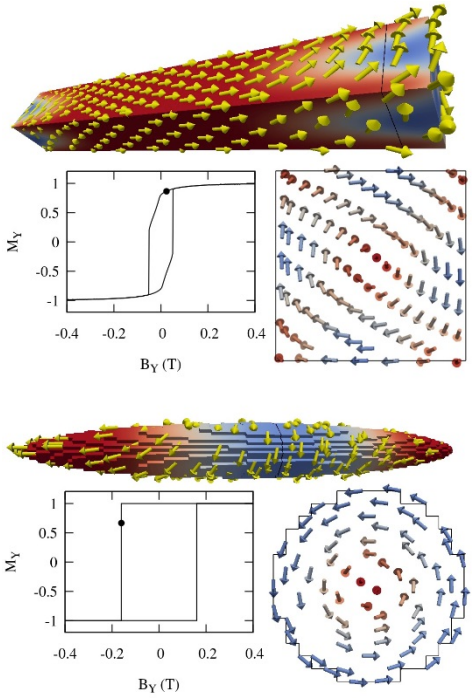

Figure 6-18: Magnetization reversal in isolated Fe-Co rods of isolated square prism and prolate spheroid.

Nanostructural non-uniformity, such as bridging, is a very common feature observed in the real alnico structures. To explore the effects of bridging, we investigate two parallel cuboid nanorods that are connected in different ways to represent different types of bridging: H-shape, U-shape, and O-shape. H-shape branching, in which two rods are connected in the mid-section, is much less detrimental to H_C than U- or O-shape bridging, in which two rods are connected at the ends. This is because the curling starts from the ends of the cuboid rod, and U- or O-types of bridging facilitate such curling and thus decrease the coercivity, while with the H-shape geometries, the curling still starts from the rod ends so that the connection in the middle is less detrimental.

Conclusions and Future Directions

We have made substantial improvements in non-RE (Fe-Co based) permanent magnet alloys based on alnico magnet alloys (primarily focused on alnico type 8H and 9) through refined chemistries and enhanced processing methods informed by advanced characterization and theory. Specifically, our new non-optimized alnico 8H magnets have an energy product that is 44% greater than commercial sintered 8H, although it is still 38% less than alnico 9. Thus, we are well on the way to synthesizing complex magnet parts with high energy density for advanced high torque electric drive motors.

Advanced TEM and 3-D atom probe results have indicated which are the key processing steps that can improve coervcivity. The predictive capability of the MC modeling, along with advanced micro-magnetic modeling, is providing the insight needed to optimize the chemistry and processing. Magnetic modeling shows that calculated coercivity is similar to experimental values and much lower than estimates from the Stoner-Wohlfarth model. We attributed this departure to the particle's tendency toward curling rather than coherent rotation during the magnetization reversal. How the various magnetic needles bridge is also very important to retaining coercivity. This insight is crucial to optimizing chemistry and processing protocols.

The sintered alloys have been shown to have superior mechanical toughness and lower thermal conductivity than commercial alnico 8H or alnico 9. This work was conducted in concert with NREL and ORNL. The powder processing has also been shown to be quite scalable and allow for forming complex shapes. We have already demonstrated half-scale magnets based on UQM's motor design.

Future Directions

The detailed characterization has identified that optimizing the magnetic anneal in crucial to developing the well-ordered spinodal structure for maximum coercivity. Further improvements in energy product will come from aligning the grains to take advantage of stress biased (or temperature gradient/seeded) solid state abnormal growth prior to the magnetic anneal. A high degree of crystallographic alignment in our powder processed magnets will increase the B_r/M_s ratio to a level of about 0.9, which is equivalent to fully aligned (by directional solidification) alnico 9. In turn, with the improvements we have made in coercivity, full grain alignment could result in an increase in energy product that is at least 50% greater than alnico 9.

We have established a couple of pathways to promote well texture magnets using solid-state grain growth. These approaches take advantage of the high grain boundary mobility during the high sintering temperature. Optimization of these techniques will be a major part of the materials processing efforts in FY2017.

To develop further up-scaled capabilities to fabricate alnico magnets in prototype sizes and shapes, the powder-based approach for binder-assisted compression molding will be up-scaled to maintain full-density final-shape as-sintered microstructures. These samples will be the starting point for development of fixtures and processing parameters to meet the challenge of grain growth and correct alignment to generate improved magnetic properties in full scale magnets.

To enable extensive experiments on compression molding and other bulk magnet fabrication methods, additional gas atomized pre-alloyed powder batches will be produced with high purity and desired composition, using methods and parameters that should be transferrable to an industrial partner. The first alloy design to be tested in a full-scale final shape (as part of a parallel project on advanced motors with UQM) will be a Co-lean alnico 8H with high Ti and minor Nb addition, as reported herein with elevated coercivity. The second magnet alloy design may also be a Co-lean version of alnico 8 that is under investigation and should be developed enough for initial testing in about a year, but will need to be adapted for the grain alignment process that may take an additional year.

The third development stage for "super-alnico" (with tetragonal distortion of the Fe-Co phase) is anticipated to be sufficiently complete in another 2 years to assess the viability of the concept, as well. If even the first alloy design stage can provide high energy non-RE permanent magnets that demonstrate improved performance in an experimental motor, this could catalyze rapid growth of the US-based high energy PM industry and lead to expansion of existing US manufacturing capacity for advanced PM traction motors.

Theoretical methods will be used to improve cluster expansion models to utilize 6-element Al-Ni-Fe-Co-Ti-Cu systems (alnico 8H and 9) to permit realistic phase equilibria testing. Monte Carlo (MC) simulations &

enabling kinetic MC simulations will be performed to study the spinodal & annealing processes. Structures and phases obtained from the MC simulations will be verified with experimental results and will be used for calculating magnetic properties and driving forces to extend phase field and micro-magnetic microstructure calculations, enabling improved selection of magnetic annealing parameters and rapid draw cycle specification.

Continue characterization of extensive series of alnico 8H and, especially, Co-lean samples to verify theory predictions/actual effects from alloy & processing variations and correlating magnetic properties and nano-structure. Utilize new NREL collaboration to add additional mechanical and thermal conductivity data, as the magnet alloys continue to be developed. Expand ORNL studies to include temperature dependent magnetic properties and FEM for motor design to help in the effective use of optimized alnico magnets.

FY 2016 Presentations/Publications/Patents

Invited Talks only

1. I.E. Anderson, “Development of Radically Enhanced alnico Magnets (DREaM)”, 13th Joint MMM-Intermag Conference, San Diego, California, Jan 14, 2016
2. I.E. Anderson, “Improving Performance of a High Temperature Permanent Magnet Alloy”, MS&T, Columbus, OH, Oct. 4-8, 2015.
3. C.Z. Wang, “Advanced computer simulations and characterization for design of improved permanent magnets”, 145th ANNUAL MEETING & EXHIBITION February 14 – 18, 2016 • Nashville, Tennessee.
4. W. Tang L. Zhou, M. J. Kramer, I. E. Anderson, and R. W. McCallum, “Role of magnetic annealing temperature, time and applied magnetic field on the microstructural and magnetic property evolution in Alnico 8 magnets”, *presented in International symposium on advanced permanent magnetic materials 2015, Beijing University of Technology, in May 9-11, Beijing, China.*
5. W. Tang, L. Zhou, A. G. Kassen, A. Palasyuk, E. M. White, K.W. Dennis, M. J. Kramer, I. E. Anderson, and R. W. McCallum, “New Alnico magnets fabricated from pre-alloyed gas atomized powder through diverse consolidation techniques”, *presented in Intermag2015, May 11-15, Beijing, China.*
6. L. Zhou, “Microstructural evolution in alnico alloys”, XXIV International Materials Research Congress 2015, Cancun, Mexico

Publications

1. I. E. Anderson, A. G. Kassen, E. M. H. White, L. Zhou, W. Tang, A. Palasyuk, K. W. Dennis, R. W. McCallum, and M. J. Kramer, "Novel Pre-Alloyed Powder Processing of Modified Alnico 8: Correlation of Microstructure and Magnetic Properties," *Journal of Applied Physics*, **117**, 17d138 (2015). 10.1063/1.4916996
2. A. Jesche, L. Ke, J. L. Jacobs, B. Harmon, R. S. Houk, and P. C. Canfield, "Alternating Magnetic Anisotropy," *Physical Review B*, **91**, 180403 (2015). 10.1103/PhysRevB.91.180403
3. L. Q. Ke and M. van Schilfgaarde, "Band-Filling Effect on Magnetic Anisotropy Using a Green's Function Method," *Physical Review B*, **92**, 014423 (2015). 10.1103/PhysRevB.92.014423
4. A. Mendoza-Garcia, H. Zhu, Y. Yu, Q. Li, L. Zhou, D. Su, M. J. Kramer, and S. Sun, "Controlled Anisotropic Growth of Co-Fe-P from Co-Fe-O Nanoparticles," *Angewandte Chemie International Edition*, **54**, 9642-9645 (2015). 10.1002/anie.201503386
5. W. Tang, L. Zhou, A. G. Kassen, A. Palasyuk, E. M. White, K. W. Dennis, M. J. Kramer, R. W. McCallum, and I. E. Anderson, "New Alnico Magnets Fabricated from Pre-Alloyed Gas-Atomized Powder through Diverse Consolidation Techniques," *IEEE Transactions on Magnetics*, **51**, 2101903 (2015). 10.1109/tmag.2015.2437355
6. X. Zhao, L. Ke, M. C. Nguyen, C.-Z. Wang, and K.-M. Ho, "Structures and Magnetic Properties of Co-Zr-B Magnets Studied by First-Principles Calculations," *Journal of Applied Physics*, **117**, 243902 (2015). 10.1063/1.4922984

7. Lanping Yue, Yunlong Jin, Wenyong Zhang, David J. Sellmyer, "Magnetic Force Microscopy Study of Zr_2Co_{11}-Based Nanocrystalline Materials: Effect of Mo Addition," *Journal of Nanomaterials* **2015,** 151740 (1-5) (2015); doi:10.1155/2015/151740.
8. Tusharbhai Rana, Priyanka Manchanda, Balamurugan Balasubramanian, Arti Kashyap, Tieren R. Gao, Ichiro Takeuchi, Jun Cui, Subhayan Biswas, Renat Sabirianov, David J. Sellmyer, and Ralph Skomski, "Micromagnetism of MnBi:FeCo Thin Films," *J. Phys. D: Appl. Phys.* ***49****, 075003* (1-6) (2016); doi:10.1088/0022-3727/49/7/075003.
9. W.Y. Zhang, R. Skomski, A. Kashyap, S. Valloppilly, X.Z. Li, J.E. Shield, and D.J. Sellmyer, "Coercivity and Nanostructure of Melt-Spun Ti-Fe-Co-B-Based Alloys," *AIP Advances* ***6***, 056001 (2016).
10. R. Skomski, J.M.D. Coey, "Magnetic Anisotropy-How Much is Enough for a Permanent Magnet?" *Scripta Materialia* **112**, 3-8 (2016).
11. R. Skomski, "Permanent Magnets: History, Current Research, and Outlook," in: *Novel Functional Magnetic Materials*, Editor: A. Zhukov, Springer, Berlin 2016, p. 359-395.

Patents/Disclosures

ISURF # 04355 - Palasyuk, et al. - Cobalt-Lean Alnico Alloy, Provisional US Patent filed November 4, 2015.

ISURF # 4487 – Anderson, et al. –Solid State Grain Alignment of Heat Treatable Permanent Magnets in Near-Final Shape, Provisional US Patent filed March 31, 2016.

6.3 Multilayered Film Capacitors for Advanced Power Electronics and Electric Motors for Electric Traction Drives

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Abstract/Executive Summary

Biaxially oriented polypropylene (BOPP) film capacitors are the most suitable technology for high voltage, high temperature, and high ripple current power electronic systems in high performance electric vehicles (EVs). These capacitors, however, occupy 1/4 to 1/3 of the power electronic unit and have a 50% voltage derating above 85°C due to their drastically deteriorated breakdown strength and lifetime at high temperature. Development of a new dielectric material system for capacitors to increase temperature use and reduce size is critical in many EV related applications. Multilayer dielectric film developed by PolymerPlus and team has demonstrated improved dielectirc constant and breakdown strength as compared to BOPP films. In this program, several film formulations were developed and investigated for dielectric performance and further down-selected for production scale up. Because this technology uses commercial polymers, fabrication of film rolls to demonstrate scalability for initial capacitor fabrication trials was successfully achieved. The film production scale up, metallization and capacitor prototype fabrication was successfully demonstrated in Year 1 of the program. The fabricated capacitor prototypes will be tested for applications in Advanced Power Electronics and Electric Motors for Electric Traction Drives. Out-performing BOPP capacitors with increased performance, it is also critical to show price reduction in multilayer film based capacitors.

Accomplishments

- Multilayer dielectric film processing and production scale-up
  - Developed and processed several film formulations with varying number of layers and film thicknesses
  - Characterized and optimized the film formulation for improved dielectric performance
  - Completed film stretching trials and alternative approaches to reduce the multilayer film thicknesses to 4 µm.
  - Demonstrated development of multilayer film in 4 to 12 µm thickness range in this year of the program.
- Multilayer film production scale-up
  - Down-selected a film formulation to demonstrate film production scale-up
  - Fabricated two rolls of 3000 ft. film (8 µm thickness) for capacitor fabrication trials
- Capacitor designing and 100 µF capacitor fabrication
  - Multilayer film rolls were metallized and delivered for capacitor fabrication

- Capacitor prototype design finalized and simulations completed
- 100 µF capacitor prototypes were fabricated and testing of the parts is in progress for advanced power electronics components

- Material understanding and new material development
  - A detailed understanding of materials is currently being developed in current material systems This knowledge will be used to develop new multilayer films for dielectric applications.

Introduction

For high performance electric vehicles (EVs), film capacitors are the most suitable technology for high voltage, high temperature, and high ripple current power electronic systems. Current state-of-the-art technology uses biaxially oriented polypropylene (BOPP) capacitors usually occupy 1/4 to 1/3 of the power electronic unit and have a 50% voltage derating above 85°C due to their drastically deteriorated breakdown strength and lifetime. Also, compared to ceramic (e.g., multilayer ceramic or glass capacitors) and electrolytic (e.g., Al) capacitors, polymer film capacitors have advantages in terms of graceful failure, ultra-stable capacitance, and capability of handling large ripple currents, and are proved to be most suitable for advanced power electronics in EVs. It is also interesting to note that BOPP has reached its development threshold and industry still requires a significant improvement in energy density and temperature use. Many attempts to develop new material systems in last decade are limited to laboratories or very small quantities. One of the key criteria for new material development is demonstrating scale-up capability in addition to improved properties.

To overcome these challenges, PolymerPlus and team proposed multilayer film based technology, which has demonstrated improved energy density films in its earlier development work. [1-9] In this program, PolymerPlus, SBE Inc., Oak Ridge National Laboratory (ORNL) and Case Western Reserve University (CWRU) are jointly working on multilayer polymer film systems to increase the high temperature performance and stability of the film, and miniaturize film capacitors to reduce cost for advanced power electronic systems in EVs. This unique multilayer film (MLF) coextrusion technology has capability to achieve high temperature capability and high energy density at the same time. The overall goal of the project is to achieve all the requirements for DC-link capacitors listed in Table 6-2. Development of a multilayered film combining a high energy density polymer with a high breakdown/low loss polymer, high energy density and low dielectric/hysteresis losses temperature, it is possible to achieve increased temperature performance.

Table 6-2: Advanced PEEM Program DC-link Capacitor Targets

Capacitance (µF)	>1000
Voltage rating (V_{DC})	650-900
Tanδ at 10 kHz	< 0.02
ESR (mΩ)	< 2
ESL (nH)	≤ 5
Temperature (ºC)	140
Ripple current (A rms)	100
Failure mode	benign
Lifetime (hrs)	>20,000
Volume (L)	≤ 0.6
Cost ($)	≤ 30
ESR: equivalent series resistance; ESL: equivalent series inductance	

In year 1 of the program, PolymerPlus demonstrated fabrication of the high temperature films by systematically investigating various material formulations. Film thickness reduction down to 4 µm was also demonstrated in this year of the program. Additionally, film production scale-up of 8 µm thickness MLF was achieved successfully for film metallization. The metallized films were further used to fabricate multilayer film based capacitors at SBE and ORNL.

Approach

Multilayer Film Processing

Using a film coextrusion process, schematically shown in Figure 6-19, multilayered films with different polymers and formulations were processed in year 1 of the program. The films were coextruded at PolymerPlus using its in-house coextrusion line to produce several hundred feet long film rolls for initial dielectric characterization. The schematic of the coextrusion processing line and the layered structure consisting of two polymers feeding through two different extruders is shown in Figure 6-19. An image of PolymerPlus coextrusion line is also shown. The coextrusion process consists of a multi-channel feedblock where two polymers, represented by Resin A and Resin B, meet to form a melt stream with two layers. As the polymer melt fed through a series of multiplier die elements, each of which doubles the number of layers through melt cutting, spreading and stacking process to create a layered structure ranging from few layers to few hundreds of layers. The number of layers is determined by the number of layer multiplier dies used in the coextrusion process. Multilayer dielectric films can contain different number of layers and the relative composition of the two polymers to achieve the optimum performance.

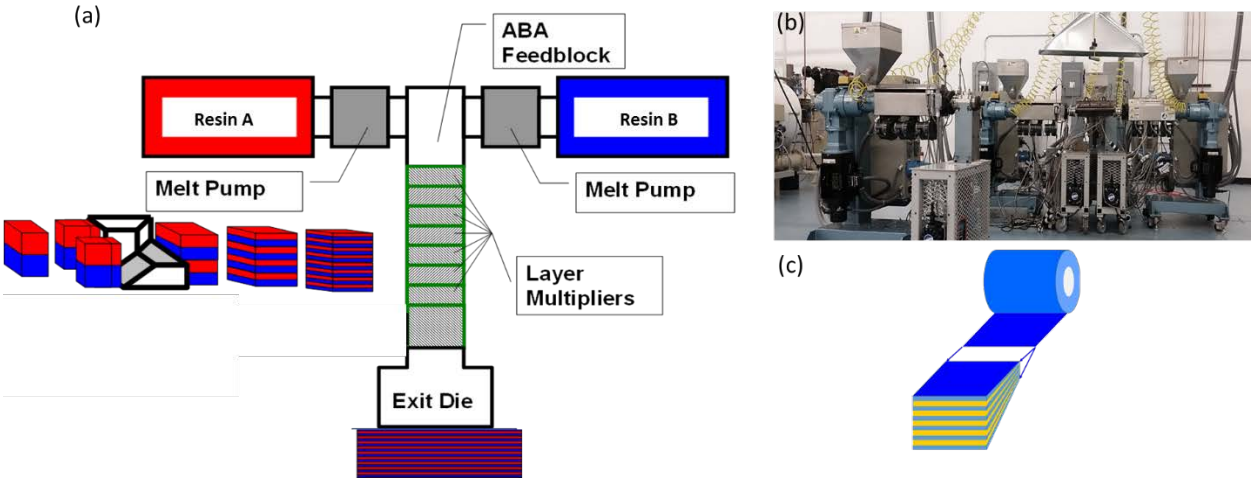

Figure 6-19: (a) Coextrusion process schematic showing a two polymer system, with alternating layers of Resin A and Resin B in a film structure. Example of layer multiplying die and layering process is also shown (b) PolymerPlus coextrusion line (c) a schematic representation of dielectric film structure consisting of alternating layers of two polymers

Prior to coextrusion process, the polymer resins are analyzed for rheological properties ensuring proper melt flow stability to achieve good layer structure, and integrity. The two resins selected for this project have following properties:

1. **Resin A:** high dielectric constant, low breakdown high energy density
2. **Resin B:** high breakdown strength, low dielectric constant

The resins were processed to achieve layer film structure, with number of layers that can be varied from 3 to 4097. In this project, examples of multilayer films with several different number of layers are discussed in this report.

Dielectric Film Production Scale-up

Various film formulations with varying number of layers and film thicknesses were processed to evaluate the dielectric performance of the film, which was followed by down-selection of one formulation for production scale-up. The film production scale-up activities included production of two 3000 ft. (length) x 12" (width) x 8

µm (thickness) rolls for metallization and capacitor prototype fabrication. Dielectric films are further characterized for thickness and breakdown strength properties prior to metallization and capacitor winding activities

Capacitor Designing and Fabrication

SBE and ORNL investigated baseline BOPP film material in an industry relevant inverter, which will be compared with multilayer film capacitor. Details of capacitor test kit and design parameters are summarized in results and discussion. The BOPP capacitor testing was performed at SBE and ORNL.

Results and Discussion

Multilayer Film Processing

A multilayer film system, with a fixed composition ratio of Resin A and Resin B was processed with number of layers varied from X to Y to Z, where X, Y and Z = 2^n+1 and n is the number of multipliers. As the ratio of the two materials was kept constant, increasing the number of layers changed the thickness significantly. The number of layers were changed approximately by a factor of 4 in these three systems i.e. for a given film thickness, the individual layer thickness of Resin A and Resin B varied by a factor 4 in these systems. It is interesting to note that film thicknesses down to 4 µm are comparable with current commercial BOPP film thickness of 3-4 µm. The individual layer thicknesses can vary from few tens of nanometers to few hundreds of nanometers in these films.

Table 6-3. Analysis of MLFs

Film System	No. of Layers	Film Thickness
1-Resin A/Resin B	X	11, 8, 6
2-Resin A/Resin B	Y	12, 8, 6, 4
3-Resin A/resin B	Z	12, 8, 6, 4

Analysis of MLFs with X, Y and Z number of layers and thicknesses ranging from 12 to 4 µm was completed for thickness and breakdown strength uniformity. High sampling frequency testing was completed on rolls at regular intervals across the film width and down the film length to understand the spatial property variation over known areas for the samples. For all the film samples the thickness variation of less than ± 1.0 was measured, with an exception of a couple of samples. For a commercial BOPP films this variation is typically within 5% of the average film thickness. As the multilayer film technology matures with process modifications, PolymerPlus will be working on improving the film thickness uniformity similar to BOPP films.

Multilayer Film Dielectric Properties

The films were also characterized for various dielectric properties such as - breakdown strength, D-E hysteresis, and broadband dielectric spectroscopy for dielectric constant. The comparison of the breakdown properties multilayer film systems with various formulations is shown in Figure 6-20. It is interesting to note that the breakdown strength properties followed a similar trend irrespective of the number of layers in the current investigation. The overall breakdown strength increased with decreasing layer thickness without any significant change in number of layers.

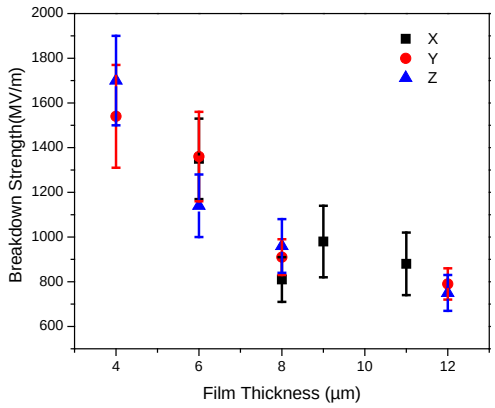

Figure 6-20: Breakdown strength of multilayer film with varying number of layers and film thicknesses

Comparison of D-E hysteresis properties: The D-E hysteresis properties of the three different number of layers and variable thicknesses were measured at different applied fields. A comparison of the hysteresis loops at 6 kV applied field is shown in Figure 6-21. The overall hysteresis losses were smaller in X layer system as compared to Y and Z layer films, as noticed from the hysteresis loop area. The D-E loops did not show any changes in the slope for most compositions. Similar slopes suggested that the dielectric constant is not affected significantly as a function of number of layers and layer thicknesses. Dielectric constant as high as 4 was measured in some formulations, measured at 1 kHz. The measured dielectric constant is 1.8X times higher than the BOPP dielectric constant of 2.2. Additionally, a significantly higher breakdown strength was observed in MLFs.

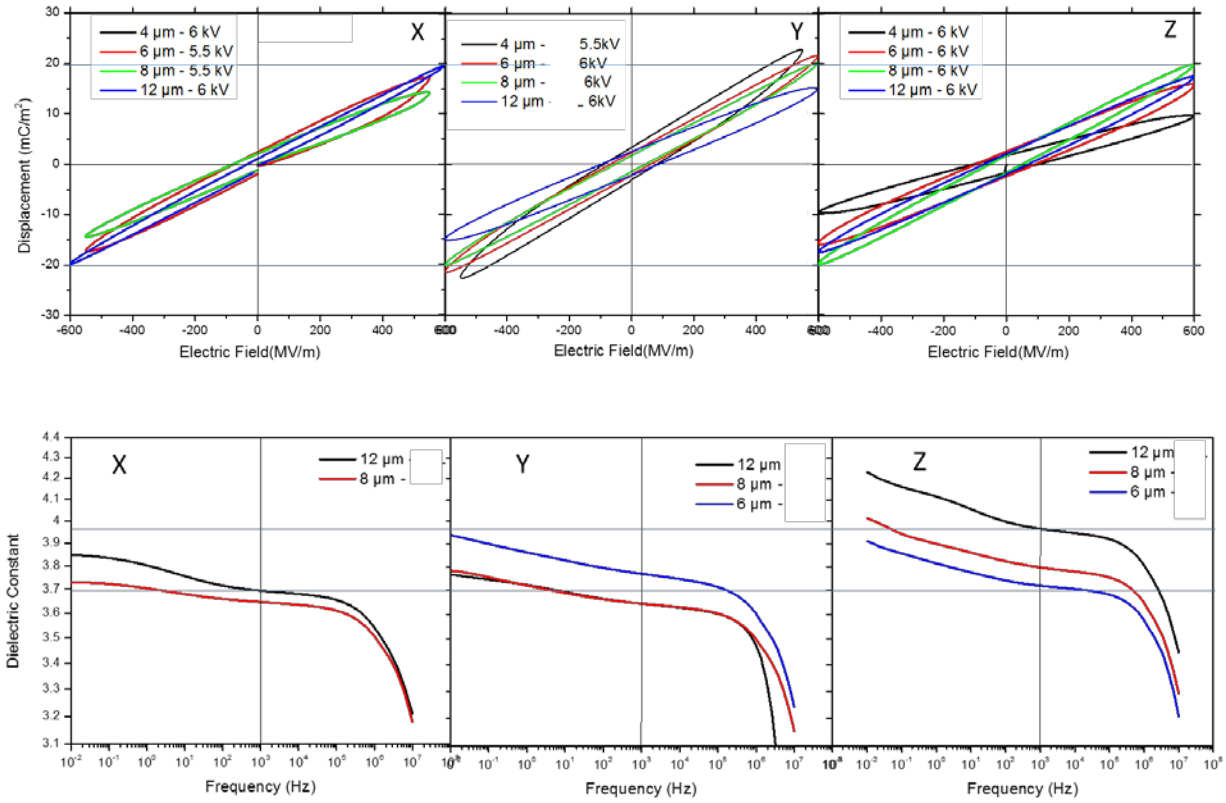

Figure 6-21: Comparison of (top) D-E hysteresis loops and (bottom) dielectric constant

Furthermore, the high temperature stability of this multilayer films was also demonstrated. An example of breakdown strength as a function of temperature in Resin A/Resin B film system with X number of layers is shown in Figure 6-22. It was observed that the breakdown strength at 140°C was as high as 1000 MV/m in 6 μm films, which is important in proposed use in DC-link capacitors.

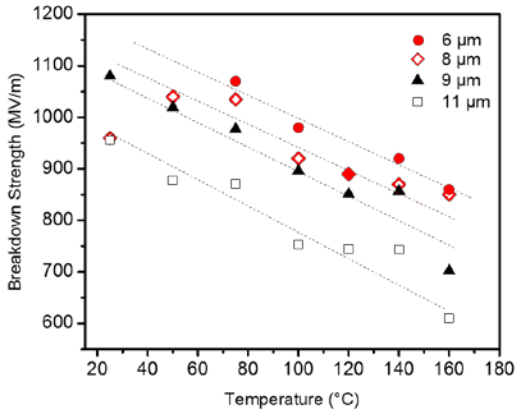

Figure 6-22: Breakdown strength of multilayer dielectric film with different thickness and same number of layers as a function of temperature

Multilayer Film Production Scale-up and Metallization

Based on the detailed analysis of various film formulations, one film system was downselected for production scale-up and capacitor fabrication trial. Two rolls of 3000 ft. films, with 8 µm thickness, were fabricated and metallized. As PolymerPlus uses commercially available resins, the film production scale-up is viable to produce commercially relevant quantities. It is interesting to note that the metallization was carried out on conventional BOPP metallizers without any equipment modifications. Multilayer film product can be directly used as a drop-in product in existing capacitor fabrication processes without significant process modifications.

Multilayer film metallization activities were also completed in the first year of the program. A 3000 ft. x 12" film roll was metallized and converted into 8 reels of 500 m film samples as shown in Figure 6-23. The metallized reels were delivered to SBE for capacitor fabrication trials.

Figure 6-23: (left) example of 3000 ft. film roll supplied for metallization, (right) 500 m reels of metallized film for capacitor fabrication trials.

Capacitor Designing and Fabrication

SBE and Oak Ridge investigated baselining BOPP material based capacitors for comparison with new MLF film capacitors using an industry relevant inverter.

The baseline evaluation of the capacitor using the inverter shown in Figure 6-24 at the ORNL NTRC was completed. While the load available did not allow exercising the inverter at full power operating conditions, the low power test results have provided very useful data. A better understanding of thermal coupling to ambient/coolant in a real application has been obtained along with the contribution of the bus bar and IGBT losses to the capacitor hotspot temperature. This data was used to adjust the SBE capacitor thermal and loss model to obtain the fit shown. With an excellent baseline for the polypropylene film capacitor, MLF windings can be incorporated into the same structure to facilitate a comparison.

Figure 6-24: Inverter using SBE capacitor/bus combined with HP DriveTM module, gate drivers, and control logic supplied by Infineon.

SBE further analyzed the metallized MLFs for mechanical properties to understand the winding parameters. Film winding trials were conducted with different winding tensions between 2.1 to 2.5 N in different metallized film reels. Due to thickness non-uniformity in the film reels, wrinkling issues were observed during winding trials. PolymerPlus has been working on upgrading its processing line with internal funding to address challenges with film wrinkling. In the first attempt by SBE, 25 µF capacitor parts were fabricated followed by mask taping, end spraying and post spray cleaning. The diameters of the windings were measured as 72.9, 72.8, 72.9 and 70.0 mm for the four parts. The measured capacitance was 23.59, 23.98, 25.08 and 22.79 µF, which was close to target value of 25 µF. The capacitors were cured at 125°C for 4 h prior to testing. Typically curing process results in shrinkage of the capacitor size, multilayer film capacitors showed little to no change due to higher temperature stability of the film. The measured capacitance values did not change significantly as <0.7% change was observed in the four parts. An example of a capacitor part is shown in Figure 6-25.

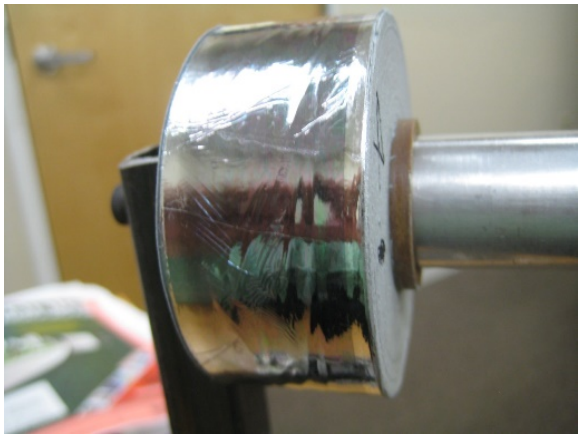

Figure 6-25: Completed winding post end spray and 125°C cure. Diagonal wrinkles were observed due to thickness non-uniformity.

In another capacitor winding trial, the metallized MLF material was used to build 100 µF windings. The two parts fabricated were end sprayed, cured and cleared. These samples were tested only to 500V as initial 25 µF windings demonstrated some issues due to poor winding/wrinkling. One winding failed and the other passed. The remaining good unit was then packaged using the reworked terminals and case for an SBE 700D349 ring capacitor. The completed functional capacitor is presently being evaluated for DC leakage subject to temperature and voltage conditions. The sequence of assembly is documented in the photos, Figure 6-26.

Figure 6-26: (top row, left) Three completed 100mF windings, (top row, right) Prepare crown terminal. (Middle row, left) Prepare base terminal, (middle row, right) Winding with crown and base terminals attached, (bottom row, left) Capacitor winding with terminals shown with plastic case and pouring fixture prior to assembly and potting with RTV (bottom row, right) Completed 100µF part after curing of RTV material

Film Stretching to Reduce Film Thickness

Achieving film thickness down to 4 µm is critical in many EV related applications. As demonstrated earlier film thickness reduction to 4 µm was successfully achieved at PolymerPlus using coextrusion process. An alternative approach to reduce the overall film thickness was also investigated during this year of the program. The approach consisted of producing thicker multilayer film, followed by uniaxial or biaxial stretching of the films to reduce the overall thickness. For film stretching trial on a commercial line, 500 ft. rolls of Resin A/Resin B, with 25 and 12.5 µm thicknesses, were produced at PolymerPlus. The stretching trial involved using oil-heated temperature-controlled roll for film pre-heating followed by slow and fast drawing of the film and annealing process. For the film samples, draw rates of 2.1X and 2.0X was achieved. The 25 µm film thickness was stretched down to 12-13 µm and 12.5 µm film thickness was stretched down to 6-7 µm.

Examples of the two small sections of the stretched film and the corresponding dielectric properties are shown in Figure 6-27. No significant difference in the breakdown properties of the films was observed. It was demonstrated that production of thicker films followed by stretching can be used successfully to achieve film thickness reduction.

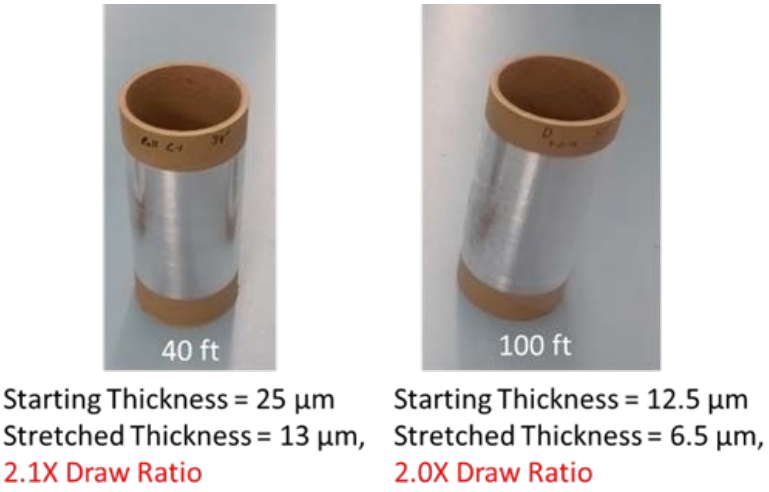

Figure 6-27: Stretched film rolls: (left) stretched from starting thickness of 25 µm to 13 µm, (right) stretched from starting thickness of 12.5 µm to 6.5 µm.

Multilayer Film Mechanisms and New Material Development

Understanding the multilayer film dielectric materials is critical for success in various applications. Some of the issues investigated in this program are as follows. A significant difference between multilayer and blend films was demonstrated in the ultimate dielectric properties such as breakdown strength and lifetime. For multilayered films higher breakdown strength than the linear average of the two components was attributed to interfacial polarization in multilayer films, which reduced electronic conduction in the sample. In contrast, blend films demonstrated various morphologies like island-in-sea and co-continuous phase, depending upon the relative ratio of the materials. Based on the observations and the data, a unique working mechanism for multilayer films was proposed as shown in Figure 6-28. In this mechanism, we propose interfacial polarization from space charges. These interfacial charges serve as effective traps for hot electrons injected from the metal electrodes. Further investigation of these phenomena will be conducted to develop detailed understanding of the multilayer film systems. New material systems will be processed during year 2 of the program.

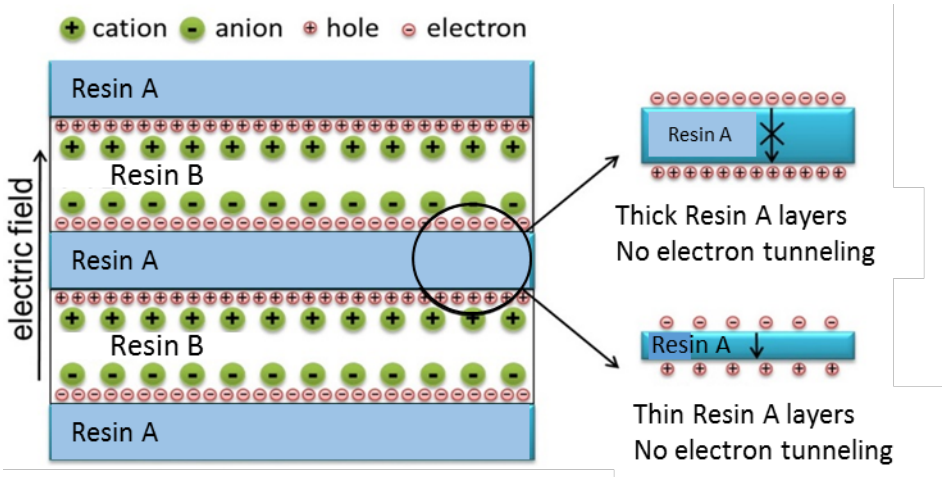

Figure 6-28: Proposed interfacial polarization from both electrons/holes and anions/cations

Conclusions and Future Directions

PolymerPlus demonstrated development of multilayer films for capacitor applications using commercial resins. Improved dielectric constant and increased breakdown strength values of multilayer films were higher than current state-of-the-art BOPP dielectric film used for capacitor applications. Several film formulations were investigated in the first year of the program to down-select for capacitors prototypes for advanced power electronics and electric motors for electric traction drives. In the film formulation investigation, a film thickness reduction from 12 to 4 µm was successfully achieved. Further film production scale-up was also demonstrated in manufacturing two 3000 ft. x 8 µm film rolls for metallization and capacitor fabrication. SBE fabricated 100 µF prototypes for evaluation at SBE and ORNL. CWRU developed fundamental understanding of multilayer dielectric films, which will be used to evaluate new film systems for increased dielectric constant and breakdown strength, and reduced losses. The metallized film was successfully used to build 100 µF windings. The completed functional capacitor is presently being evaluated for DC leakage subject to temperature and voltage conditions.

The future work will demonstrate production of 4 µm thickness film to compare against the commercial BOPP capacitors. Film production scale-up up to 10,000 ft will also be demonstrated on PolymerPlus coextrusion process. The team will also fabricate and test capacitor prototypes in 500 to 1000 µF range for proposed EV applications. A cost model will also be developed in year 2 of the program for multilayer dielectric film based capacitors and compared with BOPP capacitors.

FY 2016 Presentations/Publications/Patents

1. Deepak Langhe, Lei Zhu, Michael Brubaker, Laura Marlino, "Kick-off Meeting", November 2015
2. Deepak Langhe, Lei Zhu, Michael Brubaker, Laura Marlino, "Multilayered Film Capacitors for Advanced Power Electronics and Electric Motors for Electric Traction Drives", February 2016
3. Mike Brubaker et al. (SBE, ORNL, and Infineon) on the "ONRL NTRC inverter testing" presented at PCIM, May 2016.
4. Deepak Langhe, Lei Zhu, Michael Brubaker, Laura Marlino, "Multilayered Film Capacitors for Advanced Power Electronics and Electric Motors for Electric Traction Drives", June 2016
5. Deepak Langhe, Lei Zhu, Michael Brubaker, Laura Marlino, "Multilayered Film Capacitors for Advanced Power Electronics and Electric Motors for Electric Traction Drives", July 2016

References

1. Baer, E.; Hiltner, A.; Shirk, J. S.; Wolak, M. A. US 20100172066, 20100708, 2010.
2. Mackey, M.; Hiltner, A.; Baer, E.; Flandin, L.; Wolak, M. A.; Shirk, J. S., J. Phys. D: Appl. Phys. 2009, 42, 175304.
3. Mackey, M.; Schuele, D. E.; Zhu, L.; Flandin, L.; Wolak, M. A.; Shirk, J. S.; Hiltner, A.; Baer, E., Macromolecules 2012, 45, 1954-1962
4. Mackey, M.; Schuele, D. E.; Zhu, L.; Baer, E., J. Appl. Phys. 2012, 111, 113702.
5. Zhou Z, Mackey M, Carr, Zhu L, Flandin L, Baer E, J. Polym. Sci. Part B Polym. Phys, 50 (14), 993-1003 (2012)
6. Tseng J K, Tang S, Zhou Z, Mackey M, Carr, J M, Mu R, Flandin L, Schuele D E, Baer E, Zhu L, Polymer 55, 8-14 (2014)
7. Langhe, D.; Ponting, M.; Coextrusion Processing of Multilayered Dielectric Polymeric Films, SPE ANTEC 2015, Orlando, FL, 2015.
8. Langhe, D.S.; Ponting, M.; High Temperature Multilayered Polymeric Films for Capacitor Applications, SPE ANTEC 2014, Las Vegas, NV, 2014.
9. Langhe D., Ponting M., Manufacturing and Novel Applications of Multilayer Polymer Films, Plastics Design Library, ISBN 978-0-323-37125-4 (2016)

6.4 High Performance DC Bus Film Capacitor

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Contract No.: DE-EE0006433

Abstract/Executive Summary

For hybrid-electric and all-electric vehicles, state-of-the-art DC-link capacitors negatively impact the electric drive system due to their large volume, high weight, and low maximum temperature, which often requires cooling systems. To reduce these impacts and accelerate the adoption of electric light-vehicle transportation, the Department of Energy has proposed technical targets that are given in Table 6-3.

Table 6-3: DC link capacitor requirements

	Min	Max
Ambient temperature	-40°C	140°C
Volume		0.6 l
Cost		$30
Failure mode	Benign	
Life @ 10% capacitance loss	13,000 hrs	

To meet these requirements, GE Global Research has developed metallized-film capacitors utilizing polyetherimide films. Polyetherimide was chosen due to its relatively high dielectric constant of 3.2 and high glass transition temperature of 217°C. The high dielectric constant aids volume reduction, and the high glass transition temperature enables high temperature operation.

Manufacturing process problems were encountered and resolved for polyetherimide films, unique from the industry standard process for bi-axially oriented polypropylene films. Working with a supply chain, capacitor modules were assembled from smaller capacitor bobbins. The capacitor modules, ranging in size from 100 µF to 700 µF, were delivered for electrical testing at Delphi.

Accomplishments

- Obtained high-quality, low-electrostatic, polyetherimide 4 µm thick films capable of obtaining 80% capacitor winding yield
- Obtained high-quality, low-electrostatic, polyetherimide 3.5 µm thick films capable of obtaining 60% capacitor winding yield

- Identified process conditions that minimized electrostatic buildup in films; optimized transverse and machine-direction wrinkles; resulted in consistent, tight capacitor bobbins; optimized electrical contact through end spray; and resulted in successful integration of capacitor bobbins into larger assemblies
- Delivered Phase I prototype capacitors to Delphi for testing
  - Three 100 μF capacitor modules and two 300 μF capacitor modules were built
  - Constituent capacitors were 13 μF or 25 μF, respectively
  - Testing to be completed in the first week of November
- Completed Phase II capacitors, and delivered to Delphi for testing
  - Four 300 μF capacitor modules and three 700 μF capacitor modules were built
  - Constituent capacitors were 50 μF or 25 μF, respectively
  - Testing to be completed in second week of December
- Achieved TRL 5 for the Phase I capacitors and TRL 4 for the Phase II capacitors. MRL 3 was demonstrated for both the Phase I and Phase II capacitors.

Introduction

In a power inverter module, a capacitor is an essential component, decoupling the effects of the inductance from the DC voltage source to the power bridge. The bus link capacitor provides a low impedance path for the ripple currents associated with a hard-switched inverter. However, current commercial capacitor technology imposes significant costs and design constraints on such systems. Electrolytic capacitors suffer from low ripple current capability, high thermal resistances, bulky package, low temperature capability and lifetime.

High performance inverters for electric vehicles, aircraft, and alternative energy have turned to film capacitors. For example, Delphi and Ford have used BOPP film capacitors in inverter designs. The problem with current film capacitors is the high cost and large size, which contributes to a large under-hood footprint due to energy density limitations, and the need for thermal management as a result of limited operating temperature (<125°C).

The DOE has defined performance targets for capacitors with improved thermal capability and energy density, as well as cost targets which would enable broad adoption of such capacitors by industry.[1] Development of high-dielectric strength, low loss, thermally stable and sufficiently thin dielectric films is a key technology for meeting these capacitor performance targets.

Unlike other approaches utilizing inorganic dielectrics or high dielectric loss polymers, GE is pursuing a high temperature polymer with a moderate dielectric constant and low dielectric loss. [2-6]. GE has actively led the development of Polyetherimide (PEI) film for conversion to high temperature capacitor applications.[7-8] A glass-transition temperature of about 217°C and dielectric strength of >500 kV/mm makes it an ideal candidate to meet the DOE's DC bus capacitor performance goals. PEI films are produced by melt extrusion and commercialized in various thicknesses above 13 μm. GE's past research and development has repeatedly confirmed the superior dielectric, mechanical, and thermal performance of PEI film for film capacitor applications. A primary technical challenge for commercial use is the melt extrusion of very thin PEI films (<10 μm), with consistent thickness and no wrinkling during extrusion, winding, or subsequent conversion.[9] Meeting these goals for a film scale-up process will enable reduced system volume, weight and cost, increased thermal stability, and improved design freedom for electrical vehicle systems as envisioned by DOE.

Approach

To address the need for a small, reliable, low-cost, high-temperature, metallized-film capacitor for DC-link applications, GE Global Research has built a supply chain capable of meeting the requirements of each process step. A schematic of a metallized film capacitor supply chain is given in Figure 6-29.

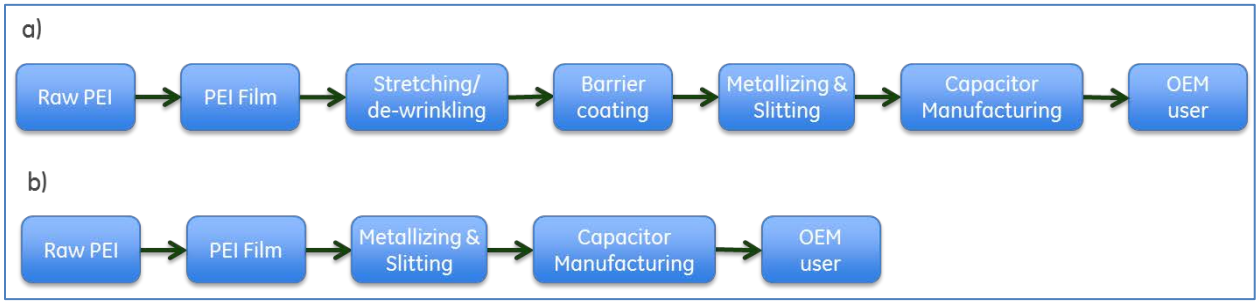

Figure 6-29: Metallized film capacitor value chains. a) The value chain envisioned at the beginning of the reporting period, and b) the value chain at the end of the reporting period. Suppliers have been validated as capable of meeting requirements for each step.

Working with multiple suppliers at each point in the value chain, GE Global Research has understood the interfaces between process steps and the unique challenges of processing PEI, an amorphous thermoplastic, compared to polypropylene, a semi-crystalline thermoplastic. When appropriate, process steps were removed, either from lack of need or from lack of economic value.

For each step in the value chain, at least two suppliers are capable or will soon be capable of process results necessary to meet the program objectives. By utilizing existing suppliers, domain expertise that already existed in the supply base did not need to be recreated, which accelerated the program.

Delphi was subcontracted to serve in the role of an OEM user. Delphi's feedback as the voice of the customer throughout the project has been influential in helping the project advance.

Results and Discussion

PEI films

Throughout the 2016 reporting period the quality of the PEI films improved even as the films were manufactured thinner. 21 rolls of film were produced in three manufacturing runs by two different suppliers. The majority, 17 rolls, were from the primary supplier, while the remaining four rolls were from the secondary supplier.

Figure 6-30 visually shows the progression of film manufacturing. In Figure 6-30a, 4 μm film from the beginning of the period is pictured. The periodic machine-direction wrinkles, or tin-can wrinkles, are apparent. Also, visible on the left edge of the image is heavy buildup at the edge of the film, which is due to film that is thicker at the edge. Figure 6-30b, on the other hand, pictures a roll of 3.5 μm film. Neither periodic, machine-direction wrinkles nor thicker edges are observed. Both pictured rolls are 2000 m long. Plots of the film thickness across the web for both 3.5 μm and 4.0 μm films are given in Figure 6-31.

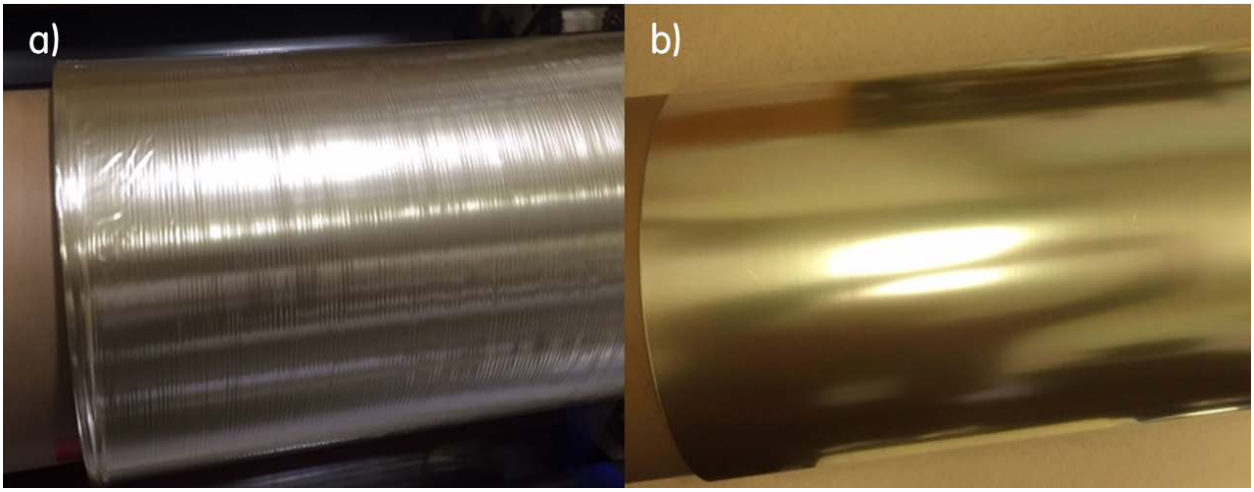

Figure 6-30: Images of PEI films. a) 4.0 µm film produced at the beginning of the reporting period exhibiting machine-direction wrinkles and thick edges and b) 3.5 µm film produced at the edge of the period showing neither wrinkles nor thick edges.

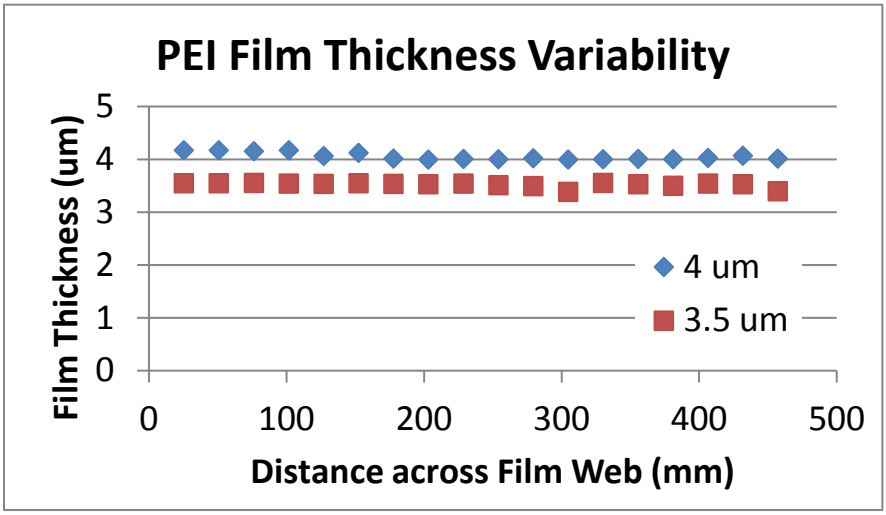

Figure 6-31: Thickness of PEI films as a function of location across the web for 4.0 µm and 3.5 µm films

Based on the continuous improvement from the primary supplier, GE Global Research believes this supplier can produce 4.0 µm and 3.5 µm films with increasing quality. In time, a roadmap could be developed to produce even thinner films.

Concurrent to working with the primary supplier, GE Global Research engaged a secondary supplier to evaluate their extruded PEI films. In depth studies with this film were not performed, but a basic understanding of supplier capability and film goodness was gained. Rolls of both 4 µm and 5 µm were produced. Generally, the quality of the films was reasonable. Some processing difficulties were encountered, but these difficulties were expected because no process optimization was performed to account for differences in the films coming from different suppliers. Several capacitor bobbins were produced that passed all initial manufacturing screening tests, validating the feasibility of PEI films from the secondary supplier.

Stretching and de-wrinkling

At the beginning of the period, there was significant technical and project risk associated with obtaining PEI films that were thin enough and without wrinkles. Poor capacitor performance and winding process yield resulted from film rolls similar to those pictured in Figure 6-30a. A secondary process in which the film was unwound, heated in an oven, and rewound was pursued. Initial results indicated that the degree of wrinkling could be reduced, although quantitative characterization was not performed.

In the same apparatus that was used to reduce film wrinkles, it was possible to stretch the film in both the transverse and the machine directions. Films with starting thickness ranging from 7 µm to 4 µm were stretched, and final thickness down to 3.3 µm were obtained. An image of a roll of 3.3 µm film is shown in Figure 6-32. The film appears nominally wrinkle free, especially in the middle. The roll is noticeably thicker on the outside edges which is confirmed with film thickness measurements presented in Figure 6-33.

Figure 6-32: Photograph of 3.3 µm thick roll of PEI film after secondary processing.

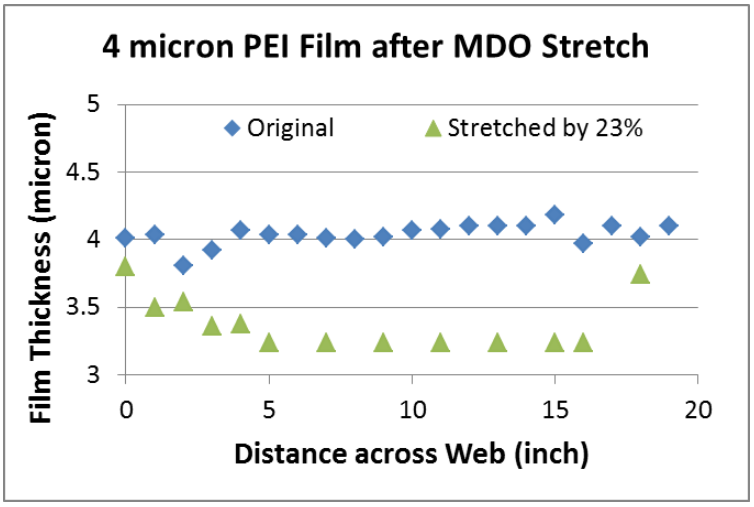

Figure 6-33: Plot of film thickness across the web for a 4 µm thick roll of film that was stretched to 3.3 µm thick in a secondary process. The stretching occurred in the center of the film, and the edges remained close to the original thickness.

In the end, the film suppliers improved the initial quality of the films to the point that secondary processing was not required and the process was abandoned. The efforts to produce acceptable films via secondary processing resulted in two invention alerts; one of which has been filed.

Barrier coating

One of the original premises of the project was that an additional dielectric coating could be applied to the dielectric film, enhancing the breakdown voltage of the film and enabling higher rated voltages with thinner films. Both SiO2 and Al2O3 thin films were considered. Oxide thin films were deposited on free-standing PEI membranes supported on frames as well as in a roll-to-roll process.

Significant phenomenology was observed for the oxide thin films. Obtaining a good oxide required careful control of the PEI film tension during deposition, which could depend on the film tension during framing or web-handling, the differential thermal expansion between the frame and the PEI during deposition, the maximum temperature of the PEI film during deposition, and the residual strain in the oxide thin film as a consequence of the deposition parameters. Some films curled so tightly after release from the mounting frame that they could not be measured. Other films showed apparent cracks in the oxide films in scanning electron micrographs, and these films exhibited poor breakdown characteristics.

An example of successful enhancement of breakdown strength due to the addition of an oxide thin film is given in Figure 6-34. A 6 µm PEI film was coated with 100 nm of SiO2. The samples with a thin film oxide exhibited approximately 15% improvement in breakdown strength as determined by the Weibull parameter. There was not a statistically significant difference if the oxide thin film was against the anode or the cathode. The test was conducted with the samples submerged in dielectric oil; the ramp rate was 500 V/s, and anode was a 1/4 in steel ball bearing and the cathode a 2 in diameter Rogovski electrode.

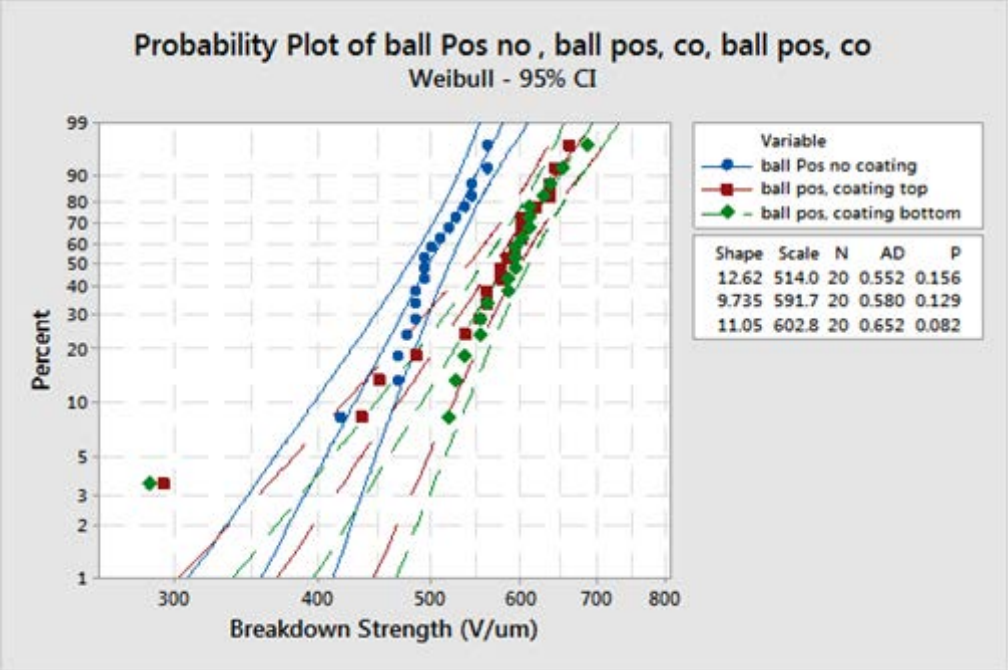

Figure 6-34: Weibull plots of breakdown voltage for a control (blue circles), the coating against the ball electrode (red squares), and the coating against the Rogovski electrode (green diamonds).

Attempting to replicate the lab process with a web process was not successful with a couple of attempts. The web process is most easily tuned with multiple long rolls of film. The 2000m rolls of PEI were too short to successfully tune and stabilize the process. There was competition among the process parameters of film tension, web speed, maximum film temperature, and winding quality. PEI films broke or melted on several occasions, each time requiring the opening of the deposition system.

The project abandoned the oxide thin film coating as a commercially viable technique due to the relatively low improvement in breakdown voltage relative to the projected cost of the vacuum coating process, which was not justified by the risk, the scope, and the cost to develop the roll-to-roll process. To be accretive, the cost of the oxide coating must displace a like cost in the PEI film, by making the PEI film thinner. With additional supply chain and logistics complexity as well as additional yield losses from the added process steps, the benefits from the oxide coating could not meet financial requirements in preliminary cost model projections.

Metallizing and slitting

Substantial progress was demonstrated metallizing the PEI film rolls. An example of a metallized role of film from early in the year is shown in Figure 6-35a, and a roll from the middle of the year is shown in Figure 6-35b. Both rolls are 4 µm films and 2000 m long. The come from different manufacturing batches; the wrinkled roll is from Batch 5 while the other roll comes from Batch 8.

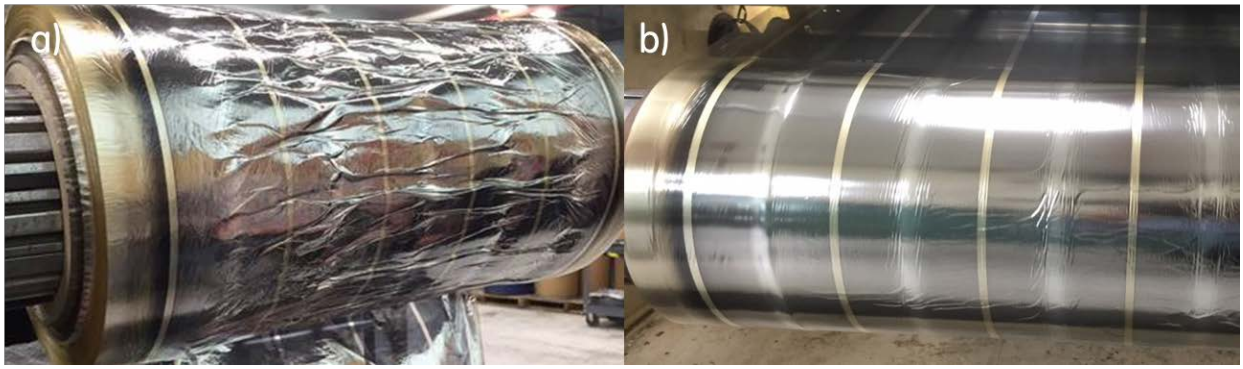

Figure 6-35: Images of two different 4 µm PEI rolls after metallization, indicating the improvement in quality after metallization. a) is from Batch 5, earlier in the period, and b) is from Batch 8, later in the period.

Film tension during metallization was a main process parameter that affected wrinkles, impacting final roll quality. To describe the role of web tension on wrinkles, a qualitative scale was established to grade the magnitude of wrinkles present on a metallized 2000 m roll in which a score of 0 corresponded to no wrinkles and a score of 10 corresponded to severe wrinkling. Several rolls were scored as a function of web tension for both transverse wrinkles (troughs and crests run across the web) and machine direction wrinkles (troughs and crests run along the web). The plot in Figure 6-36 shows the relationship between severity of wrinkles and the web tension. As expected, transverse wrinkles decrease with increasing tension, and machine direction wrinkles increase with increasing tension.

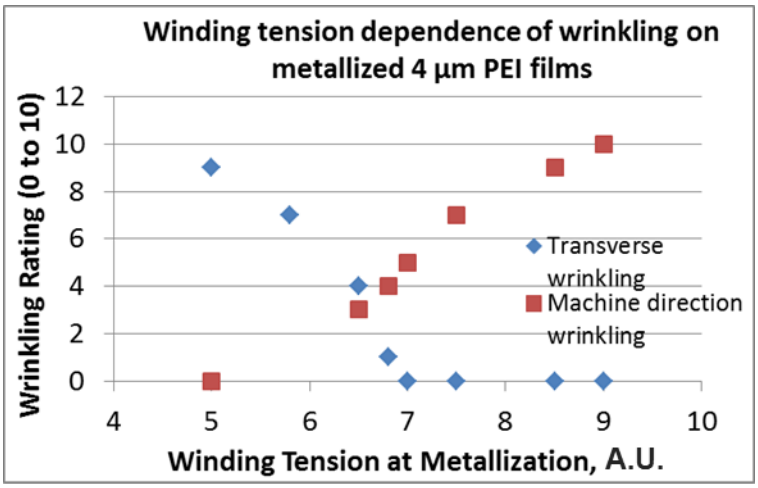

Figure 6-36: Plot of the degree of wrinkling as a function of winding tension at metallization for wrinkles in both the transverse and the machine directions.

After metallization, the rolls are unwound, slit, and rewound. Figure 6-37 shows the images of slit rolls from the beginning and end of the period. A first observation is that while not perfect, the slit and rewound rolls appear much less wrinkled than the original mother roll. Second, the slit rolls do improve in appearance over the period.

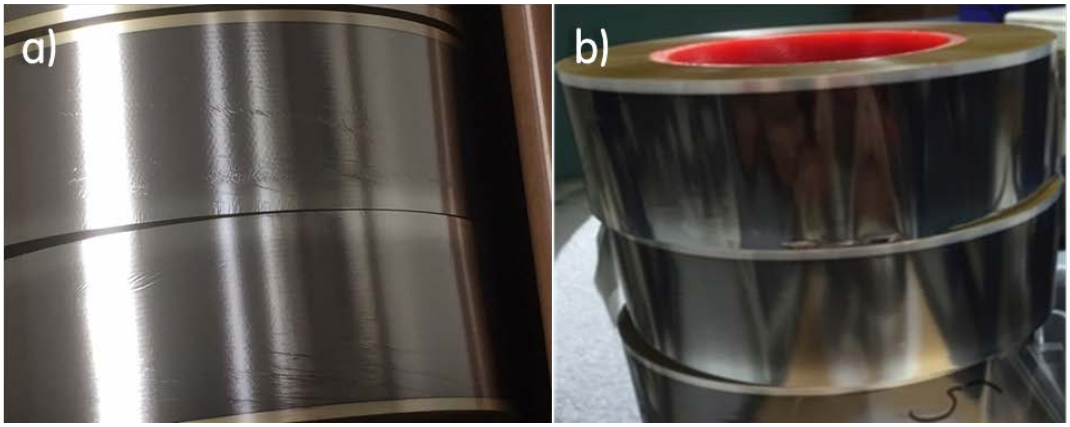

Figure 6-37: Images of 4 µm, slit film rolls from a) Batch 5 and b) Batch 8

Capacitor manufacturing

The process flow used for manufacturing capacitors is given in Figure 6-38. The areas where development effort was focused were winding, end spray, and packaging and potting.

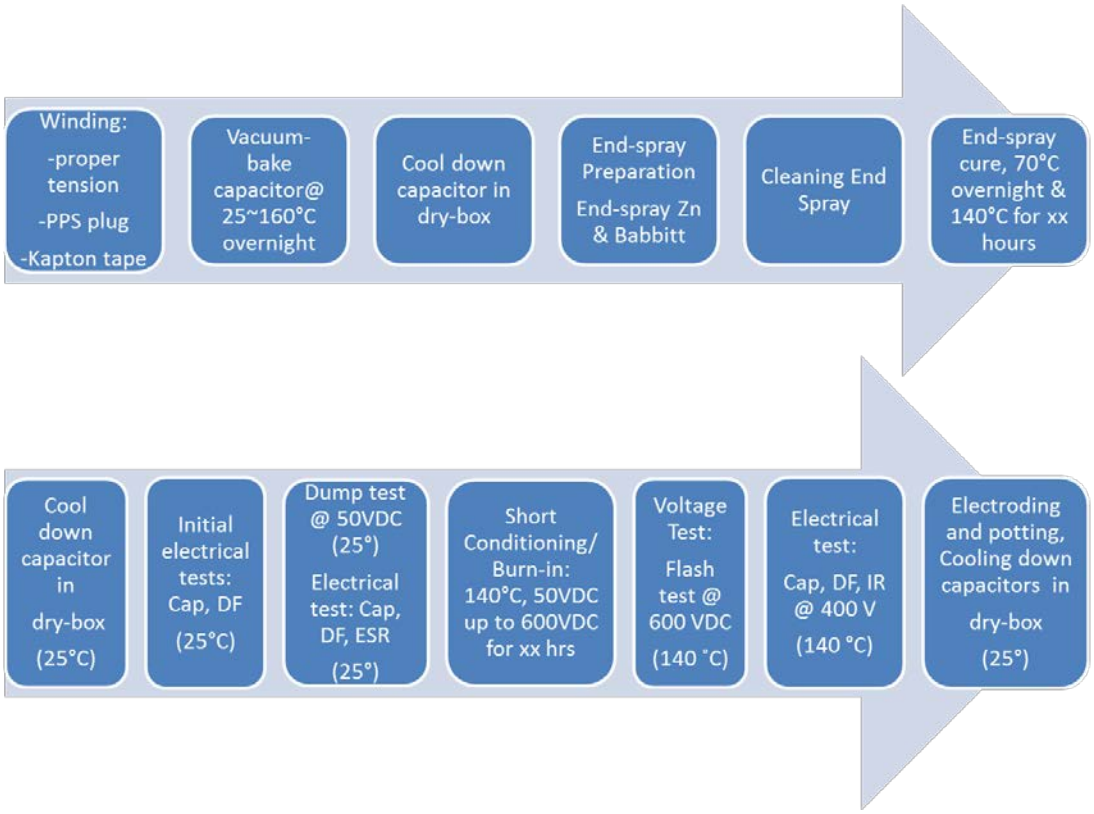

Figure 6-38: The process flow for winding capacitors.

Designs of experiment were performed to understand the role of winding tension on capacitor performance. Winding tensions between 50 g and 300 g were used. The appearance of the capacitor bobbins, the capacitance, and the dissipation factor were used to judge the outcome of the experiment. Images of the profiles of bobbins for various tensions is shown in Figure 6-39. Note that the capacitors are often out of round and the roll edge surface is irregular.

Figure 6-39: Visual examples of capacitor bobbin profiles at various winding tensions. Note the ridged and rough top surface and the out-of-round profile.

Conclusions were difficult to draw from the first experiments due to lack or repeatability of results. Three factors were discovered which enabled a successful second set of experiments.

First, the winding mandrel must be well polished and extremely straight. A mandrel diameter of 3.1 mm gave best results, and deformed or rough mandrels gave very poor capacitor yields.

Second, low static electricity in the PEI film is critical to prevent blocking during winding. Blocking causes the film to stick to itself upon winding and prevents the winding from pulling tight. To minimize static during winding two ionizing sources were installed on the winding machine. At the same time the state of static electricity on the raw PEI films went down as did any additional static that was added during metallization. At this time, the factors that cause static electricity in the films are not well understood and are a subject for future work.

Third, the dissipation factor was a function of the location on the roll from which the capacitor was wound. Capacitors from the beginning and middle of a roll had lower dissipation factor than capacitors from the end of the roll. The plot in Figure 6-40 shows the dissipation factor by manufacturing sequence number for two different pairs of slit rolls. The two plots (1 &2 and 3 & 4) indicate the location of the slit rolls from the original master roll. The factors leading to the change in dissipation factor are not understood at this time. The critical parameters could be in the winding process itself or any of the upstream processes.

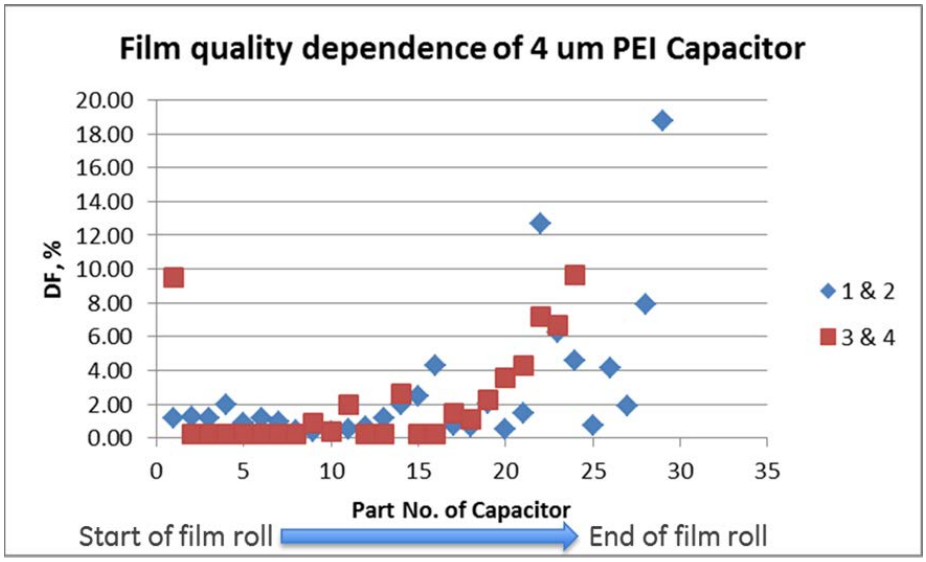

Figure 6-40: Dissipation factor as a function of manufacturing sequence from slit rolls. Low sequence number indicates the beginning of the roll. The slit rolls come from different lanes of the master roll. The numbers, 1 & 2 or 3 & 4, indicate the position of the slit roll on the master roll.

After understanding the three issues another design of experiment was performed, and the optimum winding tension was determined to be between 65 g and 80 g. Winding yields went from less than 20% to greater than 80% as shown in Figure 6-41. Figure 6-42 shows the reduction in variance for dissipation factor with successive manufacturing trials. Figure 6-43 shows all 55 capacitor bobbins from one manufacturing trial, visually demonstrating the uniformity of the batch. Finally, Figure 6-44 shows a process control chart for the diameter of the capacitor bobbins, showing that there are no capacitors outside the 3σ control limits.

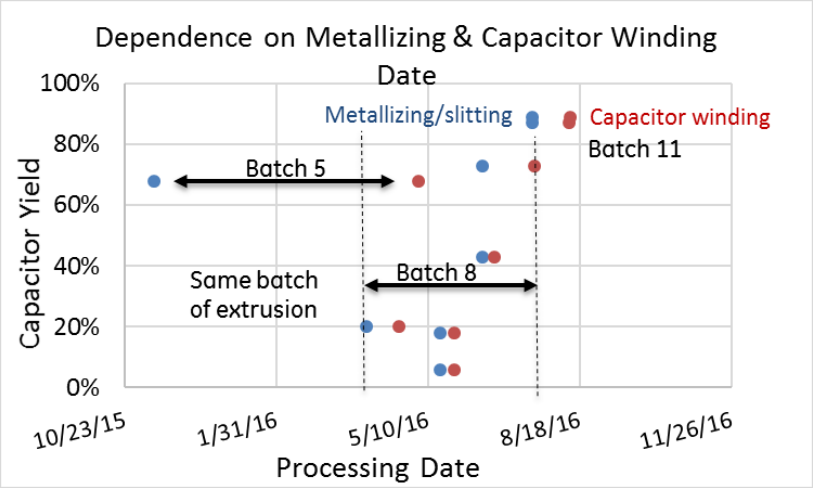

Figure 6-41: Capacitor winding yield by the date of metallization and by the date of capacitor winding.

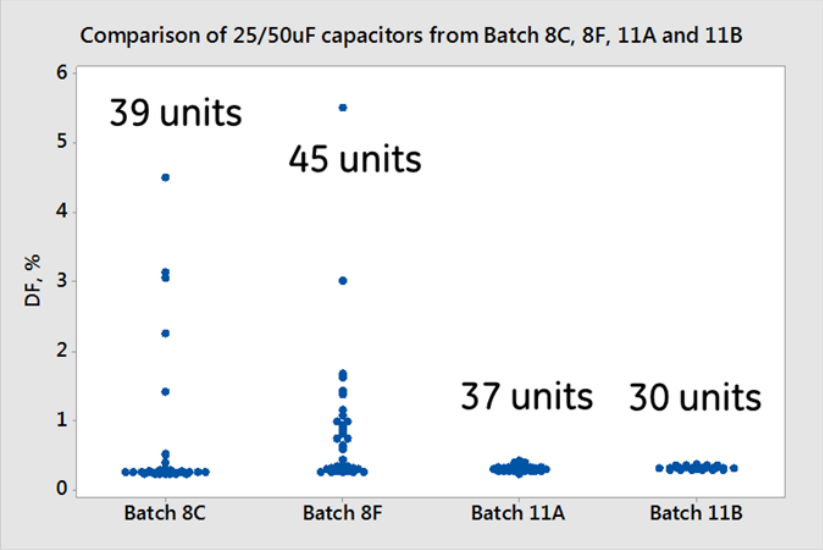

Figure 6-42: Dot plot of dissipation factor for capacitors from various film batches. Dissipation factor improves over time.

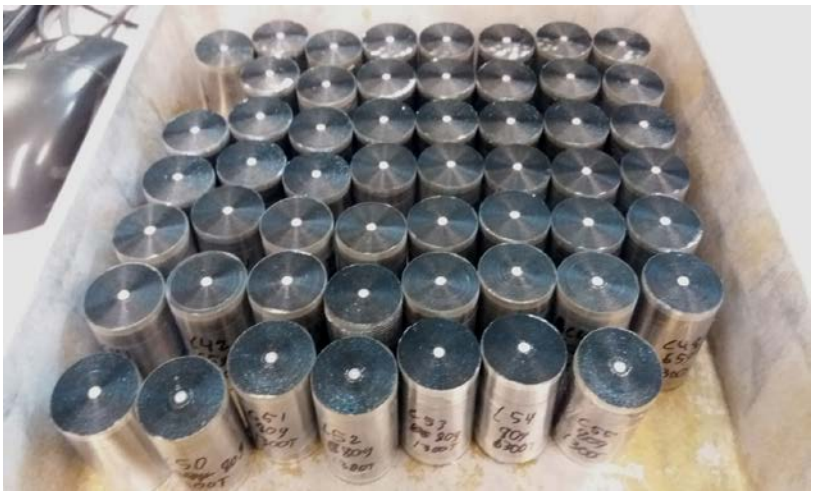

Figure 6-43: All 55 capacitors from Trial 23, Batch 8F. These bobbins have nominal capacitance of 25uF.

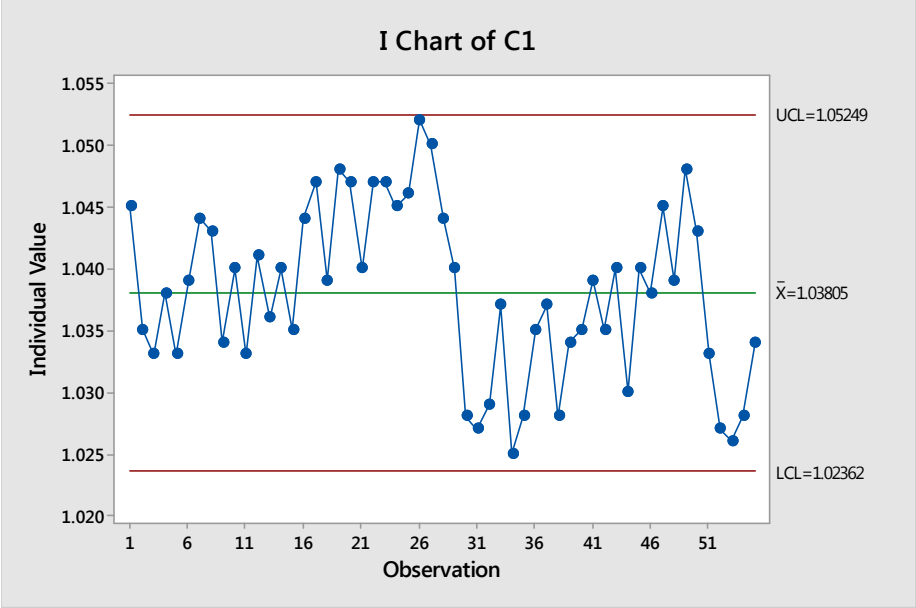

Figure 6-44: Control chart of capacitor bobbin diameter, indicating that the diameter is under good control.

Capacitor bobbins that exhibited good electrical properties after end spray often had the dissipation factor degrade after subsequent thermal processes. A micro-computed tomography x-ray image presented in Figure 6-45 shows delamination of the Babbit from the edges of the bobbin. The end spray was changed from Babbit to only Zn, and the frequent increase of dissipation factor was reduced.

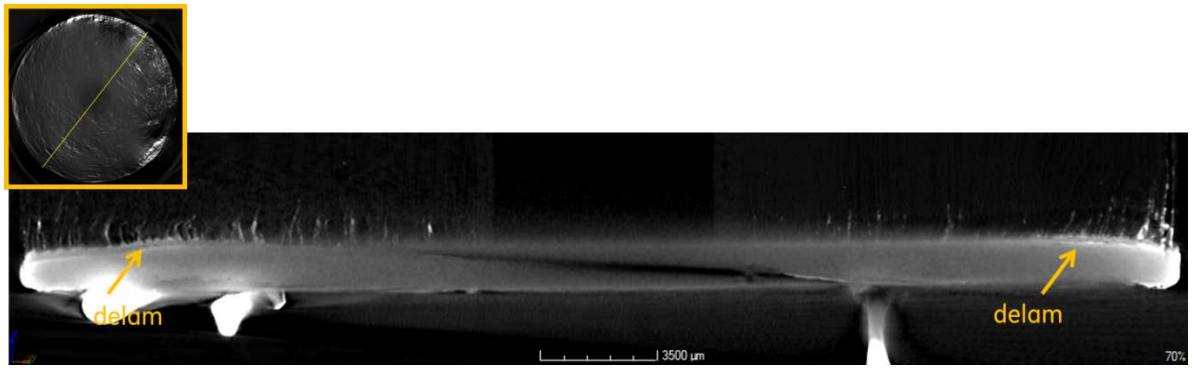

Figure 6-45: CT images of one end of the end sprayed capacitor produced using automatic winder followed by potting. The inset shows the face of one end.

Transitioning from capacitor bobbins to high-capacitance assemblies, several case materials were considered prior to selecting Ultem 1010 as the most suitable material. The selection was empirically validated placing dummy bobbins in candidate cases and potting with the standard 20-3660 electronic-grade high-temperature epoxy. An image of typical case bowing is shown in Figure 6-46.

Figure 6-46: age of typical case bowing after potting epoxy cures.

Ultem 1010 was the best selection because there is no thermal expansion mismatch between the case and the bobbins, which are both made of Ultem 1010. Likewise, Ultem 1010 has the same thermal expansion coefficient as the potting epoxy, 47×10-6 K-1. Rejected case materials include G10 and Ultem 9085. Capacitors were assembled for the Phase II deliverables. Four 300 µF capacitor modules with six 50 µF bobbins were assembled. Additionally, three 700 µF capacitor modules with 28 25 µF bobbins were assembled. These capacitors were delivered to Delphi for testing.

Various stages of 300 µF module assembly are shown in Figure 6-47. Panel a) shows the electrical assembly of capacitor bobbins and bus. Figure 6-47b shows the empty case, and in Figure 6-47c the capacitors are shown sitting in the case. Finally the potted capacitor module is shown in Figure 6-47d. The case was 3D printed for prototyping speed and cost. Representative images of an empty case and a fully assembled capacitor module for 700 µF module assemblies are shown in Figure 6-48.

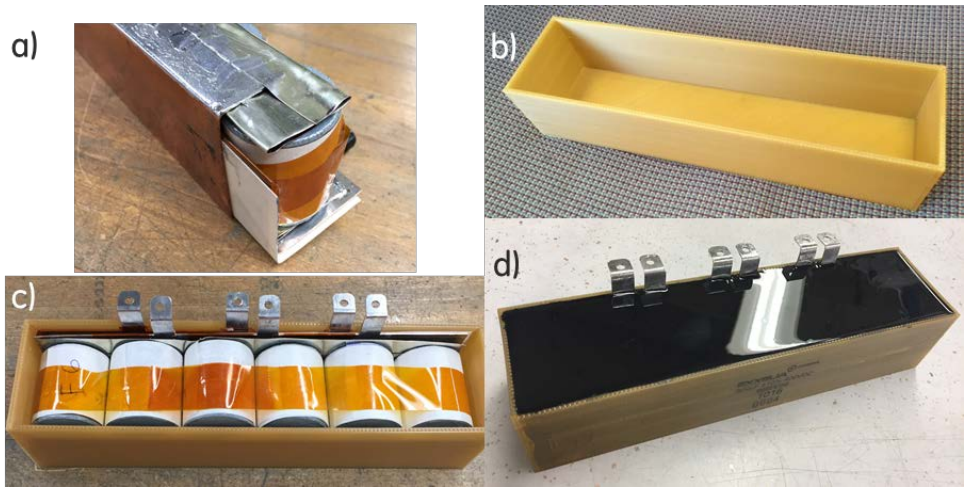

Figure 6-47: 300 µF capacitor module assembly. a) Bus bars on bobbins b) The empty case c) Bobbin assembly inserted into the case d) The completed module ready for delivery.

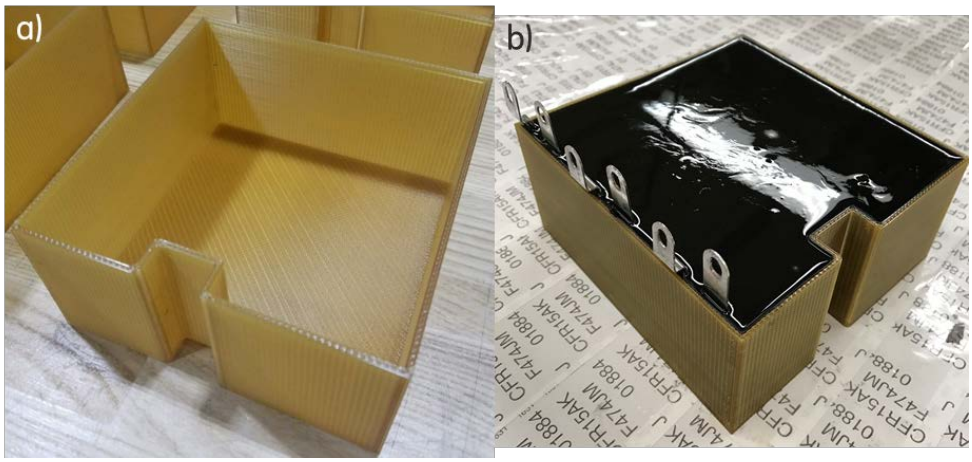

Figure 6-48: 700 µF capacitor module assembly. a) An empty case b) A fully assembled capacitor module ready for shipment.

Delphi has tested the performance of the Phase I capacitors. The testing has followed two tracks: thermal endurance performance and thermal cycling performance. The Phase I capacitors were not fully packaged, so the results should be considered indicative of the final modules, but there may be different results. The testing results are presented below.

The three 100 µF capacitor modules and two 300 µF capacitor modules that were delivered to Delphi were split in two groups for testing. The first group was subjected to 140°C storage testing, and the other group was subjected to thermal cycles between -40°C and 140°C. The test plan calls for the capacitors to be subjected to 1000 thermal cycles, and these will be completed in the first week of November. The testing was interrupted at various points, and the electrical performance of the capacitors was measured.

The measured electrical performance parameters were the capacitance, the dissipation factor and the resistance. These results should be representative of the future Phase II deliverables, but the packaging is incomplete, so there could important deviations from the final results. The results for the storage testing are given in Figure 6-49, and the results for the incomplete thermal cycle testing are given in Figure 6-50. The results indicate that it is worthwhile to perform testing on the Phase II deliverables.

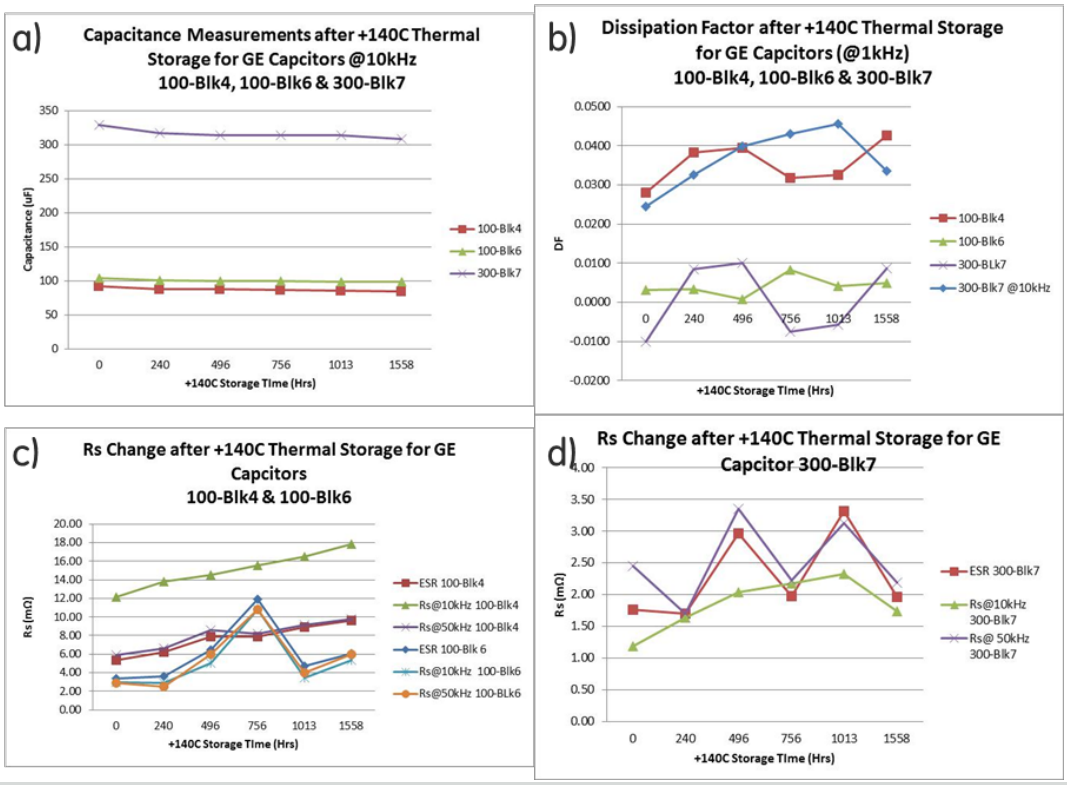

Figure 6-49: Testing results for Thermal Storage stress on Phase I capacitor modules. a) Capacitance b) Dissipation factor c) Rs for 100 uF modules d) Rs for 300 uF module

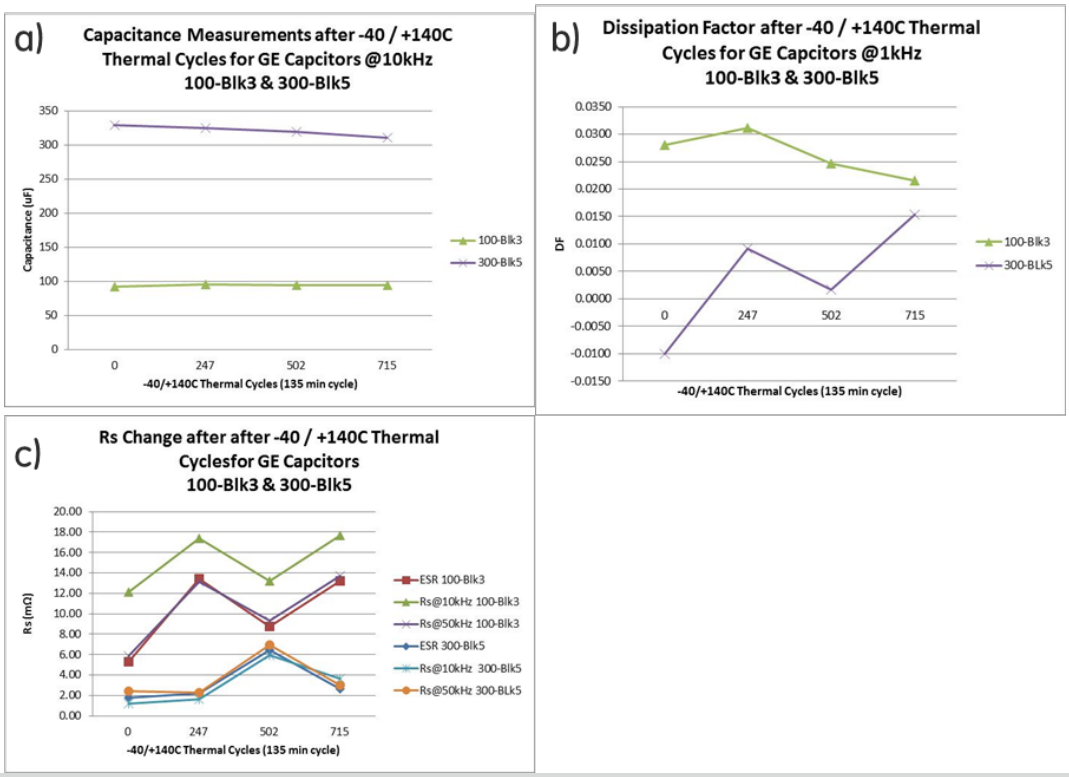

Figure 6-50: Testing results for Thermal Cycling stress on Phase I capacitor modules. a) Capacitance b) Dissipation factor c) Rs

Conclusions and Future Directions

During the reporting period, a supply chain was demonstrated with the capability to complete the Phase I capacitor deliverables. Three 100 μF capacitor modules and two 300 μF capacitor modules were built and delivered to Delphi for testing, which will be completed in the first week of November. The constituent capacitor bobbins in the modules were either 13 μF or 25 μF. TRL 5 and MRL 3 were achieved.

Likewise, a supply chain was demonstrated with the capability to complete the Phase II capacitor deliverables. Four 300 μF capacitor modules and three 700 μF capacitor modules were built and delivered to Delphi for testing, which will be completed in mid-December. The constituent capacitor bobbins in the modules were either 50 μF or 25 μF. TRL 4 and MRL 3 were achieved.

The value chain was simplified. The oxide coating was eliminated because the performance improvement was too small for the cost increase, and no path existed to bring the cost within range of meeting the project targets. Film de-wrinkling and stretching was removed from the value chain because the film extrusion process improved to the point that wrinkle-free, low-static films of nearly the desired thickness were achieved without the need for additional processing. For each step in the value chain, at least one supplier has demonstrated capability to meet the project objectives.

For this project, future work must be completed to test the Phase I and Phase II capacitors and to interpret the results. A roadmap to meeting the cost objectives of the project must be completed. Current projections for the cost of the PEI film are $700 per 700 μF capacitor at volumes of less than 1000 per year.

Additional future work must be performed to gain statistical control of the manufacturing process. Main effects and process controls must be understood for their impact on capacitor performance and manufacturing yield. The incoming process requirements for both materials and work in progress must be statistically defined, and the outgoing process success criteria for each process step must also be determined. Additional module packaging trials must be completed with production ready cases. A roadmap for further reduction of the PEI film thickness must be established to further reduce weight, cost, and volume. Finally, a self-sustaining ecosystem must form around the value chain established in this project that enables launching products and cycles of continuous improvement.

FY 2016 Presentations/Publications/Patents

1. Daniel Tan, DOE APEEM Annual Merit Review; High Performance DC Bus Film Capacitor; June, 2016.
2. Norberto Silvi, Kevin Flanagan, Daniel Tan, Jeffrey Sullivan, "Biaxially-stretched, Amorphous, High Temperature Polymer Films for Dielectric Applications," invention alert.
3. Norberto Silvi, Kevin Flanagan, Daniel Tan, Jeffrey Sullivan, "A Novel Method to Produce Thin, High Temperature Amorphous Polymer Films for Dielectric Applications, and Films produced by this Method," application filed.

References

1. Advanced Power Electronics and Electric Motors Program. DOE EERE Vehicle Technologies Office, 2008.
2. U. Balachandran, M. Narayanan, S. Liu, B. Ma, Development of film-on-foil ceramic dielectrics for embedded capacitors for power inverters in electric drive vehicles, Jpn. J. Appl. Phys. 52, 05DA10, 2013.
3. M. Manoharan, C. Zou, E. Furman, N. Zhang, D. Kushner, S.Zhang, T. Murata, and M.Lanagan. "Flexible Glass for High Temperature Energy Storage Capacitors." Energy Technology 1: 5-6, 313-318, 2013.
4. S. Fries-Carr, S. Adams and J. Weimer, R.L.C. Wu, H. Kosai, K. Bray, T. Furmaniak, E. Barshaw, S. Scozzie and R. Jow, SAE Technical Paper 2004-02-3216, Power Systems Conference, Nevada, 2004.

5. Shihai Zhang, Chen Zou, Xin Zhou, Douglas Kushner, “High Temperature Polymer Capacitor Film with High Dielectric Constant” 2011 CARTS USA, March 28-31, 2011, Jacksonville, FL. http://strategicpolymers.squarespace.com/capacitors 2011. Strategic Polymer Sciences Inc.
6. K.W. Browall, M.W. DeVre, S.M. Gasworth, C.W. Reed, S.J. Rzad, ”High Energy Storage Capacitors for Pulse Power, ARL-CR-150, Contract DAAL01-91-C-0149, 1994.
7. Q. Tan, P.C. Irwin, Y. Cao, Advanced Dielectrics for Capacitors, IEEJ Transactions on Fundamentals and Materials, 11, 11532-1159 Vol 126 (2006).
8. D. Tan, Q. Chen, Y. Cao, P. Irwin, S. Heidger, “Polymer Based Nanodielectrics for Capacitors”, EMA 2010, Orlando, FL, (2010).
9. Bruce Mixer, High Temperature Inverter—Delphi Automotive S, Advanced Power Electronics and Electric Motors Program. DOE EERE Vehicle Technologies Office (2013).

6.5 High Temperature DC Bus Capacitor Cost Reduction & Performance Improvements

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Subcontractor: Delphi Automotive Systems, LLC
Subcontractor: Oak Ridge National Laboratory
Contract No.: DE-EE0006438

Objectives

- Reduce the cost, size and weight of the DC-link capacitor by >50%
  - Increase durability in high temperature environments

Technical Barriers

- The performance and lifetime of capacitors available today degrade rapidly with increasing temperature (ripple current capability decreases with temperature increase from 85˚C to 105˚C). Therefore, today's capacitors are typically twice the size (up to 40% of the inverter's volume) and too costly (up to 30% of the inverter's cost).

Technical Targets

- For Phase 1 the GEN 1 targets will be
  - A PML capacitor that will have a rating of 800 µF / 400 Vdc / 650Vtransient
  - Designed for a 30 kW continuous, 55 kW peak (30 seconds) inverter
  - Operating temperature: -40°C to +140°C
  - Projected volume: < 0.2L
  - Dissipation factor: < 0.01 up to 160°C
  - Ripple current: 130Arms continuous
  - Energy density: > today's PP caps
  - Cost: < $30
  - Benign failure mechanism.

Accomplishments

Sigma and their partners Delphi Automotive (Delphi) and Oak Ridge National Laboratory have made significant progress in completing Phase 2 work including, Program Management, Develop PML Gen 2 Capacitors, Package Gen 2 Capacitors, Fabricate Packaged PML GEN 2 DC-Link Capacitors and Develop a Business Plan for Production. Full size (300µF, 500µF and 700µF) capacitors have been produced which meet or exceed the Technical Targets outlined above and packaged life testing shows stability under various environmental conditions.

Introduction

The proposed project focuses on process development and scale-up to produce application-specific DC-link capacitors for automotive inverter applications. In Phase I of the program (2013 – 2015), the development work addresses optimization of the polymer dielectric formulation and thickness, to produce GEN 1 capacitors with a rating of 800 µF / 400 Vdc / 600 Vtransient. GEN 1 will demonstrate operation at -40°C to 140°C, a benign failure mode, >2X reduction in the volume and weight, compared to today's baseline polypropylene (PP) capacitors and have met the product cost target. A significant part of the Phase I effort was to scale-up process steps to allow manufacture and assembly of an adequate number of parts for the various test protocols and to meet the Phase I deliverables. In the Phase II effort (2015 – 2016), GEN 2 capacitors were produced that further decreased capacitor volume by optimizing the polymer dielectric and capacitor electrode design. GEN 2 capacitors are now packaged for integration into a Delphi inverter, and long-term reliability tests to confirm the all target specifications have been met.

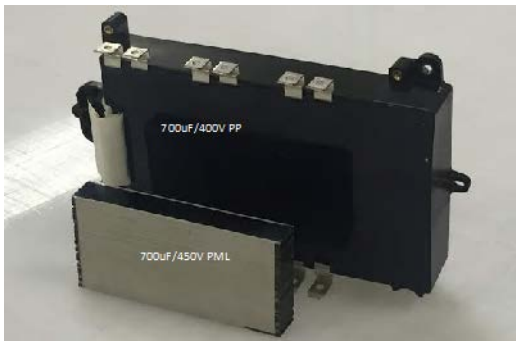

Figure 6-51: Back: State of the art metalized PP 700µF-400V/600Vmax/105°C DC-link capacitor used in automotive inverters. Front: PML capacitor 700µF-450V/650Vmax/140°C.

Approach

Sigma has developed a solid-state Polymer-Multi-Layer (PML) capacitor comprising 1000s of radiation cured polymer dielectrics and Al electrodes to form a large area nanolaminate (Mother Capacitor) that is segmented into individual capacitors.

- Having a prismatic shape with low ESL and ESR
- Operating temperature range of -40°C to 140°C
- Dissipation Factor (DF) < 0.01
- Amorphous high breakdown strength dielectrics with intrinsic breakdown strength >1000V/µm
- Dielectric constants in the range of $3.0 < k < 6.2$
- Benign failure mode
- Low-cost materials and process.

This PML technology is a transformational and potentially disruptive technology in the following ways:

- The current supply chain to manufacture metallized PP capacitors involves a film manufacturing operation, an electrode metallizing operation and a capacitor manufacturing operation. Virtually all capacitor manufacturers use the same base PP dielectric films, which leaves little room for innovation and advancement of the technology to meet market needs.
- PML "Mother Capacitor" material which comprises a large sheet of multilayer material (10s of square feet), is produced in a one step process by inputing liquid monomer and Al wire into a process chamber.
- The capacitor OEM has control of all key material and process parameters, including the dielectric formulation, dielectric thickness (as low as 0.1µm), electrode material, electrode thickness, capacitor shape and capacitor size. Surface mount polymer dielectric capacitors have been made with

dimensions as small as small 1mm x 1mm that can compete with MLCs and as large 300mm x 300mm (in thin sheet form with 1000s of layers), that cannot be produced by any other capacitor technology.

- The PML capacitor technology can reduce the cost of metallized polymer capacitors and allow a capacitor OEM to innovate and create application-specific products with different polymer dielectric properties.

Results and Discussion

2016 activities for Phase 2 of the project consisted of completing the following 4 tasks:

- Task 7 – Program Management
- Task 8 – Develop PML GEN 2 Capacitors
- Task 9 – Package GEN 2 Capacitors
- Task 10 – Fabricate Packaged PML GEN 2 DC-Link Capacitors
- Task 11 – Develop a Business Plan for Production

A brief summary of the work performed for each of these tasks follows.

Task 1 – Program Management

Sigma Technologies and Delphi have worked closely together over the final phase of the project. There have been monthly review meetings involving Sigma and Delphi, as well as correspondence via email and phone calls. All quarterly Research Performance Progress Reports and other reporting requirements have been submitted on time to the DOE.

Task 8 – Develop PML GEN 2 Capacitors

To produce the GEN 2 Capacitors Sigma did extensive work both on examining alternative monomers and eliminating process related defects this year. Also, numerous parts were produced to examine lead attach methods, conduct electrical, thermal and environmental test and investigate different packaging designs. Process issues which have been addressed include:

- Contamination of the "mother" material to improve yield
- Methods for quick removal of the mother capacitor material from the process drum
- Advance methods of electrode passivation to maximize corrosion resistance in high humidity environments

Parts were produced for thermal testing with imbedded thermistors to allow monitoring of internal temperatures.

Sigma has successfully produced multiple large PML DC-Link Capacitors this year (see Figure 6-52), that have passed all electrical, thermal and mechanical requirements. The capacitance of the parts is determined by the application requirements and not by limits to the process. These parts have been successfully tested at 400V/600Vpeak with no degradation to performance. Both Capacitance and Dissipation Factor show excellent results over temperatures from -40°C to 160°C.

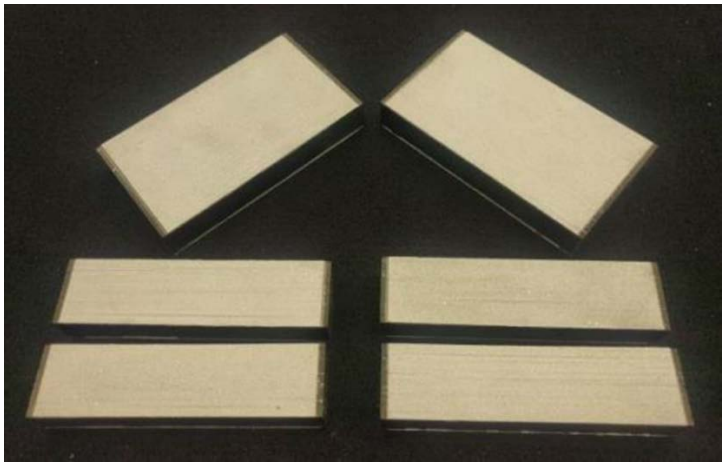

Figure 6-52: Top - 700uF parts. Bottom - 4 x 350uF parts

The capacitance and dissipation factor of the larger capacitor is quite stable over the temperature range of -40C to +160C. Figure 6-53 shows that at the maximum operating temperature of 140C the dissipation factor is well below the target 0.01. Combined with an ESR<0.5mohm and an inductance <10nH, the PML capacitors exhibit superior electrical characteristics in addition to their higher operating temperature and smaller size.

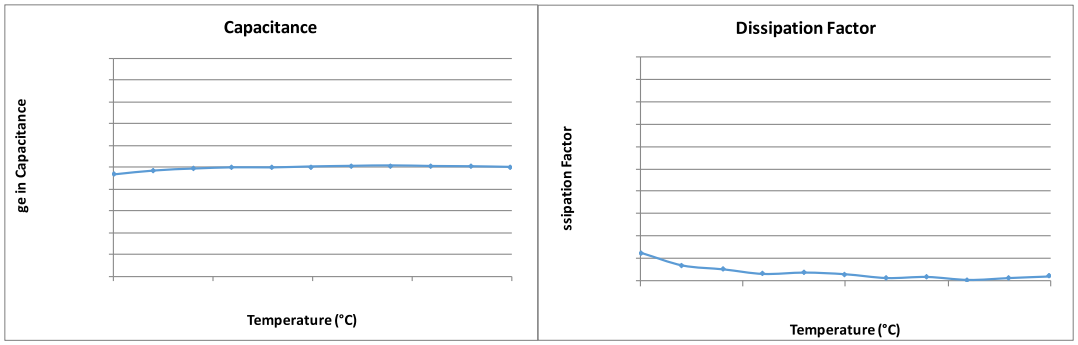

Figure 6-53: Capacitance and dissipation factor variation of a 350uF PML capacitor as a function of Temperature

Task 9 – Package GEN 2 Capacitors

Delphi has focused on developing a overmold or transfer molding method for packaging the PML capacitors. This process was chosen because it is a low cost method that lends itself to packaging PML capacitors due to their superior mechanical and thermal properties. Initial work using smaller capacitor parts (see Figure 6-54) has faced some challenges due to poor alignment of the part in the mold cavity. Proper fixtures have been developed to correct resolve this issue. I parallel to the molding process development a box potting package is pursued which the industry standard for PP capacitors. An epoxy material has been developed that matches the properties of the PML capacitor at high temperatures and as shown in Figure 6-54, some parts have been packaged and placed in an accelerated humidity lefe test. So far that potted parts show no significant capacitor degradation, suggesting that the package in combination with a unique electrode passivation process provide good protection against corrosion of the aluminum electrodes. This material has been successfully used for current Poly Propylene capacitors overmoulding could not be used for PP due to the heat and temperatures involved.

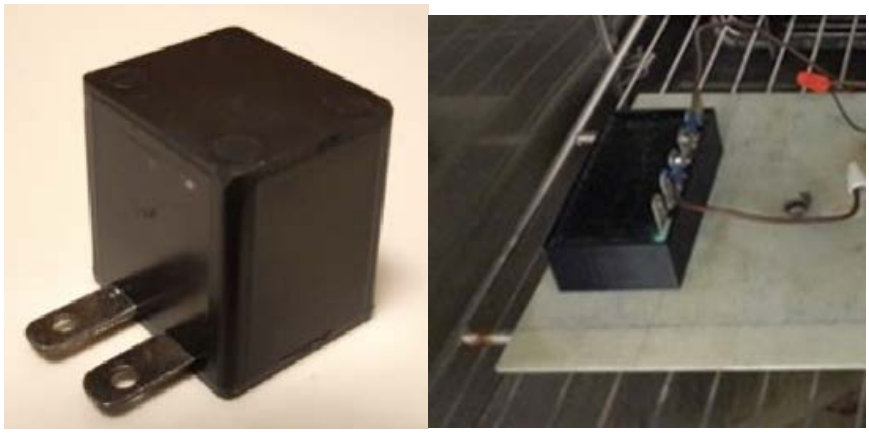

Figure 6-54: Left: 50uF test part packaged using an overmolding process, Right: 350uF part packaged using a potting process.

Task 10 – Fabricate and Test Packaged PML GENII Capacitor

PML capacitors up to 700uF have been fabricated with high current copper leads designed to fit a Delphi inverter and are in the process of been packaged before integrated into the inverter for the final series of tests.

Task 11 – Develop a Business Plan for Production

Sigma has completed, and continues to refine, a business plan that focuses on the scale-up and commercialization of its capacitor technology for automotive inverter applications. The plan outlines the capital required for a) commissioning of a first full-scale production facility in Tucson, Arizona, b) hiring key management, engineering, and production personnel, and c) developing the market for high energy density capacitors based on Sigma's technology. Sigma is in the process of designing and fabricating a production scale machine to manufacture the Mother Capacitor material.

Conclusions and Future Directions

In conclusion, Sigma and their partners, Delphi Automotive and Oak Ridge National Laboratory, have successfully produced capacitors which meet or exceed the DOE requirements. Work is continuing on optimizing packaging and transitioning this research and development program into full scale production for the automotive and other applications.

FY 2016 Presentations/Publications/Patents

1. 2016 DOE Annual Merit Review meeting presentation
2. One patent application was filed that claims key design and process elements involved the production higher voltage and temperature PML capacitors.

6.6 Cost-Effective Fabrication of High-Temperature Ceramic Capacitors for Power Inverters

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Abstract/Executive Summary

- This project addresses the overall size, cost, and high-temperature operability barriers of the presently used polymer-based capacitors in automotive power inverters. Current DC bus capacitors occupy a significant fraction of volume (≈35%), weight (≈25%), and cost (≈25%) of the inverter module, cannot tolerate temperatures >85°C, and suffer from poor packaging, and inadequate reliability. Traditional capacitor architectures with conventional dielectrics cannot adequately meet all of the performance goals for capacitance density, weight, volume, and cost. The technology being developed in this project will substantially reduce the size, weight, and cost of DC-link capacitors, which will enable the fabrication of smaller, lighter, and less costly electric drive vehicle power inverters.
- The goal of this project is to develop an efficient, cost-effective process for fabricating compact, high-temperature, Pb-La-Zr-Ti-O (PLZT)-based DC-link capacitors for advanced power inverters in electric drive vehicles, and to achieve EDT targets for capacitance density, weight, volume, and cost requirements. Success in this project will benefit the implementation of highly fuel efficient and environmentally friendly electric drive vehicles and other high power green energy applications.

- Technical targets of this project is to develop a high-rate, room-temperature aerosol deposition (AD) process to economically manufacture PLZT-based capacitors with permittivity (k) that is ≈30 times that of presently used polymer-based film capacitors over the temperature (-40°C to +140°C), voltage (450 V nominal/600 V transient), and frequency (≈10 kHz) ranges required for automotive power electronics and to scale-up the AD process for high-throughput production.

Accomplishments

- Optimized aerosol deposition (AD), a high-rate, room-temperature film deposition process to economically fabricate the PLZT capacitors. Argonne developed AD process has been integrated onto a rotating-wheel deposition system at Sigma Technologies for scaling up for high throughput production. Delphi has verified that the properties of the samples produced by the AD process meet requirements for the high-temperature power invertors.
- Demonstrated that the PLZT-based ceramic capacitor's properties meet EDT objectives. The results have been validated by our industry and university collaborators.
- Developed solution chemistry to synthesize submicron PLZT powders suitable for AD process and identified a commercial supplier of powders for large-scale manufacturing of PLZT capacitors.
- Fabricated ≈8-µm-thick PLZT film on metallized polyimide films in ≈20 min by AD process (vs. a week by spin-coating process used to demonstrate PLZT's properties).
- Transferred the ANL developed AD process on to a rotating wheel deposition system at Sigma Technologies International, LLC.
- Demonstrated graceful failure mode in single layer PLZT films.
- Demonstrated long-length PLZT tapes (~15 cm long x 2.5 cm wide) on flexible metalized polymer films.
- Measured mean breakdown voltage of 990 V, high energy density of 10 J/cc and low leakage current density of <0.1 µA/square-cm at ≈500 V bias in a ≈8-µm-thick PLZT capacitor fabricated on metallized polyimide films by AD process.
- PLZT films made by high-rate AD process has high dielectric constant and low loss over the advanced power inverter's operational temperature, voltage, and frequency range.
- Defined capacitor specification for the inverter and established materials cost targets to meet the EDT program requirement.

Introduction

Capacitors are essential components of power electronics for carrying out a host of functions in pulse power and power electronics applications such as pulse discharge, filtering, voltage smoothing, coupling, de-coupling, DC blocking, power conditioning, snubbing, electromagnetic interference suppression, and commutation in power electronics. They are a critical to the performance of power inverter modules within electric drive vehicles (EDVs) which directly affects fuel efficiency and battery life. Capacitors occupy ≈35% of the inverter volume and account for ≈25% of the weight in current designs. Thus, even if all other components in an inverter are reduced significantly, the capacitor requirement is a serious impediment to achieving the required volume and weight reduction. In addition, the use of high-temperature coolants further exacerbates the situation because existing film capacitors lose their capability to absorb ripple currents at elevated temperatures, necessitating the addition of extra capacitors. Increasing the volumetric performance (capacitance per unit volume) of DC bus capacitors is required, and their maximum operating temperature also must be increased to assure reliability requirements. Ceramic capacitors have the greatest potential for volume reduction; they could be as small as 30% of the volume of a polymer-based capacitor currently used in EDVs. Ceramics offer high dielectric constants and breakdown fields and, therefore, high energy densities. They also can tolerate high temperatures with a low equivalent series resistance (ESR), enabling them to carry high ripple currents even at elevated temperatures.

Driven by the increasing demand for power electronics with improved performance, high reliability, and reduced size and weight, we developed fabrication technology to make high-temperature, high-dielectric constant ceramic capacitors. Our research [1-4] had shown that the lead lanthanum zirconate titanate

(Pb0.92La0.08Zr0.52Ti0.48O3, PLZT) films deposited on base metal foils possess excellent dielectric properties, which are promising for high power applications such as plug-in hybrid electric vehicles. Use of base-metal foils reduces the cost of the capacitor. The stacked and embedded capacitors approaches significantly reduce component footprint, improves device performance, provides greater design flexibility, and offers an economic advantage for commercialization. This technology will achieve the high degree of packaging volumetric efficiency with less weight. Device reliability is improved because the number and size of interconnections are reduced. The vision of DC bus capacitors by film-on-foil processing of PLZT-based capacitors is compelling and offers U.S. automotive companies a substantial technological advantage over their foreign counterparts.

In power electronics, capacitors with high capacitance are required to work under high voltages. This requirement imposes the additional challenge of fabricating thicker (>5 μm) films. However, due to the well-known critical thickness effect, per-layer thickness that can be achieved by conventional sol-gel method is generally limited to ≈0.1 μm, thus making the conventional spin coating method less attractive to industry when thicker films are needed to meet the operation voltage requirement. A high-rate aerosol deposition (AD) process being developed at Argonne can produce thick PLZT films with desirable high voltage properties at significantly shorter time. AD process can produce dense ceramic films at room temperature without the needs for high temperature sintering; thus making the process amenable for depositing the PLZT films on variety of substrates such as polymer, glass, and metal foils. Therefore, it is a cost-effective method for manufacturing ceramic film capacitors for power inverters in EDVs.

In this project, the team will collaborate to develop a high-rate, economically attractive AD manufacturing process to produce PLZT-based DC-link capacitors with dielectric properties suitable for advanced power inverter applications. Our R&D efforts focus on developing a lab-scale AD process that is amenable to large-scale manufacturing of PLZT films for EDV inverters, evaluating the underpinning issues of ceramic film capacitor performance and reliability, scaling-up and transferring the AD process technology to industry for manufacturing, and fabricating high-voltage-capable PLZT capacitors defined by the inverter application requirements. Overall project goal is to transfer basic AD process on to a high-throughput rotating-wheel coating system, fabricate and characterize proto-type capacitor, verifying its performance satisfies the requirements for power invertors, and perform detailed costing and commercialization plan to meet DOE's cost and performance targets.

Approach

In our earlier work we have demonstrated that PLZT film capacitors meet EDT performance objectives. However, the spin coating process used to demonstrate PLZT's attractive properties involved several time consuming steps and it is not practical to make large quantities of films needed for practical applications. Therefore, our approach in this project is focused on developing high-rate deposition process to economically make high-dielectric constant, high-temperature, low-cost ferroelectric PLZT dielectric films on thin metal and polymer substrates. Ferroelectrics possess high dielectric constants, breakdown fields, and insulation resistance. With their ability to withstand high temperatures, they can tolerate high ripple currents at under-the-hood conditions. High-dielectric constant materials significantly reduce component footprint, improve device performance, provide greater design and packaging flexibility, achieve high degree of volumetric efficiency with lightened weight, and offer an economic advantage. A high-rate, room-temperature, AD deposition process has been identified as an economically attractive process to make PLZT-based capacitors. PLZT film capacitors made by AD process were evaluated to provide feed-back for process optimization. In collaboration with our industry partners, substantial amount of effort is focused on transferring the AD process to Sigma's rotating-wheel deposition system to make long length PLZT film on moving metalized thin polymer substrate, fabrication and characterization of prototype capacitors, and perform detailed costing and commercialization plan to meet DOE's cost target. The longer-length PLZT films deposited on metalized polymer films will be characterized and characterization results are analyzed for improving the process parameters for the rotating-wheel deposition system. The PLZT films produced by the rotating-wheel deposition system at Sigma will be evaluated at multiple laboratories in order to validate the results and improve the AD process.

Results and Discussion

In our earlier work, we demonstrated the suitability of using the PLZT film capacitors prepared by sol-gel spin coating fabrication process [5, 6] for power inverter applications. We fabricated high-temperature PLZT film

capacitors with high dielectric constant, low dielectric loss, and high dielectric strength by solution deposition techniques [5, 7, 8]. Prototype stacked PLZT film capacitors with capacitance ≈10 μF was fabricated, tested, and verified by Delphi Electronics & Safety Systems. Despite all the success and positive outcomes with chemical solution process for fabricating PLZT film capacitors, the process itself is slow and requires multiple layers of coatings and intricate heating/annealing schemes to produce capacitors with thickness that can withstand the high voltage (≈450 V) required for DC-link capacitor application. The time consuming sol-gel spin coating process is not practical to make large quantities of PLZT films for practical applications. To overcome this drawback, we developed a high-rate, room temperature aerosol deposition (AD) process that can produce large area dense PLZT films at speeds that are hundreds of time faster than the sol-gel spin coating process.

In the spin coating process, we utilized a conductive oxide buffer layer to enable heat-treatment of ceramic PLZT coating in air and still prevent the undesirable oxidation of low coat base metal foils. Base metal substrates were polished by chemical-mechanical planarization (CMP) to a root-mean-square surface roughness of ≈2 nm (measured by atomic force microscopy in the tapping mode with 5 μm × 5 μm scan size). Prior to being coated, polished substrates were ultrasonically cleaned in distilled water, and then wipe-cleaned with acetone and methanol in sequence. For nickel (Ni) and aluminum (Al) substrates, conductive oxide film of LaNiO3 (LNO) was coated by spin coating prior to the deposition of PLZT. LNO precursor solutions with 0.2 M concentration were prepared by dissolving an appropriate amount of lanthanum nitrate hexahydrate and nickel acetate tetrahydrate in 2-methoxyethanol (all from Sigma-Aldrich) and refluxing for 2 h inside a chemical glove box. PLZT precursor solutions with 0.5 M concentration were prepared by a modified 2-methoxyethanol synthesis route [5, 6] using an appropriate amount of titanium isopropoxide, zirconium n-propoxide, lead acetate trihydrate, and lanthanum nitrate hexahydrate (all from Sigma-Aldrich). The resulting stock solution contained 20% excess lead to compensate for lead loss during the heat treatments described below. The LNO and PLZT precursor solutions were filtered through Restek polytetrafluoroethylene (PTFE) syringe filters (Restek Corp., Bellefonte, PA) with 0.22-μm open pore size. The filtered LNO precursor solution was spin coated with a Laurell WS400 spin processor (Laurell Technologies, North Wales, PA) at 3000 rpm for 30 s on the Ni or Al substrates, pyrolyzed at 450°C for 5 min, and annealed at 625°C for 2-5 min in air. This process was repeated three times to build the desired ≈0.4-μm-thick LNO buffer film. Subsequently, filtered PLZT precursor solution was spin coated on the LNO-buffered Ni substrates at 3000 rpm for 30 s, followed by pyrolysis at 450°C for 5 min and annealing at 650°C for 5-10 min for each coating. After every three layers of coating, additional annealing was performed at 650°C for 15 min. Solution coating and firing were repeated to produce films of desired thickness. All pyrolysis and annealing were performed in air in Lindberg Blue M tube furnaces. Each coating resulted in a PLZT film of ≈0.115-μm thickness after pyrolysis and crystallization. It takes about a week to fabricate a ≈8-μm-thick PLZT film on base-metal substrate by the spin coating process.

We developed a room-temperature AD process at Argonne for high-speed fabrication of PLZT films on thin base metal foils, metallized silicon, and flexible metallized polymer films. During AD process, PLZT particles are accelerated toward the substrate and, if their speed exceeds a critical value, the particles consolidate upon impact without additional heating of the substrate. Because AD is done without heating the substrate, flexible materials such as polymers, plastics, thin metal foils, glass, etc. can be used as the substrate. By using flexible substrates, PLZT-based capacitors can be produced in a wound configuration, similar to the currently used polymer-based capacitors with benign failure features.

Figure 6-55 shows the 2θ X-ray diffraction (XRD) patterns of PLZT films deposited on platinized silicon substrates by sol-gel spin-coating process (shown in Figure 6-55a) and by aerosol deposition process (shown in Figure 6-55b). The XRD data indicate that both samples are well crystallized without preferred orientation. All peaks are indexed according to JCPDS 56-0900. A closer look at the two diffraction patterns shown in Figure 6-55 revealed that the PLZT peaks in Figure 6-55a shifted to higher angle compared to those peaks for the same index shown in Figure 6-55b. With the regular θ-2θ scan configuration, diffraction patterns are measured on these crystallites with the diffraction plane parallel to the substrate surface. According to Bragg's equation, a peak shift to higher 2θ angle indicates compression of d-spacing in the out-of-plan direction as a result of tensile strains in the in-plane directions that are parallel to the substrate surface. In-plan tensile strain in the PLZT on PtSi substrates deposited by sol-gel spin coating process is a result of high temperature (≈650°C) heat treatment [9]. On the other hand, the PLZT on PtSi produced by room-temperature aerosol deposition process bears compressive strain due to the high-speed collision and kinetic energy consolidation process [10]. High degree of crystallinity in PLZT films produced by both types of fabrication process yields

films with high dielectric constant and ability to withstand high operation temperatures. Similar to the PLZT films, Pt bottom electrodes of the sol-gel processed samples bear in-plan tensile stress; while Pt bottom electrodes of the AD processed films exhibit in-plan compressive stress. In addition, we observed peak broadening in the AD processed samples which is indicative of either nonuniform lattice distortion in the film as a result of high-speed collision and deformation of PLZT particles or some degree of amorphousness in the material.

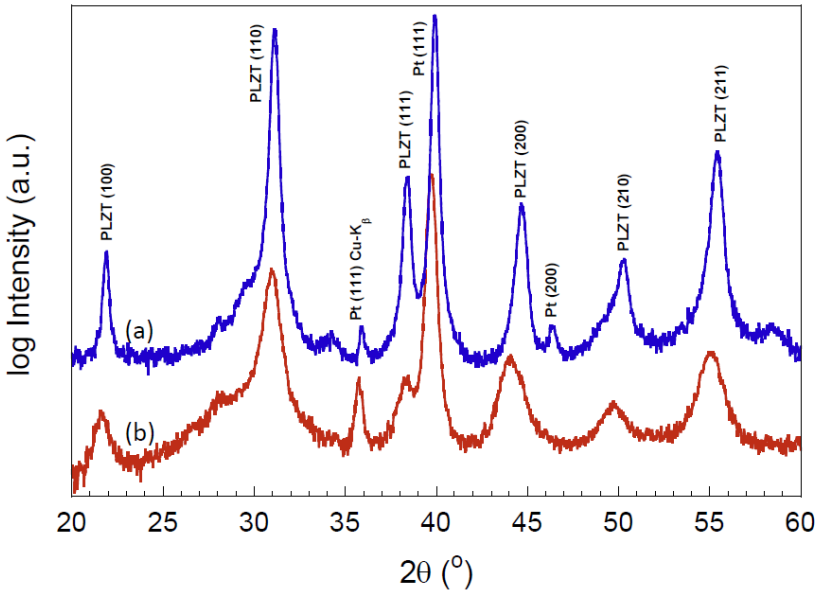

Figure 6-55: X-ray diffraction patterns of PLZT films produced by (a) sol-gel spin-coating and (b) aerosol deposition process.

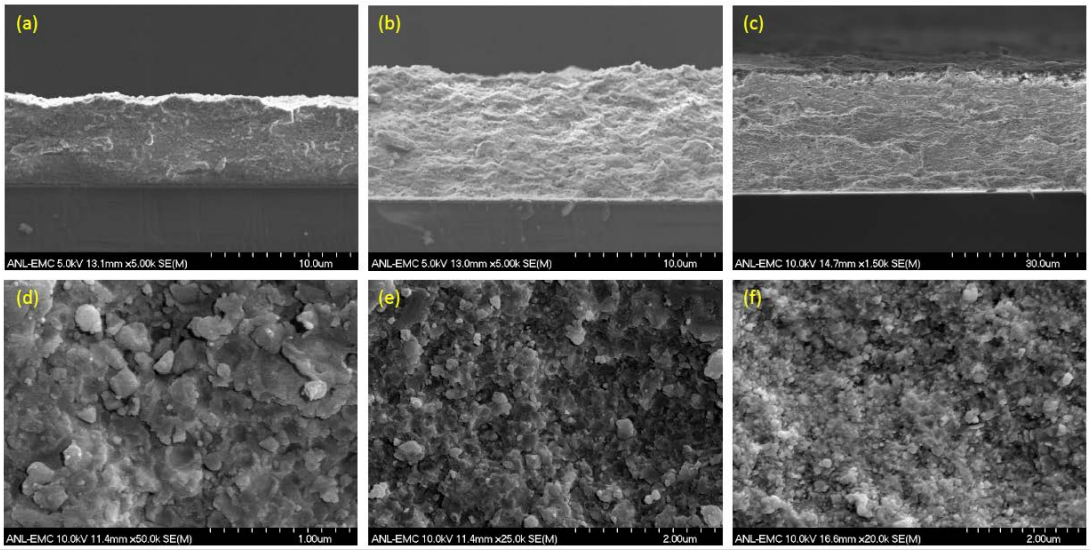

Figure 6-56: Cross-sectional and plan-view SEM microimages of AD PLZT films of various thicknesses deposited on PtSi substrates.

Figure 6-56 shows SEM microimages of AD PLZT films of various thicknesses deposited on PtSi substrates. Figure 6-56a and Figure 6-56d are SEM microimages of PLZT films of ≈6 µm thickness, Figure 6-56b and Figure 6-56e are SEM microimages of ≈8 µm thick PLZT films, and Figure 6-56c and Figure 6-56 are SEM microimages of ≈30 µm thick PLZT films. All the films are dense and uniform, no density variation across the thickness of the film is observed.

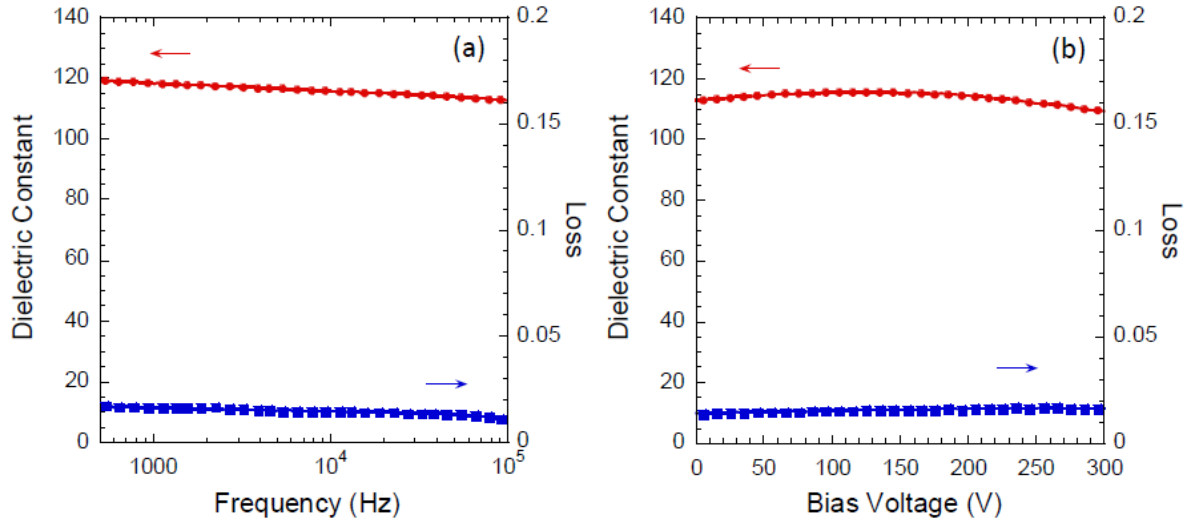

Figure 6-57: Dielectric properties of ≈6-µm-thick AD PLZT films deposited on PtSi substrates as a function of (a) frequency and (b) applied bias voltage.

Figure 6-57a shows frequency dependent dielectric property measured in the range from 500 Hz to 100 kHz on a ≈6-µm-thick PLZT film deposited on platinized silicon substrate by AD process. Dielectric constant exhibits good linear dependence on logarithm of frequency. At room temperature and 10 kHz, we measured dielectric constant of ≈115 and dielectric loss of ≈0.016. We have observed good linear dependence of dielectric constant on frequency for data measured with high bias voltages, indicating that the frequency response of domain motion in AD PLZT dielectric films is not strongly affected by the applied bias field. It is likely due to the high concentrations of defects in the AD PLZT films. Those defects act as pinning centers to retard domain movement. Dielectric constant first increases and then slowly decreases with increasing applied bias voltage while dielectric loss is nearly independent of applied bias as shown in Figure 6-57b.

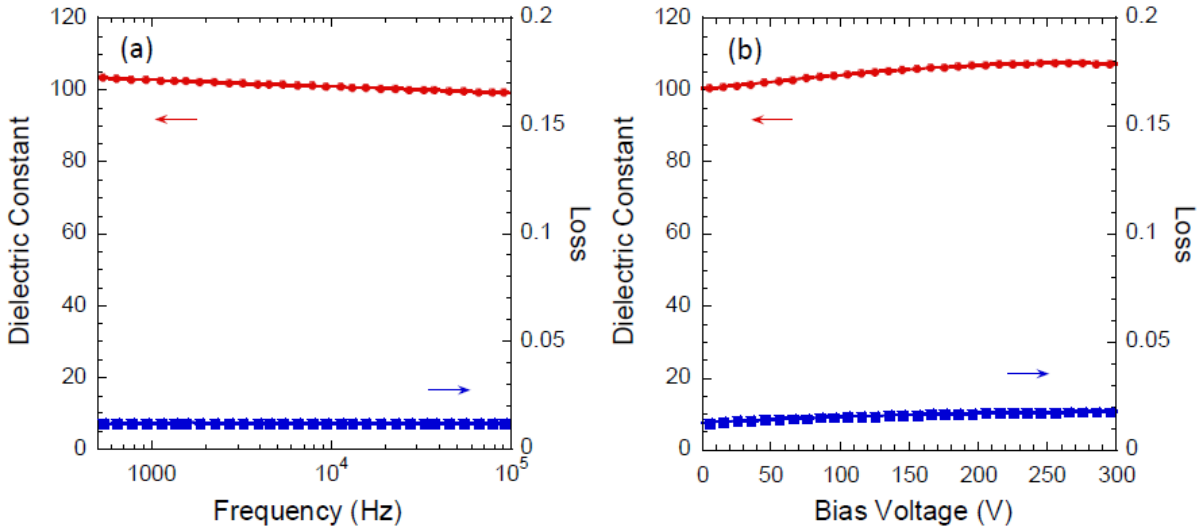

Figure 6-58: Dielectric properties of ≈8-µm-thick AD PLZT films deposited on aluminum metallized polyimide substrates as a function of (a) frequency and (b) applied bias voltage.

Figure 6-58 shows dielectric properties of a ≈8-µm-thick PLZT film deposited on aluminum metallized polyimide film (Al/PI) by AD process. Similar to the AD films deposited on PtSi substrates, dielectric constant of AD PLZT deposited on Al/PI exhibits good linear dependence on logarithm of frequency, as shown in Figure 6-58a. At room temperature and 10 kHz, we measured dielectric constant of ≈100 and dielectric loss of ≈0.015. The dielectric constant of PLZT grown on Al/PI is about 15% lower than that measured for AD PLZT on PtSi but the dielectric losses are comparable to each other. As seen in Figure 6-58b the AD PLZT deposited on Al/PI substrate exhibit weak dependence of dielectric properties on applied bias voltage up to 300 V (corresponding to an electric field of ≈400 KV/cm).

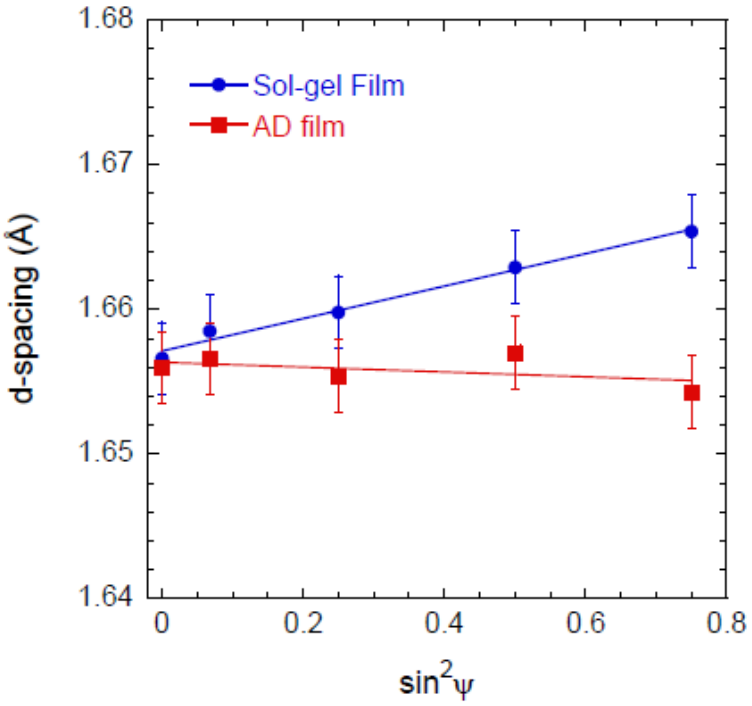

Figure 6-59: Lattice d-spacing as a function of sin2ψ of sol-gel and AD films measured from PLZT (211) diffraction peaks.

Residual stresses in the AD PLZT and the sol-gel PLZT films were investigated. To experimentally determine residual stress of PLZT films, we measured XRD patterns with various tilt angle, ψ = 0, 15, 30, 45, and 60°. The slopes of linear fitting to the experimental data, as shown in Figure 6-59, were plugged into the following equation to determine residual stress σ_ϕ.

$$\sigma_\phi = \left(\frac{E}{1+\nu}\right)_{(hkl)} \cdot \frac{1}{d_{\phi 0}} \cdot \frac{\partial d_{\phi\psi}}{\partial \sin^2\psi} \qquad (1)$$

where E and ν are Young's modulus and Poisson ratio of the thin film, and $d_{\phi 0}$ and $d_{\phi\psi}$ are the lattice d-spacing in a stressed sample that was measured at tilt angles of zero and ψ, respectively. Using E = 72 GPa and ν = 0.3, we measured tensile stress of 373 MPa in PLZT deposited on PtSi by sol-gel process and a compressive stress of -56 MPa in the PLZT films deposited by AD process on PtSi substrates [9].

Figure 6-60 shows the time relaxation current density measured with various levels of applied voltage for a ≈8 μm thick PLZT film deposited on aluminum metallized polyimide film by AD process. Steady state leakage current density can be extracted by fitting the relaxation data to Curie–von Schweidler equation,

$$J(t) = J_S + J_0 \cdot t^{-n} \qquad (2)$$

where J_S is the leakage current density, J_0 is a fitting constant, t is relaxation time in seconds and n is the slope of the log–log plot. Steady state leakage current density as a function of applied voltage is plotted in Figure 6-61. Leakage current density increases with increasing applied electric field. Under an applied electric field less than 500 kV/cm, we observed good linear dependence of steady state current density on applied electric field as shown in Figure 6-61. At room temperature, we measured leakage current density of ≈20 nA/square-cm at 100 kV/cm and <0.2 μA/square-cm at 500 kV/cm for a ≈8-μm-thick PLZT film deposited on aluminum metallized polyimide film by the AD process.

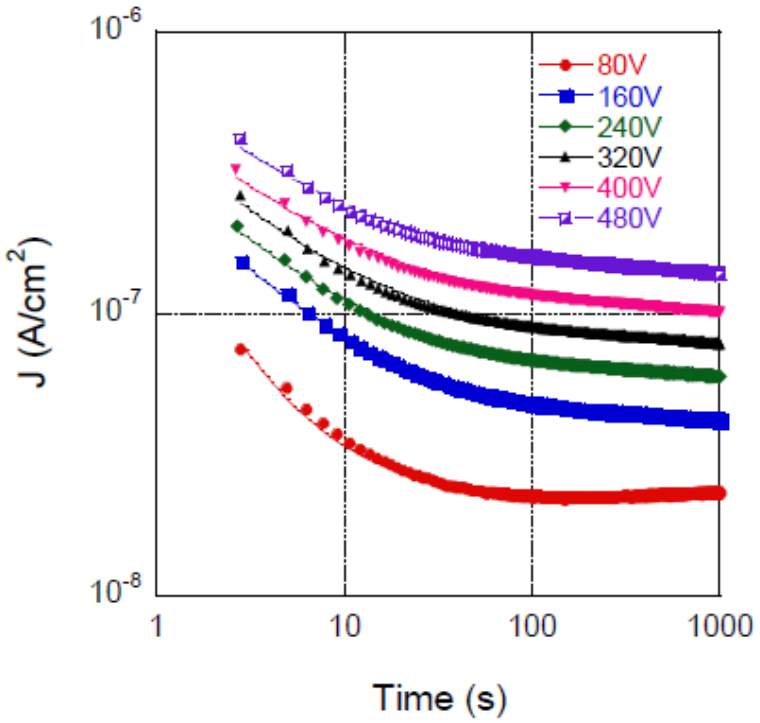

Figure 6-60: Time relaxation current density for a ≈8 µm thick AD PLZT film deposited on aluminum metallized polyimide film.

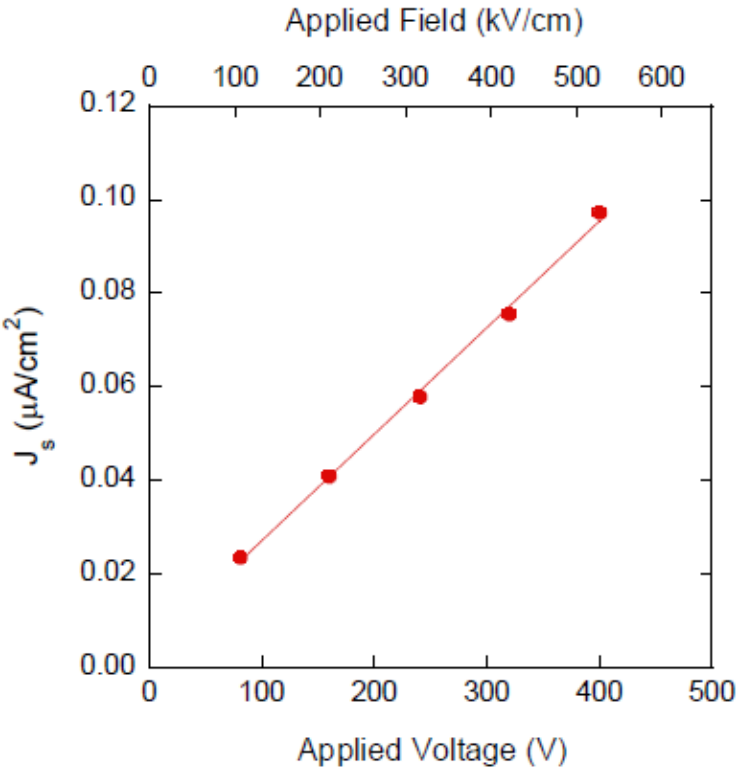

Figure 6-61: Leakage current density as a function of applied electric field for a ≈8 µm thick AD PLZT film deposited on aluminum metallized polyimide film.

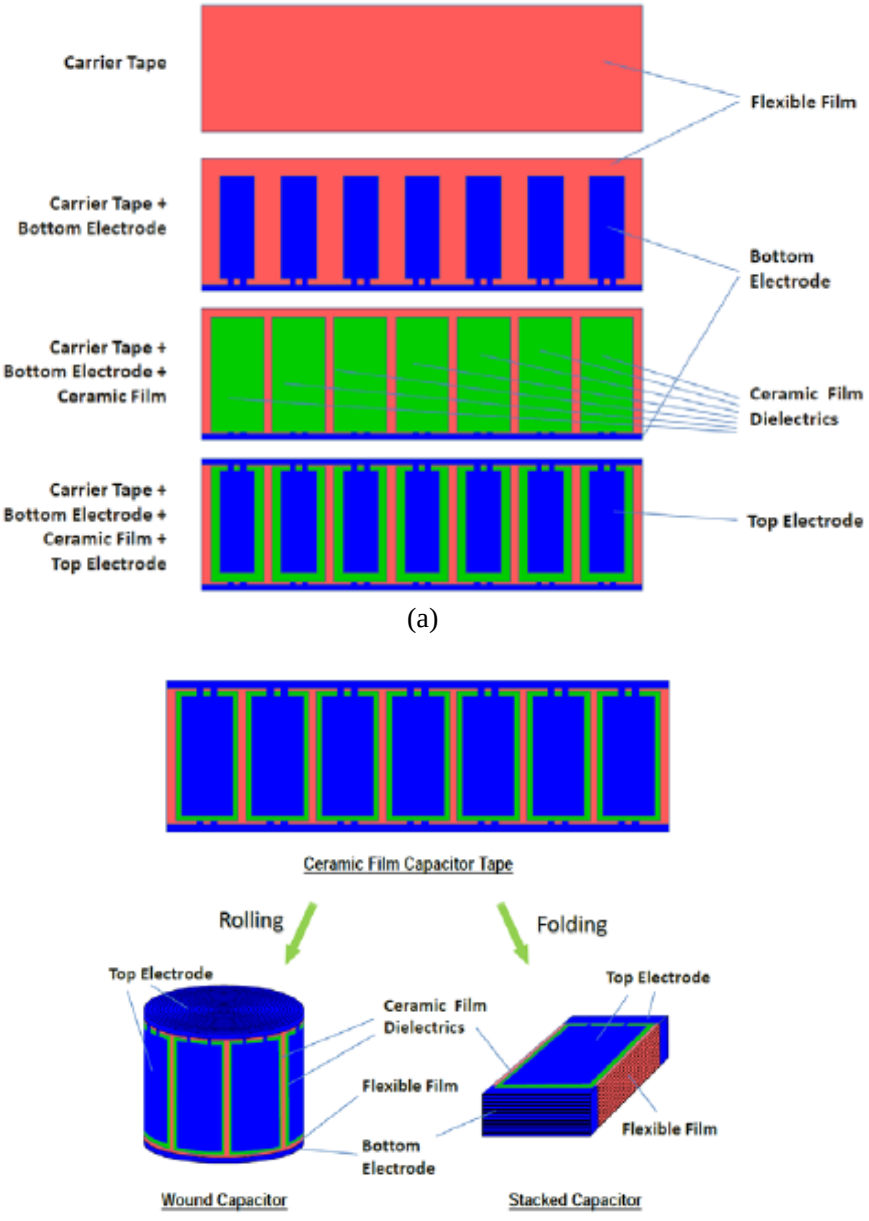

Figure 6-62: Schematic illustrations for making segmented PLZT tapes (a) and producing wound or stacked capacitors (b).

In addition to optimizing the processing conditions for producing high-quality PLZT films on metalized flexible films, we focused our effort on transferring Argonne developed room-temperature AD process to Sigma Technologies for producing long length dense PLZT films on flexible tapes. Our approach is to fabricate segmented PLZT film capacitors on long-length flexible tapes by reel-to-reel process [11,12] as illustrated by the schematic show in Figure 6-62a. The PLZT tapes with the above mentioned electrode design will be used to produce wound or stacked capacitor as illustrated by the drawing in Figure 6-62b.

Figure 6-63 shows a segment of a ~15-cm long PLZT film deposited on a flexible polymer tape with bottom and top electrodes. This sample consists of four separate capacitors with top electrodes of 156.7, 199.0, 191.3, and 152.6 square-millimeters in sizes. The average thickness of the PLZT film is about 4.5 µm. They were evaluated at Delphi at temperatures ranging from room temperature up to 140°C. Table 6-4 lists the dielectric properties measured at 10 kHz and temperatures ranging from RT to 140°C on one of the capacitors (capacitor c in Figure 6-63). Also listed in the Table are the dielectric constant and the variations of capacitance and dissipation factor (D.F.) from their room temperature values. The dielectric constant is in agreement with the

short length samples produced at Argonne, whereas the dissipation factors of these capacitors are still little higher. Optimization of the fabrication conditions will produce higher quality PLZT tapes.

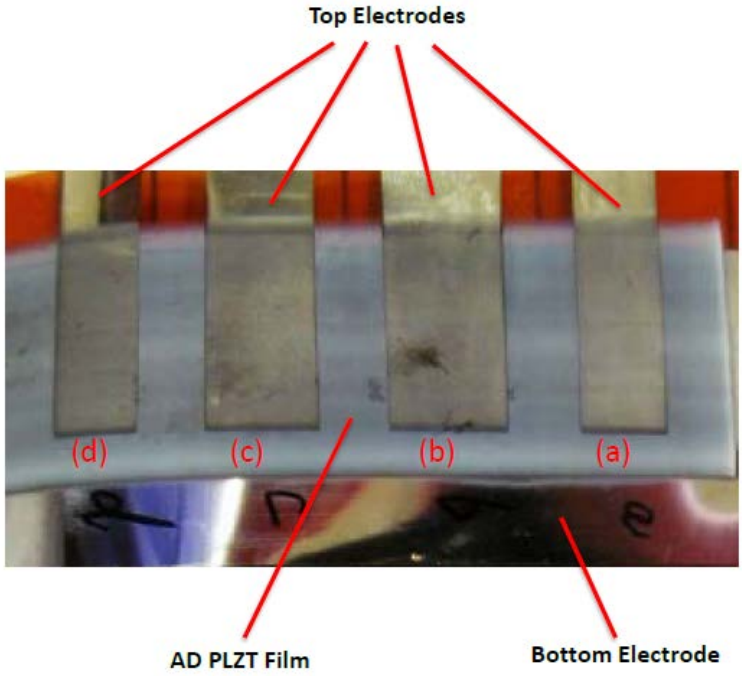

Figure 6-63: Photograph of a segment of a long-length AD PLZT film on flexible tape with electrodes.

Table 6-4: Dielectric properties of an AD PLZT sample deposited on Al/PI tape at Sigma Technologies and characterized at Delphi Electronics and Safety

Temperature	Cap (nF)	D.F.	ΔCap	Δ D.F.	Dielectric Constant
27°C	28.123	0.0812	0.00%	0.00%	74.77
40°C	28.245	0.0838	0.43%	3.20%	75.09
60°C	28.434	0.0851	1.11%	4.80%	75.60
80°C	28.853	0.0871	2.60%	7.27%	76.71
100°C	29.310	0.0894	4.22%	10.10%	77.93
120°C	29.930	0.0971	6.43%	19.58%	79.57
140°C	30.869	0.1154	9.76%	42.12%	82.07

Conclusions and Future Directions

During FY 2016, our effort was focused on two important tasks: (1) optimize process parameters of a lab-scale high-rate aerosol deposition process to cost-effectively fabricate PLZT films on thin polyimide substrates, and (2) successfully transfer the AD process to industry for producing long length PLZT tapes. We have succeeded in both tasks. The AD process allows deposition of dense PLZT films at room temperature on variety of substrates. AD PLZT films exhibit superior volumetric and gravimetric specific capacitance. The measured properties show that the PLZT-based ceramic film capacitors meet the EDT requirements for advanced high-temperature capacitors. We successfully optimized fabrication conditions to produce PLZT films by AD

process on aluminum metallized polyimide films. PLZT films fabricated by the AD process exhibited a high dielectric constant of ~100, low dielectric loss of <0.02, weak-dependence on applied field, and suitable for high field and high temperature operation. The AD process offers the greatest potential for producing low-cost, reliable, high temperature, compact and light-weight ceramic film capacitors for power inverters. Focus of our FY 2017 effort is to continue working with our industrial partners and optimize the AD processing conditions for producing long-length, high-quality PLZT tapes on a rotating-wheel coating system, fabricate and characterize proto-type capacitors, demonstrate self-healing in the proto-type capacitors, and perform detailed costing and commercialization plan to meet DOE's cost and performance targets.

FY 2016 Presentations/Publications/Patents

1. U. Balachandran, B. Ma, T.H. Lee, S.E. Dorris, "Development of PLZT Film Capacitors for Power Invertors," Presented at 2016 International Union of Materials Research Societies - International Conference on Electronic Materials, Singapore, Jul. 4 - 8, 2016.
2. U. Balachandran, B. Ma, T.H. Lee, S.E. Dorris, "Fabrication and Characterization of PLZT Films for Advanced Power Invertors in Electric Drive Vehicles," Presented at 2016 Electronics Materials and Applications Conference (EMA), Orlando, FL, Jan. 20 - 22, 2016.
3. B. Ma, T.H. Lee, S.E. Dorris, U. Balachandran, "Ceramic Film Capacitors for High-Temperature Electrics," Presented at the 2015 Materials Science and Technology Conference (MS&T2015), Columbus, OH, Oct. 4 - 8, 2015.
4. Z. Hu, B. Ma, M. Li, R.E. Koritala, U. Balachandran, "Ferroelectric PLZT Thick Films Grown by poly (1-vinylpyrrolidone-co-vinyl acetate) (PVP/VA)-Modified Sol–gel Process," Materials Research Bulletin 75, 167-171, 2016.
5. B. Ma, Z. Hu, R.E. Koritala, T.H. Lee, S.E. Dorris, U. Balachandran, "PLZT Film Capacitors for Power Electronics and Energy Storage Applications," Journal of Materials Science: Materials in Electronics 26, 9279-9287, 2015.
6. D.-H. Choi, C. Randall, E. Furman, B. Ma, U. Balachandran, S. Zhang, M. Lanagan, "Energy and power densities of capacitors and dielectrics," Proceedings of the 2015 IEEE International Workshop on Integrated Power Packaging (IWIPP), pp. 52 - 55, Oct. 12, 2015
7. B. Ma, S. Liu, Z. Hu, M. Narayanan, U. Balachandran, "Effect of Manganese Oxide Insertion Layer on the Dielectric and Ferroelectric Properties of Pb0.92La0.08Zr0.52Ti0.48O3 Films Grown by a Sol-gel Process," Materials Research Bulletin 67,134-139, 2015.
8. U. Balachandran, M. Narayanan, B. Ma, S.E. Dorris, "Low Resistivity Materials for Use in Electrodes," US Patent Application 20160278215 A1, published 09/22/2016.
9. M. Narayanan, B. Ma, U. Balachandran, S.E. Dorris, "Method for producing thin film electrodes," US Patent No. 9,359,223 B2, issued 06/07/2016.
10. B. Ma, U. Balachandran, S.E. Dorris, T.H. Lee, "Ceramic Dielectric Films, Method for Making Ceramic Dielectric Films," US Patent Application 20160153084 A1, published 06/02/2016.
11. B. Ma, M. Narayanan, U. Balachandran, S. Chao, S. Liu, "Method for fabrication of crack-free ceramic dielectric films," US Patent No. 9,355,761 B2, issued 05/31/2016.
12. M.R. Fairchild, R.S. Taylor, C.W. Berlin, C.W. Wong, B. Ma, U. Balachandran, "PLZT Capacitor on Glass Substrate," US Patent No. 9,299,496 B2, issued 03/29/2016.
13. M.R. Fairchild, R.S. Taylor, C.W. Berlin, C.W. Wong, B. Ma, U. Balachandran, "PLZT Capacitor on Glass Substrate," US Patent No. 9,230,739 B2, issued 01/05/2016.
14. B. Ma, U. Balachandran, S.E. Dorris, T.H. Lee, "Wound/Stacked Ceramic Film Capacitors, Method for Making Ceramic Film Capacitors," US Patent Application 20150364257 A1, published 12/17/2015.

References

1. B. Ma, M. Narayanan, S.E. Dorris, U. Balachandran, "Method for Fabrication of Ceramic Dielectric Films on Copper Foils," US Patent 8.974,856 B2, issued March 10, 2015.
2. U. Balachandran, D. K. Kwon, M. Narayanan, B. Ma, "Development of PLZT Dielectrics on Base Metal Foils for Embedded Capacitors," J. European Cer. Soc., 30, 365, 2010.
3. B. Ma, M. Narayanan, U. Balachandran, "Dielectric Strength and Reliability of Ferroelectric PLZT Films Deposited on Nickel Substrates," Materials Letters, 63, 1353, 2009.
4. U. Balachandran, M. Narayanan, S. Liu, B. Ma, "Development of Film-on-Foil Ceramic Dielectrics for Embedded Capacitors for Power Inverters in Electric Drive Vehicles," Jpn. J. Appl. Phys. 52, 05DA10, 2013.
5. B. Ma, D.-K. Kwon, M. Narayanan, U. Balachandran, "Chemical Solution Deposition of Ferroelectric Lead Lanthanum Zirconate Titanate Films on Base-Metal Foils," J. Electroceram. 22, 383-389, 2009.
6. K.D. Budd, S.K. Dey, D.A. Payne, "Sol-Gel Processing of PbTiO3, PbZrO3, PZT, and PLZT Thin Films," Proc. Br. Ceram. Soc. 36, 107, 1985.
7. B. Ma, S. Tong, M. Narayanan, S. Liu, S. Chao, U. Balachandran "Fabrication and Dielectric Property of Ferroelectric PLZT Films Grown on Metal Foils," Materials Research Bulletin 46, 1124-1129, 2011.
8. S. Chao, B. Ma, S. Liu, M. Narayanan, U. Balachandran, "Effects of Pyrolysis Conditions on Dielectric Properties of PLZT Films Derived from a Polyvinylpyrrolidone-Modified Sol–Gel Process," Materials Research Bulletin 47, 907-911, 2012.
9. B. Ma, S. Liu, S. Tong, M. Narayanan, R.E. Koritala, Z. Hu, U. Balachandran, "Residual Stress of (Pb0.92La0.08)(Zr0. 52Ti0.48)O3 Films Grown by a Sol-Gel Process," Smart Materials and Structures 22, 055019, 2013.
10. J. Akedo, "Aerosol Deposition of Ceramic Thick Films at Room Temperature: Densification Mechanism of Ceramic Layers," J. Am. Ceram. Soc. 89, 1834-1839, 2006.
11. B. Ma, U. Balachandran, S.E. Dorris, T.H. Lee, "Wound/Stacked Ceramic Film Capacitors, Method for Making Ceramic Film Capacitors," US Patent Application 20150364257 A1, published 12/17/2015.
12. B. Ma, U. Balachandran, S.E. Dorris, T.H. Lee, "Ceramic Dielectric Films, Method for Making Ceramic Dielectric Films," US Patent Application 20160153084 A1, published 06/02/2016.

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