Highly Integrated Wide Bandgap Power Module for Next Generation Plug-In Vehicles

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Overview

Timeline

- Start – 1 January 2016
- Finish – 30 September 2019
- 20% Complete

Funding

- Project Budget $5.67 million
  - $3.79M Federal Share
  - $1.88M GM Cost Share
- $378,929 funds received FY16
- $1.2M funds planned FY17

Vehicle Technology Barriers

- Lower Cost Electric Drive Systems
- Higher Efficiency, long range EV
- Higher Performance and Lifetime
- Lower Mass and Volume

Project Team

- Lead:
  - General Motors, LLC
- Subrecipients:
  - Virginia Polytechnic Institute and State University
  - Oak Ridge National Lab
  - Monolith Semiconductor, Inc.
- Key Suppliers:
  - Wolfspeed (Cree Power)
- Collaborations:
  - PowerAmerica

Project Relevance

Research Focus Area: Inverter

- WBG Semiconductor based power stage
- Technical development for key components needed for a WBG Power Stage: gate drive, capacitor, high bandwidth current sense

Objective

- Automotive power module with SiC MOSFET dies
- Reduce Inverter and Motor losses over the drive cycle
- Implement selected bonding, joining and thermal management technology to reduce thermal impedance, improve high temperature reliability and reduce volume

Addresses Targets

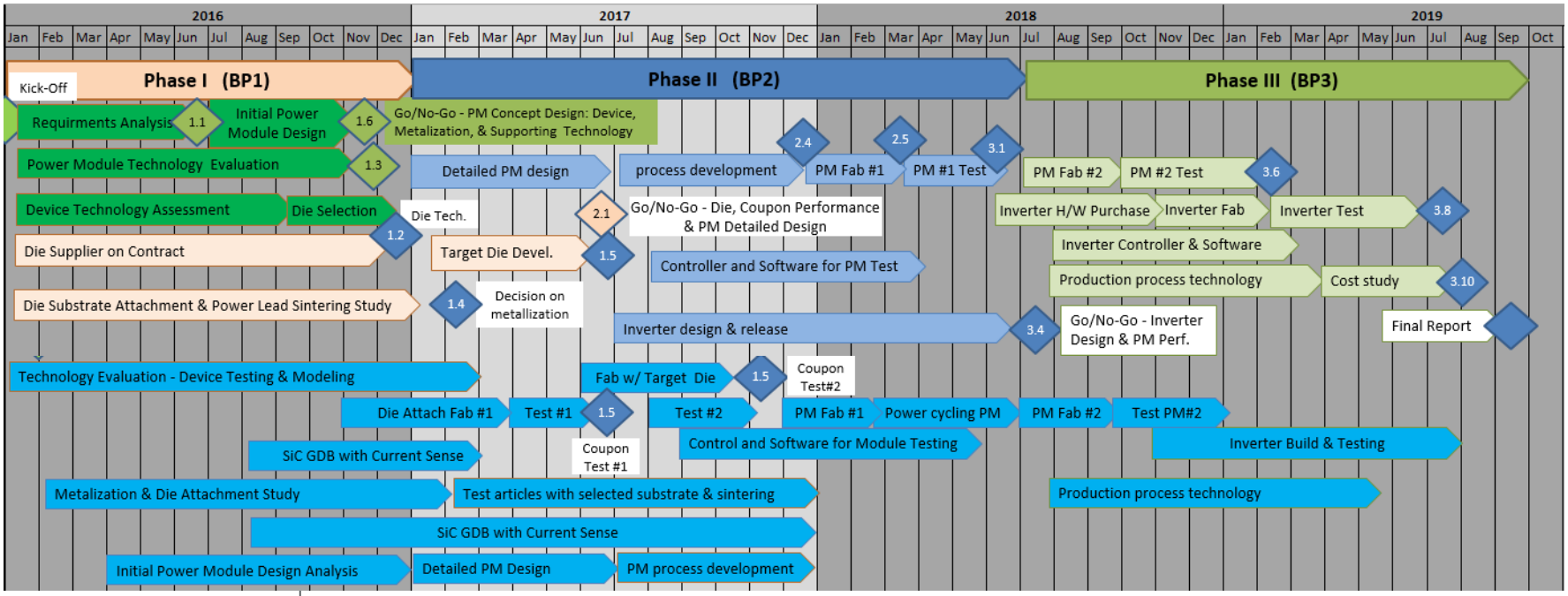
- Enable inverter to meet or exceed DOE 2020 targets:
- Power Density: 13.4kW/l; Specific power: 14.1kW/kg & $3.3/kW
- Efficiency >94% (10%-100% speed at 20% rated torque)

Uniqueness and Impacts

- Compact, high temperature, low inductance automotive package

Milestones

Date	2016-2017 Milestone or Go/No-Go Decisions	Status
Nov - 2016	Device Technology Assessment - Milestone	Completed
Dec - 2016	Initial Power Module Design - Go/No-Go #1	Go
Feb - 2017	SiC MOSFET Top Side Metallization decision	Completed
June - 2017	Detailed Power Module Design - Go/No-Go #2	On-Track
Dec - 2017	Prototype Manufacturing Process Development	On-Track



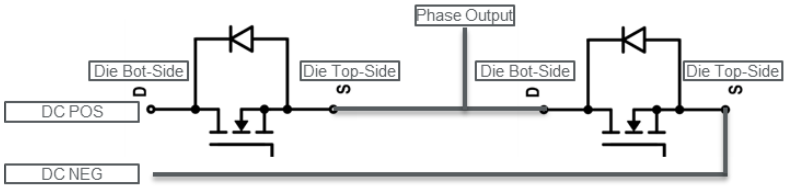
Overall Technical Approach & Accomplishments

Key Technical Approaches for Phase One - Design Concept Development Phase

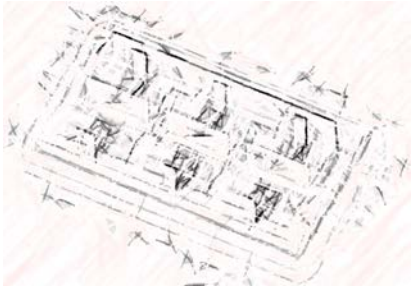
- Achieve 600Vdc, 425Apk, 300Arms rated automotive power module with SiC MOSFET dies, in a high temperature (200°C), low inductance (5 nH) package
- Show Concept will reduce electric drive system losses over critical drive cycles
- Select dies, bonding, joining and thermal management technology to reduce thermal impedance, improve high temperature reliability and reduce package volume

Phase One Technical Implementation & Accomplishments

- Evaluate candidate die for use in the SiC MOSFET automotive power module
- Electrical & thermal margin to eliminate external Schottky Barrier Diode(SBD) diodes
- Employ a two-sided sinterable metallization concept in packaging to enhance cooling
- Use bottom side pin-fin cooling with thermal connectivity from die top to baseplate
- Develop concept for multi-layer sintered substrates to reduce loop inductances
- Two patents filed: P036622 for Two Layer Sintering, and P036694 Power Module



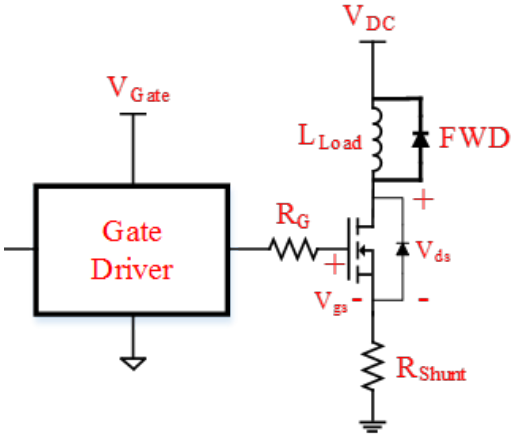
Low Inductance Electrical Packaging Concept



Power Module Concept

Static & Dynamic Die Evaluation

Double Pulse Test Circuit



DPT Test Values		
L_{load}	=	1 mH
R_{Shunt}	=	25.28 mΩ
R_G	=	3.01 Ω

Parameter*	Comp. A	Comp. B		Comp. C
Vds_Max	0.75	1	1	0.54
Rds_On	0.4	1	0.4	0.92
Id_Max	1.33	1.17	2.5	1.33
Test Voltage	1	1	1	0.67
Rds_on @ 100°C	0.28	0.42	0.25	0.28
Gate Charge, Qg	1.08	1.00	N/A	1.43
E_on + E_off	**0.15**	**0.14**	**0.15**	**0.11**

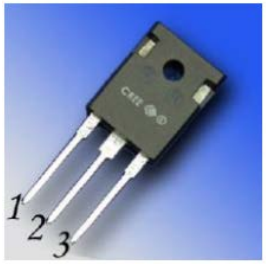
*** All values are on per unit basis**

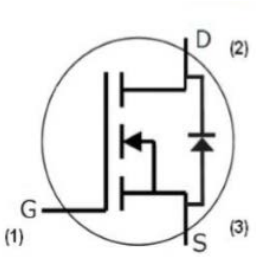
Target die have industry leading performance and meet expectations for the application

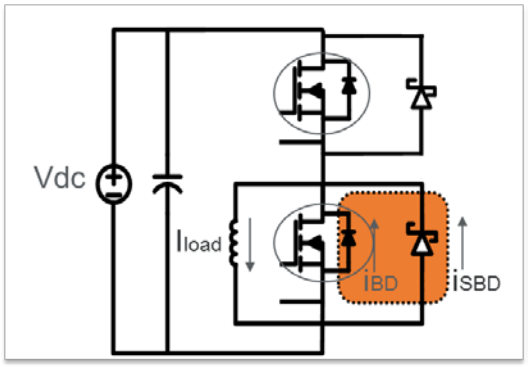
Performed by subrecipient: Virginia Polytechnic Institute and State University & GM

Extra Loss without External SiC Schottky Barrier Diode(SBD) is Low

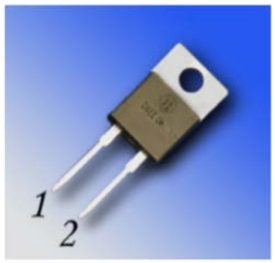
3rd Gen. SiC MOSFET







4th Gen. SiC SBD



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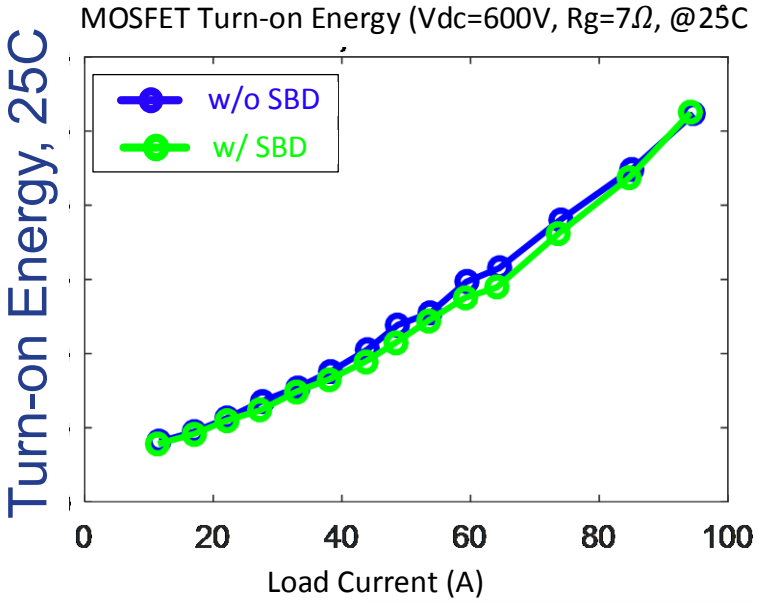
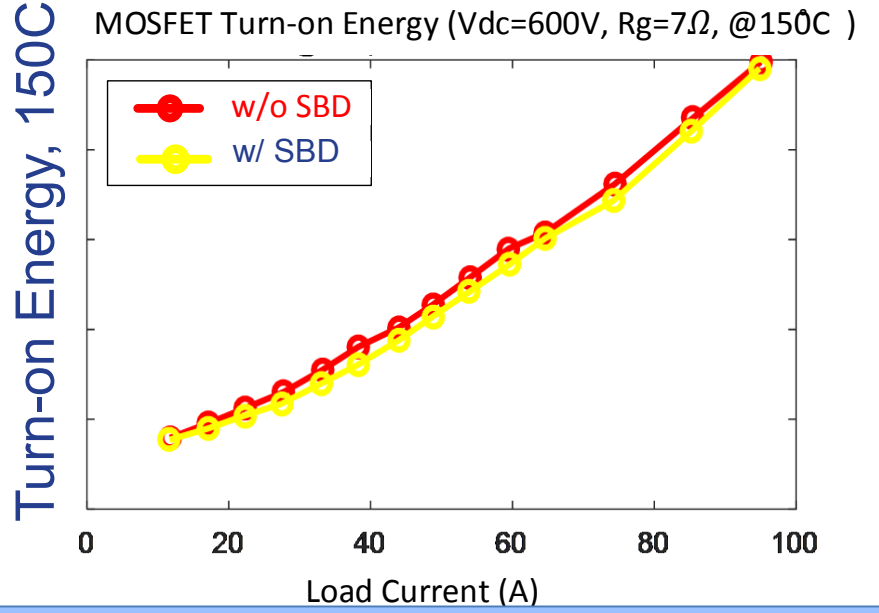




GENERAL MOTORS

SBD does not have a significant role in reducing switching electrical losses for 3rd Gen SiC MOSFET

Testing performed by subrecipient: Virginia Polytechnic Institute and State University

Concept has Sufficient Thermal Margin to Eliminate External SBD

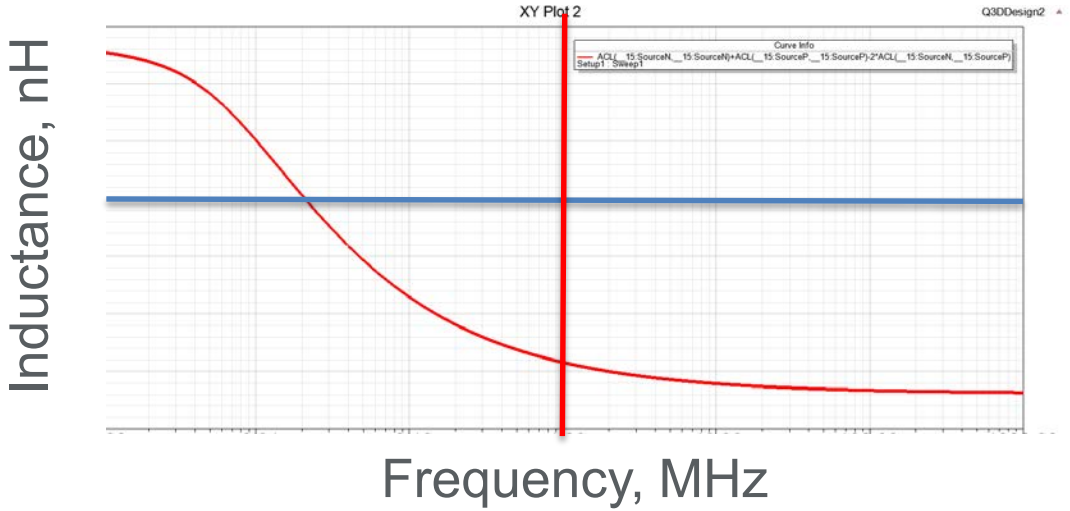
- Thermal modeling was performed on the design concept
- Maximum die temperature is estimated to have 10°C margin
- Analysis performed at target coolant temperature and flow
- Steady state condition utilized measured die loss
- Power module thermal performance has margin without SBD

CAE shows design concept with minimum die per switch meets target performance with 10 °C margin

Work performed by subrecipient: Virginia Polytechnic Institute and State University

Concept Meets Inductance Targets

- Module CAD Model simplified & imported to CAE tool
- Power module power and signal path analyzed
- Inductance calculated from FEA modeling
- Power loop inductance predicted to be below target
- Signal loop inductance predicted to be below target

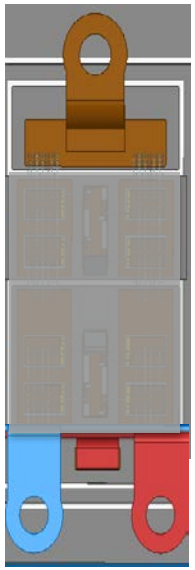


Design concept inductance predicted to be below targets

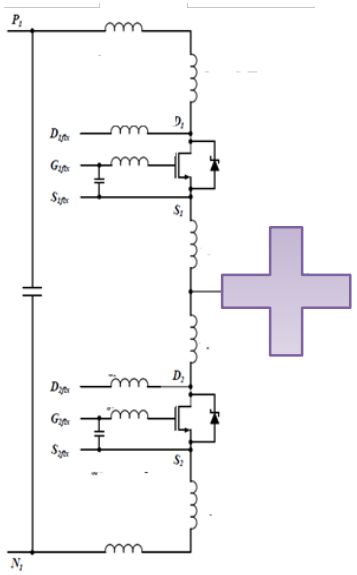
Modeling performed by General Motors, LLC

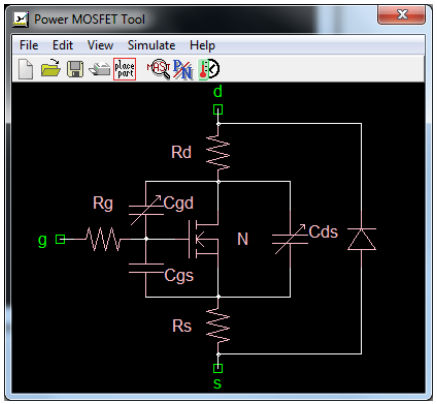
Power Module Concept Physical Extraction to Electrical Model

Parasitic Extraction

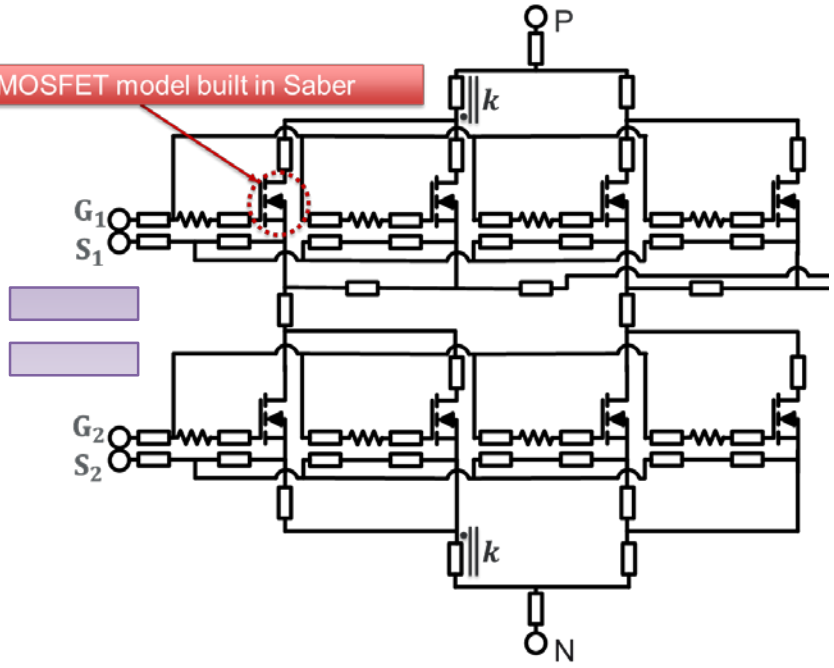


Concept





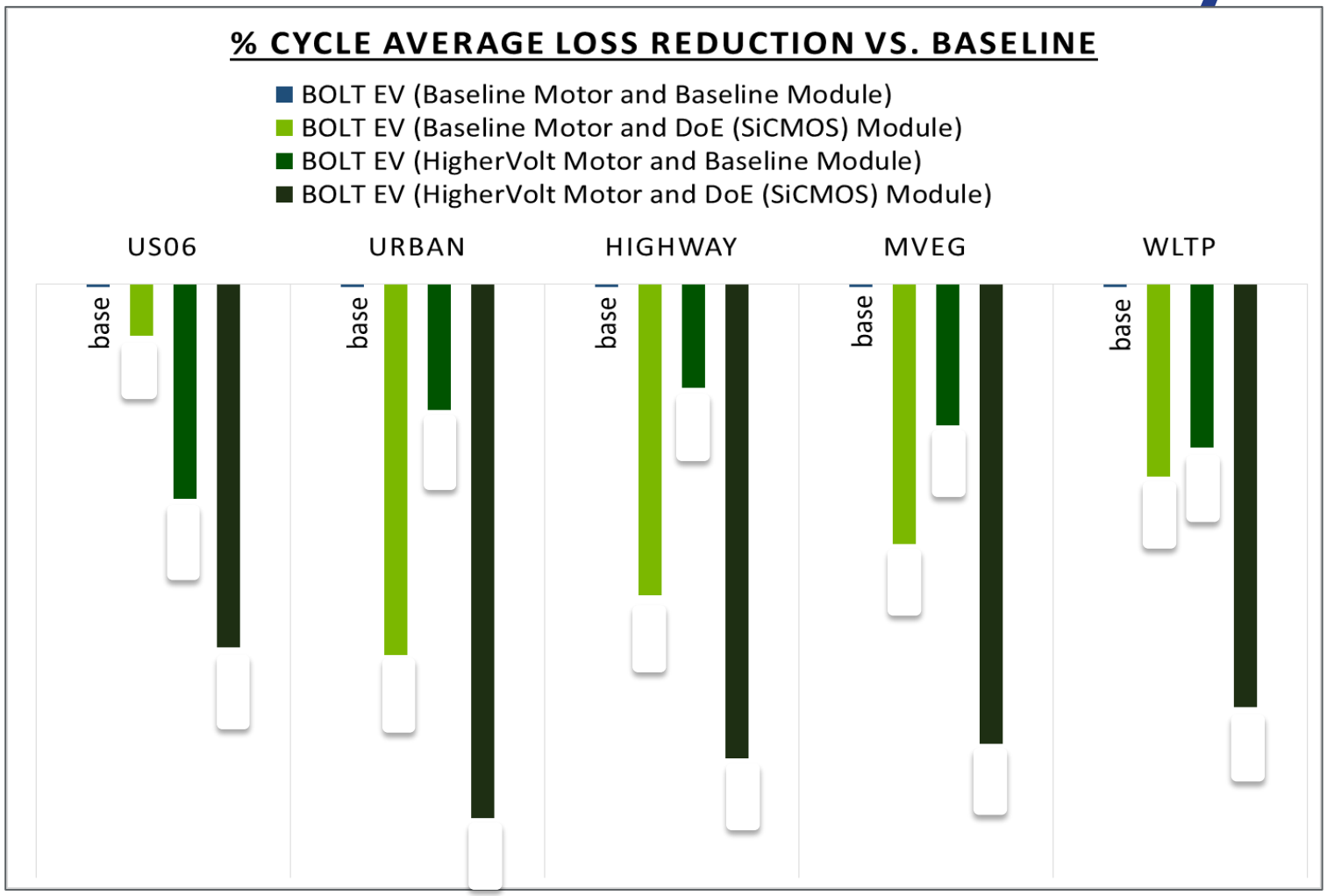
Die Model



Design concept electrical model developed for system simulations

Modeling performed by General Motors, LLC

Potential Electric Drive System Loss Reduction in Critical Drive Cycles



Employing high voltage motor compatible with WBG voltage significant cycle average loss reductions possible

Modeling performed by General Motors, LLC

Remaining Challenges Barriers & Future Plans

Challenges & Potential Barriers

- Higher temperature encapsulates & capacitors
- High bandwidth low cost current sensing
- Gate Drive improvements: Three times faster short circuit protection, than typical Si IGBT "De-Sat" protection schemes, High common-mode transient immunity (CMTI)

Future Plans (FY2017)

- Perform sintering trials on various coupon configurations with both Pressured and pressure-less techniques
- Build half bridge test coupons to verify phase one models
- Build prototype Gate Drive PCB with Rogowski Coil Current sensing for current measurement & short circuit protection
- Perform power module detailed design and inverter concept
- Identify prototype build processes and partner for fabrication

Proposed future work is subject to change based on funding levels and Go/No-Go gate review

Summary

- Die from project partners, demonstrate industry leading performance as compared to other early samples tested
- Addition of SBD does not play an obvious role in reducing electrical switching energy in 3rd Gen SiC
- Design concept package footprint is about half the size of industry leading silicon IGBT power modules
- Package inductance, and thermal performance have been modeled & are below targets
- Project goal to “operate more efficiently” has been analyzed
- Project is progressing to phase two - detailed design, coupon construction & confirmation tests