650V SiC Integrated Power Module for Automotive Inverters

Monty B. Hayes

Delphi Automotive Systems, LLC

Project Number: EDT083

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06/07/2017

Project Overview

Timeline

Project Start Date: January 1, 2016
Project End Date: February 28, 2018
Percent Complete: 40%

Barriers

Cost ($/kW)	<3.3
Specific Power (kW/kg)	>14.1
Power Density (kW/L)	>13.4

Budget

Total Project Funding:	$2,161,561
DOE Share:	$1,488,303
Contractor Share:	$673,258
Funding Received in 2016:	$656,921
Funding for FY 2017:	$831,381

Partners

Delphi - Lead
Wolfspeed
Oak Ridge National Labs
Volvo

Relevance Project Objectives

- Develop a double-sided cooled 650V Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) packaged power device
  - Capable of traction drive inverter application targeted to meet DOE's 2020 electric drive vehicle (EDV) inverter targets as shown

Parameter	Target
Cost ($/kW)	< 3.3
Specific Power (kW/kg)	> 14.1
Power Density (kW/L)	> 13.4

Double-side cooled 650V SiC MOSFET Packaged Power Device

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Milestones

- Optimization of SiC MOSFET with top-side metallurgy
- Semiconductor package design/layout turn 1
- SiC MOSFET power semiconductor device fabrication and characterization
- Semiconductor package characterization
- Prototype inverter performance

Milestones

Budget Period 1

Milestone	Type	Description	Status
Configuration Selection	Technical	Selection of 650V SiC MOSFET power semiconductor device/module with an Rdson of 7-8 mΩ. The down selection will include device rated breakdown voltage, current rating and switching frequency for the inverter application.	Complete
Fabrication Completed	Technical	SiC MOSFET device fabrication completed	In Progress
Device Build Completed	Technical	SiC MOSFET packaged devices build completed	In Progress
Traction Drive Inverter System Design Completed	Technical	Complete design of Traction Drive Inverter System	Complete
Characterization Completed	Go/No-Go	SiC MOSFET packaged devices characterized across temperature and design of inverter. Provide characterization data for the 7-8 mΩ device and projected inverter performance comparison to the DOE 2020 goals. The potential to meet cost and performance goals are assessed to determine if the project should proceed.	Complete

Budget Period 2

Milestone	Type	Description	
Characterization and Pre-Qualification Completed	Technical	Characterization of SiC MOSFET device completed	In Progress
Prototype Design Completed	Technical	Prototype inverter design/layout completed	In Progress
Traction Inverter Build and Evaluation Completed	Technical	Build and evaluation of the traction drive inverter completed	Not Started
Prototype Test Completed	Technical	Prototype inverter hardware build, debug and test completed	Not Started
Characterization Completed	Technical	Semiconductor package characterization and evaluation completed	Not Started

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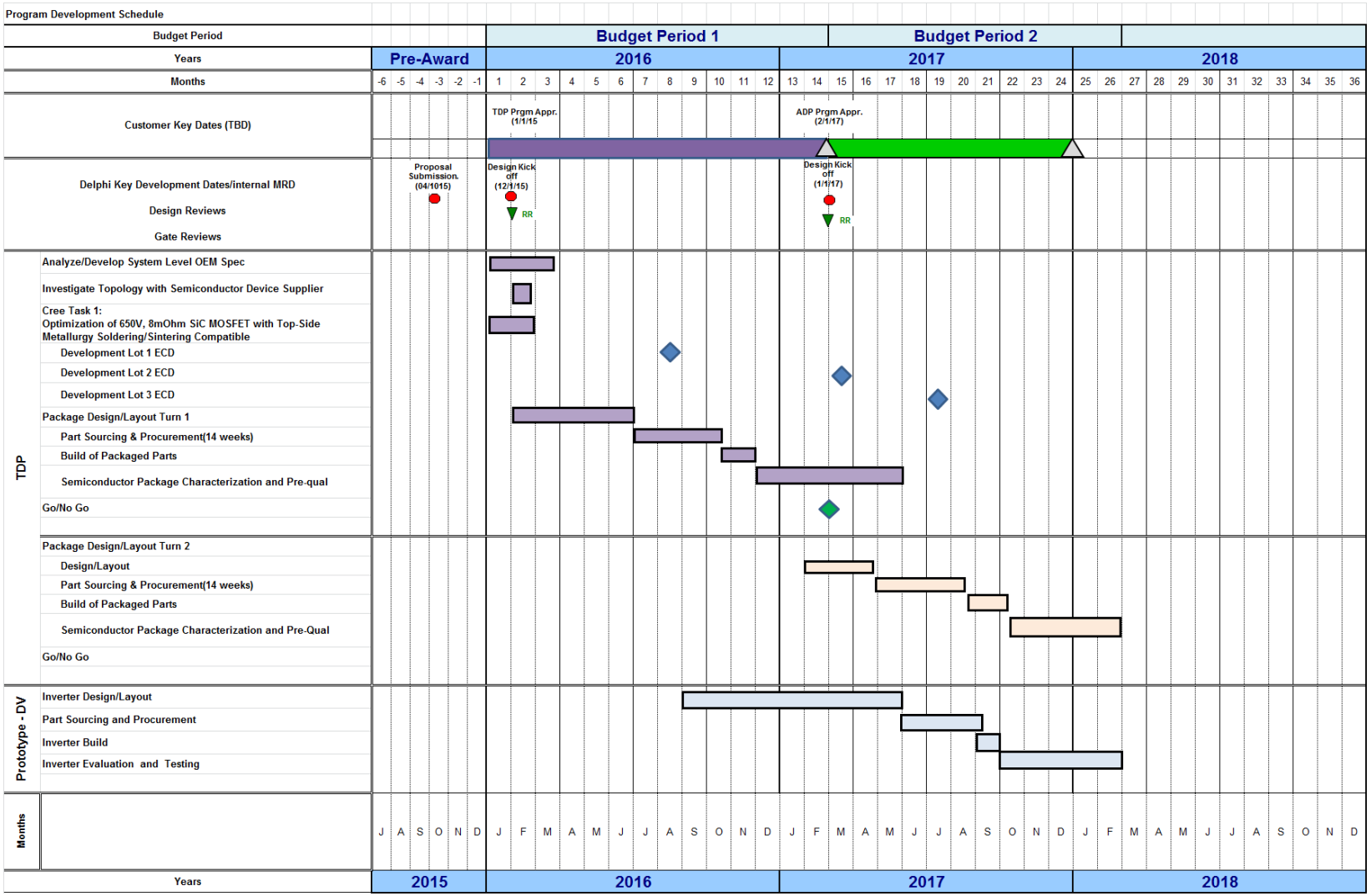
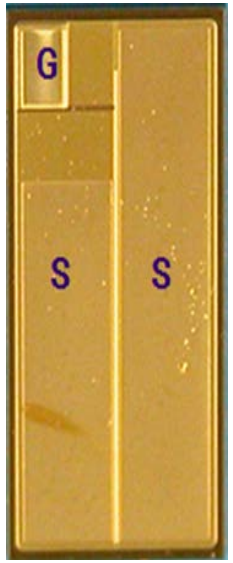
Approach


Program Development Schedule
Budget Period
Budget Period 1
Budget Period 2
Years
Pre-Award
2016
2017
2018
Months
-6 -5 -4 -3 -2 -1 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36
Customer Key Dates (TBD)
TDP Prgm Appr. (1/1/15
ADP Prgm Appr. (2/1/17)
Delphi Key Development Dates/internal MRD
Design Reviews
Gate Reviews
Proposal Submission. (04/1015)
Design Kick off (12/1/15)
RR
Design Kick off (1/1/17)
RR
TDP
Analyze/Develop System Level OEM Spec
Investigate Topology with Semiconductor Device Supplier
Cree Task 1:
Optimization of 650V, 8mOhm SiC MOSFET with Top-Side Metallurgy Soldering/Sintering Compatible
Development Lot 1 ECD
Development Lot 2 ECD
Development Lot 3 ECD
Package Design/Layout Turn 1
Part Sourcing & Procurement(14 weeks)
Build of Packaged Parts
Semiconductor Package Characterization and Pre-qual
Go/No Go
Package Design/Layout Turn 2
Design/Layout
Part Sourcing & Procurement(14 weeks)
Build of Packaged Parts
Semiconductor Package Characterization and Pre-Qual
Go/No Go
Prototype - DV
Inverter Design/Layout
Part Sourcing and Procurement
Inverter Build
Inverter Evaluation and Testing
Months
J A S O N D J F M A M J J A S O N D J F M A M J J A S O N D J F M A M J J A S O N D
Years
2015
2016
2017
2018

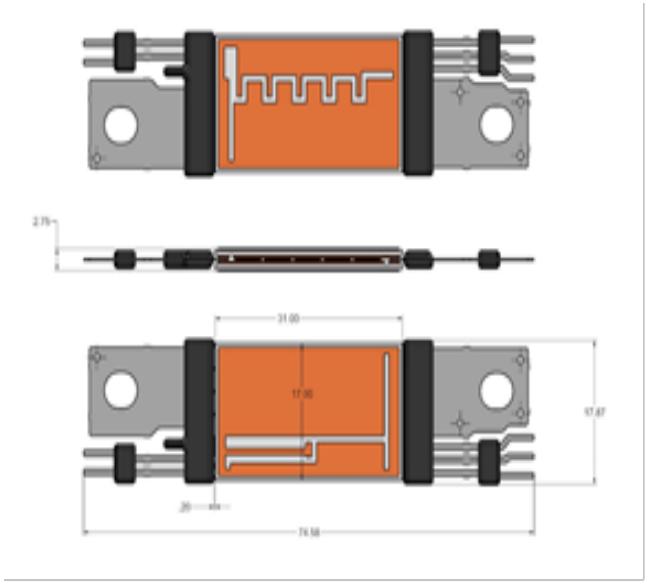
Technical Accomplishments
Layout of Wolfspeed 650V SiC MOSFET

- Wolfspeed 650V G3 MOSFETs on a 4” wafer
  - Die size 37mm^2
  - 1st Development lot received
  - Mean Rdson ~7.7mΩ (at 75A, 25°C)
  - Mean avalanche voltage 964V (25°C)
  - V_{th} > 2V
  - Top-side metallization for Delphi packaging
  - 500 samples shipped



Technical Accomplishments
Dual-sided Cooled Packaged Device Assembly

- Delphi packaged power device
  - 5 MOSFETs in parallel
  - Thermistor
- Pb-free solder
- Build 1
  - 90+% package electrical yield
  - 50 packaged parts
  - 250 Lot1 MOSFETs



SiC Package Designed for 500Arms Capability

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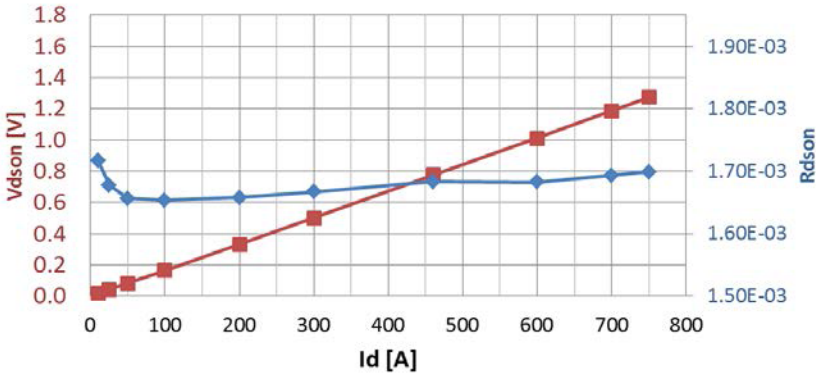
Technical Accomplishments
Static Characterization Packaged Semiconductor

25°C DC characterization data

	Mean	Std. Dev.	
IGSS +20V	26.3	43.5	pA
Vf (100mA-4V)	2.539	0.001	V
VT 200mA	2.088	0.116	V
IDSS 700V	3.69	1.69	uA
BVDSS 10mA	978.8	16.0	V
VDSON 750A	1.274	0.034	V
RON750	1.699	0.045	mOhms

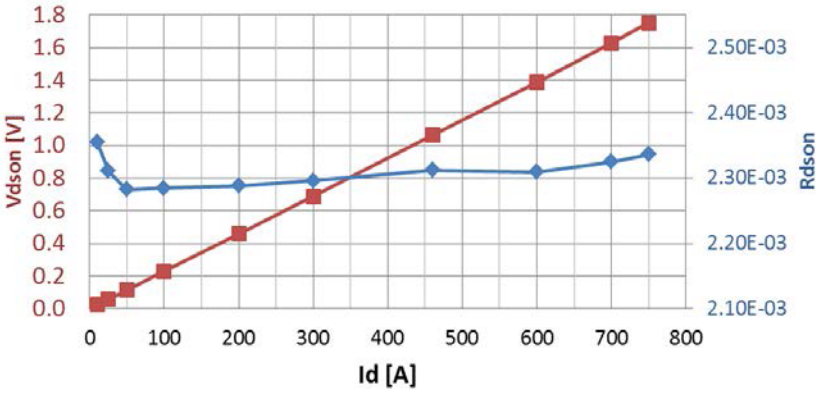
25°C Package VDSON, RDSON



175°C DC characterization data

	Mean	Std. Dev.	
IGSS +20V	360.7	99.8	nA
Vf (100mA-4V)	2.203	0.006	V
VT 200mA	1.480	0.095	V
IDSS 700V	29.91	7.18	uA
BVDSS 10mA	986.6	15.1	V
VDSON 750A	1.752	0.036	V
RON750	2.336	0.048	mOhms

175°C Package VDSON, RDSON



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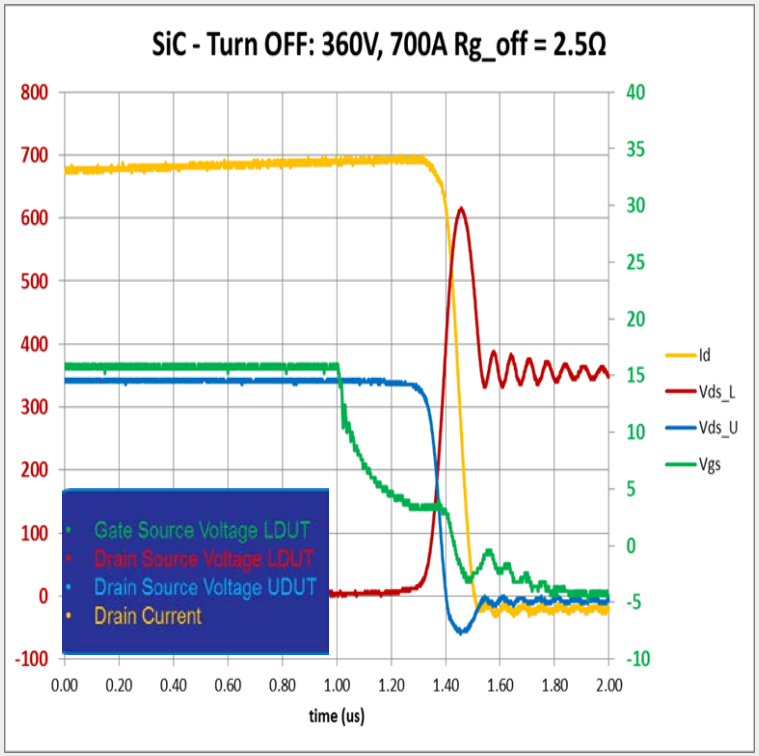
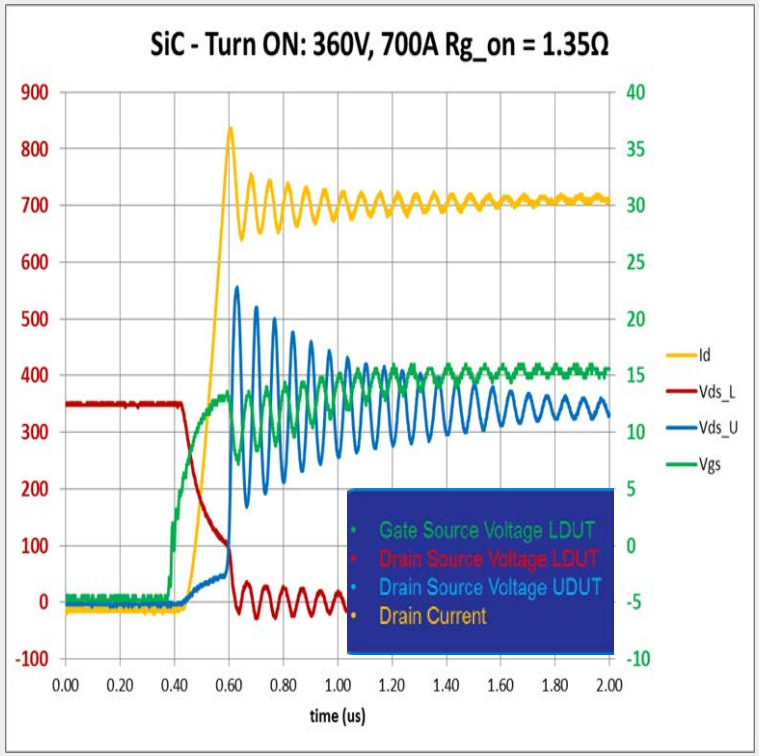
Technical Accomplishments
Dynamic Characterization Packaged Semiconductor

Turn OFF waveforms



Turn ON waveforms



Packaged SiC MOSFET: Switching Waveforms

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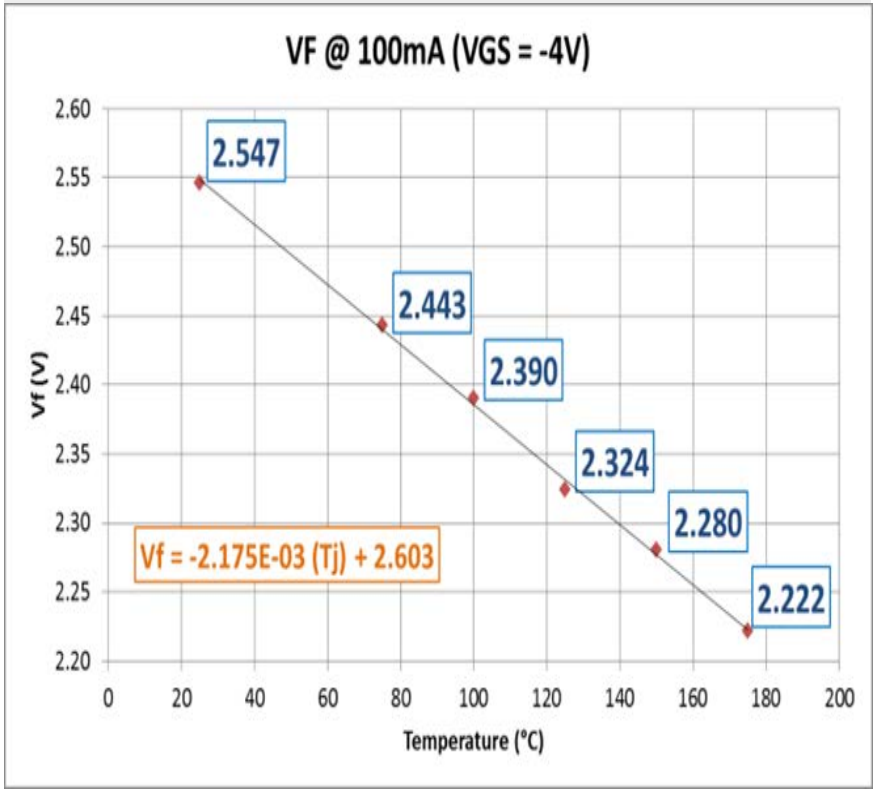
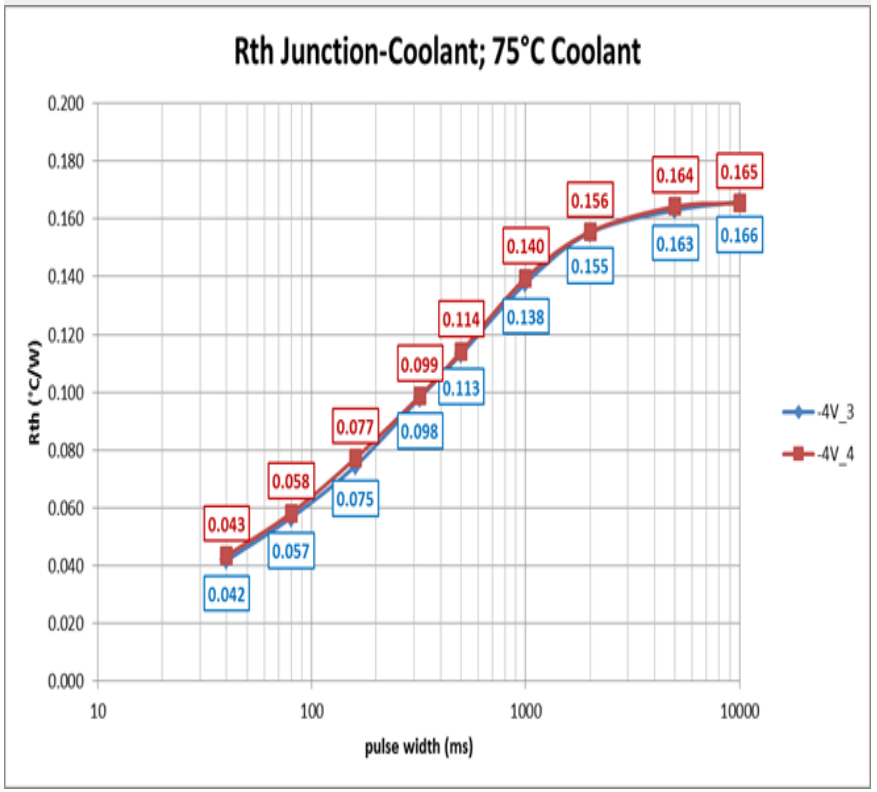
Technical Accomplishments
Thermal Characterization of Heat Sink Assembly

Body Diode VF vs. Temperature



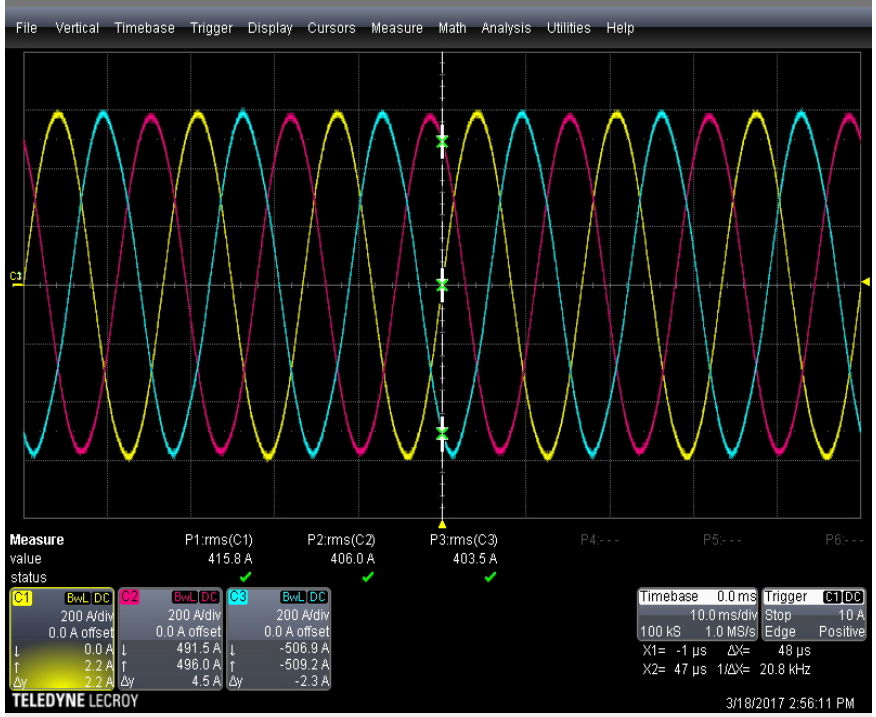
Transient Thermal Resistance in Heat Sink Assembly



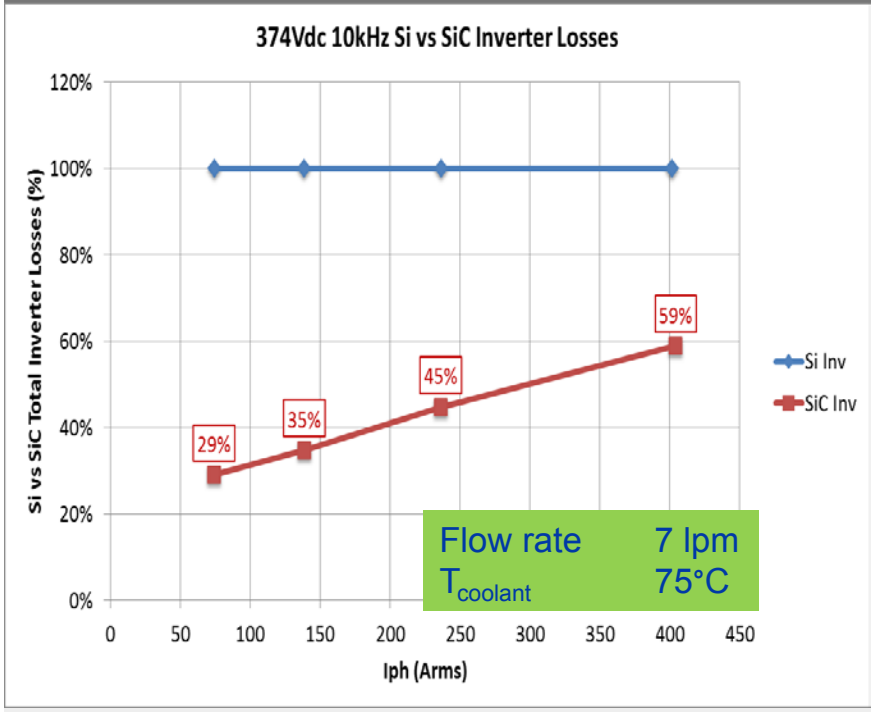
Thermal characterization of heat sink assembly

Technical Accomplishments
Inverter Losses Using 3-Phase Inductive Load

3-ph Inverter output: 410Arms



Silicon and Silicon Carbide Total Inverter Losses



SiC Inverter Performance

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Responses to Previous Year Reviewers' Comments

- The project was started in 2016 and was not reviewed at the previous year's Annual Merit Review

Collaboration and Coordination with Other Institutions

- Delphi -
  - Semiconductor device floorplan
  - Power semiconductor design, build and characterization
  - Inverter design, build and characterization
  - Device and power module pre-qualification testing

- Wolfspeed
  - 650V SiC MOSFET design and layout
  - Fabrication and characterization of the SiC MOSFET
  - Pre-qualification testing at the die level

- Oak Ridge National Laboratory
  - Inverter gate drive optimization
  - Modeling of power module

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Remaining Challenges and Barriers

- Optimizing the design for cost and performance for high currents in the order of 650 - 900Arms is a challenge.
- Developing accurate cost models for the SiC based on realistic potential volumes is a challenge.
- Cost is potentially a barrier for some applications and may inhibit widespread adoption for some applications.
- Optimized gate drive perfromance is a challenge
- Sort Circuit Safe Operating Area is a concern
- Meeting EMC performance for automotive applications is a challenge due to the high switching speeds

Proposed Future Research

- Continue build of Single Switch device
- Continue reliability testing at the die and package level
- Complete design of half-bridge semiconductor package
- Build and characterize half-bridge semiconductor package across temperature
- Complete second turn of inverter with half-bridge semiconductor package
- Optimization of gate drive for SiC half-bridge semiconductor module
- Quantify potential costs at significant SiC device modules for comparison to Si based IGBT and Diode traction drive inverter

Any proposed future work is subject to change based on funding levels.

Summary

Single Switch Power Device and Packaging

- To date a dual side cooled 650V single switch power semiconductor device has been designed and fabricated
  - 500Arms capability
  - Die size 37mm^2
  - Mean Rdson ~7.7mΩ (at 75A, 25°C)
- Statically and dynamically test at the device and package level
- Thermal performance in heat rail has been characterized
- Tested in a dual side cooled traction inverter application configuration
- SiC inverter losses have been compared to state-of the art Si IGBT and Diode

Half-bridge Power Semiconductor Device and Packaging

- Device has been designed

Thank You