Gate Driver Optimization for WBG Applications

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Oak Ridge National Laboratory

2016 U.S. DOE Vehicle Technologies Office Review

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Overview

Timeline

- Start – FY15
- End – FY17
- 58.3% complete

Budget

- Total project funding
  - DOE share – 100%
- Funding received in FY15: $250K
- Funding for FY16: $200K

Barriers

- Achieving $8/kW (peak) integrated traction motor-inverter system
- Mass production and deployment of energy efficient technologies into electric propulsion drives
- Attaining >4kW/L traction drive system power density

Addressed through achievement of higher levels of integration, and increased frequency operation

Partners

- Wolfspeed—formerly a CREE Company
- CoolCAD Electronics, LLC
- University of Tennessee, Knoxville
- ORNL team members: Chuck Britton, Laura Marlino, Shane Frank, Dianne Ezell, Leon Tolbert, Jack Wang

Project Objective and Relevance

- Overall Objective
  - Bridge a technology gap presently not addressed by industry
  - Design, develop and fabricate a reliable, highly efficient, integrated gate drive for use with Wide Bandgap (WBG) switching devices, incorporating slew rate control
  - Significantly reduce the size of existing power electronics in inverters by more completely assimilating the gate drive with the power devices
- FY16 Objective
  - Design and implement an advanced gate drive (AGD) circuit using commercial off the shelf (COTS) components
  - Validate the topology and approach by bench testing with commercial SiC switches and an inductive load
  - Prepare the advanced gate drive design for translation to an integrated circuit

Milestones

Date	Milestones and Go/No-Go Decisions	Status
April 2016	Milestone: Complete the design, simulation, and board level prototyping of the advanced gate driver using COTS components.	In Process
June 2016	Milestone: Complete bench testing the COTS advanced gate driver prototype using a SiC MOSFET device and an inductive load.	In Process
Aug 2016	Milestone: Iterate & finalize the bench prototype advanced gate driver design.	In Process
Sept 2016	Milestone: Complete IC selection process.	Begins July 2016
Aug 2016	Go/No-Go decision: If bench testing does not show the ability for closed-loop dynamic control of the gate drive waveform, the project will be re-directed or halted.	

Approach/Strategy

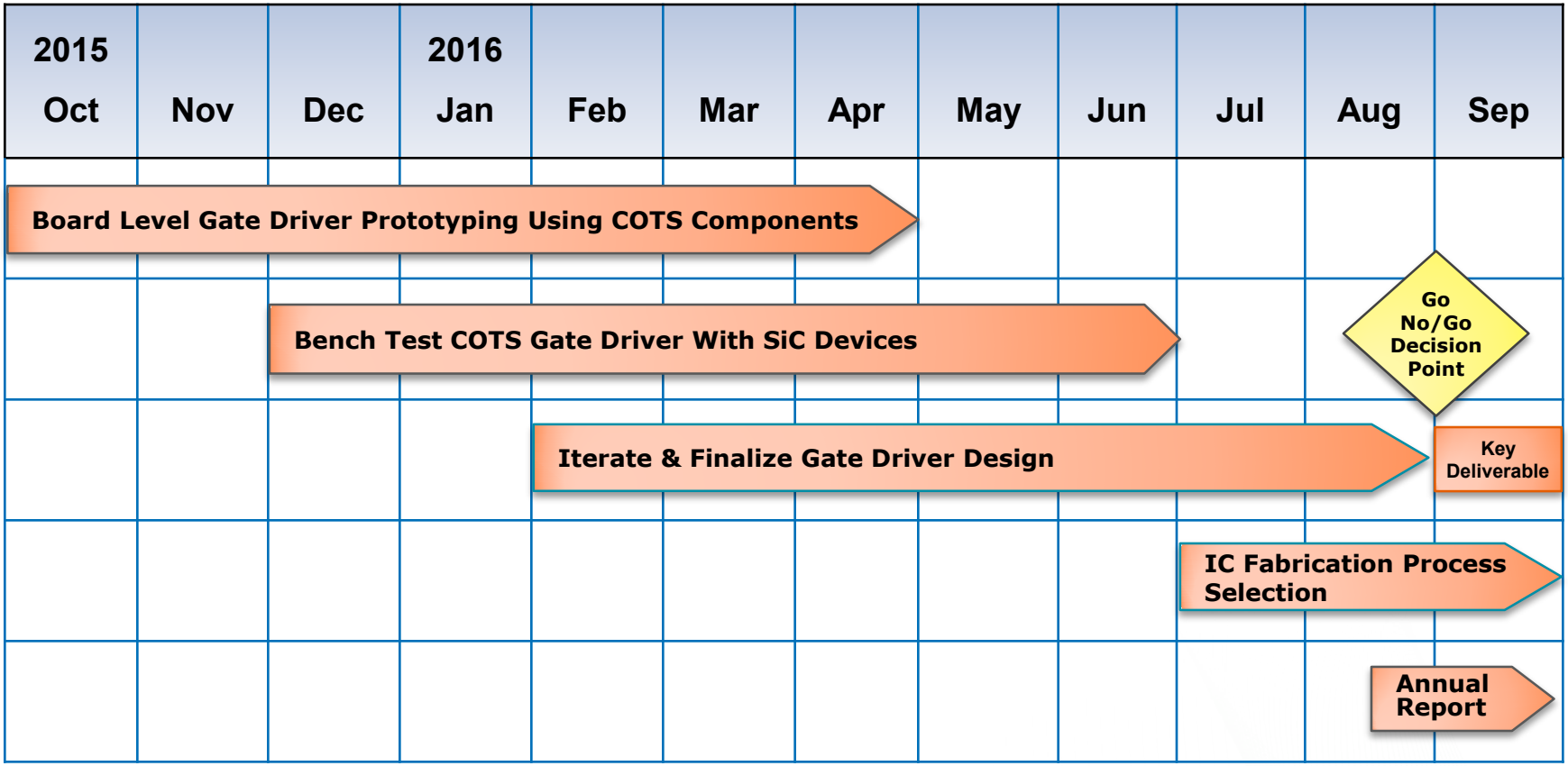
Strategy:

- Create a cost-effective, efficient gate drive topology for monitoring and performing dynamic slew control for WBG power devices
- Implement in an integrated circuit process with protection circuits

Proposed design will achieve:

- Higher inverter reliability and efficiency
- Reduction in gate drive electronics volume
- Higher motor reliability
  - Reduced insulation breakdown
  - Reduced bearing currents
- Lower drive systems costs through parts reduction
- Decreased EMI filtering

FY16 Approach



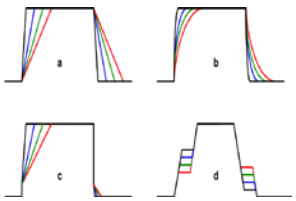
Go No/Go Decision Point: If bench testing does not show the ability for closed-loop dynamic control of the gate drive waveform, the project will be re-directed or halted.

Key Deliverable: Annual report detailing finalized gate driver design test results and results of the fabrication process selection.

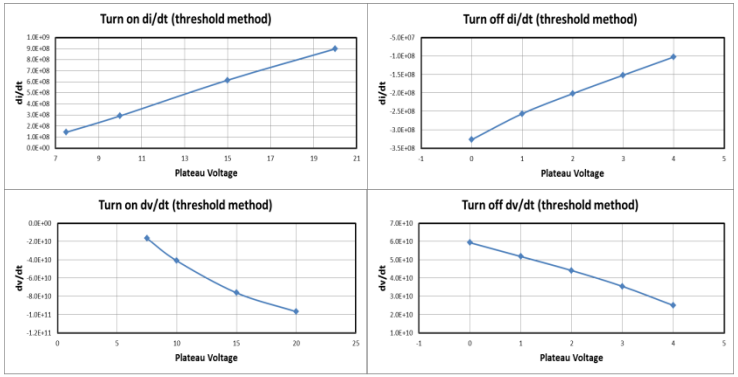
Technical Accomplishments – FY 15

- Completed literature search and selected source inductance method for measuring di/dt
- Investigated multiple gate drive waveforms for di/dt and dv/dt control efficacy
- Performed double pulse testing of representative SiC MOSFET device
- Compared CoolCAD SPICE simulation results with measured results from double pulse testing
- Designed AGD simulation-level topology for closed loop control
- Performed closed loop SPICE simulations using single slope method that indicated **proper loop stability** and **WBG device transient control**

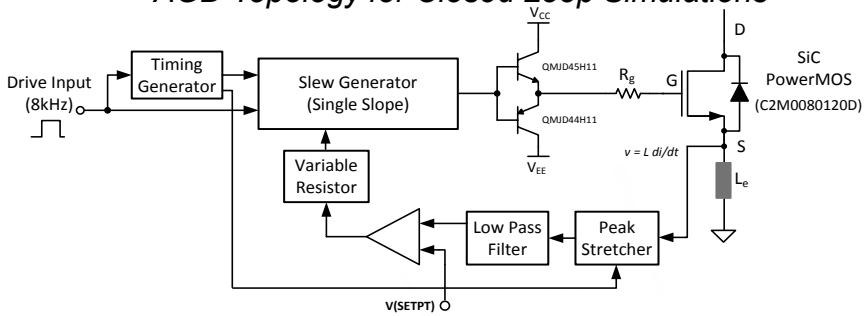
Candidate Gate Drive Waveforms



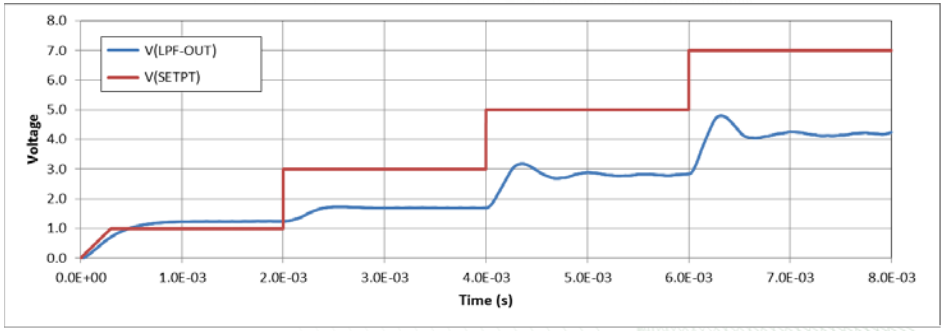
Simulations Showing di/dt and dv/dt Control Using Source Inductance Sensing



AGD Topology for Closed Loop Simulations



AGD Topology Closed Loop PSPICE Simulation Result



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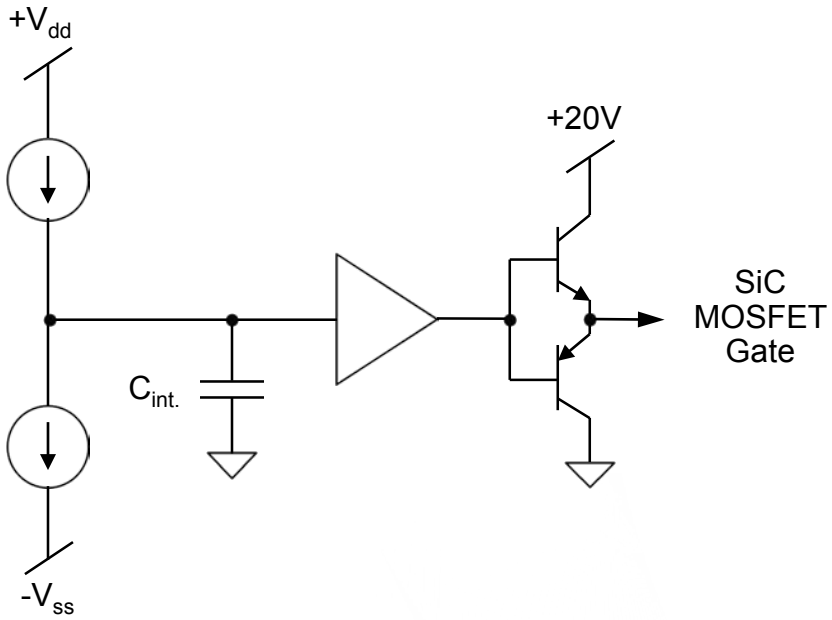
Technical Accomplishments – FY 16

Completed Design and SPICE Simulation of the AGD Gate Waveform Generator – Task 1

- Incorporates a more complex and effective gate drive waveform than other examined methods
  - Single slope
  - Dual slope
  - RC-based
- Rapidly charges the SiC switch gate to a determined level, then delays before completing the full charge
- Performed on both the rising and falling edges of the drive waveform



Simplified AGD Waveform Generator

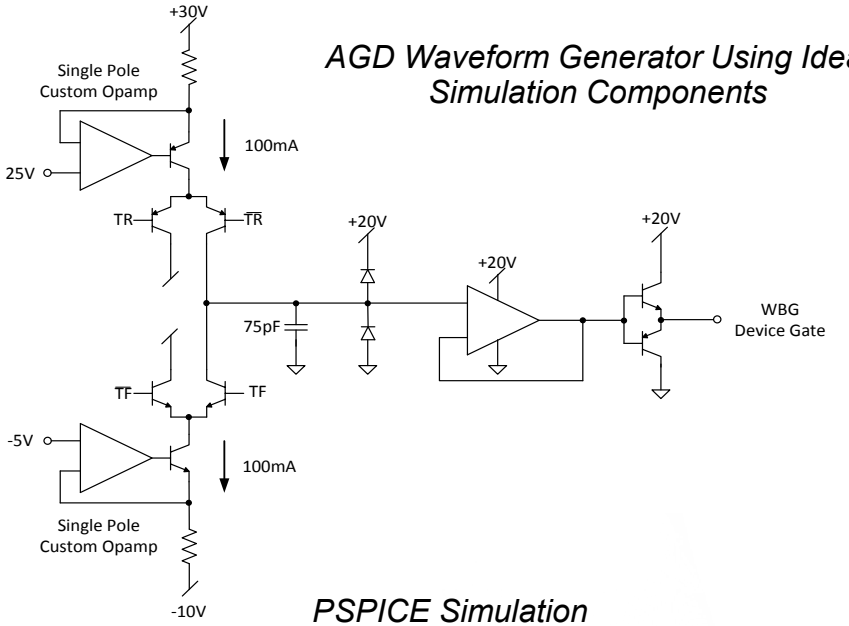
This waveform/method will produce optimum gate drive control and will compensate for temperature- and time-related WBG threshold voltage shifts.

Technical Accomplishments – FY 16

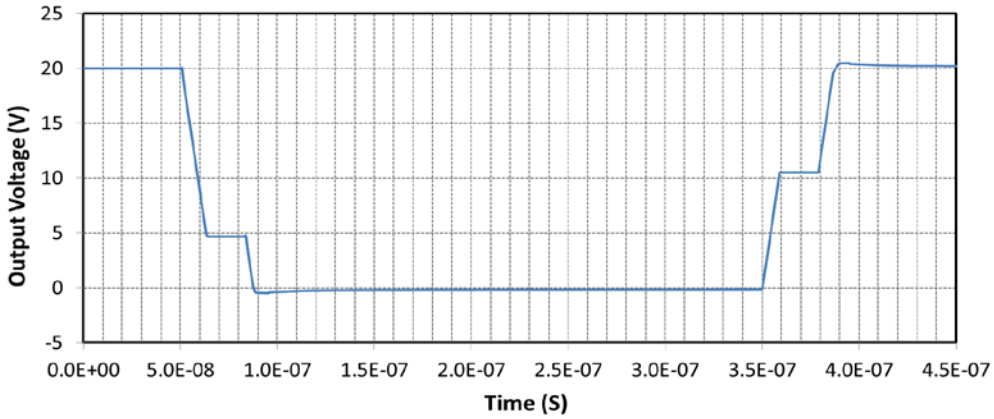
Completed Design and SPICE Simulation of the AGD Gate Waveform Generator – Task 1 (continued)

- The waveform generator block was implemented for SPICE simulation using ideal components.
- The timing functions were generated using ideal pulse signal sources in SPICE.
- Ideal simulations indicated expected output waveform.

AGD Waveform Generator Using Ideal Simulation Components



PSPICE Simulation

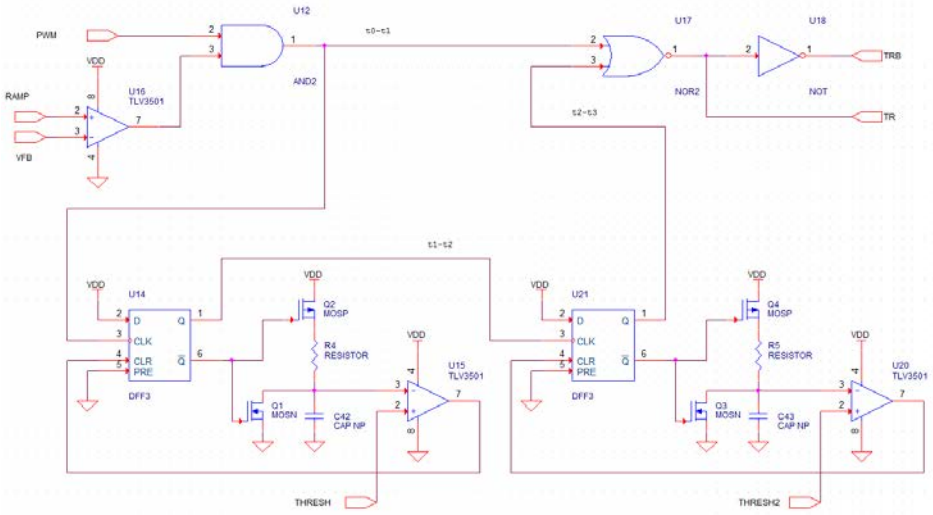


Technical Accomplishments – FY 16

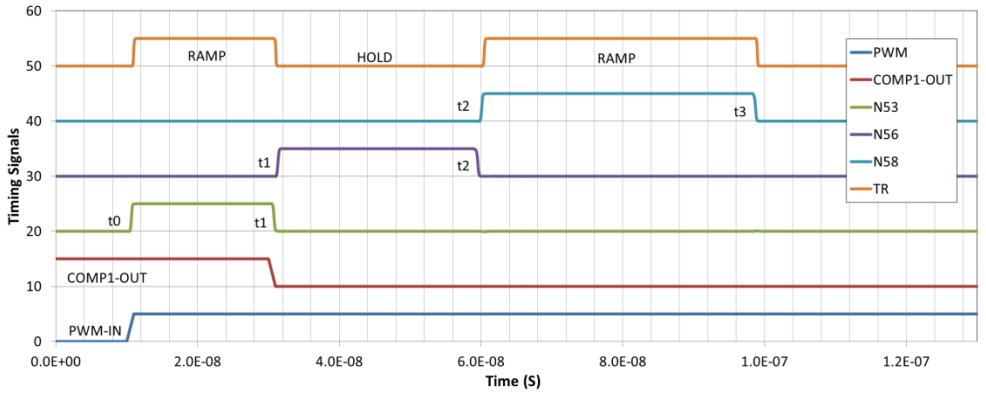
Translated Timing Circuits To COTs Design And Simulated Using Vendor Supplied SPICE Models (Task 1).

- The ideal timing circuits were translated to models based on practical components.
- SPICE simulation results indicated expected performance.
- The bench prototype circuits will use a quartz crystal timing reference and a digital programmable logic device (CPLD) for timing signal generation.

AGD Waveform Generator Timing Circuits For PSPICE Simulations



PSPICE Simulation



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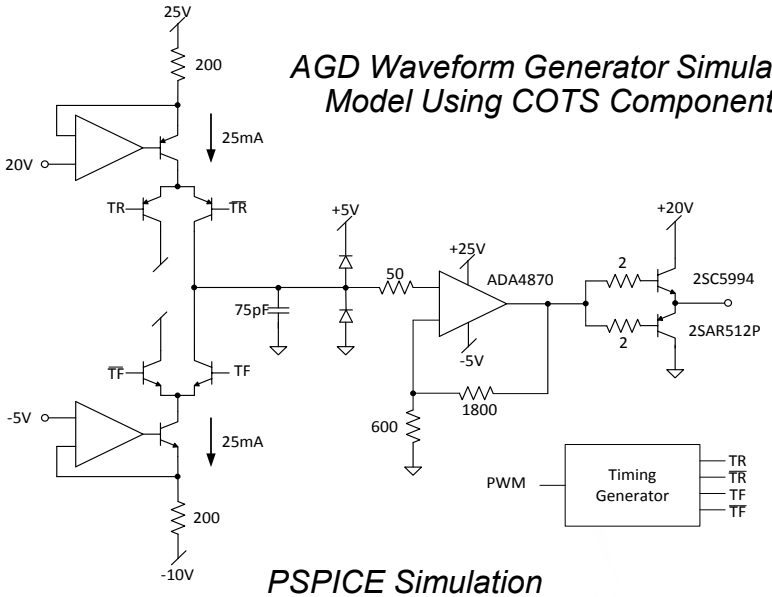
Technical Accomplishments – FY 16

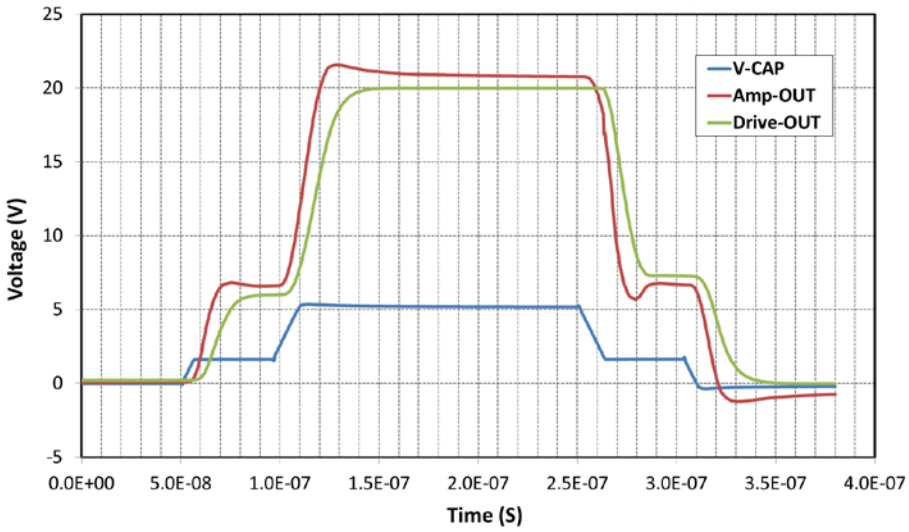
Translated The Waveform Generator Design To COTS Design And Simulated Using Vendor Supplied SPICE Models (Task 1).

- The previous ideal waveform generator design was modified for implementation using COTS components.
- A fast buffer/low gain amplifier was identified (very limited selection available).
- Simulations were performed using commercial SPICE models.
- Anticipated parasitics associated with PCB layout were incorporated.
- SPICE simulation results indicated expected performance.

AGD Waveform Generator Simulation Model Using COTS Components



PSPICE Simulation

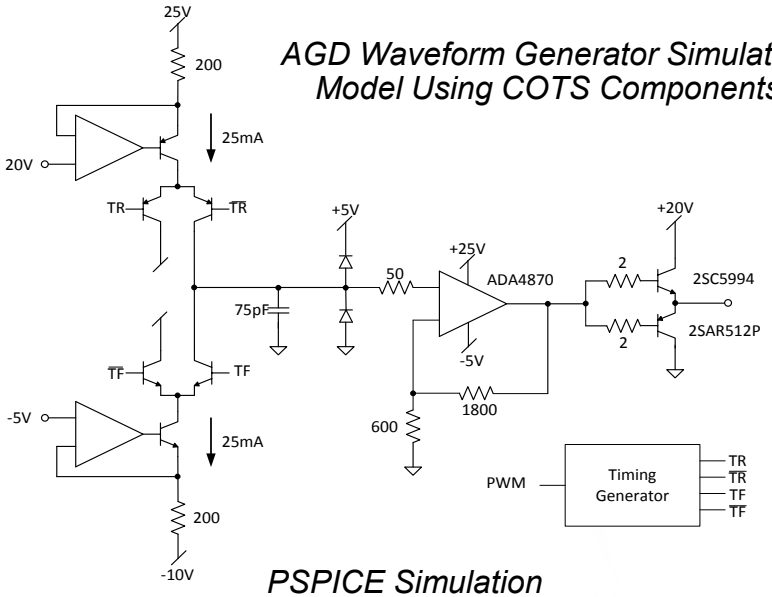


Technical Accomplishments – FY 16

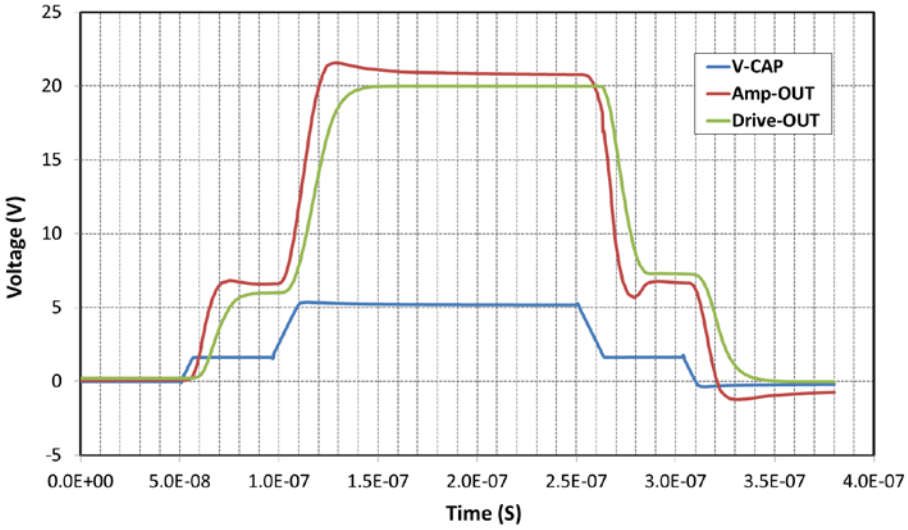
A Number Of Challenges Were Resolved During Translation Of The Waveform Generator To COTS Components (Task 1).

- Selection of the Integrator Buffer/Gain Stage Amplifier
- Amplifier Selection Involved Simultaneous Meeting Multiple Requirements:
  - Slew Rate >= 1333V/µs
  - Bandwidth >= 23.3 MHz
  - Output Current >= 1.5A
  - Useable Output Voltage Range >= 20V
- Only 2 COTS Amplifiers Found That Meet All Specifications
- Voltage Levels For Timing Generation Required Translation
- 'Good' SPICE Models For All COTS Components Is Not A Given

AGD Waveform Generator Simulation Model Using COTS Components



PSPICE Simulation

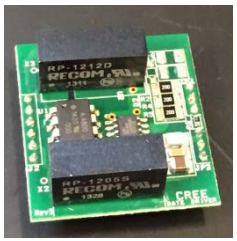


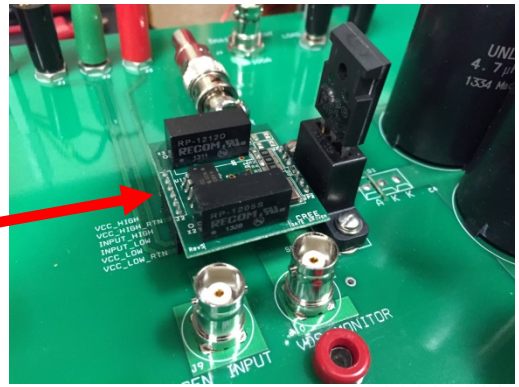
Technical Accomplishments – FY 16

The Closed Loop AGD Board Layout Is in Process (Task 1).

- Initial Overall AGD Circuit COTS Design Is Near Complete
- Configured To Be A Single Printed Circuit Board (PCB) Module
- Designed to Accommodate Rapid PCB/Design Revision And Fabrication Cycles
- This Will Be An Iterative Process

Modular AGD PCB Approach





Technical Accomplishments – FY 16

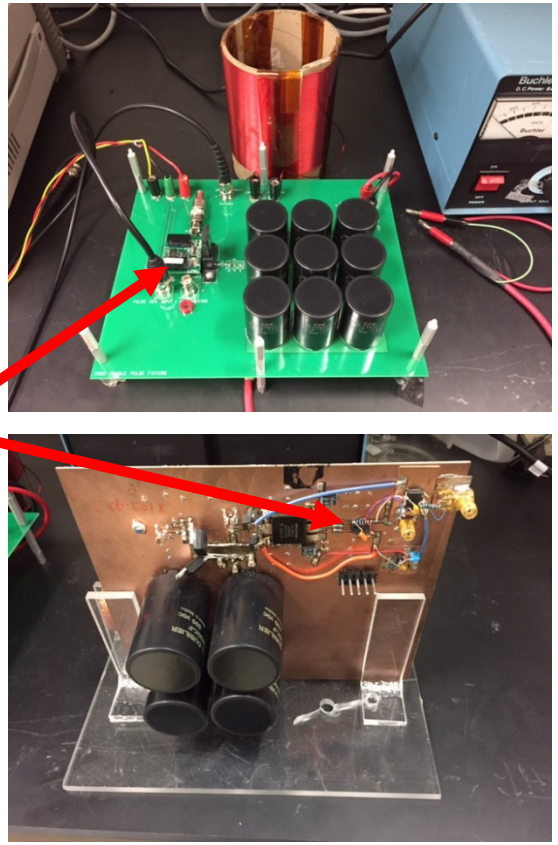
WBG-based Bench Test Design – Task 2

- Reviewed two existing WBG test platforms (Wolfspeed design and custom ORNL design)
- Design will allow both di/dt and dv/dt monitoring
- In process of making modifications for improved transient measurements

Wolfspeed Design

Gate Driver

ORNL Design



Careful design and construction of the test bench is critical for proper gate drive, and for evaluation of the WBG transient behavior.

Responses to Previous Year Reviewers' Comments

Reviewer comment 1: This reviewer would like to see a review or solicitation added where the proposed functions are presented to various inverter implementers, and comments requested with the intent of getting a broad set of requirements. Once this is done then the team can determine what makes sense to implement in a reasonably priced device. As mentioned above the requirements are a good start but fault modes need to be identified such as shoot through over current, shorts, bias supply issues, etc. The reviewer realizes that restraint needs to be applied to keep this chip from becoming the best gate drive device that nobody can afford.

Response/Action 1: We agree that the program would benefit significantly from increased industry input on the specifications and requirements. To facilitate this discussion, draft specifications for the advanced gate drive will be prepared and discussed with the EETT. Additionally, it is planned to hold a comprehensive design review with industry participants following the initial design completion in early FY17.

Reviewer comment 2: One concern this reviewer had with this project is what its aim is; for example, is it for the purpose of developing an understanding of what a systems integrator/designer needs to know or is it to get this gate driver produced. If to produce, then significant collaboration/partnerships would be needed for this to be successful.

Response/Action 2: The aim of the program is to produce an advanced gate drive technology enabling more integrated and reliable gate drivers for SiC MOSFET devices. A desired and expected outcome is an increased understanding of how to effectively use such a device. We agree that increased industry involvement would be very beneficial, if not essential, and have added a task to specifically address this need.

Collaboration and Coordination with Other Institutions

- **Wolfspeed**— SiC MOSFET Consultation
- **CoolCAD Electronics, LLC –** SiC Device Modeling & Simulation
- **The University of Tennessee –** Consultation and Chip Design Collaboration

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Remaining Challenges and Barriers

- Cost effective
  - integration of all AGD components onto a single integrated circuit including protection circuits
  - high-temperature, capable packaging for integration into a power module
- Achieving acceptable isolation and shielding for electromagnetic compatibility in the power module
- Variability of parasitics in the modules and their effect on di/dt and dv/dt controls

Proposed Future Work

- Remainder of FY16
  - Complete Task 2 – Bench Test COTS Gate Driver With WBG Devices
    - Involve CoolCAD in Obtaining Improved WBG Device Models
  - Complete Task 3 – Iterate And Finalize Gate Driver Design
  - Complete Task 4 – IC Fabrication Process Selection
- FY17
  - Task 1. Obtain Industry Partner Involvement
    - Increase Involvement And Review/Direction From Industry
  - Task 2. AGD System Architecture Design For Chip Integration
    - Design the System Architecture including the AGD, Protection (UVLO, Desaturation) and Support Circuits (Voltage Regulators, etc.)
  - Task 3. Waveform Generator Translation To Chip
    - Produce Design and associated Chip Layout for SPICE Simulation
    - Optimize Timing Control Circuits to Maximize Application Flexibility

Summary

- Relevance: Reduce size, weight, and cost of electronic drive systems while increasing system efficiency to accelerate market adoption of electric and hybrid vehicles.
- Approach: Develop highly integrated and advanced gate drive methods for WBG drives using integrated circuit technology.
- Collaborations: Wolfspeed, CoolCAD, Inc., The University of Tennessee, Knoxville.
- Technical Accomplishments:
  - Designed and simulated an architecture for closed loop control of di/dt and dv/dt through inductance-based voltage sensing
  - Implemented a threshold-based gate drive waveform generator and simulated in PSPICE
  - Initiated prototyping of the AGD for bench testing
  - Initiated design and construction of the bench test system for testing the AGD with a SiC MOSFET device and inductive load
- Future Work:
  - Complete the bench testing to validate the AGD measurement and control method
  - Further engage industry in AGD specifications, design reviews, and commercialization activities
  - Investigate and select appropriate IC fabrication process for AGD integration