Gate Driver Optimization for WBG Applications

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Project ID: EDT068

ORNL is managed by UT-Battelle
for the US Department of Energy

OAK RIDGE
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Overview

Timeline

- Start – FY15
- End – FY17
- 17% complete

Budget

- Total project funding
  - DOE share – 100%
- Funding received in FY14: $0K
- Funding for FY15: $250K

Barriers

- Achieving $8/kW (peak) integrated traction motor-inverter system
- Mass production and deployment of energy efficient technologies into electric propulsion drives
- Attaining >4kW/L traction drive system power density

Addressed through achievement of higher levels of integration, and increased frequency operation

Partners

- Cree Inc., University of Tennessee-Knoxville
- ORNL team members: Chuck Britton, Laura Marlino, Shane Frank, Dianne Ezell, Leon Tolbert, Jack Wang

Project Objective and Relevance

- Overall Objective
  - Bridge a technology gap presently not addressed by industry.
  - Design, develop, and fabricate a reliable, elevated temperature capable, highly integrated gate drive for use with Wide Bandgap (WBG) devices incorporating slew rate control as an enabler for incorporation of the inverter with the traction motor.

- FY15 Objective
  - Investigate prior and present art in advanced gate drive, slew control and sensing methods.
  - Select/develop an improved topology and associated sensing methods and verify using circuit simulation.

Milestones

Date	Milestones and Go/No-Go Decisions	Status
Dec 2014	Milestone: Complete research of existing methods for slew rate limiting/control for feasibility and monolithic compatibility.	**Complete**
June 2015	Milestone: Complete initial gate driver architecture design including circuit topology and measurement methods.	**In Process**
Aug 2015	Milestone: Complete the advanced gate driver circuit design and simulation using a WBG load.	**In Process**
Aug 2015	Go/No-Go decision: If simulations do not show the ability to dynamically control the gate drive slew rate, the project will be halted or redirected.	

Problem to be Addressed

- **Present gate drives are not optimized for use with WBG devices**
  - Faster di/dt and dv/dt of WBG devices impose unique system limitations.
  - Fast switching reduces the motor insulation reliability; imposes additional costs in motor, cabling, and EMI filtering.
- **Present methods for slew control are lacking:**
  - Limited commercial solutions exist – none are dynamic.
  - No methods have been vetted specifically for WBG applications.
  - No methods have been demonstrated for integrated circuit realization or high temperature operation.
- **Commercial gate drives are optimized for Si switching speeds– not for the high frequency of WBG devices**

Improved Gate Drive Methods Are Needed for Full Realization of Reliable WBG-Based Systems

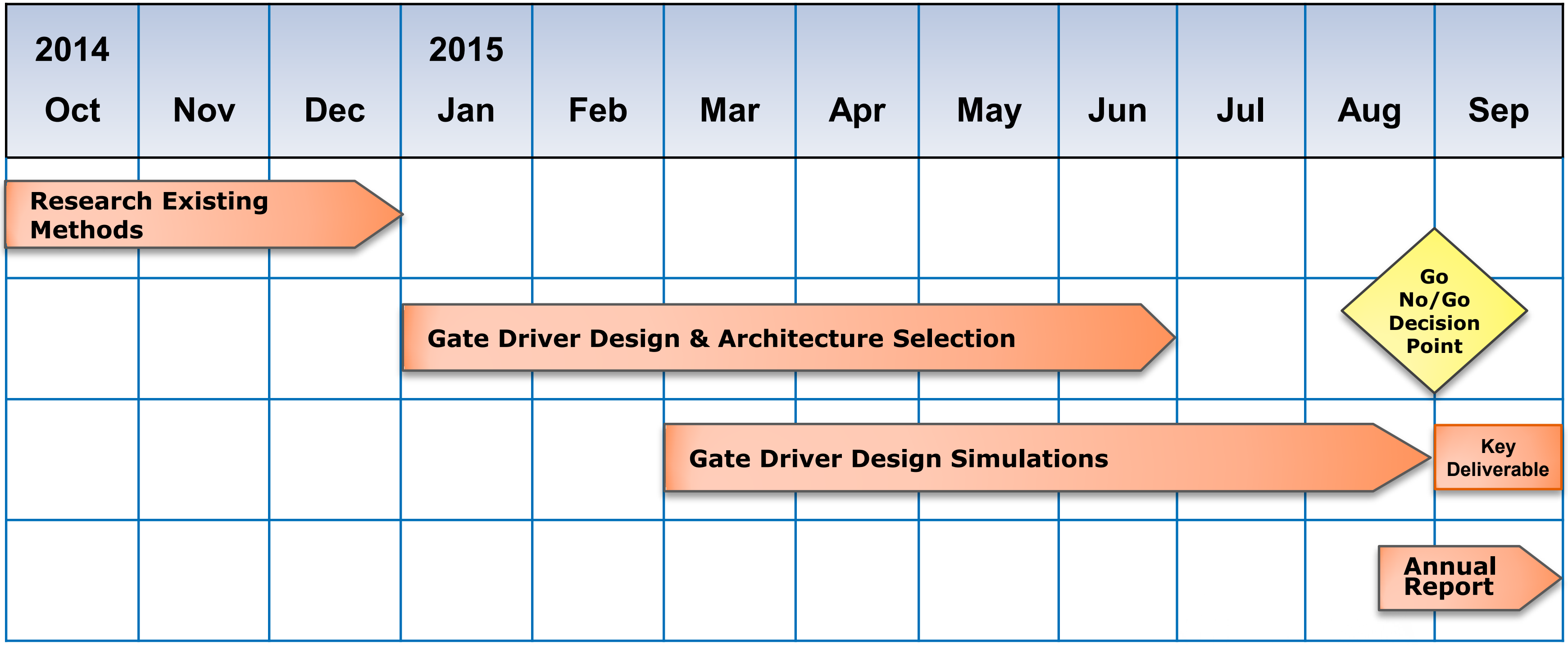
Approach
Strategy to Address Limitations of SOA

Strategy: Create a cost-effective, efficient topology for monitoring and performing dynamic slew control of WBG device gate drive.

Proposed design will achieve:

- Higher inverter reliability and efficiency
- Reduction in gate drive electronics volume
- Ultimately, higher temperature capability (>200°C)
- Higher motor reliability
  - Reduced insulation breakdown.
  - Reduced bearing currents.
- Lower cost gate drive systems through parts reduction
  - Gate driver integration.
  - Decreased EMI filtering.

Approach FY15 Timeline



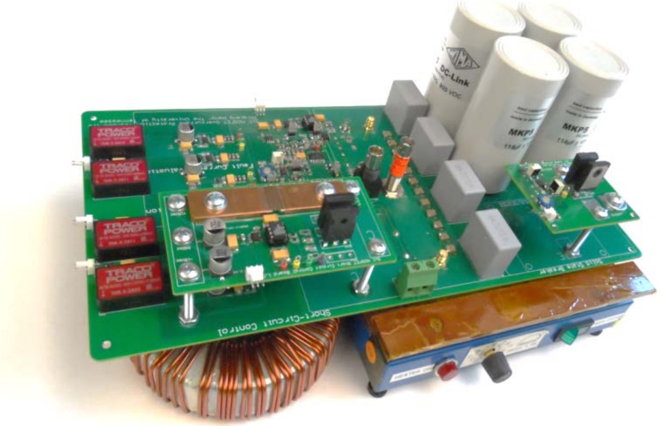
Go No/Go Decision Point: If simulations utilizing the improved gate driver with WBG switches do not show the ability to dynamically control the gate drive slew rate (dynamic range of ≥ 4X), the project will be halted or redirected.

Key Deliverable: Annual report including design and simulation results of the selected gate driver architecture demonstrating dynamic slew control for dv/dt limiting.

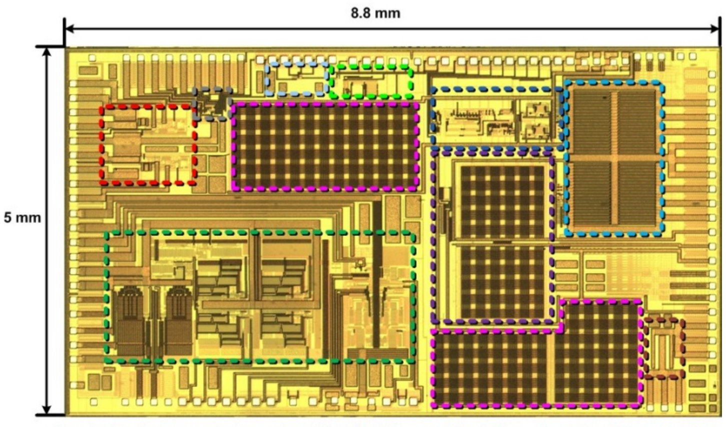
Technical Accomplishments - Previous

Significant Prior Gate Driver R&D Has Been Performed at ORNL/UT

- ***Overcurrent Protection Methods***
  - Solid State Circuit Breaker
  - Fault Current Evaluation
  - Desaturation Detection
- ***SOI Gate Driver Chip***
  - Temperature Sensor
  - Under Voltage Lockout (UVLO)
  - Desaturation Detection
  - Integrated Charge Pump and Volt. Reg.
  - -55C to 200C Operating Range
  - 10V-30V Operation



Overcurrent Protection Method Test System



Silicon-on-Insulator Gate Driver Chip

Technical Accomplishments – FY15

Comparison of Conventional Current Measurement Methods

Sensor Type	Insertion Loss	External Power	Circuit Isolation	Bandwidth	Size	Accuracy	Relative Cost
Sense Resistor	High	Low	Low	DC to 50MHz	Medium	Medium	Low
Sense Inductor	Low	Low	Low	DC to 50MHz	Small	Low	Low
Open-Loop Hall Effect	Low	Low	High	DC to >100 kHz	Small	Medium	Medium
Closed-Loop Hall Effect	Low	Medium	High	DC t0 1MHz	Medium/Large	Medium	Medium
Current Transformers	Medium	None	High	30Hz to 70MHz	Medium/Large	Low-High	High

Sources: Allegro STP98-1-AN, Rev.2, Pearson 2878 Data Sheet

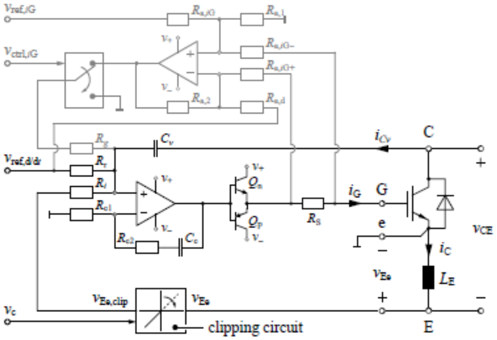
The Use of Source-Inserted Passive Devices For Current Measurement Provides the Lowest Cost Solution But Requires Additional Circuitry

Technical Accomplishments – FY15

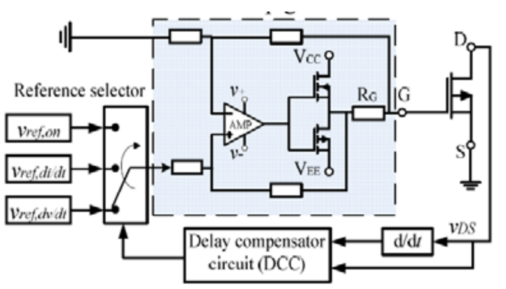
Published Active Gate Drive (AGD) Methods Address Si-based Power Switch Technologies

Reference	di/dt	dv/dt	Complexity	i Meas. Method	Chip Compatible	Notes
Lobsinger 2012	Y	Y	Moderate	L_e	Y	IGBT
Lobsinger 2015	Y	Y	Moderate	L_e	Y	IGBT
Wang 2013	Y	N	Low	L_e	Y	IGBT
Park 2003	Y	Y	Low	L_e	Y	IGBT / MOSFET
Gerster 1996	Y	Y	Low	L_e	Y	IGBT
Riazmontazer 2015	N	Y	Moderate	---	Y	IGBT / MOSFET
Chen 2009	Y	Y	Low	L_e	Y	IGBT

L_e = emitter or source inductance measurement



Lobsinger 2012, 2015



Riazmontazer 2015

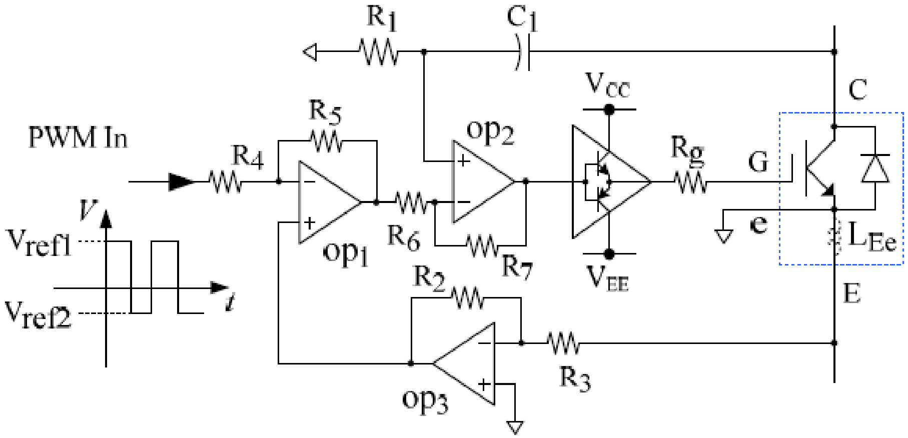
Riazmontazer 2015

These AGD Methods Are Monolithically Compatible, But Have Yet to Address the Specific Drive Needs of SiC Power Devices

Technical Accomplishments – FY15

Active Gate Drives Can Be Divided Into Two Broad Categories

- Gate "Voltage" Control
  - Gate voltage is fed through a resistor from an amplifier or buffer
  - Implementation Advantages
    - Simple
    - Voltage amplifier can be used.
    - Can be used to control both di/dt and dv/dt loops
  - Implementation Disadvantages
    - Amplifier/resistor combination needs to be able to handle both turn-on and turn-off switching
    - Gate voltage is dropped across a resistor

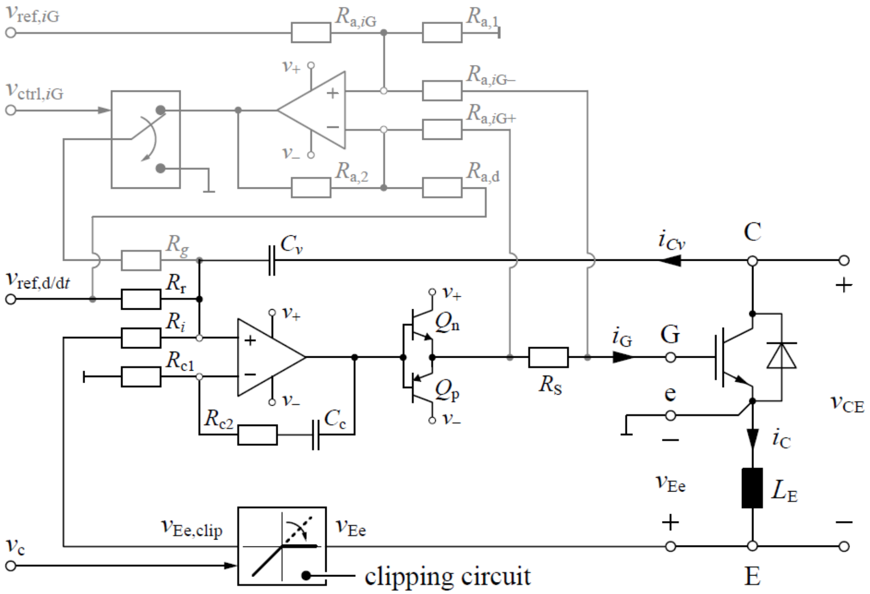


Lihua Chen; Peng, F.Z., "Closed-Loop Gate Drive for High Power IGBTs," Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, (APEC 2009), pp.1331-1337, Feb. 15-19, 2009.

Technical Accomplishments – FY15

Active Gate Drive Can Be Divided Into Two Broad Categories (cont.)

- Gate "Current" Control
  - Current through a resistor is monitored
  - Implementation Advantages
    - Actual gate voltage is sensed
    - More opportunity for control with greater complexity
    - Can be used to control both di/dt and dv/dt loops
  - Implementation Disadvantages
    - More complex
    - Potentially harder to compensate

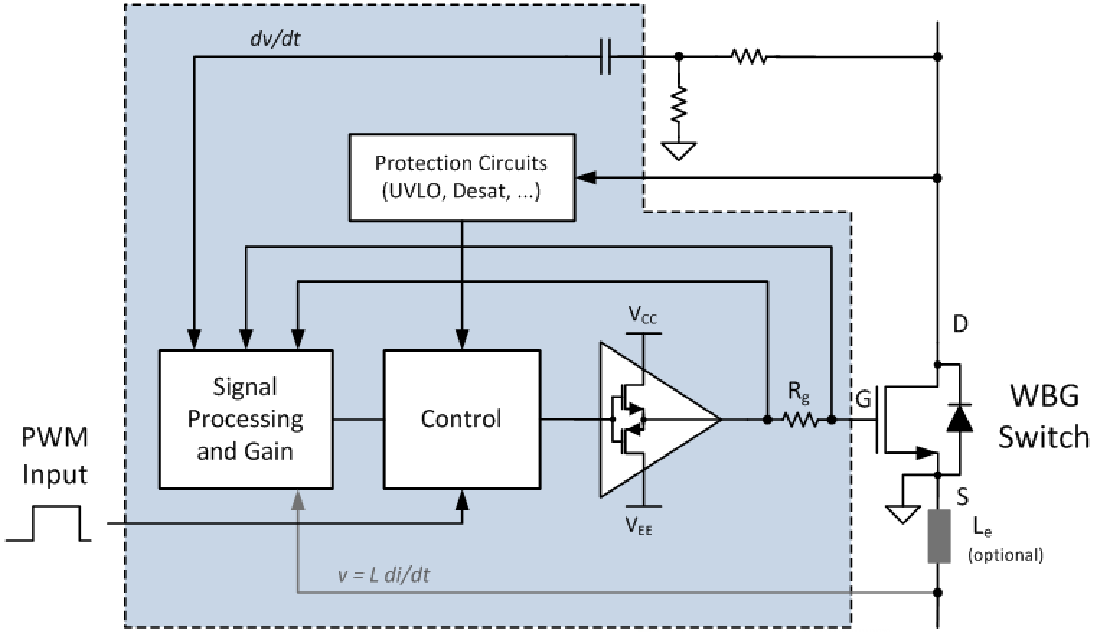


Y. Lobsiger, J.W. Kolar, "Closed-loop IGBT gate drive featuring highly dynamic di/dt and dv/dt control," *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE* , pp.4754,4761, Sept. 15-20, 2012.

Technical Accomplishments – FY15

Active Gate Drive Topology – Initial Design

- Monitor only dv/dt initially.
- Add di/dt capability if simulations indicate a need.
- Incorporate protection circuits including UVLO, desaturation detection, shoot-through protection and short-circuit protection.
- High loop bandwidth ~ 50MHz.
- Provide programming flexibility allowing applicability to varying WBG gate drive needs.
- Maximize compatibility with integrated circuit fabrication for future cost and size reduction.

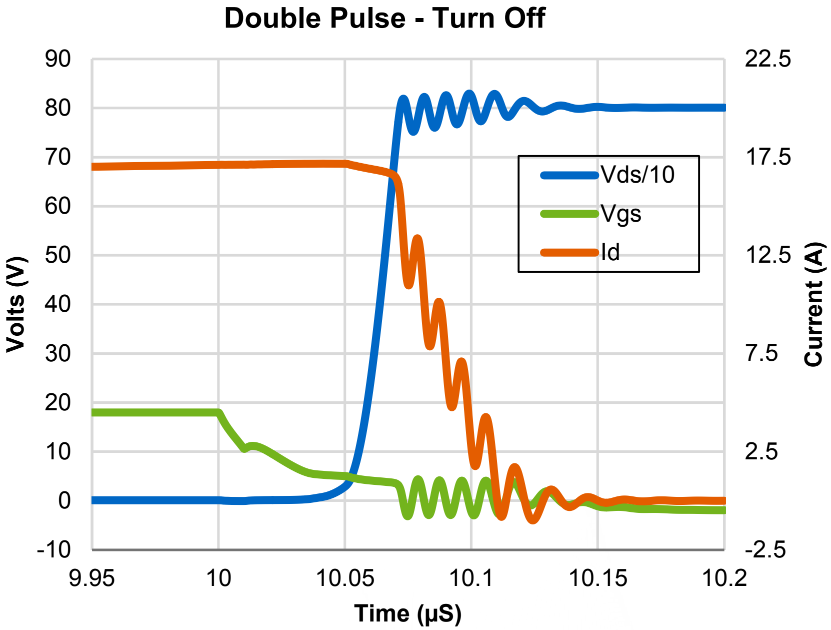


ORNL Active Gate Drive Integrated Circuit Topology

Technical Accomplishments – FY15

SiC MOSFET – Modeling and Simulation

- Perform a comparison of the vendor-supplied model to measured devices.
- Utilize ORNL WBG power device test and characterization system.
- Perform double pulse testing for observing both turn-on and turn-off characteristics.
- Compare results with vendor provided SPICE simulation models.
- Iteratively modify SPICE models to improve simulation agreement with actual measurements.
- The SiC device ac and dc SPICE model accuracy is key for active gate driver topology optimization.



Turn-off simulation result, using vendor supplied SPICE model (C2M0080120D, 1200V, 20A, R_{ds}=80mΩ, Cree Inc.)

Accurate Simulation Models Are Essential For AGD Topology Design

Technical Accomplishments – FY15

Summary

- Completed review of closed-loop gate drive techniques.
- Completed review of current and voltage measurement methods.
- Sensing method selected – dv/dt measured from WBG device drain (low cost, miniature, reliable).
- Will investigate performance implications of not monitoring di/dt and will add the L_e-based di/dt measurement if determined necessary.
- Initiated Active Gate Driver (AGD) feedback and control topology design.
- Performing testing of SiC MOSFETs to improve SPICE simulation models.
- Initiated AGD circuit simulation using a commercial/custom WBG device model.

Responses to Previous Year Reviewers' Comments

- This Project is a New Start.

Partners/Collaborators

- **Cree, Inc.**
  - Consultation regarding commercial WBG device characteristics, modeling and application.
- **University of Tennessee, Knoxville**
  - Collaboration on integrated circuit design, simulation, layout, and testing.

Remaining Challenges and Barriers

- Refining the AGD architecture and sensing methods for performance and cost-effective implementation.
- Translation of prior circuit designs to SOI.
- Integration of all AGD components onto a single integrated circuit.
- Cost-effective high-temperature packaging for integration into a power module.
- Isolation and shielding packaging requirements in the module for electromagnetic compatibility.
- Variability of parasitics in modules and effect on di/dt and dv/dt controls.
- Availability of high temperature integrated circuit process for highly integrated module.

Proposed Future Work

- **Remainder of FY15**
  - Gate Driver Design & Architecture Selection
  - Gate Driver Design Simulations
  - Annual Report
- **FY16**
  - Board Level Gate Driver Prototyping Using COTS Components
  - Bench Test COTS Gate Driver With WBG Devices
  - Iterate & Finalize Gate Driver Design
  - IC Fabrication Process Evaluation/Selection
  - Annual Report
- **FY17**
  - Gate Driver Integrated Circuit Design and Fabrication
  - Gate Driver Packaging
  - System Test Using the Advanced Gate Driver IC
  - Annual report

Summary

- Relevance: Enable size, weight, and cost reduction of electronic drive systems to enable more rapid and reliable deployment of WBG in electric drive systems.
- Approach: Develop highly integrated and advanced gate drive methods for WBG drive using integrated circuit technology.
- Collaborations: Cree, Inc., The University of Tennessee, Knoxville.
- Technical Accomplishments:
  - Completed review of closed-loop gate drive techniques.
  - Completed review of related current and voltage measurement methods.
  - Selected dv/dt as primary sensing method.
  - Initiated AGD feedback and control topology design.
  - Initiated AGD circuit design and simulation activities.
  - Performing WBG power device testing and SPICE modeling.
- Future Work:
  - Complete AGD simulation level design.
  - Translate AGD to COTS equivalent and characterize performance with WBG load.
  - Design, layout, simulate, fabricate AGD design in high temperature SOI process (200C).
  - Package for high temperature and characterize AGD integrated circuits with WBG load.
  - Publish research results.
  - Engage OEMs on potential applications for various traction drive platforms.