

# **DOE AMR Review**

#### Cree, Inc., EE0006920 "88 Kilowatt Automotive Inverter with New 900 Volt Silicon Carbide MOSFET Technology"

#### June 9, 2015

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Project ID # EDT073

## **Project Overview**

#### Timeline

<ul> <li>Project Start – Dec. 11, 2014</li> <li>Project Complete – Dec. 10, 2016</li> <li>5% Complete</li> </ul>	<ul> <li>Cost (A) – Target &lt; \$8/kW by 2020</li> <li>Weight (C) – SiC expected to improve power density (&gt;1.4kW/kg by 2020)</li> <li>Reliability &amp; Lifetime (D) – SiC ↓ FIT 10x</li> <li>Efficiency (E) – SiC expected to improve light-load efficiency and vehicle range</li> </ul>			
Budget	Partners and Subcontractors			
<ul> <li>Govt. Share: \$1,937,752.00</li> <li>Cost Share : \$2,107,744.00</li> <li>Total : \$4,045,496.00</li> </ul>	<ul> <li>Cree, Inc. lead; 900V SiC power MOSFET</li> <li>APEI – sub; SiC power modules &amp; inverter</li> </ul>			

**Barriers** 

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### **Relevance of program targets at macro level**

- Depending on topology, x-EV drive system, and motor, the primary target is to make x-EV more affordable through better fuel efficiency, lower system cost, and lower weight
  - 900V, 10mΩ SiC MOSFET developed, sampled and AEC-Q101 qualified at chip level
  - At low-frequency, the SiC MOSFET has better light-load efficiency than Si IGBT
  - Better efficiency leads to reduced cooling costs
  - Record low switching losses expected for 900V semiconductor switch
  - Avalanche energy expected to be 10X that of Si components for better reliability

Metrics	DOE	FUPET (Japan	Delphi	Cree/APEI/FORD targets
	Specified	consortium w Nissan)		
Semiconductor	Si or WBG	1200 V SiC FET @ 3.1 mΩ·cm <sup>2</sup>	Si IGBT	900 V SiC FET @ 2.2 mΩ·cm <sup>2</sup>
Year	2010	2011	2013	2016
Cost (100k units)	\$5/kW	-	\$5/kW	< \$5/kW
Specific Power	12 kW/kg	-	17 kW/kg	> 22.5 kW/kg
Power Density	12 kW/L	30 kW/L*	15 kW/L	>21.5 kW/L

\*- doesn't include controllers, sensors, or gate drivers & power supplies. Ref Materials Science Forum Vols. 740-742, pp 1081-1084, (2013) Trans Tech Publications, Switzerland



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#### **Relevance to Commercialization**



Budget Period	Start/End Date	Milestone	Type Description		Status
1	12/15/2014 – 12/14/2015	Characterization of third optimization of wafer lot of 900 V SiC MOSFET.	Go/No-Go Go/No-Go Test the third power MOSFET lot and measure performance against the target specifications.		On-track. First 900V, 10mΩ SiC MOSFET lot in fab with ECD of
2	12/15/2015 – 12/14/2016	Single-phase traction drive demonstration.	Technical	Perform single-phase traction drive demo using 900V, 200A, ½ bridge power modules and evaluate impact of SiC performance on automotive traction drive system.	Not started. This is for FY16.

Interim Milestones are defined in the SOPO and PMP









### Approach

Task #	900V, 10m $\Omega$ SiC MOSFET development & qual	Wafers	Start	ECD
1.1	Die centering – lot #1	9	Feb 2015	June 2015
1.1	R <sub>DSON</sub> vs t <sub>SC</sub> - lot #2	6		Sept 2015
1.1	Re-center lot based on feedback (Go / No-go milestone) – lot #3	6		Nov 2015
1.2	Pre-qual lot – lot #4	6		Jan 2016
1.2	Qualification Lot #1 – lot #5	12		Mar 2016
2.1	Qualification Lot #2 – lot #6	12		Apr 2016
2.1	Qualification Lot #3 – lot #7	12		May 2016
2.1	Qualify 900V, 10m $\Omega$ SiC MOSFET chip by AEC-Q101 standards			Nov 2016

Task #	900V ½ bridge power module develop & qual	Modules	Start	ECD
1.3	Assemble, characterize and benchmark power modules (900V, >200A, ½ bridge)	6	June 2015	Sept 2015
2.2	Assemble, characterize and benchmark power modules (900V, >200A, $\frac{1}{2}$ bridge)	70	May 2016	Aug 2016
2.2	Qualification of module using a mix of JEDEC and AEC-Q101 standards		Aug 2016	Dec 2016

Task #	88kW peak traction drive demo	Modules	Start	ECD
2.3	Single phase traction drive demo	5	June 2015	Sept 2015
2.3	Three phase traction drive demo	25	May 2016	Aug 2016
2.3	Benchmark 900V SiC based technology with competing technologies		Aug 2016	Dec 2016





# Approach - 900V, 10 m $\Omega$ SiC MOSFET Estimated $R_{\text{DSON}}$ vs T



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## Approach – MOSFET Qualification Plan at 175 $^{\circ}\text{C}$

- Die to be qualified at a  $T_{J,Max}$  of 175  $^{\circ}C$  under this program
- Reliability at 200 °C will be investigated; qualifying at 200 °C will be a stretch goal
- AECQ101 die level qualification tests in TO-247

Test	Stress Conditions	Duration	Wafer lots sampled	Total devices sampled
HTGB	VGS = 18 V, VDS = 0, Ta=175 °C	1000 hrs	3	231
H3TRB	85 °C, 85% RH, VDS = 100 V, VGS=0	1000 hrs	3	231
HTRB	VDS = 720 V, VGS = 0, Ta = 175 °C	1000 hrs	3	231
тс	-55 °C / +175 °C, JESD22-A104 condition H, soak mode 1	1000 cycles	3	231
IOL	5 min on / 5 mins off, $\Delta Tj \ge 100 \text{ °C}$ , Tmax $\ge 175 \text{ °C}$	6000 cycles	3	231
ESD-HBM	Classification at 25 °C	n/a	1	5
ESD-MM	Classification at 25 °C	n/a	1	5
ESD-CDM	Classification at 25 °C	n/a	1	5







## **Approach - 900V SiC MOSFETs : Avalanche Ruggedness**

- Low defect density material and processing allows SiC MOSFETs to withstand avalanche energy
- Stretch goal will be to avalanche rate 900 V SiC MOSFETs



#### **Preliminary Characterization**

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#### Technical Accomplishment - 900V, 65m $\Omega$ SiC MOSFET

- Target applications
  - ON-board EV chargers
  - Switch mode power supplies
  - Solar inverters
  - High power DC/DC converters
- AECQ101 qualification effort in progress
  - Expected to be completed in Q2 2015
- Commercial release planned in 2015

#### 100mm 900V, 65 m $\Omega$ SiC MOSFET wafer







#### **Technical Accomplishment – 150°C JEDEC qualification**

- 900V, 65 m $\Omega$  JEDEC Qualification Status (TO-247 Package)
- Qualification complete

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Test	Stress Conditions	Duration	Wafer lots sampled	Total devices sampled	Status
HTGB	VGS = +15 V, VDS = 0, Ta=150 °C	1000 hrs	3	75	Complete
HTGB	VGS = -5 V, VDS = 0, Ta=150 °C	1000 hrs	3	75	Complete
H3TRB	85 °C, 85% RH, VDS = 100 V, VGS=0	1000 hrs	3	75	Complete
HTRB	VDS = 720 V, VGS = 0, Ta = 150 °C	1000 hrs	3	75	Complete
тс	-55 °C / +150 °C, JESD22-A104 condition H, soak mode 1	1000 cycles	3	75	Complete
IOL	5 min on / 5 mins off, ∆Tj ≥ 100 °C, Tmax ≥ 150 °C	6000 cycles	3	75	Complete
ESD-HBM	Classification at 25 °C	n/a	1	5	Complete
ESD-MM	Classification at 25 °C	n/a	1	5	Complete
ESD-CDM	Classification at 25 °C	n/a	1	5	Complete





#### **Technical Accomplishment – smaller chip demonstrated**

- Full turn-ON achieved at +15 V Gate Bias
  - Convenient gate drive using commercial IGBT and MOSFET drivers. —





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### Technical Accomplishment – lower R<sub>DSON</sub> vs T demo

- 900V SiC MOSFET has a low temperature coefficient of resistance compared to Silicon and GaN
- Enables higher power ratings





# Technical Accomplishment – 6X lower R<sub>DSON</sub> · E<sub>OSS</sub>



SiC is <u>4x Better at 25 °C</u> and <u>6x Better at 150 °C</u> due to lower R<sub>DS,ON</sub> temperature coefficient

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#### **Technical Accomplishment – ultra low measured E**<sub>sw</sub>

**Measured Switching Energy compared to Current** 









- New project
- No reviewer comments from last year





• None for public disclosure





- AEC-Q101 qualification of lowest  $R_{DSON}$  SiC power transistor (10m $\Omega$ ) of any voltage range to date
- Inverter demo single phase and three phase
- Verifying expected light load efficiency improvement from SiC in drive train
   Inverter Loss Estimation Tool



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WBG drive reduces inverter losses, especially at light load





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- In 2015:
  - Finish three lots of 900V,  $10m\Omega$  SiC MOSFETs and sample to automotive OEM and Tier One suppliers
  - Build 900V, 200A, ½ bridge power module using new SiC MOSFET chips
  - Simulate the light load efficiency in the drive cycle using the new 900V
     SiC MOSFET
- In 2016:

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- AEC-Q101 qualification of 900V, 10mΩ SiC MOSFETs at chip level
- Build 70 ½ bridge power modules using new 900V SiC MOSFETs
- Test MTTF and IOL of SiC MOSFET based power modules
- Perform single phase and three phase inverter demo's using new 900V
   SiC MOSFET power modules

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- Cree will develop and optimize a 900V, 10 m-Ohm SiC MOSFET aimed at x-EV applications, based on specifications provided by Ford and other automotive Tier One suppliers.
  - 200-600 MOSFETs for external sampling from optimization lots.
  - 1,100 MOSFETs to APEI for module assembly from qual lots.
  - Cree will qualify the optimized SiC MOSFET <u>chip</u> according to AEC-Q101 (~1,500 MOSFETs)
- APEI will construct 900V, 200A, ½ bridge power modules using the 900V SiC MOSFET and benchmark against other technologies. Benchmark includes performance & reliability.
  - APEI will valuate the ½ bridge power module in an 88 kW peak power traction drive inverter for x-EV.

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• Ford will provide technical input on system specifications, and evaluation of new 900V SiC products developed.

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70 modules

~3k MOSFETs