U.S. DEPARTMENT OF ENERGY

OAK RIDGE NATIONAL LABORATORY
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Smart Integrated Power Module

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Project ID: APE046

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Overview

Timeline

- Start – FY12
- Finish – FY14
- 15% complete

Budget

- Total project funding
  - DOE share – 100%
- Funding received for FY12
  - $475K
- Funding request for FY13
  - $800K

Barriers

- Converter volume, weight, cost
- Converter high temperature capabilities

Inverter targets

- Power density: 14 kW/l (2020 target)
- Specific power: 14 kW/kg (2020 target)
- Cost: $5/kW (2015 target)

Partners

- **ORNL team members:** Laura Marlino, Zhenxian Liang, Chuck Britton, Nance Ericson
- **The University of Tennessee**

Project Objectives

- Develop a highly integrated, high temperature power module that also contains gate drive functions and current and temperature measurement as well.
- Package current and temperature sensors that can be integrated into the power module. IC would cost less than $1 each in mass production. Examine orientation and shielding issues to eliminate unwanted noise in measurements.
- Smart gate drive that has protection features, high current capability, and active gate control to minimize switching loss and chance of noise-induced gate turn-on that can lead to shoot-through.
- Final goal is to produce 55 kW inverter phase leg modules that can work at high temperatures and meet 2020 Targets of 14 kW/l, 14 kW/kg, and 2015 Targets of 5 $/kW, and 98 % efficiency.

- **FY12 Objective:** Develop gate drive buffer, isolation, and current measurement circuits that can be integrated into module.

Milestones

Month/Year	Milestone or Go/No-Go Decision
Sept-2012	Milestone: Development of a current measurement ASIC that can make high fidelity measurements of currents in PCB trace.
May-2012	Go/No-Go decision: Buffer and isolation designs that have prospects for working at elevated temperatures.

Problems Addressed by this Research

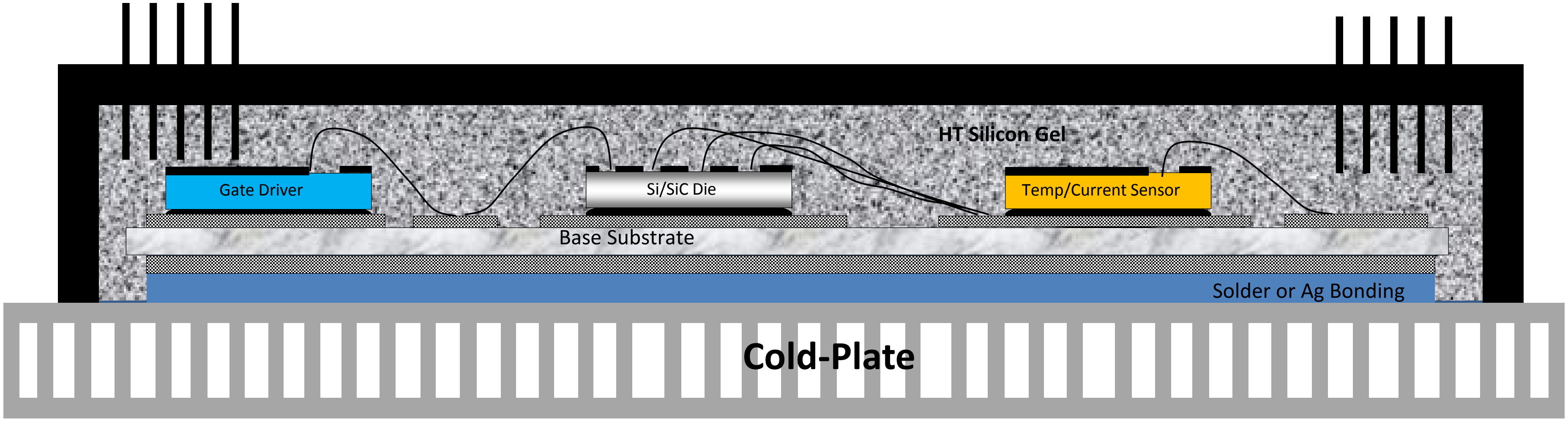
Problem #1: Cooling systems in HEVs / PHEVs are too bulky because they require a second 65°C coolant loop (in addition to the 105C engine coolant loop).
Approach: Develop high temperature packaging techniques.

Problem #2: Hall effect window type current transducers (LEM) cost $10 to $20 each, with traction drives using anywhere from two to six of these.
Approach: Use low cost (<$1) Hall effect IC and package inside power module.

Problem #3: Long tail times limit switching frequency of Si IGBTs. Cannot take advantage of WBG high-speed switching capabilities - switching speed of devices in phase leg limited by switching loss and noise-induced interference that can cause shoot-through.
Approach: Develop active gate control techniques to maximize switching frequency yet avoid spurious gate signals.

Description of Technology/Approach

Packaging Structure Schematic
Integrated High Temperature Power Module

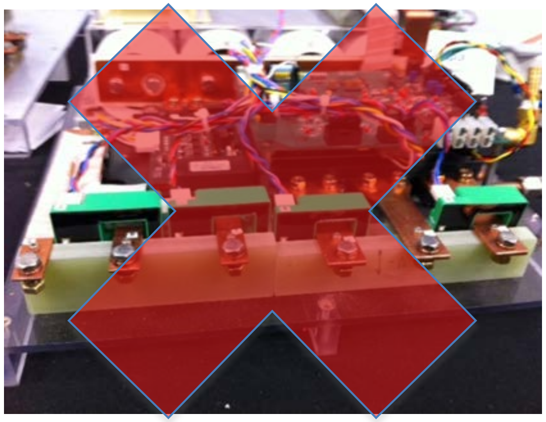


- Determine isolation and shielding requirements for electromagnetic compatibility for integrating gate drive components and sensors in a module.
- Identify and test high temperature adhesives for gate driver, current sensor, isolation / buffer die.
- Identify and test high temperature solders and brazing techniques and encapsulants.

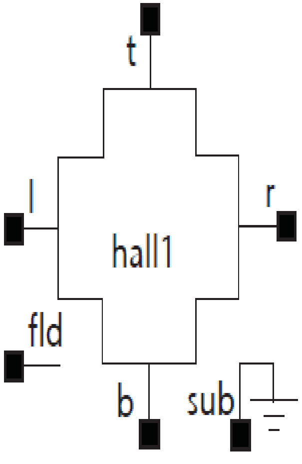
Technology/Approach

Develop an Application Specific Integrated Circuit (ASIC) that will measure both temperature and current and can be integrated into the power module.

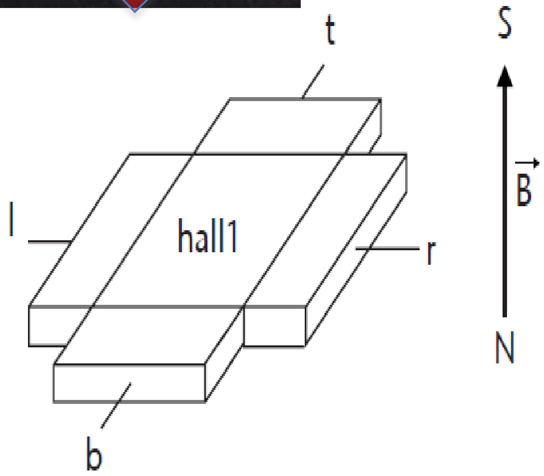
- Application requires a voltage-independent temperature measurement.
- In addition, we will provide a Hall-effect sensor on the ASIC for measuring current.
- Current measurement will be used for protection and control of module (fed back to converter controller).



Traditional Hall-effect current sensors in inverter

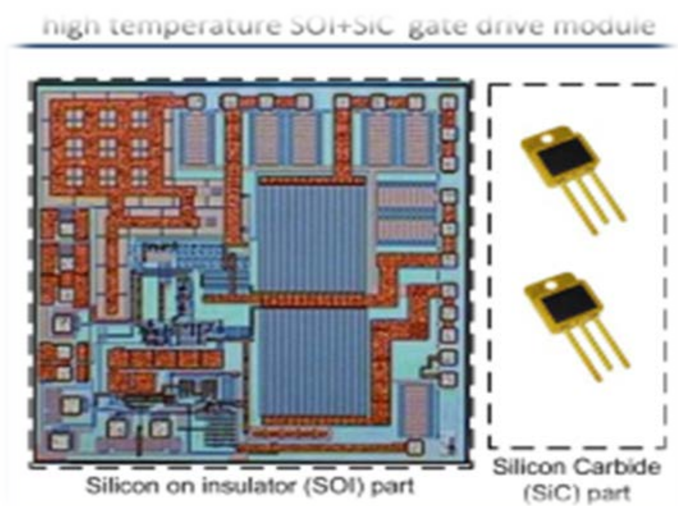


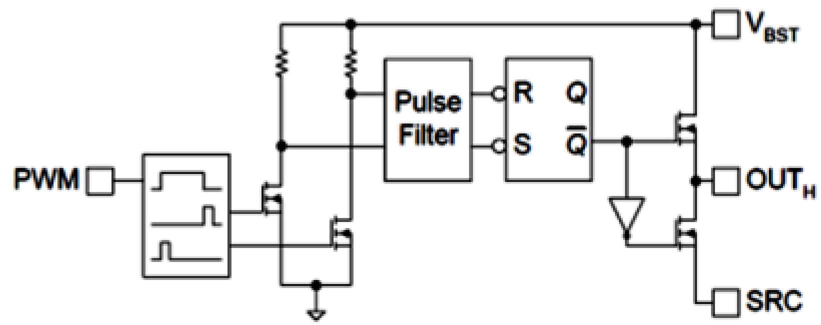
fld = Magnetic Field



Technology/Approach – Buffer and Isolation

- Design a buffer to increase current drive capability of SOI high temperature gate drive. Investigate active gate control techniques that can minimize switching losses and increase possible switching frequency of converter.





MOSFET/JFET Non-Complementary Totem-Pole Buffer Example

- Develop gate drive high temperature galvanic isolation techniques and incorporate the most promising into the power module.

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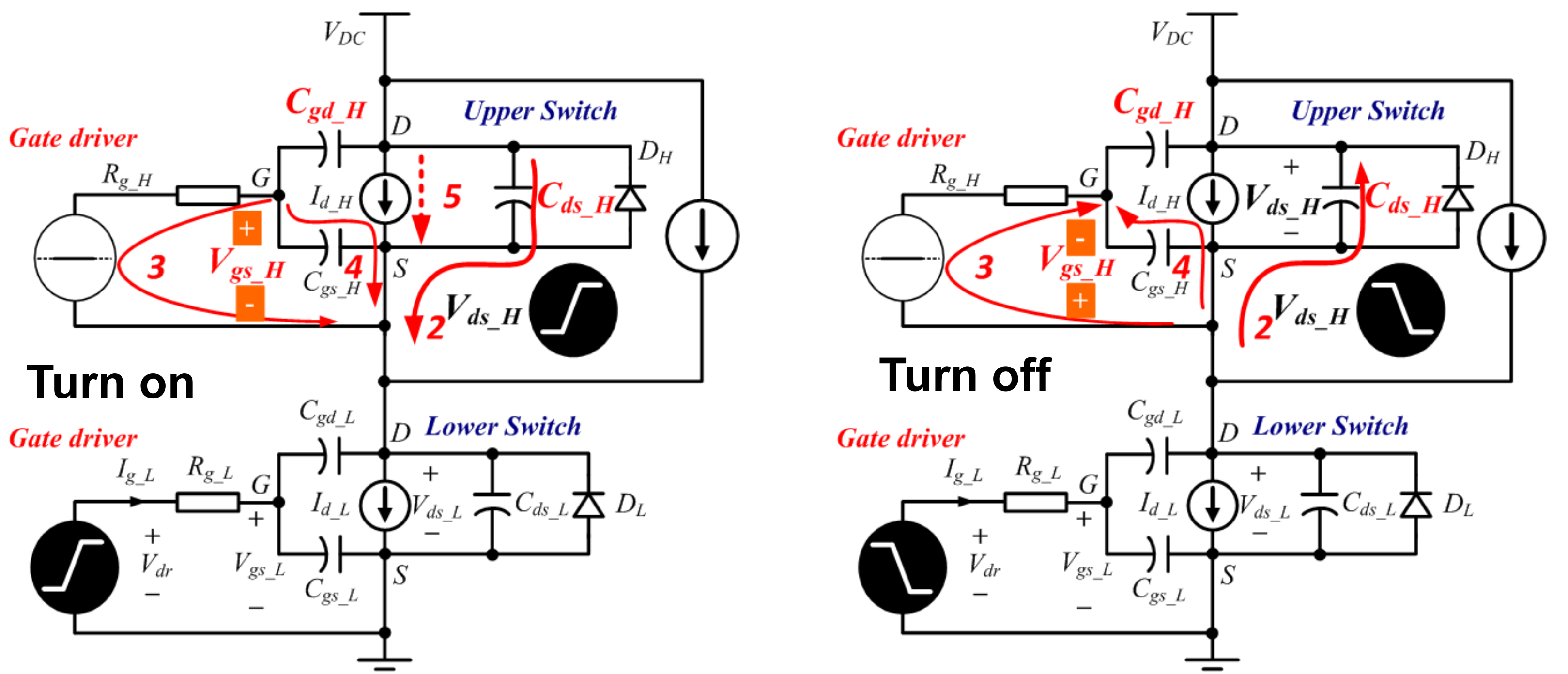
Phase Leg Module Challenges

Fast switching speed available with WBG devices brings us

- Low switching loss, high power efficiency
- Short dead time in the phase-leg, high power quality
- High switching frequency, high power density & EMI immunity

Switching speed in the phase-leg limited by

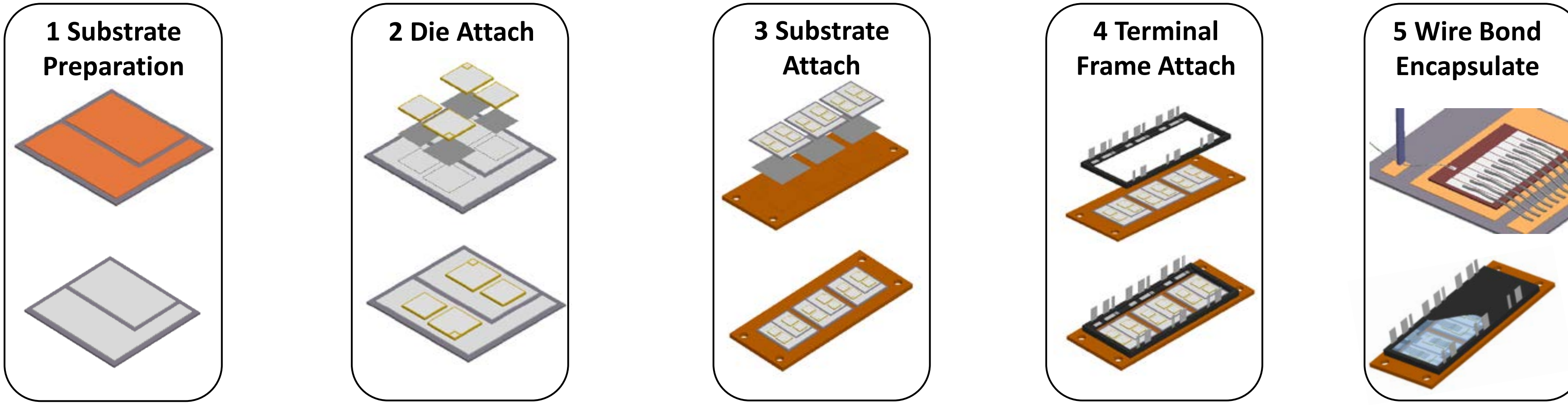
- Noise induced interference between two switches, leading to
  (1) Excessive switching losses (2) Device breakdown



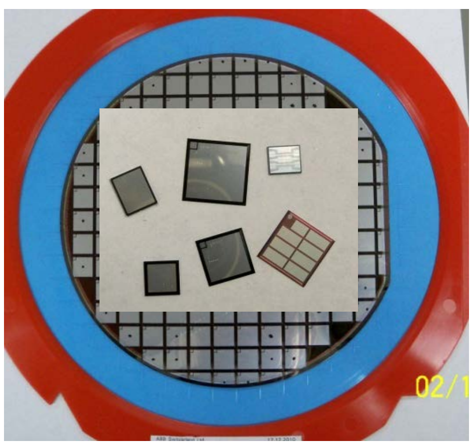
FY12 Approach Highlights

- Analyze packaging approaches needed for gate drive and buffer chips and for the current / temperature measurement ASIC.
- Development of an ASIC that can measure current and temperature with the prospect of integrating it into a power module.
- Design of input isolation scheme for integrating into a high temperature power module.
- Design of gate drive buffer and active gate control that allows faster switching and higher gate drive currents.

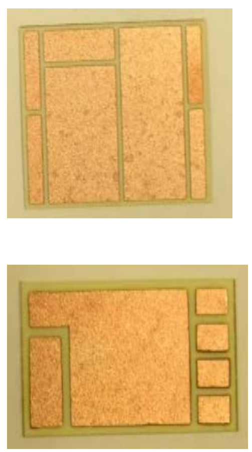
Development of Smart Power Module Packaging Technologies



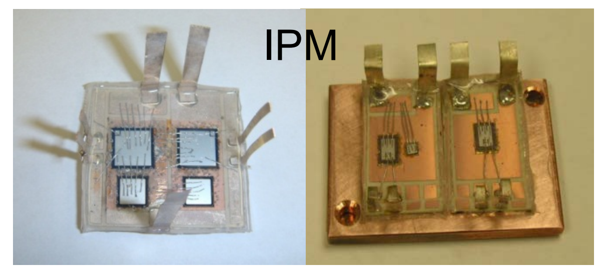
Packaging Processing Steps

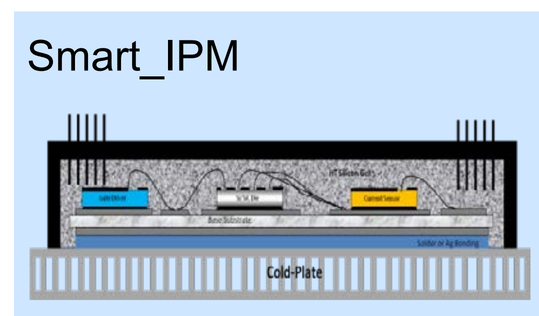


Power Switches Dies and Sensor Chips



Substrates

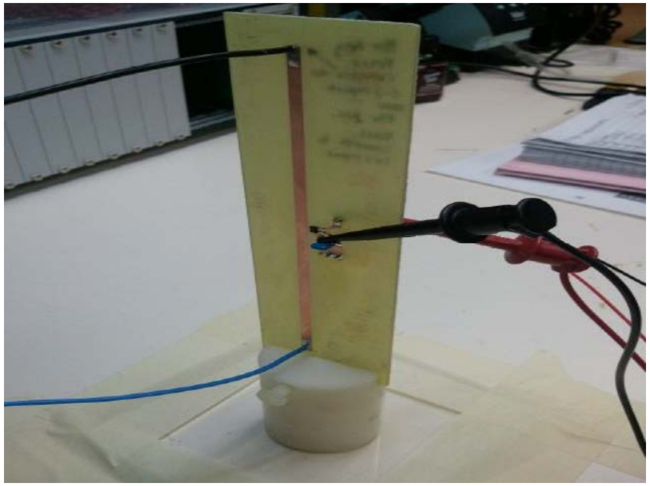




Example IPMs and Smart IPM Design

FY12 Accomplishments – Current Sensor

- Hall Effect devices exhibit good linearity and can be temperature compensated.
- FY12 work has concentrated on evaluation of commercially available devices.
- To date we have measured the DC response of the Allegro A1324 sensor.

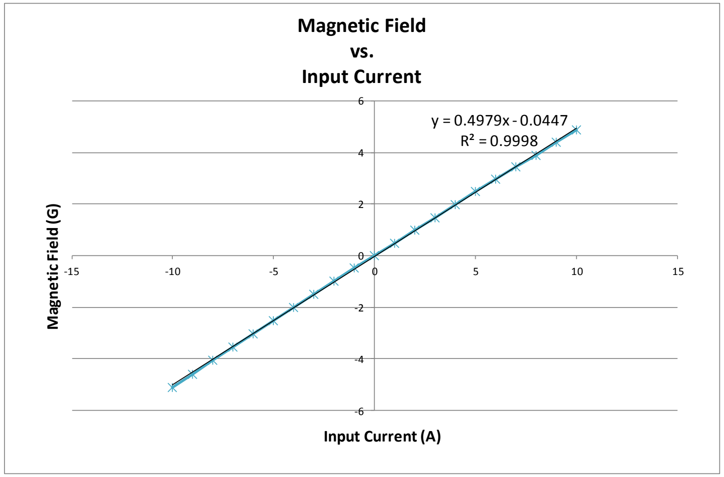


- **Hall Effect devices respond to the *B* field generated by a flowing current.**
- ***B* field for an infinite wire of arbitrary width can be found to be**

$$B = \frac{\mu_0}{2\pi} * \frac{I}{r2 - r1} * \ln\frac{r2}{r1}$$

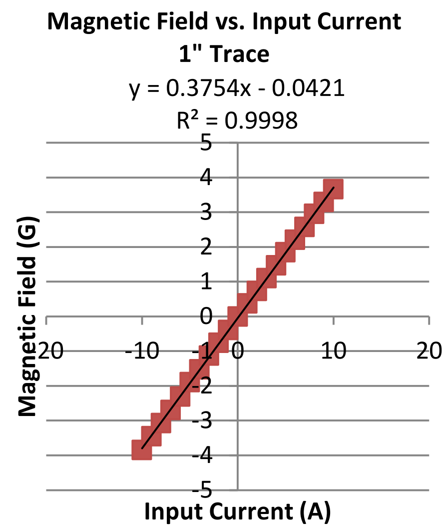
where *r1* is the edge of the conductor closest to the sensor and *r2* is the edge furthest.

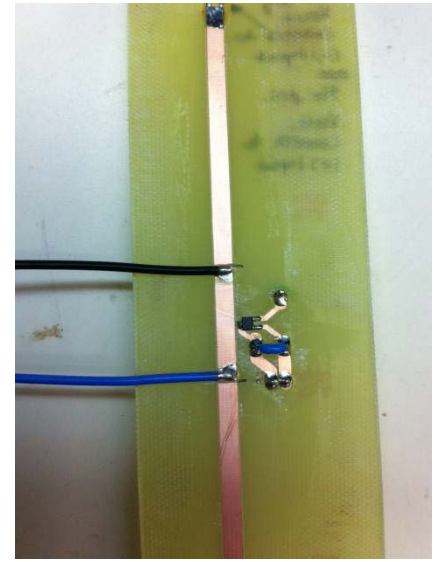
- **Results show excellent agreement with theory**
  - **We should see, in theory, a value of 0.56 G/A**
  - **We measure 0.5 G/A**

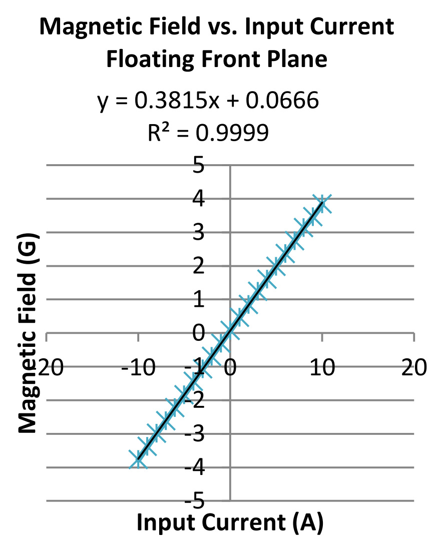


FY12 Accomplishments – Current Sensor

- Next, shortened the current path to more closely approximate realistic geometry.
- Measurements indicated a reduction of field from 0.5 to 0.38 G/A.
- Next, performed several runs of differing configurations with non-ferrous shielding to examine the effects at DC which could cause errors.
- Results showed essentially no effect, as expected.



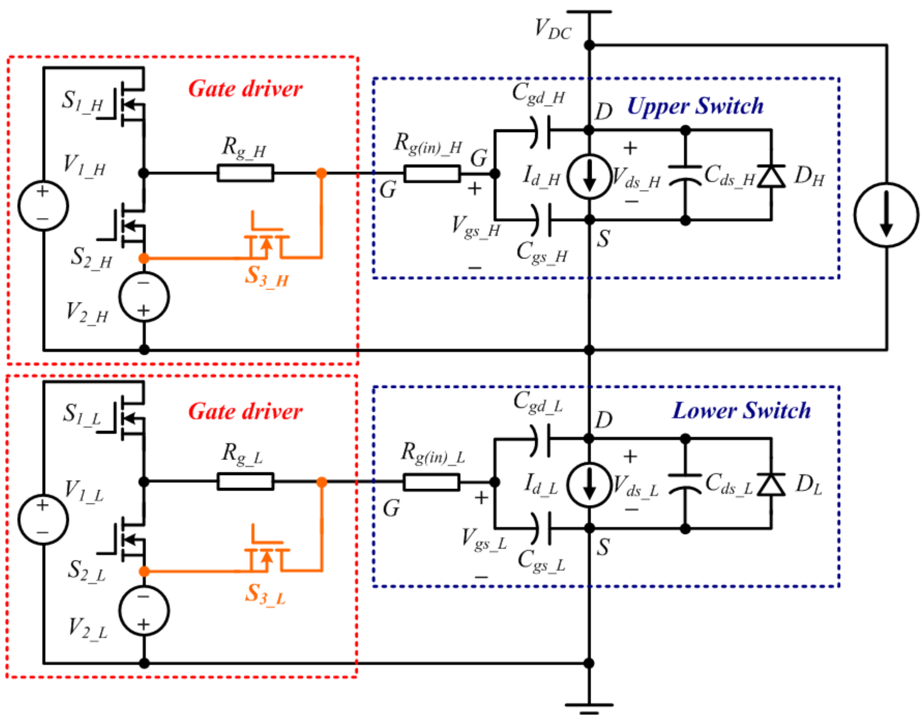




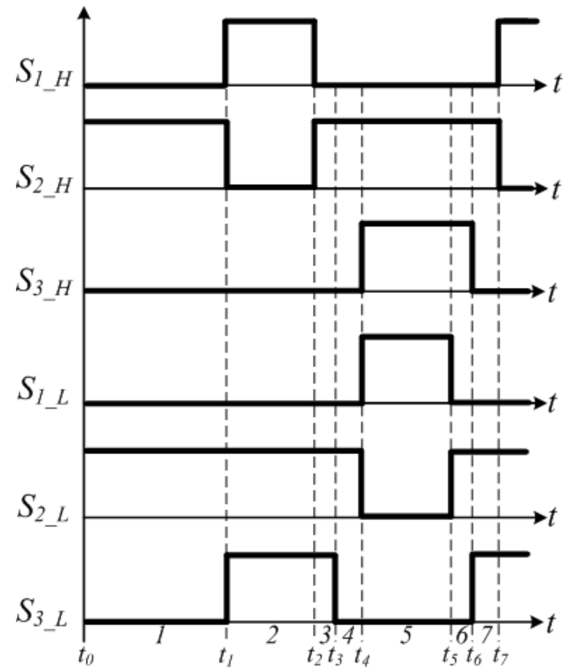
FY12 Accomplishments - Intelligent gate drive circuit for active gate control

Developed proposed circuit:

- Mitigate noise induced interference in the phase-leg configuration
- Increase switching speed



A proposed intelligent gate drive circuit

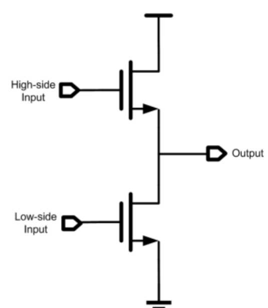


Logic signals for intelligent gate drive circuit

FY12 Accomplishments - Buffer

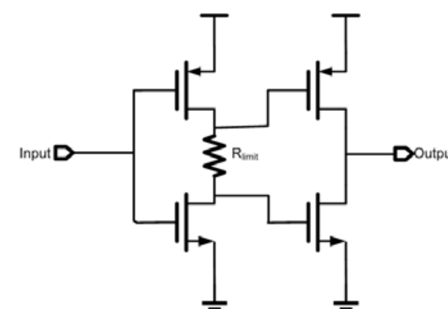
- **2 NFETs Buffer**

  - **2 NFETs buffer has been found to have a better composite FOM compared to CMOS buffer.**
  - **The requirement for both low-side and high-side inputs can be met by connecting to the internal signal pins available on SOI gate driver.**
  - **NXP PSMN013-30YLC (Si FET) and EPC2014 (GaN® FET) have been selected for their superior FOMs.**



- **CMOS Buffer**

  - **CMOS buffer is determined to be easier to drive, and the high output capacity of the SOI IC can be fully taken advantage of.**
  - **Current limiting resistor is used to mitigate shoot-through in the 1st stage and provide dead time for the 2nd stage.**
  - **Dual N&P-channel MOSFET IC (FDS4897C) is selected to minimize interconnection parasitics.**

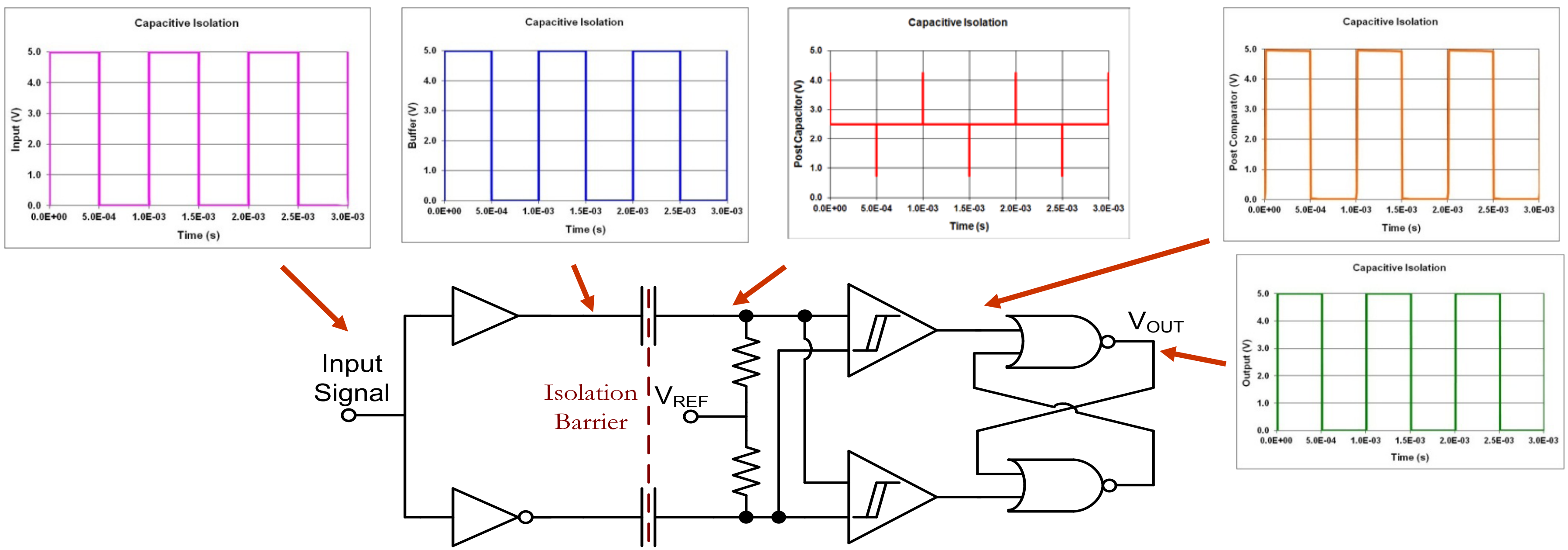


FY12 Accomplishments – Input Isolation

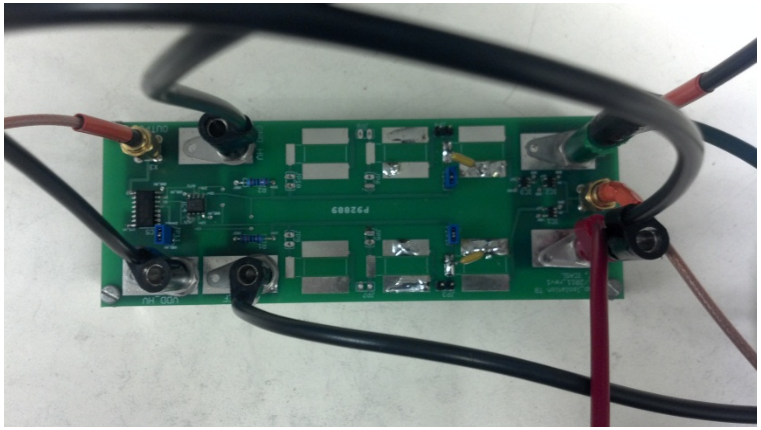
- Input isolation circuitry is required to protect/isolate the microcontroller from possible high-voltages feedback (EMI) present in the phase-leg power module
  - Design objective ≥3.0 kVrms isolation
  - Three methods have been under investigation for the galvanic isolation
    - Optical isolation
    - Capacitive-based isolation
    - Transformer-based isolation
  - Integrate high temperature isolation solution with module

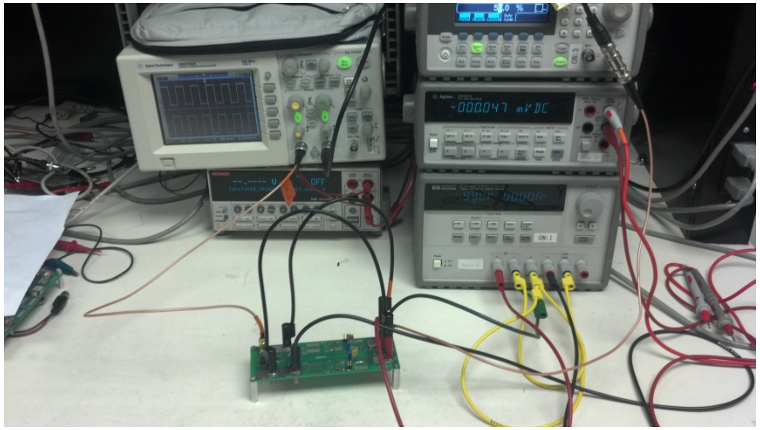
FY12 Accomplishments – Input Isolation

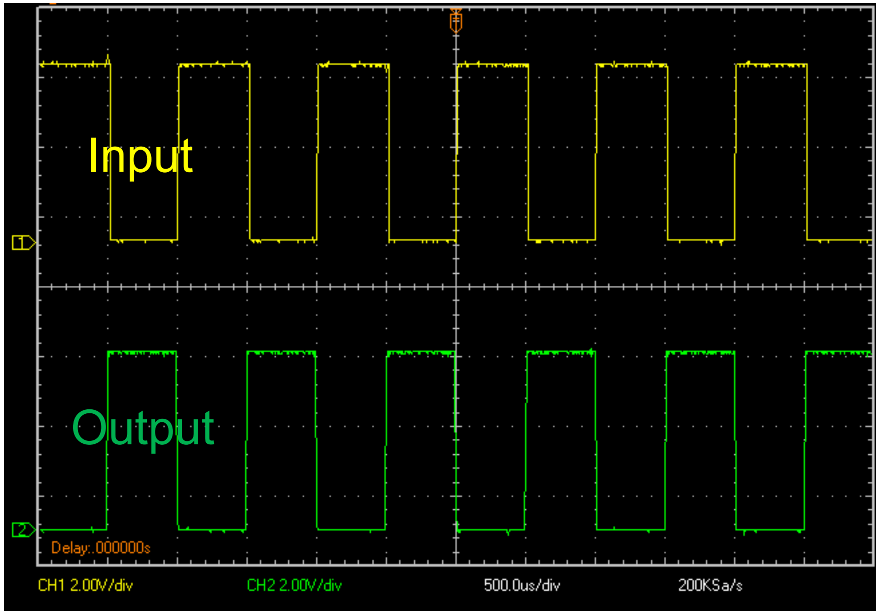
- **Capacitive coupling**
  - Simpler to implement than transformer based input isolation circuitry (no modulation, no oscillator, etc.)
  - Requires off-chip capacitors (high voltage, high temperature)
  - Potentially slower than the transformer-based isolation
  - More difficult to pass data back to control circuitry



FY12 Accomplishments - Capacitive Coupling



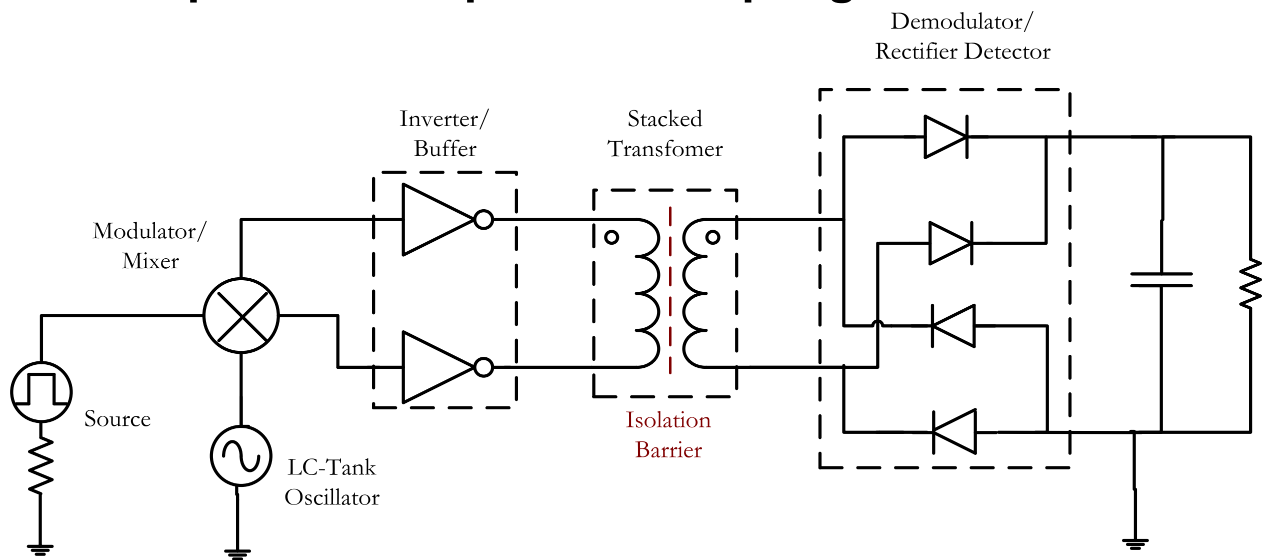




- Test board for capacitive-coupling isolation
  - Input signal : 1 kHz 5 $V_{peak\text{-}to\text{-}peak}$
  - Working on revised design to increase the operating frequency
    - Implementing high speed comparator
    - Investigating substrate-based capacitor

FY12 Accomplishments – Transformer isolation

- Requires modulation/demodulation circuitry
- Requires off-chip transformer
  - Investigating using a coreless transformer constructed on the substrate of the module
  - Designing a polyimide board with printed coils to evaluate functionality
- Higher voltage isolation than capacitive coupling
- Can modulate control signals to send back to microcontroller
- Faster than capacitive coupling
- Circuitry more complex than capacitive coupling

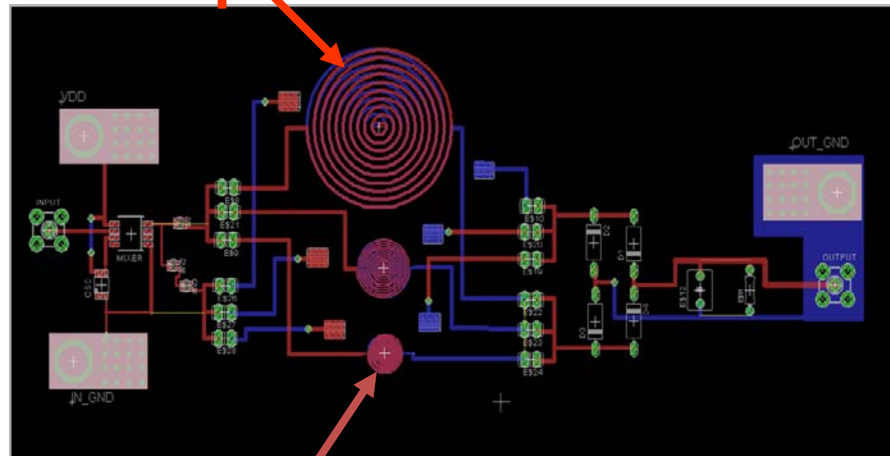


FY12 Accomplishments – Transformer-Based Isolation

- **Coreless PCB Transformer Characteristics**
  - **Top Transformer – Line Width 0.6 mm**
    - **Mutual Inductance = 2.173 μH**
    - **Leakage Inductance = 0.206 μH**
    - **With C_{res} = 390 pF → High Efficiency Range (gain > 0.8) = 2 MHz to 7.5 MHz**
  - **Bottom Transformer – Line Width 0.2 mm**
    - **Mutual Inductance = 0.266 μH**
    - **Leakage Inductance = 0.267 μH**
    - **With C_{res} = 680 pF → High Efficiency Range = 6 MHz to 9 MHz**
- **For the best signal transfer, the input control signal must be modulated to operate in the frequency range just below the resonant frequency of the coreless transformers.**
- **The resonant frequency is set by a resonant capacitor and the inductance of the transformers.**

$$f_{res} = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}}$$

Top



Bottom

PCB Characteristics

- **Thickness – 0.062" or 1.57 mm**
- **Electrical Strength**
  - **FR-4 : 43 kV/mm**
  - **Polyimide : 44 kV/mm**

References

•S.C. Tang, S. Y. Ron Hui, Henry Shu-Hung Chung, "A Low-Profile Converter Using Printed Circuit Board (PCB) Power Transformer with Ferrite Polymer Composite," *IEEE Transactions on Power Electronics*, Vol. 16, July 2001.

•S.C. Tang, S. Y. Ron Hui, Henry Shu-Hung Chung, "Optimal Operation of Coreless PCB Transformer-Isolated Gate Drive Circuits with Wide Switching Frequency Range," *IEEE Transactions on Power Electronics*, Vol. 14 May 1999.

FY 13 Plans – Current Measurement

- Single-point magnetic field sensors suffer from interference generated by other local sources.
- We are looking at mitigation of this by
  - Eddy-current shielding using non-magnetic materials
  - Common-mode correction of external fields using appropriately-positioned hall sensors (possible patent disclosure)
- Remainder of FY12 and FY13 will focus on
  - AC current measurements
  - Correction of external field interference

FY 13 Plans – Input Isolation

- Input Isolation
  - Input isolation scheme (down select from two types) will be selected for implementation in the power module
    - Current research indicated either transformer or capacitive based isolation approach will be utilized
  - Complete test bed for the isolation scheme will be developed
  - Work on the final integrated solution
    - Selected approach will likely require both in-module passives and on-chip integrated circuit electronics

FY13 Plans - Buffer and Active Gate Drive

- **Integration of the buffer (down select) into the power module together with the SOI gate driver and the power switches.**

- **Optimize SOI gate driver interface with the buffer stage (lower output resistance, larger output amplitude).**

- **Integrate active gate control with buffer.**

Collaborations

- The University of Tennessee
  - Highly Integrated Active Gate Drive
    - Input Isolation
    - SOI Gate Drive Chip – previously developed jointly with ORNL
    - Buffer
- Leveraging ORNL's packaging research efforts and ORNL's expertise on materials science and technology
  - Packaging material
  - High temperature packaging being done on other projects
- Leveraging ORNL's measurement and instrumentation science expertise
  - ASICs for current and temperature measurement

Summary

- This project will develop a highly integrated smart power module that can operate in higher temperature environments or with engine coolant (105C).
- We are developing an ASIC that can measure current and temperature and high temperature packaging techniques for power electronics in HEVs / EVs.
- We are developing a high temperature active gate drive, isolation, and buffer.

Addresses Targets

- 55 kW inverter phase leg modules developed by this project will enable a converter to have 14 kW/l, 14 kW/kg, 5 $/kW, and 98 % efficiency. These research efforts will further the Program's efforts to reach the 2020 Tech Team targets for size and weight and 2015 cost and efficiency targets.