High-Voltage, High-Power Density Traction Drive Inverter

(Keystone Project #1)

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Project ID: ELT209

Overview

Timeline

- Start Date: FY19
- End Date: FY24
- 30% Complete

Barriers

- Passive components are bulky; DC bus capacitor takes 20% - 30 % of inverter volume
- Meeting DOE ELT 2025 High Voltage Power Electronics Targets
  - Power Density: 100kW/L
  - Cost: $2.7/kW
  - Peak Efficiency: > 97%
  - Reliability: 300,000 mile lifetime or 15 years

Budget

- Total project funding
  - DOE share – 100%
- Funding for FY20: $400K

Partners

- National Renewable Energy Laboratory
- Virginia Tech
- ORNL Team Members: Randy Wiles, Emre Gurpinar, Shajjad Chowdhury

Any proposed future work is subject to change based on funding levels

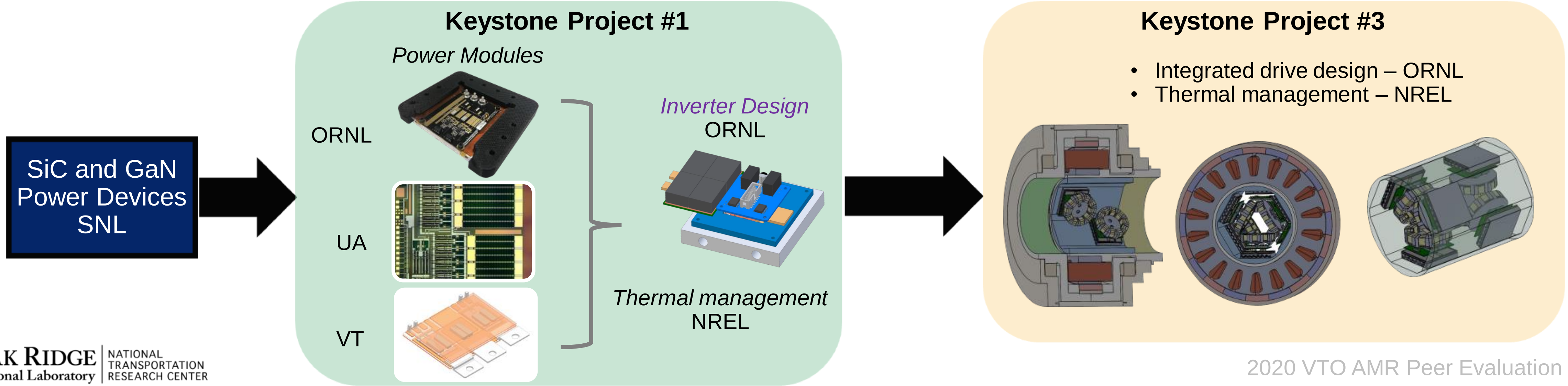
Relevance – Project Objectives

Overall Objective:

- Develop technologies for next generation traction drive power electronic systems to achieve DOE ELT 2025 target of 100 kW/L
- Focus on traction drive inverter architecture, optimization of bus bar design, minimization of passive components

FY 2020 Objectives:

- Develop driving cycle-based tools for DC bus capacitor life-expectancy prediction and sizing
  - Inverter loss profiles
  - Capacitor transient thermal impedance models
  - Capacitor ripple current and temperature profiles
- Develop direct-cooled DC bus bar designs
  - Embedding cooling channels
  - Using cold plates
- Evaluate the impact of direct-cooled bus bars on the DC bus capacitors in various power modules



Milestones and Go/No-Go Decision

Year	Quarter	Milestones and Go/No-Go Decision	Status
FY2020	Q1	**Milestone**: Develop driving cycle based inverter DC bus capacitor analysis tools.	Completed
	Q2	**Milestone**: Design a bus bar using distributed and integrated capacitors with direct cooling for a 100kW segmented inverter.	Completed
	Q3	**Milestone**: Evaluate the impact of the direct-cooled bus bars on the DC bus capacitors in various power modules.	On-track
	Q4	**Go/No-Go decision**: If the direct-cooled bus bar design can significantly improve inverter performance and power density, finalize the design for use in the next inverter prototype design.	On-track
FY2021	Q1	**Milestone**: Design a 100kW high voltage, segmented inverter using ORNL power modules (developed in ELT208).	On-track
	Q2	**Milestone**: Evaluate the design against the DOE ELT 2025 targets.	On-track
	Q3	**Go/No-Go decision**: Finalize the design and determine if it can meet the DOE ELT 2025 power density target.	On-track
	Q4	**Milestone**: Build a 100kW prototype.	On-track

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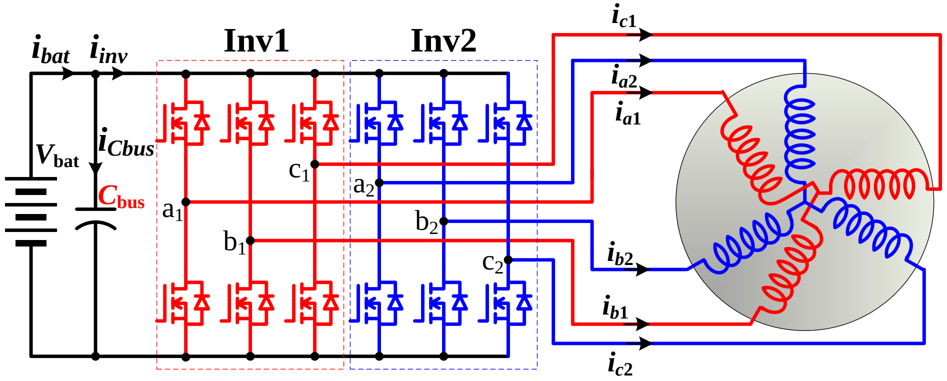
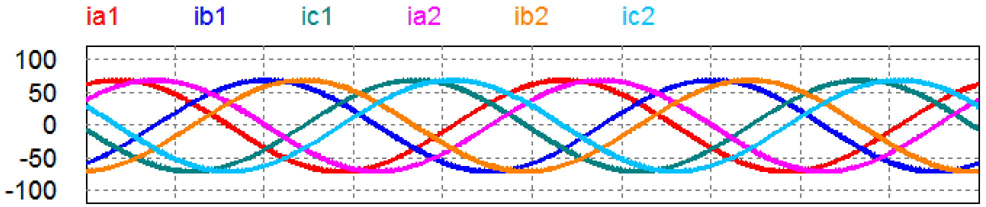
Approach

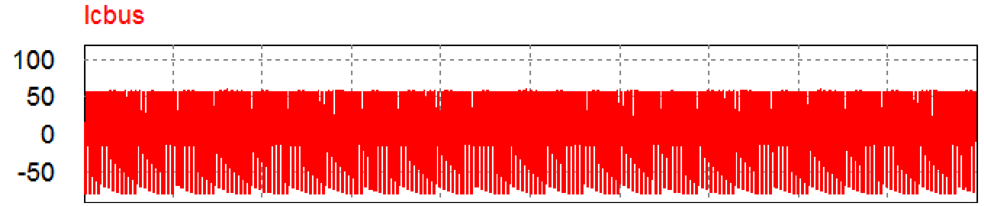
Goal: Increase traction drive power electronics system power density to meet DOE ELT 2025 targets (100kW/L) by focusing on power inverter architecture research and bus bar designs for reduction of passive components

- **Inverter architecture to reduce capacitor requirements:**
  - Multiphase inverter (asymmetrical six-phase)
  - Segmented inverter arrangement
- **Increase DC bus voltage (800V+):**
  - Better utilize SiC switching devices' inherently higher voltage ratings
  - Reduce the size of SiC dies (lower cost)
  - Reduce phase and DC bus current
  - Evaluate impact of insulation requirements
- **Optimize DC bus bar designs:**
  - Direct cooling of DC bus bars
  - Embedded and distributed capacitors



Asymmetrical six-phase inverter (30 degrees phase-shift between phase a_1 and a_2)





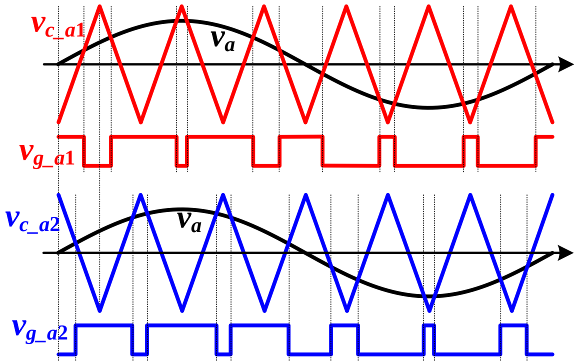
Simulation waveforms for the asymmetrical six-phase inverter using segmented PWM-switching: >50% reduction in DC bus capacitance over the three-phase inverter

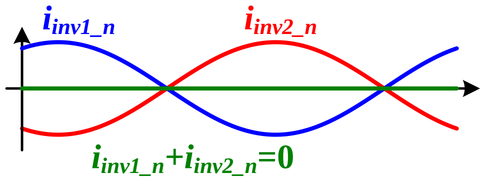
Any proposed future work is subject to change based on funding levels

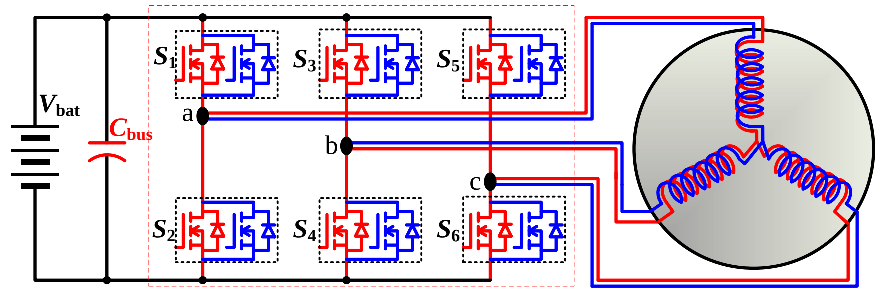
Approach-Use segmented inverter to reduce the DC bus capacitance

- **Segmented inverter**
  - Separate inverter switch dies and stator windings into two sets of drive unit
  - No changes needed in control of the motor except modifying the pulse width modulation (PWM) scheme
  - Interleaving the switching timings to reduce the DC bus ripple current

Reduction of capacitor ripple current with interleaved switching for carrier-based PWM methods

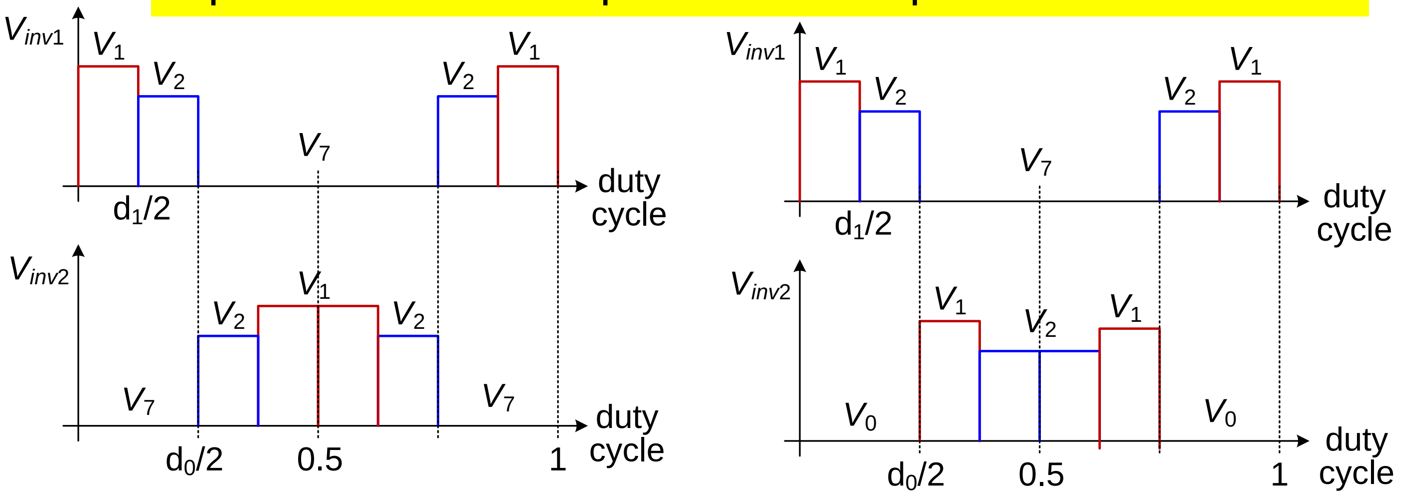




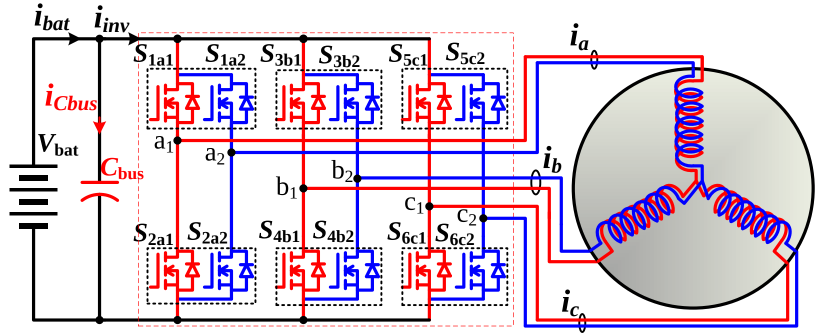


Standard 3-phase inverter

Optimal zero vector placement in space vector PWMs



For sector 1

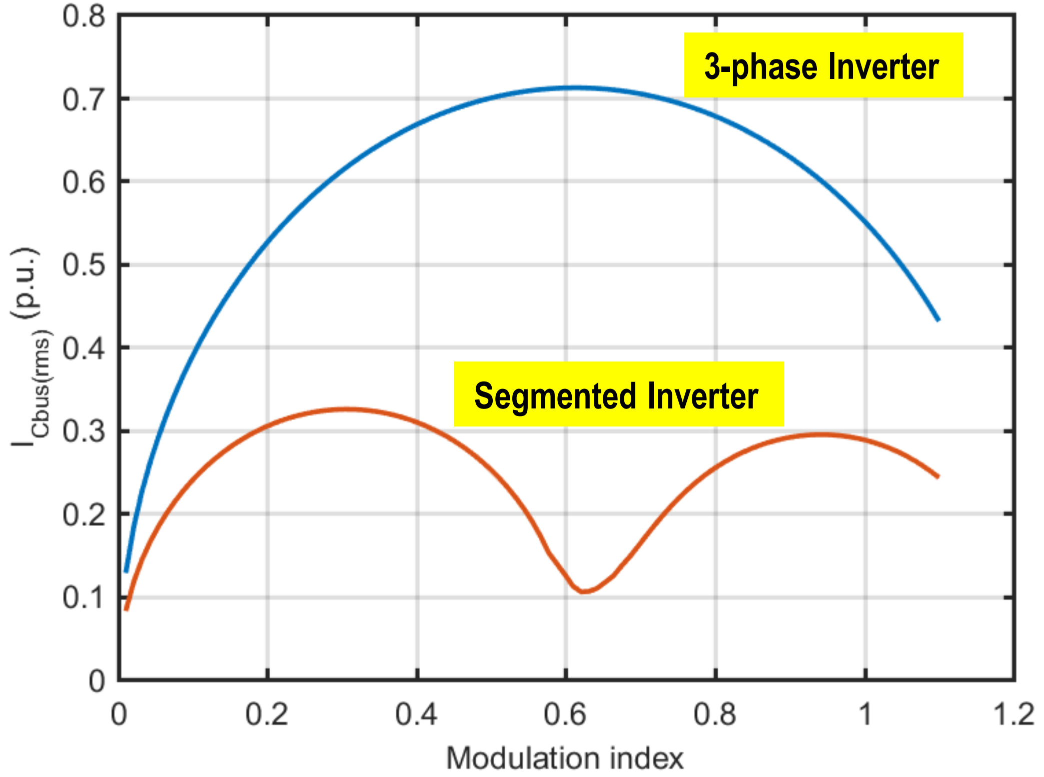


Segmented 3-phase inverter

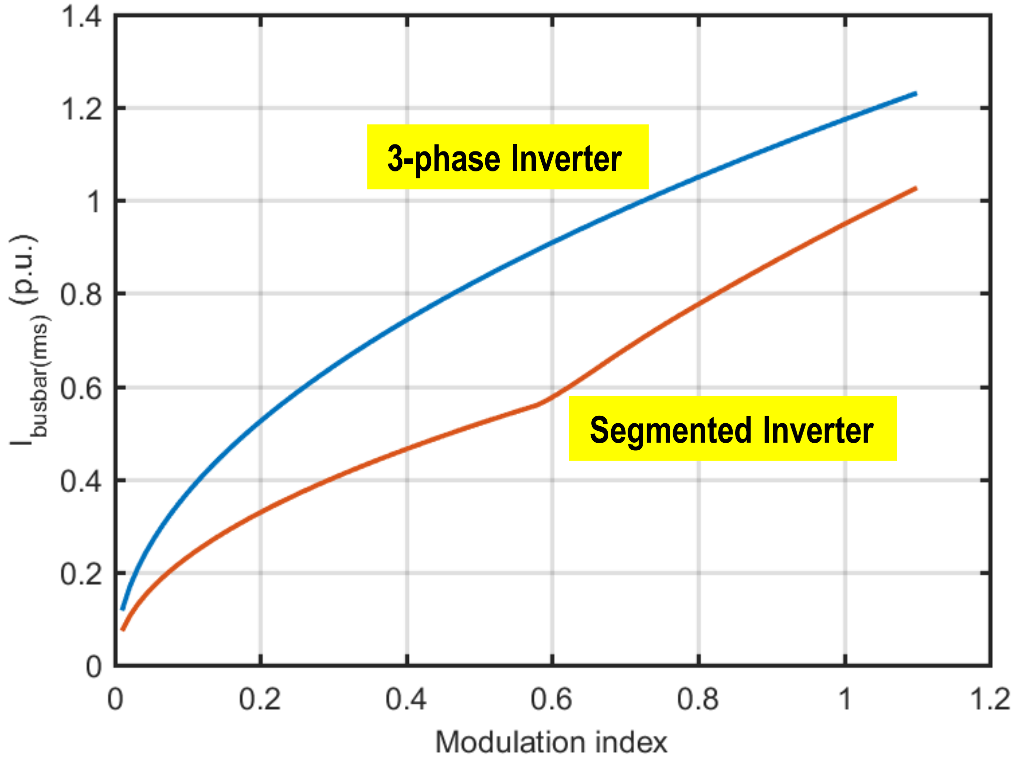
Technical Accomplishments – FY19

Developed a switching timing-based method for computing the inverter capacitor ripple current and bus bar current and implemented in MATLAB

- Advantages
  - Faster than circuit simulation
  - More accurate and easier to implement various PWMs than using analytical formulae



Comparison of normalized capacitor ripple current vs modulation index for 3-phase and segmented inverters

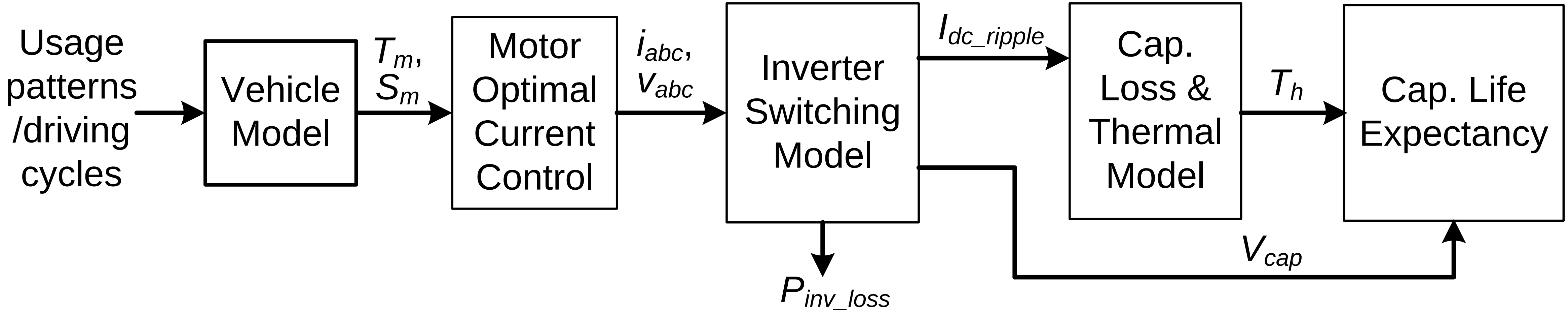


Comparison of normalized bus bar current vs modulation index for 3-phase and segmented inverters

Technical Accomplishments – FY20

Developed a driving cycle-based DC bus capacitor life-expectancy prediction and sizing tool

- Vehicle model: acceleration and drag losses
- PM motor model: maximum torque per amp
- Inverter switching model: switching timing-based loss computation
- Capacitor loss and thermal model: transient impedance thermal model

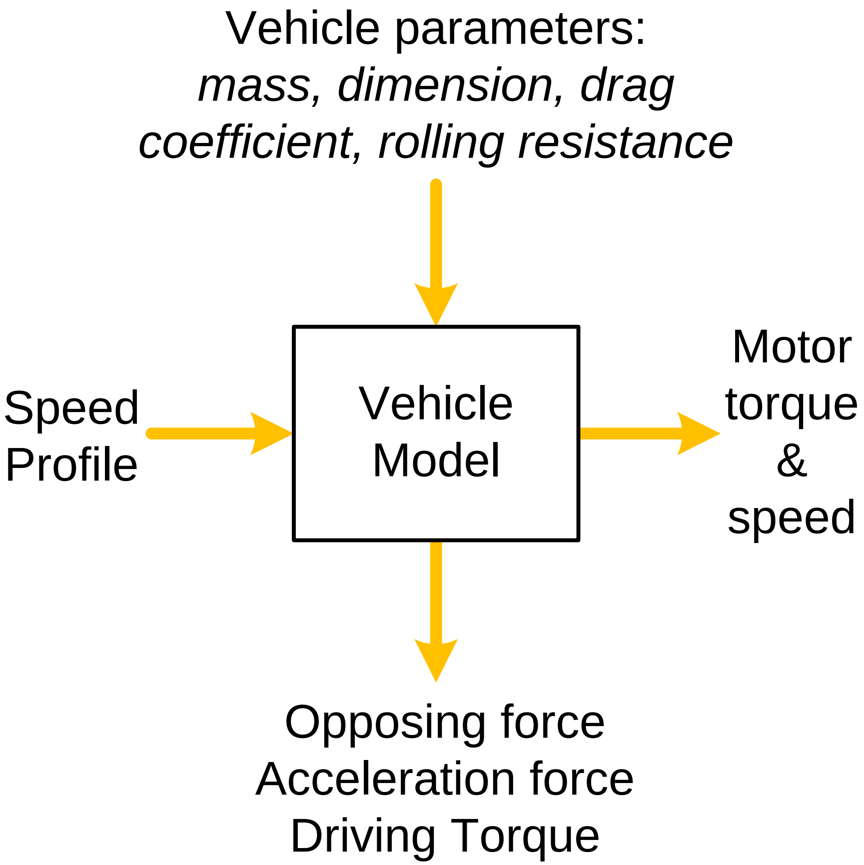


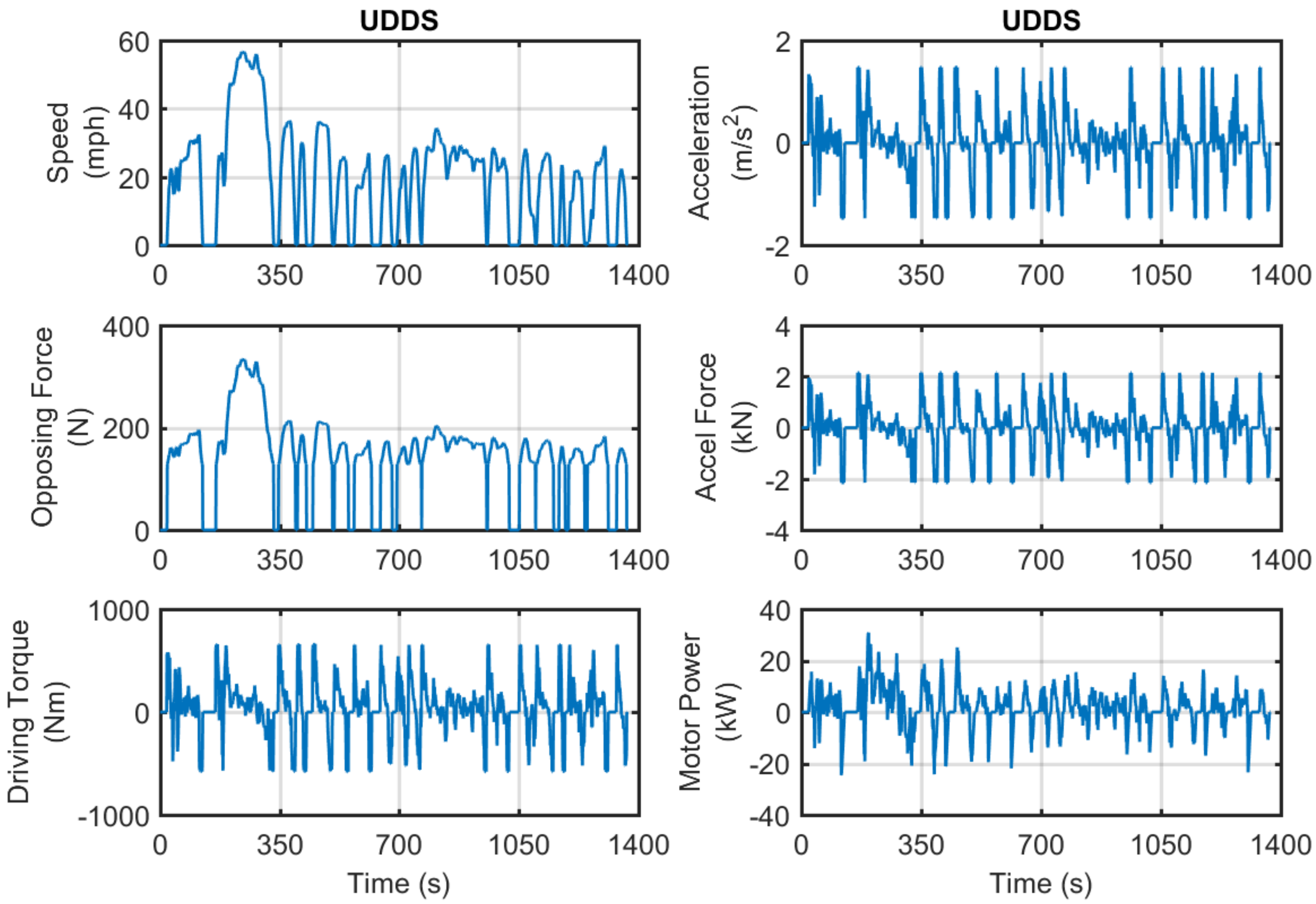
Block diagram for driving cycle–based DC bus capacitor life-expectancy prediction and sizing tools

Technical Accomplishments – FY20

Developed a driving cycle-based DC bus capacitor life-expectancy prediction and sizing tool

- Modeling results for UDDS - *Vehicle model outputs*

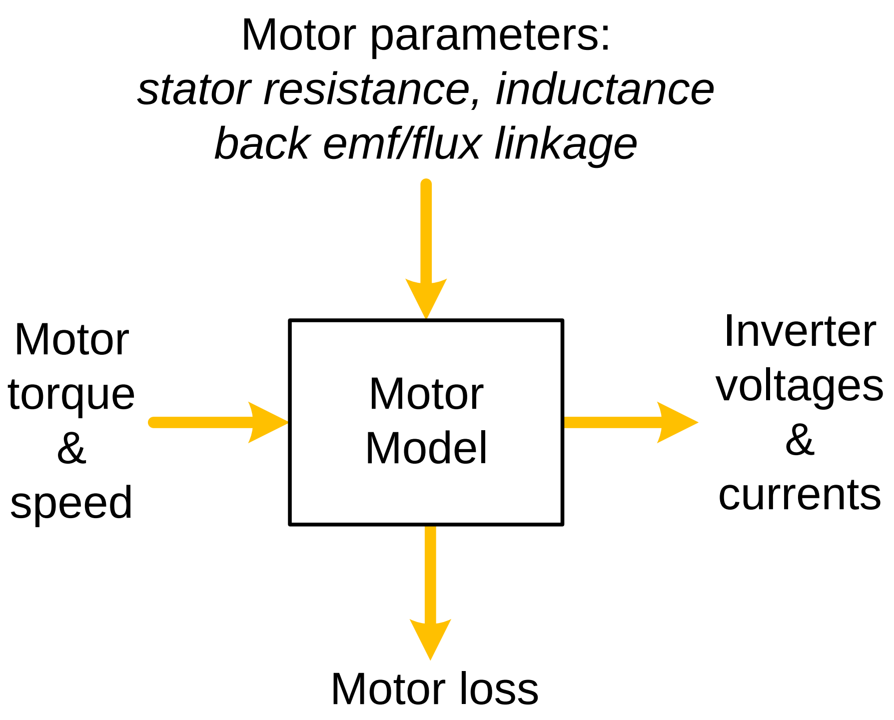


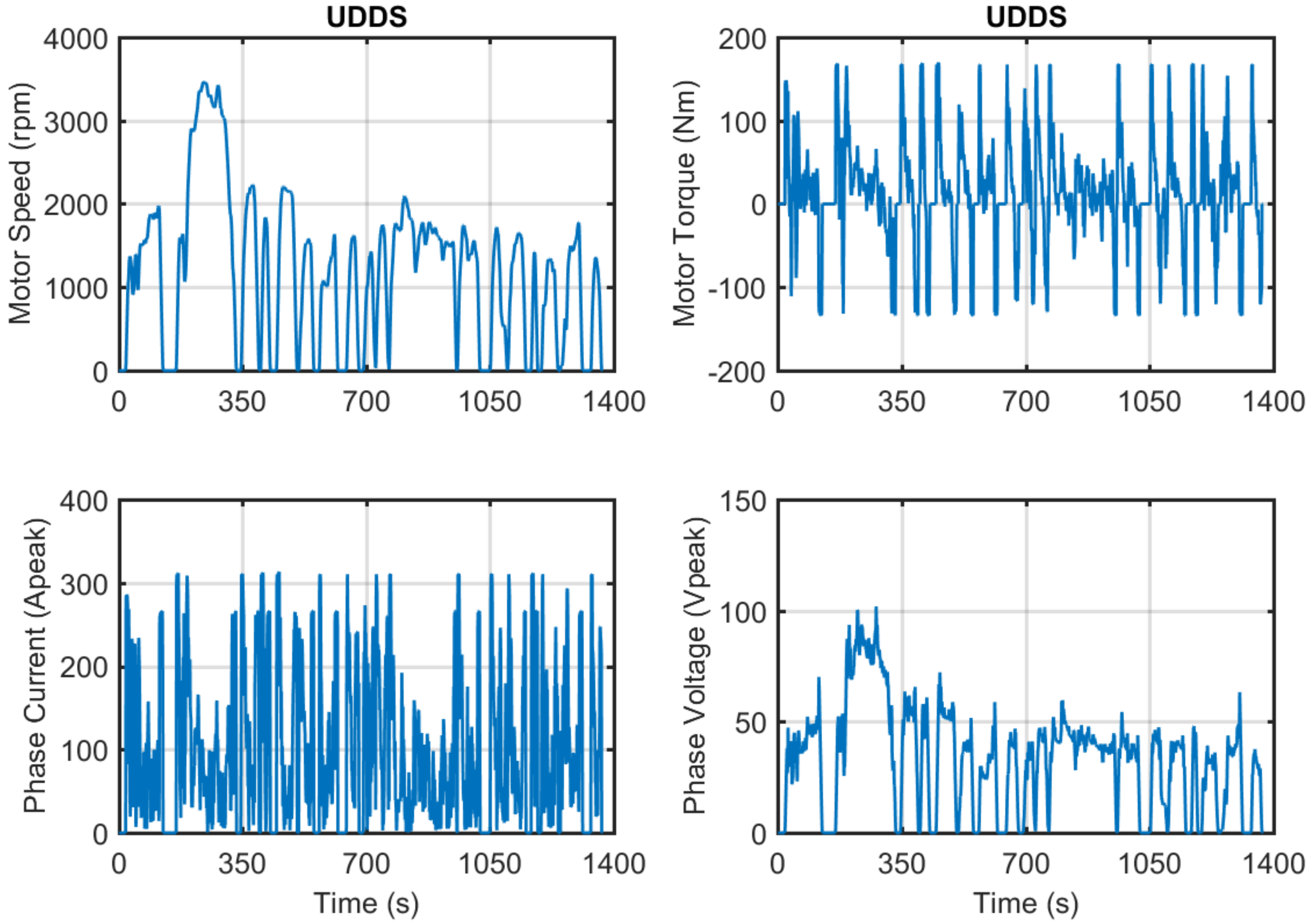


Technical Accomplishments – FY20

Developed a driving cycle-based DC bus capacitor life-expectancy prediction and sizing tool

- Modeling results for UDDS - *Motor model outputs*

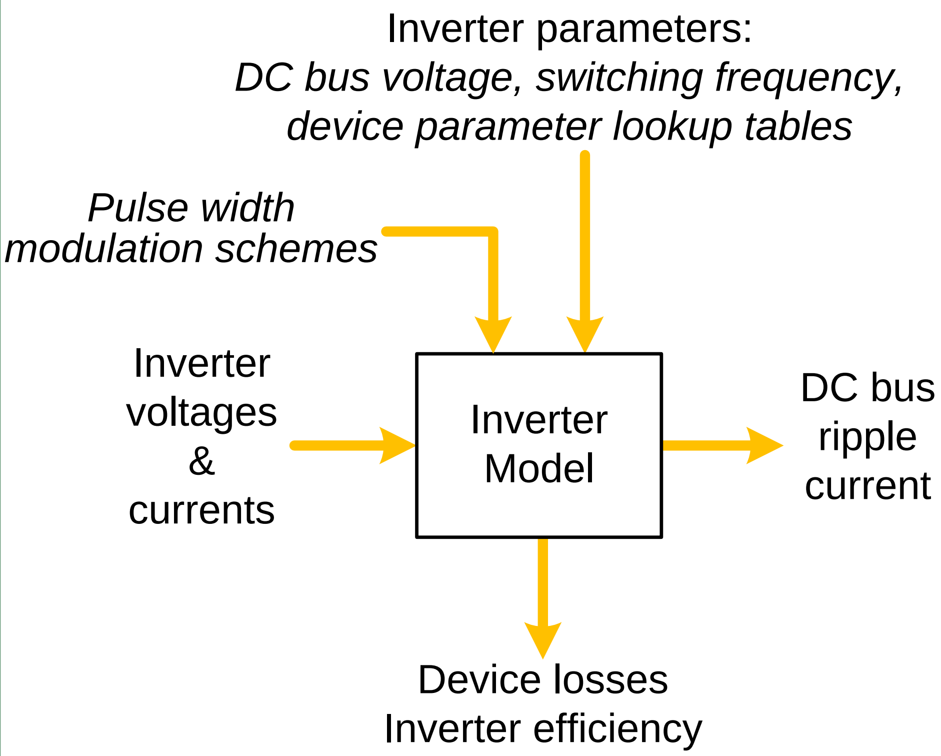


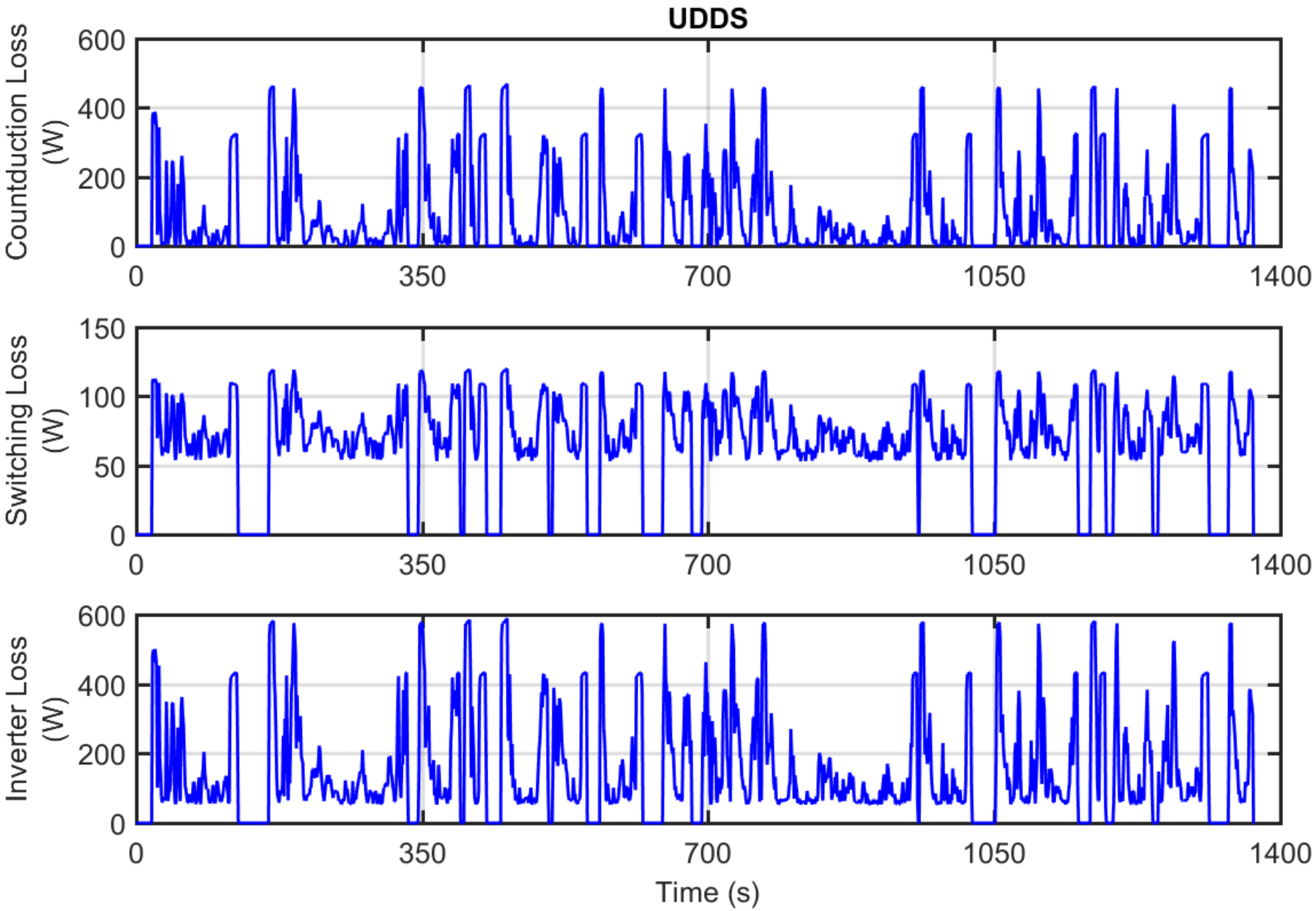


Technical Accomplishments – FY20

Developed a driving cycle-based DC bus capacitor life-expectancy prediction and sizing tool

- Modeling results for UDDS - *Inverter model outputs*

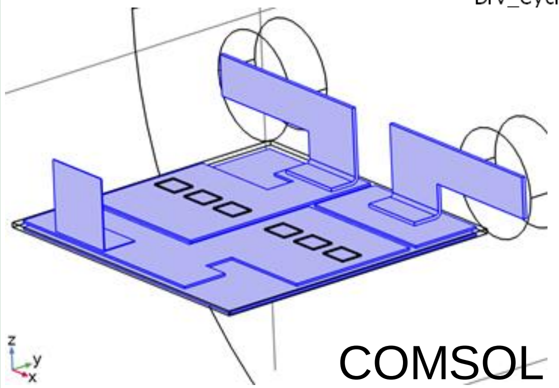




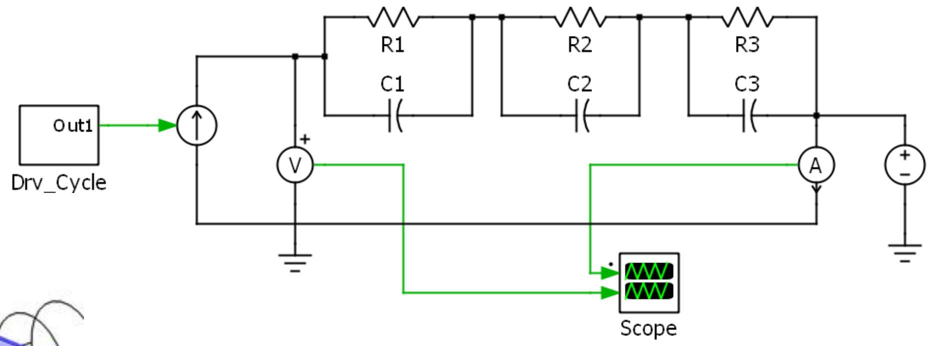
Technical Accomplishments – FY20

Developed capacitor transient thermal impedance models

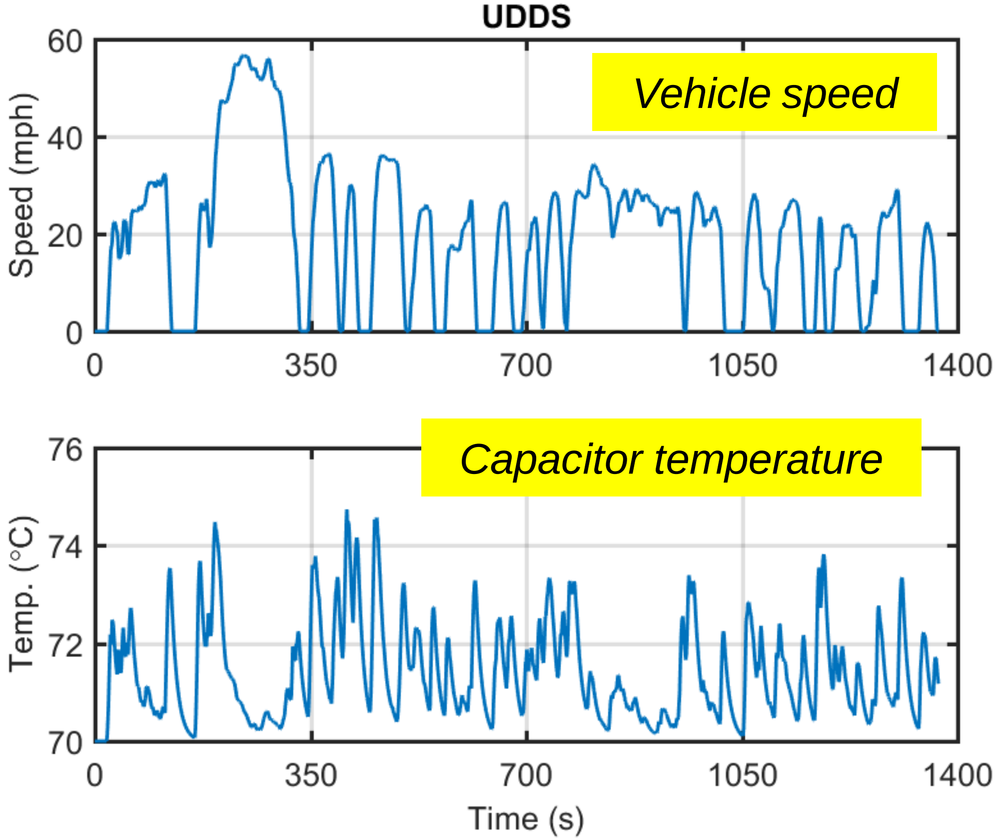
- Developed a thermal model for a DBC-based inverter assembly in COMSOL and performed time domain thermal analysis for the DC bus capacitor.
- Built a transient thermal impedance model for evaluating the heating effect of the inverter switch losses on the DC bus capacitor.
- Implemented a thermal simulation model for the DC bus capacitor in PLECS that is driven by driving cycle inverter losses.



COMSOL model



PLECS thermal model for the inverter DC bus capacitor

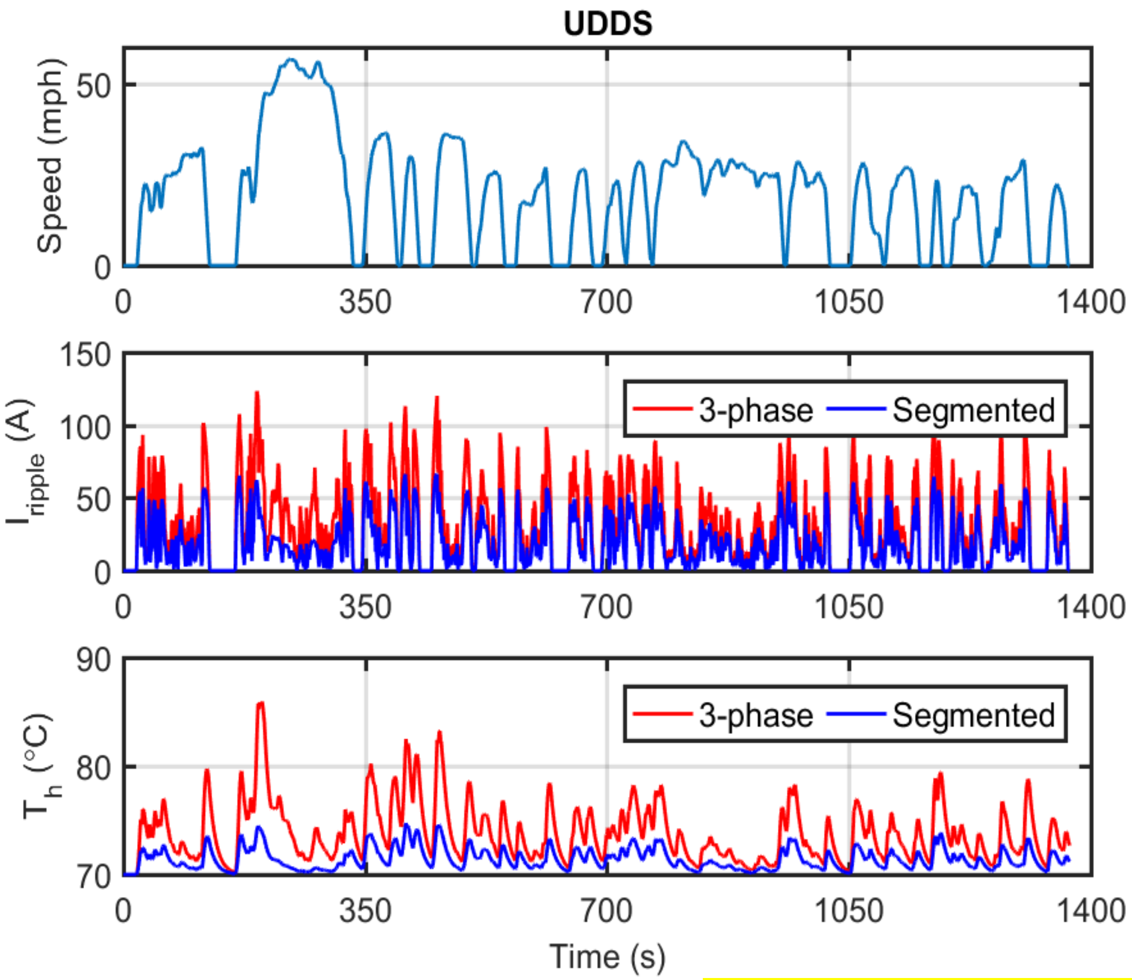


Simulation results for capacitor temperature over the UDDS driving cycle

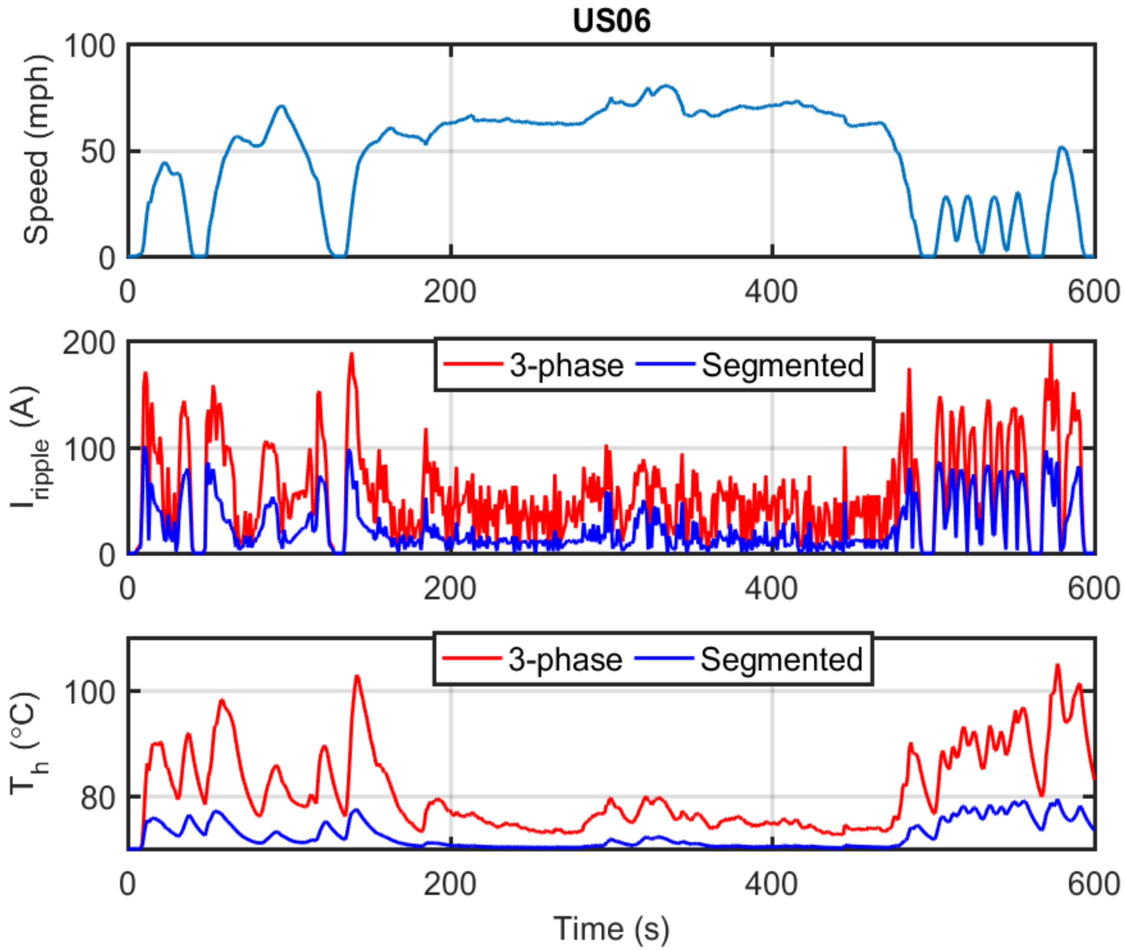
Technical Accomplishments – FY20

Segmented inverter can significantly reduce the capacitor hot spot temperature

- Implemented the driving cycle based thermal simulation model for the DC bus capacitor in MATLAB; no longer need to convert to a circuit model in PLECS



UDDS



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The segmented inverter brings significant reductions in both ripple current and temperature over the two driving cycles

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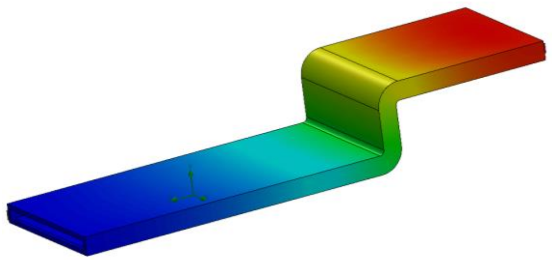
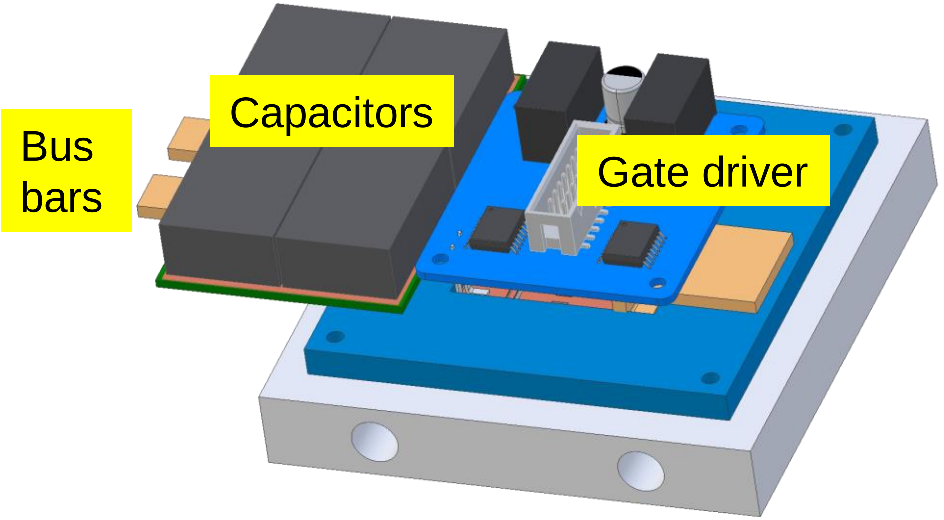
Technical Accomplishments – FY20

Complete a direct-cooled bus bar design

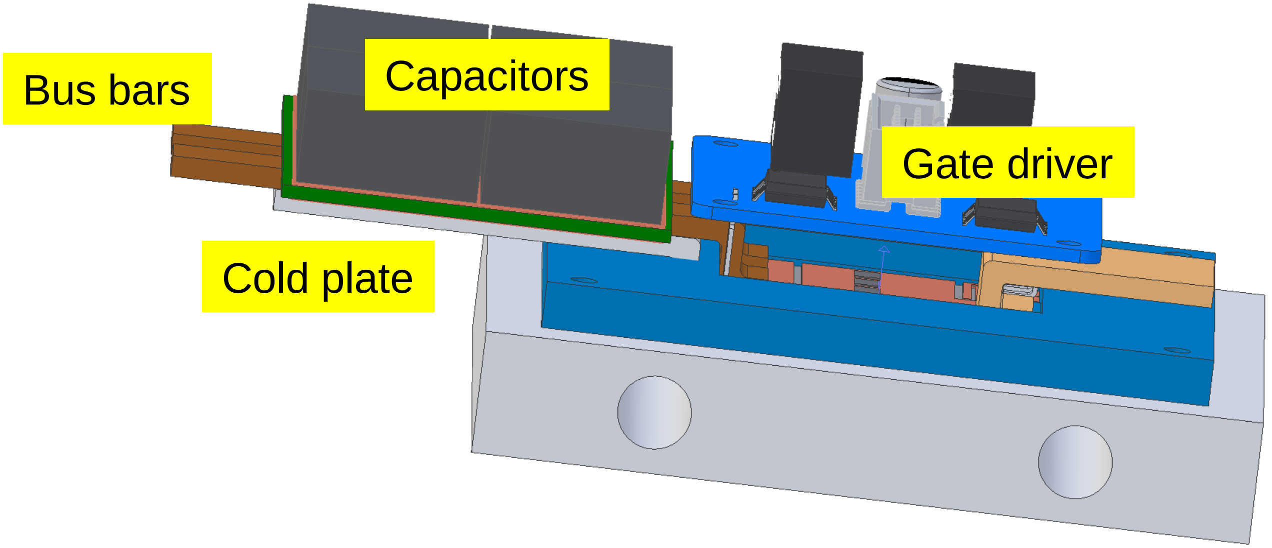
- Direct-cooled bus bar design
  - Printed bus bars with embedded cooling channels
  - Printed thin aluminum cold plate attached to the bus
- Completed a design for an inverter phase leg module using the direct-cooled bus bars
  - Inverter coolant is siphoned to the bus bar cooling channels



Direct-cooled bus bar modeling in COMSOL.



(a) Bus bars with embedded cooling channels



(b) Bus bars with a thin aluminum cold plate attached

Inverter phase leg module with direct-cooled bus bars

Response to Previous Year Reviewers' Comments

- **Reviewer:** The project does not discuss the potential to the electric machine and machine control with multiphase and segmented inverter topologies.
  Response: The segmented inverter works well with multipole motors, in which two sets of three-phase stator windings can be located in their own slots to eliminate the need for interphase isolation between the two winding sets. For PM motors, this configuration can also remove the uncontrolled rectification mode by halving the back EMFs. The doubling of motor leads will not be an issue in integrated tractions drives. Regarding motor control, no changes are required in control algorithms, except minor changes in the generation of PWM signals. Since a six-phase drive operates essentially as two three-phase systems, all the three-phase motor control methods can be readily applied.

- **Reviewer:** If the voltage is increased to 800V the current is reduced to half. Therefore, the reviewer asked why the project team needs to use a 6-phase system to cut the current phase more.
  Response: 800V, six-phase drives are better suited for higher power traction drive systems, while the segmented inverter is well suited for a wide range of power levels. In addition, an 800V DC bus leads to better utilization of the SiC MOSFETs, which are technologically most matured at 1200V.

- **Reviewer:** How system cost is affected by adding more power switches to the inverter and more windings to the motor to help cancel cap ripple voltages.
  Response: For the segmented inverter, there is no change in the total area of semiconductor dies or the number of motor stator windings. Only the connection of the windings are modified to form two sets of three-phase windings. Cost saving comes from the significant (up to 60%) reduction in the bus capacitance and its cost, which is more than offsetting the increase in the gate drives.

Collaboration and Coordination with Other Institutions

NREL NATIONAL RENEWABLE ENERGY LABORATORY	**National Renewable Energy Laboratory** • Incorporate thermal management research results into inverter designs • Validate inverter thermal designs
VT VIRGINIA TECH	**Virginia Tech** • Requirements for inverter power modules • Power module for inverter design

Remaining Challenges and Barriers

- Accurate transient thermal impedance models for capacitors with unpublished material properties.

- Impact of higher DC bus voltage on the system insulation requirements needs to be evaluated.

Proposed Future Research

- **FY 2020**
  - Evaluate the impact of the direct-cooled bus bars on the DC bus capacitors in various power modules
  - Finalize a direct cooled DC bus bar design for use in an inverter porotype in FY2021

- **FY 2021**
  - Design a 100kW high voltage, segmented inverter using ORNL power modules
  - Evaluate the design against the DOE ELT 2025 targets
  - Build a prototype

Any proposed future work is subject to change based on funding levels

Summary

- **Relevance**: Reducing inverter DC bus components will remove some of the barriers in inverter designs to achieve the ELT 2025 targets of 100kW/L and 300,000 mile lifetime
- **Approach**: Develop inverter topologies, increase DC bus voltage, and investigate direct bus cooling to minimize the inverter DC bus design
- **Technical Accomplishments**:
  - Developed a driving cycle-based DC bus capacitor life-expectancy prediction and sizing tool in MATLAB
  - Developed capacitor transient thermal impedance models
  - Verified significant reductions with the segmented inverter in the DC bus capacitor ripple current and temperature over the EPA test cycles
  - Completed a direct-cooled bus bar design
- **Collaborations and Coordination with Other Institutions**:
  - **NREL**: On-going discussions on inverter thermal management
  - **Virginia Tech**: Discussions on inverter power module designs
- **Future Work**:
  - Design a 100kW high voltage, segmented inverter using ORNL power modules
  - Evaluate the design to identify gaps (if any) against the DOE ELT 2025 targets
  - Refine the design, build, and test a prototype

Any proposed future work is subject to change based on funding levels