

High-Dielectric-Constant Capacitors for Power Electronic Systems*

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Project ID# APE-008

***Work supported by the U.S. Department of Energy, Vehicle Technologies Program.**

Overview

Timeline

- Project start date: FY05
- Project end date: FY13
- Project continuation & direction determined annually by DOE
- Percent complete: 75

Budget

- Total project funding
 - DOE share: 100%
- Funding received in FY11: \$2050K
- Funding for FY12: \$1950K

Barriers addressed

- **A & C (Cost & Weight): Overall size and cost of inverters**
Capacitors are a significant fraction of the inverter volume ($\approx 35\%$), weight ($\approx 23\%$), and cost ($\approx 23\%$).
- **D (Performance & Lifetime): High-temperature operation**
The performance and lifetime of presently available capacitors degrade rapidly with increasing temperature (ripple current capability decreases with temperature increase from 85°C to 105°C).

Partners

- Penn State University
- Delphi Electronics
- Project Lead: Argonne National Laboratory

Relevance - Objectives

- **Overall objective:** Develop technology for fabricating high performance, economical, ceramic dielectric capacitors for power electronic systems in electric drive vehicles. The purpose is to build and test a capacitor prototype capable of operating at 140°C at 450 V.

DC bus capacitors for inverters (DOE-APEEM Goals)

- (450 V, 1000 μ F, <3 m Ω ESR, < 5 nH ESL, 100 A ripple current, 140°C, benign failure)

- **Specific objective for March '11 – March '12:** Advance the proven laboratory scale technology to produce high-voltage capable dielectric films on Ni foils (“film-on-foils”) that will have the potential, upon scale-up, to meet DOE-APEEM goals.
- The dielectric films will have:
 - An operational temperature range of -50°C to +140°C
 - 450 V DC bus capability (peak transient 650 V)
 - High k (>100) under bias voltage of 450 V and breakdown strength (\approx 200 V/ μ m, i.e., \approx 2 MV/cm) to meet weight & volume target

Relevance to Overall DOE Objectives of Petroleum Displacement

- Future availability of advanced high-temperature (together with lower cost, weight, & volume) inverters will advance the marketplace application of highly fuel-efficient & environmentally beneficial electric drive vehicles.
- Current polymer capacitors have temperature limitation.
- Capacitors have direct impact on overall size, cost, & performance of inverters.

This project is developing dielectric films that, due to their increased capacitance density & better capability for high temperature operation, have potential to reduce the size, weight, and cost of capacitors in inverters (addressing barriers A, C, & D).

Milestones

Month/Year	Milestones or Go/No-Go Decision	Progress Notes
Sept. 2011	Fabricate high-voltage-capable film-on-foils with high breakdown strength.	Fabricated $\approx 3\text{-}\mu\text{m}$ -thick dielectric film with $k \approx 110$ & loss ≈ 0.004 (i.e., 0.4%) @ 300 V bias at room temperature (Slide 9).
Sept. 2012	Fabricate a high-voltage-capable, multilayer capacitor with end-termination.	Fabricated a 10 μF multilayer capacitor (unbiased) and $\approx 3.5 \mu\text{F}$ at 54 V bias with end termination by stacking film-on-foils with Cu end termination (Slide 10).
Dec. 2012	Identify fabrication methodology to improve dielectric properties and reduce capacitor cost.	Fabricated PLZT films with thin TiO_2 insertion layers that doubled the breakdown voltage and decreased the loss by $\approx 50\%$. Process needs optimization (Slide 12). Effort to prepare sub-micron size PLZT powder is on-going. Sub-micron size powders are essential for the success of developing very fast film deposition processes.

Technical Approach/Strategy

- Our approach is to develop high-dielectric-constant, high-temperature ceramic (Pb-La-Zr-Ti-O, PLZT) films on base-metal foils (“film-on-foil”) that are either stacked on or embedded directly into the PWBs.
 - PLZT possess high dielectric constants, breakdown fields, and insulation resistance. With their ability to withstand high temperatures, they can tolerate high ripple currents at under-the-hood conditions.
 - Integration of base-metal (Ni, Cu) electrodes provides a significant cost advantage over noble metal electrodes.
 - Stacked and/or embedded capacitors significantly reduce component footprint, improve device performance, provide greater design flexibility, achieve high degree of volumetric efficiency with less weight, and offer an economic advantage.

Argonne’s project addresses the technology gap in an innovative manner

Uniqueness of Project and Impact

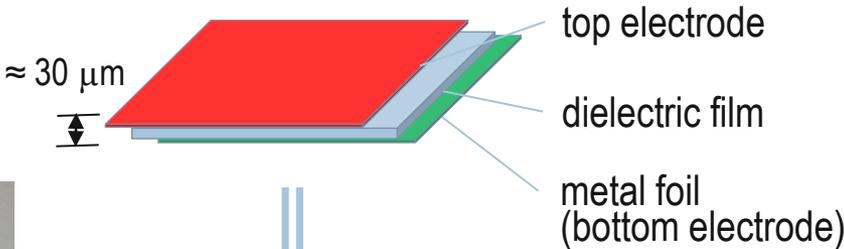
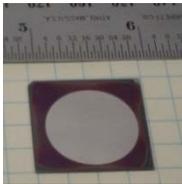
(caps embedded directly into PWB – caps are “invisible”)

Basic Element

Metal foil coated with thin film Pb-La-Zr-Ti-Oxide (PLZT) dielectric

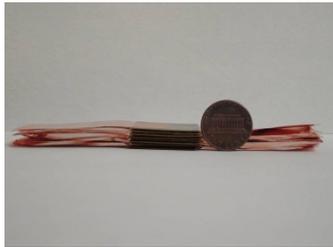
- PLZT/Ni Film-on-Foil
- PLZT/Cu Film-on-Foil

Film-on-foil capacitor (FoF)

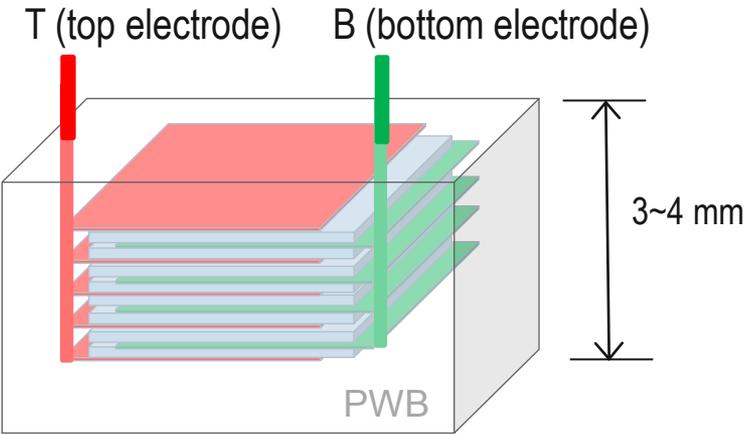


Component

Stack on or embed coated foils directly into printed wire board for power electronics in EDVs



Stack of 8 FoFs



Advantages

- Reduces component footprint
- Shortens interconnect lengths
- Reduces parasitic inductive losses & electromagnetic interference

PWB Embedded capacitor with interconnections

Reliability is improved because the number & size of interconnections are reduced. Solder joints that are most susceptible to failure are no longer needed.

Technical Accomplishments & Progress

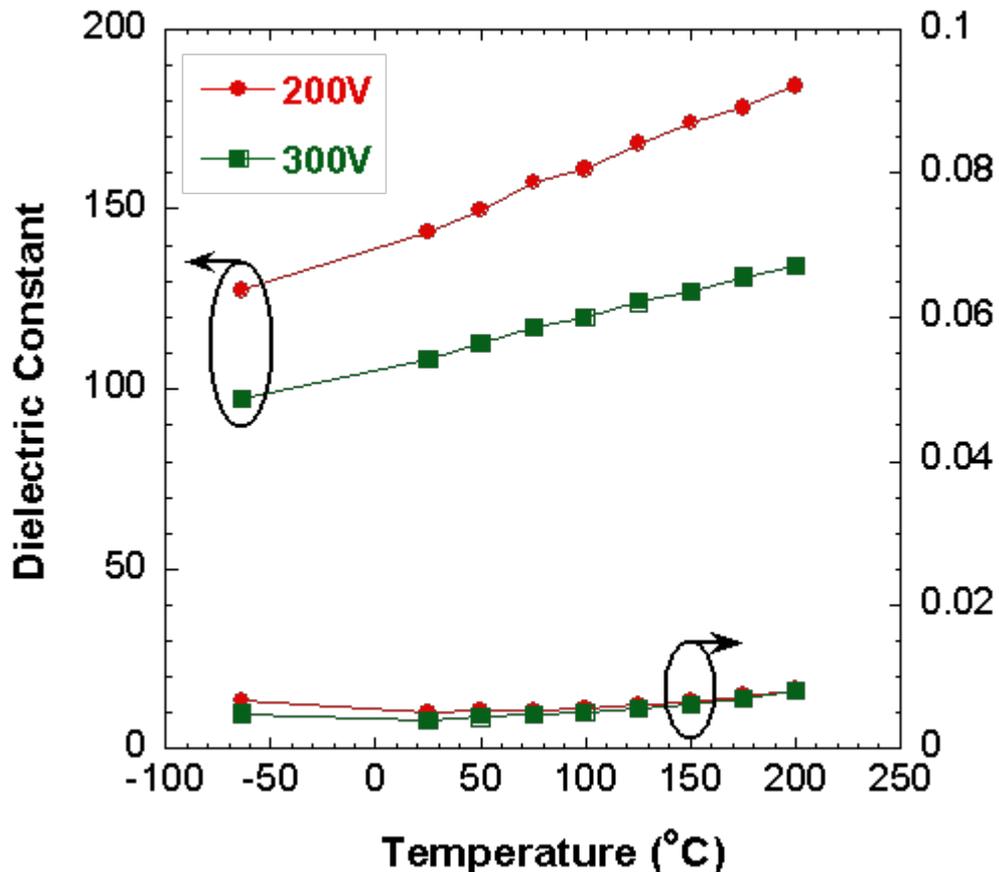
- Measured $k \approx 110$ & loss ≈ 0.004 (0.4%) at 300 V bias on a ≈ 3.0 μm -thick film (for comparison, k of polymer films are ≈ 5).
- Fabricated a 20-mm diameter film-on-foil (PLZT thickness ≈ 0.7 μm) with capacitance of ≈ 3 μF at 15 V/ μm bias.
- Fabricated ≈ 10 μF capacitor (unbiased) by stacking 1" x 1" film-on-foils (capacitance density ≈ 4.3 $\mu\text{F}/\text{cm}^2$). Measured ≈ 3.5 μF at 54 V bias.
- Measured factor of two increase in breakdown strength and $\approx 50\%$ decrease in loss by inserting thin TiO_2 layers within PLZT film.
- Dielectric properties under bias (300 V) show an increase in k and decrease in loss with temperature increasing from -50 C to +150°C.
- Dielectric films are thermally cycled (about 1000 cycles) between -50°C and +150°C with no measurable degradation in k .
- Over 50 publications and presentations have been made. One patent was issued & four patent applications were filed.



Argonne's capacitor technology is recognized with a 2011 R&D 100 Award

Technical Accomplishments/Results (Contd.)

Temperature dependent properties - PLZT/Ni



Measured $k \approx 110$ & loss ≈ 0.004 (i.e., 0.4%) @ 10 kHz & 300 V bias at room temperature on a 3 μm thick PLZT on Ni-foil

ESR = $DF/2\pi fc$ (DF = loss factor; f = frequency; c = capacitance).

Calculated ESR for 1000 μF cap. based on measured material properties

Bias Voltage (V)	ESR @ -64°C (m Ω)	ESR @ RT (m Ω)	ESR @ 150°C (m Ω)
200	0.11	0.08	0.10
300	0.08	0.06	0.10

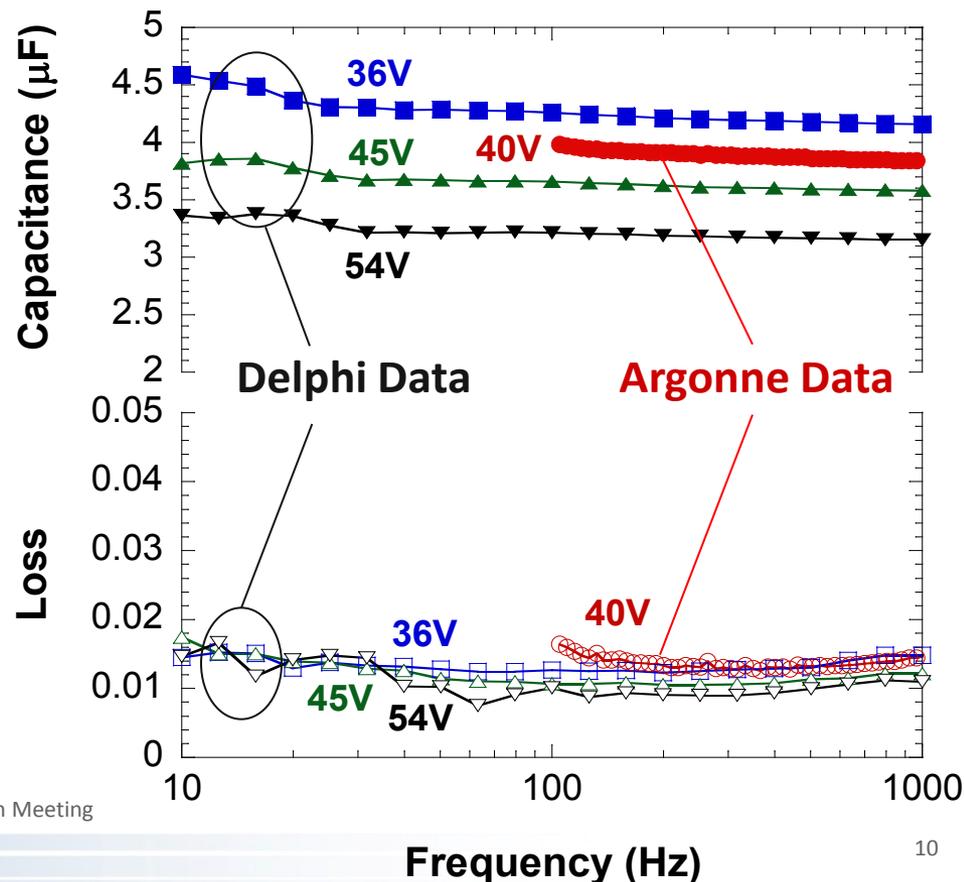
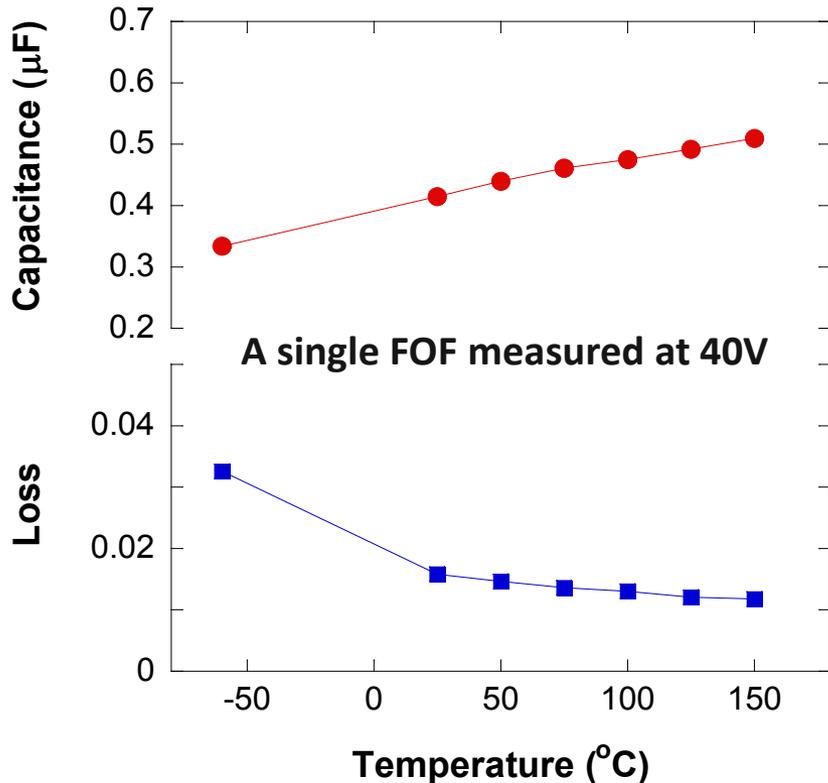
➤ DOE-VT DC Bus Capacitor Goal ≤ 3 m Ω

ANL's film-on-foil has high dielectric constant at high voltages and high-temperature capability

Technical Accomplishments/Results (Contd.)

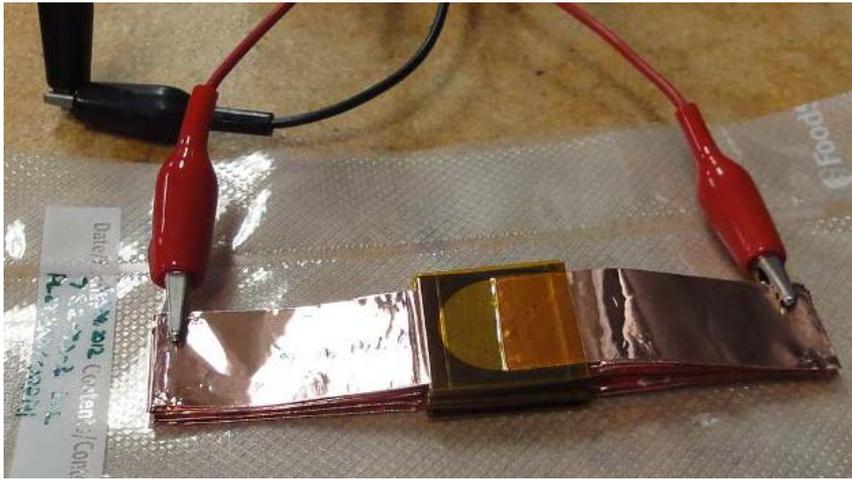
Prototype Multilayer Capacitor with Leads

- Fabricated a stacked capacitor with copper termination, measured capacitance $\approx 10 \mu\text{F}$ (cap. density $\approx 4.3 \mu\text{F}/\text{cm}^3$, unbiased), and capacitance $\approx 3.5 \mu\text{F}$ at 54 V
- Capacitor was tested at Delphi and confirmed our results



Technical Accomplishments/Results (Contd.)

Prototype Multilayer Capacitor with Leads



For the fabrication we used:

- Nine film-on-foils that were coated with 20-mm-dia. top electrodes
- Ni foil thickness $\approx 400 \mu\text{m}$
- PLZT film thickness $\approx 3 \mu\text{m}$
- Cu ribbons (thickness $\approx 80 \mu\text{m}$)

**Measured capacitance $\approx 3.5 \mu\text{F}$
@ 54 V bias (Cap. density $\approx 1.5 \mu\text{F}/\text{cm}^3$ using thick Ni & Cu ribbons and lots of gap between individual films)**

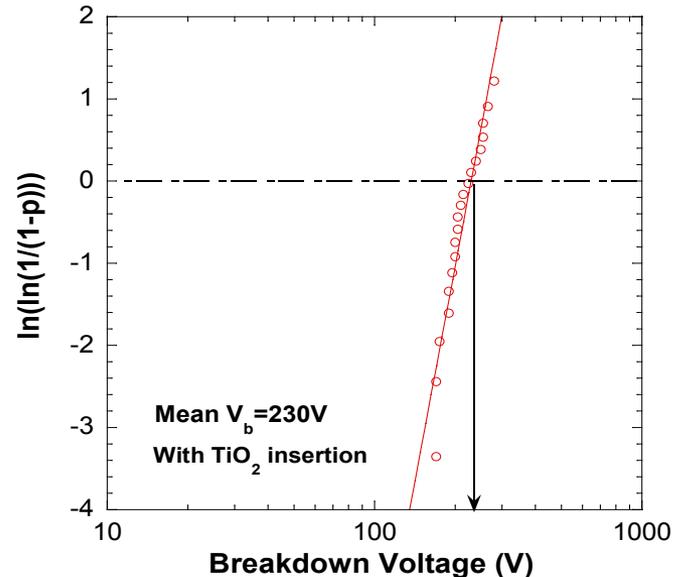
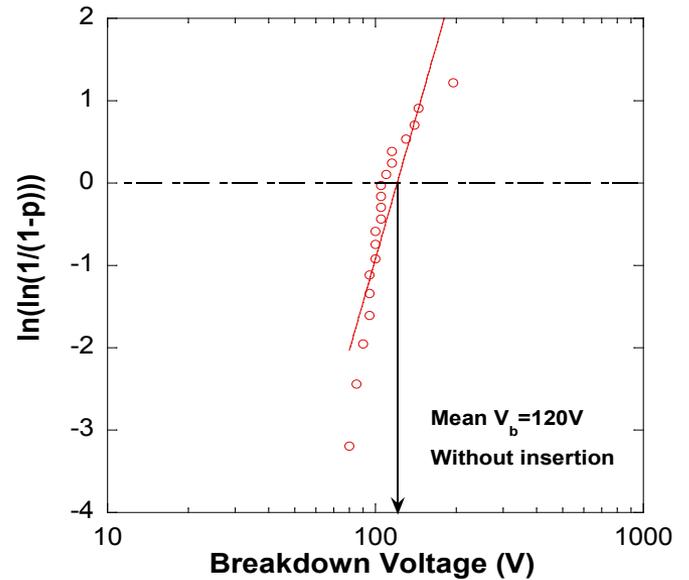
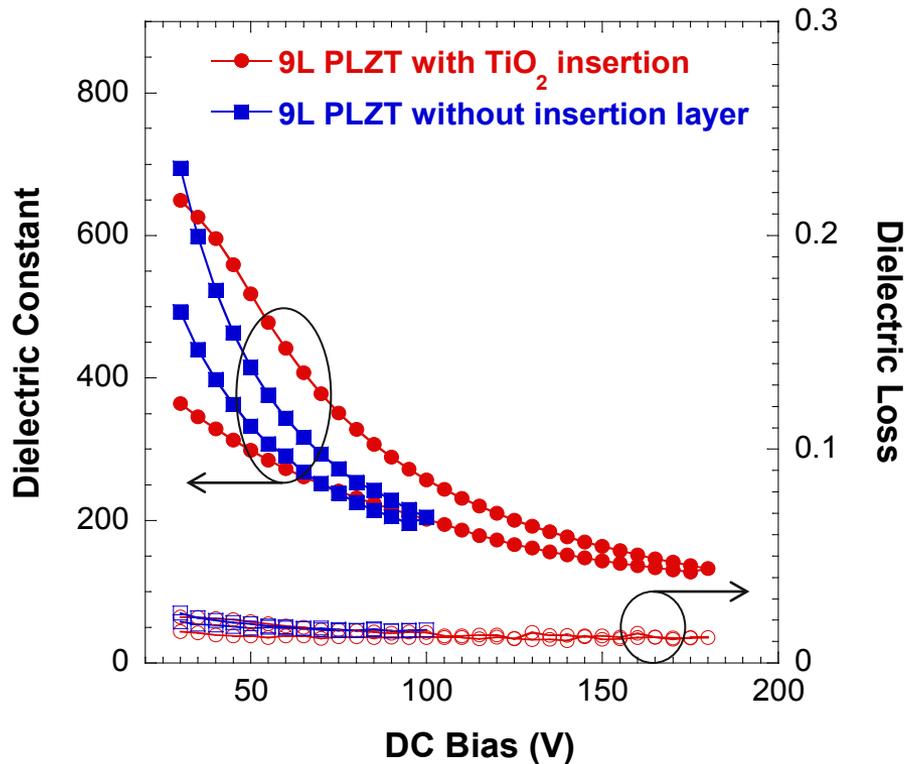
Calculation of the Volume of 1000 $\mu\text{F}/450 \text{ V}$ Cap:

- Volume will be $\approx 0.55 \text{ L}$ if $\approx 80 \mu\text{m}$ thick Ni foil & $\frac{1}{2}$ oz. Cu ribbon ($\approx 17 \mu\text{m}$) is used.
- DOE-VT DC Bus Capacitor Goal $\leq 0.6 \text{ L}$
- Volume and capacitance of current polymer film capacitor module/housing in Camry $\approx 2.6 \text{ L}$ (2,098 μF), Lexus LS 600h $\approx 4.0 \text{ L}$ (2,629 μF) & 2010 Prius $\approx 2.0 \text{ L}$ (888 μF). Ref: ORNL/TM-2007/190, ORNL/TM-2008/185, & ORNL/TM-2010/253 reports.

ANL film-on-foils have potential to meet volumetric target

Technical Accomplishments/Results (Contd.)

Enhancement of dielectric properties via superstructure film growth



- Measured Improved dielectric properties with insertion of thin intermediate layers
 - 2X improvement in breakdown strength
 - $\approx 50\%$ decrease in loss

Collaboration and coordination with other institutions



Dielectric characterization, reliability testing, electrode design & deposition, defining capacitor specifications & test protocol for APEEM



Industry partner/CRADA, inverter design engineering (direct customer for the technology), stacking & connecting multilayer film-on-foils (Delphi works closely with a PWB manufacturer)



Electrode deposition, defining capacitor specifications & test protocol for APEEM



Strain tolerance of film-on-foils

Proposed Future Work

The primary emphasis of our future work is on advancing the proven laboratory scale film-on-foil technology and fabricating $\approx 10 \mu\text{F}$, high-voltage-capable (operating voltage of 450 V) capacitors.

- Produce high-voltage (450 V) capable PLZT film-on-foils
 - Optimize precursor solution chemistry [Polyvinylpyrrolidone (PVP)-modification] to adjust viscosity & increase critical per coating thickness due to structural relaxation
 - Incorporate superstructure film growth process (insertion of thin TiO_2 , ZrO_2 , HfO_2 layers) to improve dielectric properties
- Develop fabrication methodology to reduce capacitor cost
 - Develop process for making sub-micron PLZT powders
 - Fabricate PLZT films by processes at rates much faster than obtained from current spin coating method (colloidal spray & aerosol deposition, screen printing)

Proposed Future Work (Contd.)

- Develop electrode architecture for carrying large currents and provide graceful failure in large-area PLZT films
 - Evaluate effects of electrode material, size, shape, and thickness on capacitor performance
 - Adopt segmented electrode architecture to overcome charge accumulation
- Fabricate & test multilayer capacitors and provide samples to partners for testing/validation of results
 - In collaboration with partners, results will be analyzed and course of action will be determined

Summary

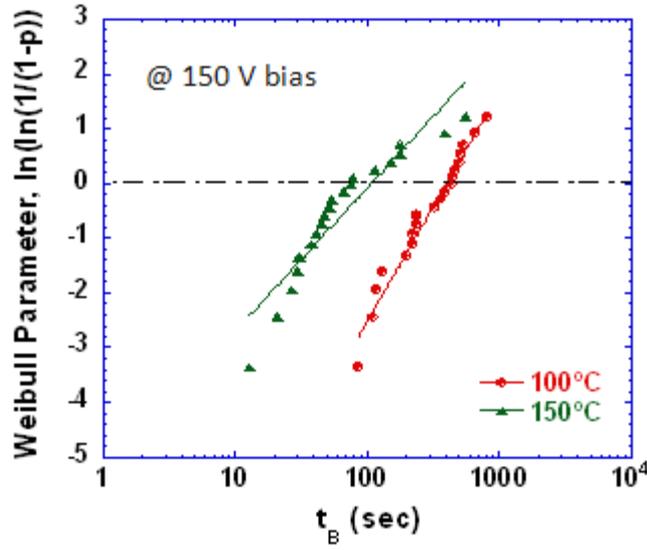
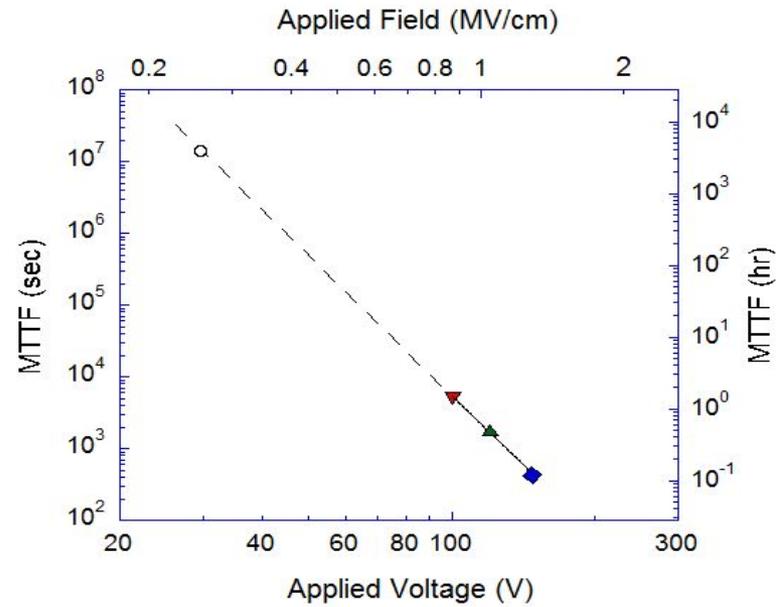
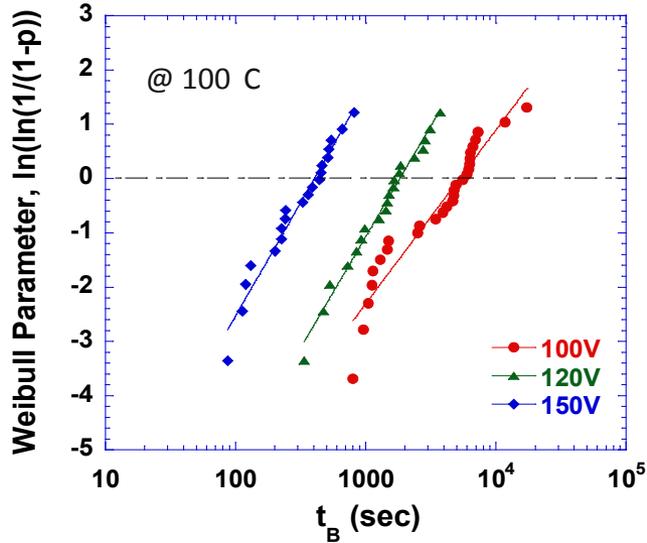
We are developing dielectric films with increased capacitance density & capability for high temperature operation that have potential to reduce the size, weight, and cost of capacitors in inverters in electric drive vehicles.

- Made PLZT films with $k \approx 110$ & loss ≈ 0.004 (0.4%) under 300 V bias; breakdown field ≈ 270 V/ μm .
- Fabricated ≈ 10 μF capacitor (unbiased) with end-termination, cap. density ≈ 4.3 $\mu\text{F}/\text{cm}^3$, and measured capacitance ≈ 3.5 μF at 54 V bias.
- Based on measured properties, there is no decrease in ripple current capability up to ≈ 200 $\hat{\text{O}}$.
- Improved dielectric properties are measured in PLZT films with thin TiO_2 insertion layers.
- Based on measured values at 300 V, the volume of a 1000 $\mu\text{F}/450$ V capacitor will be 0.55 L (DOE-OVT goal ≤ 0.6 L).
- Collaborating with partners to overcome the barriers of this technology for inverter application and to commercialize the technology.

Technical Back-up Slides



HALT Analysis on PLZT/LNO/Ni Films

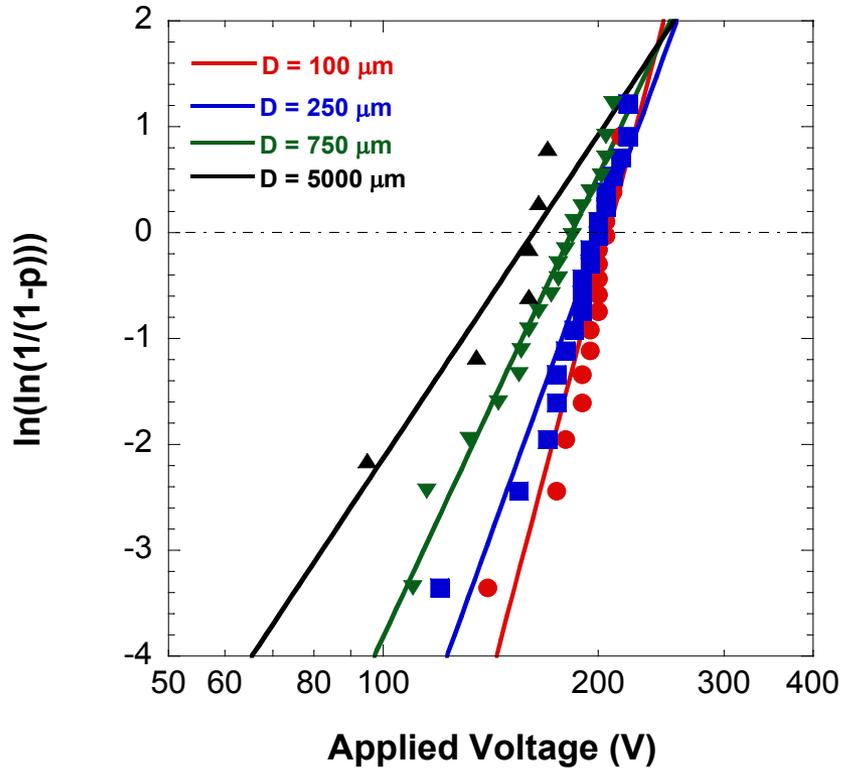


$$t = C \cdot V^N \exp\left(\frac{E_a}{k_B \cdot T}\right)$$

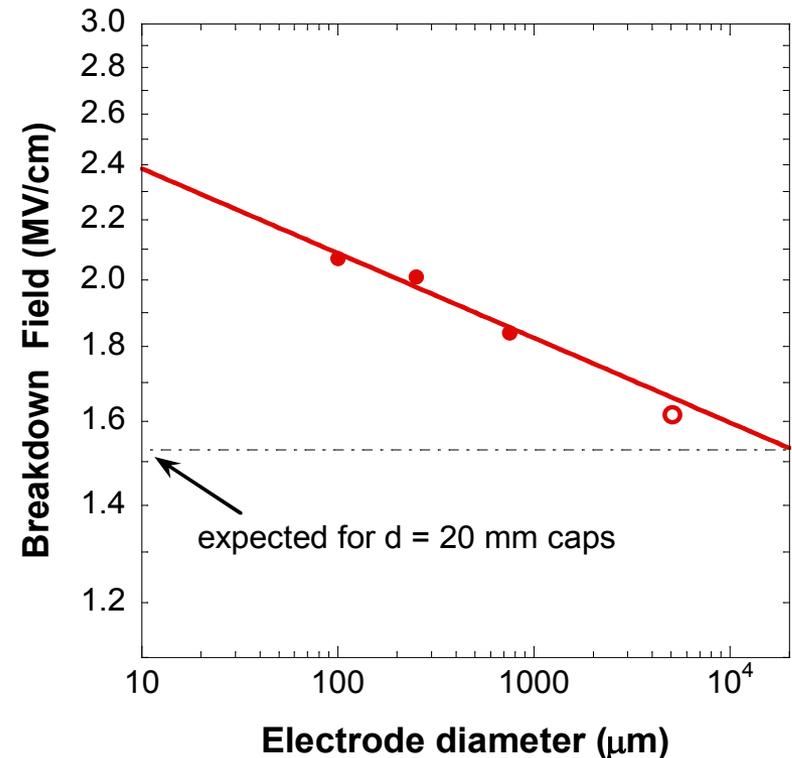
- Lifetime estimated by measuring time to failure vs. applied voltage as function of temperature.
- Mean time-to-failure (MTF), voltage acceleration factor (N), and activation energy (E_a) are obtained from reliability measurement.



Breakdown Strength of PLZT/LNO/Ni Films



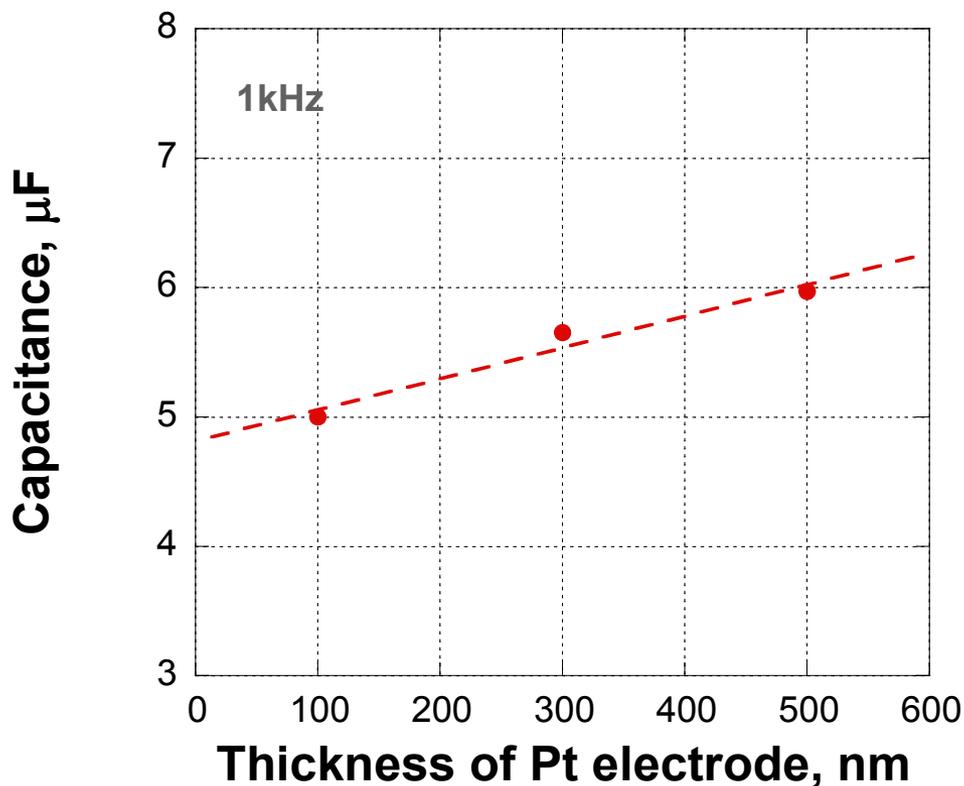
- Breakdown strength was measured on capacitors of various electrode sizes.
- Extrapolated the data for prediction of breakdown strength of larger size capacitors.



$$\frac{E_{B1}}{E_{B2}} = C \cdot \left(\frac{A_2}{A_1} \right)^m \exp \left[\frac{E_a}{k_B} \cdot \left(\frac{1}{T_1} - \frac{1}{T_2} \right) \right]$$

Effect of Electrode Material & Thickness

(Pt electrode diameter: 20 mm)



Electrode	Thickness (nm)	Ω/\square
Pt	50	2.0
Pt	100	1.0
Pt	500	0.2
Al	50	0.5
Al	100	0.25
Al	500	0.05

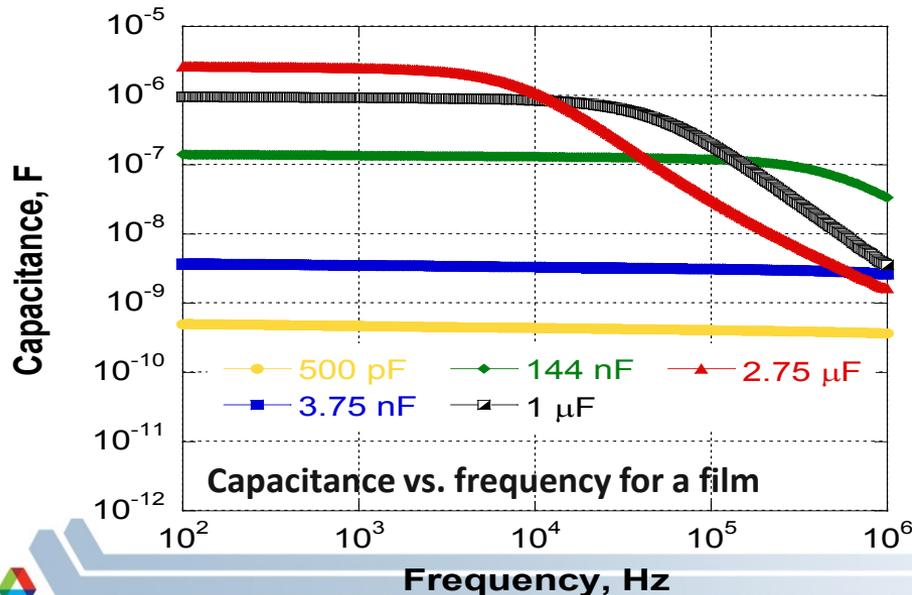
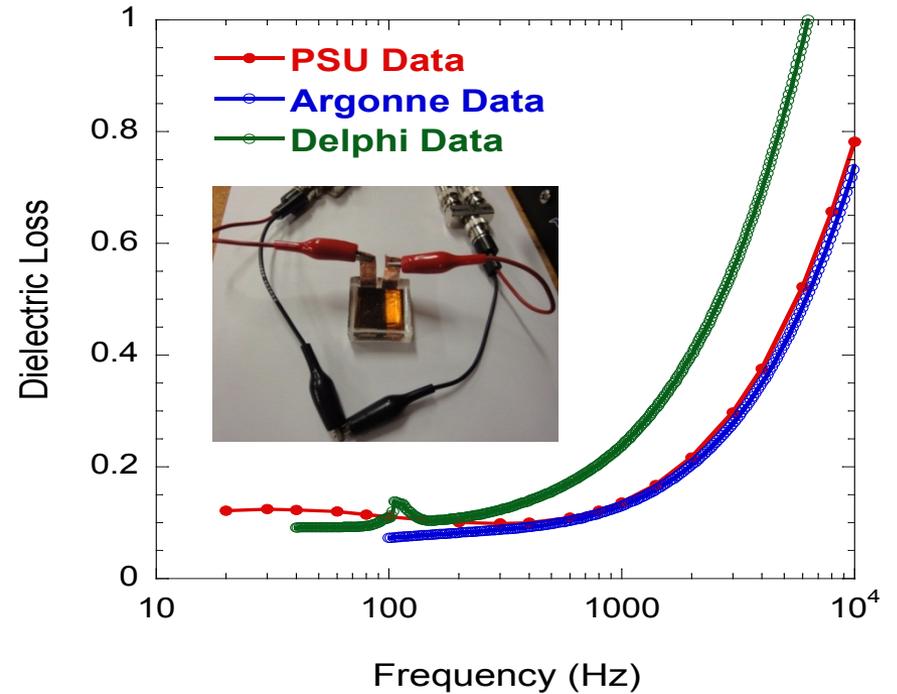
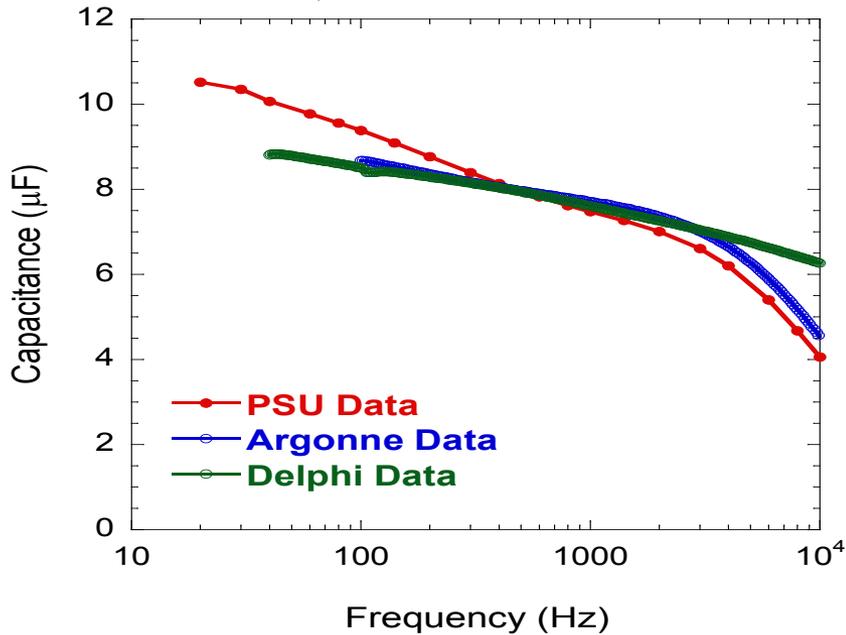
$$\rho \text{ of Pt} = 1.05 \times 10^{-7} \Omega\text{-m}$$

$$\rho \text{ of Al} = 2.82 \times 10^{-8} \Omega\text{-m}$$

- Electrodes should carry large currents and, at the same time, provide benign failure mode in multilayer architecture.
- Electrode surface resistivity is consistent with commercial polymer film capacitors carrying large ripple currents.

Stacked Capacitor Made Using Four Film-on-foils

(Characterized at ANL, Penn State, & Delphi)



Measurements made at Penn State & Delphi confirmed Argonne result