VIRGINIA TECH

CPES
Center for Power Electronics Systems

2020 DOE Vehicle Technologies Office Annual Merit Review

Heterogeneous Integration Technologies for High-Temperature, High-Density, Low-Profile Power Modules of Wide Bandgap Devices in Electric-Drive Applications

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Virginia Tech

Project ID: elt242

June 2nd, 2020

Overview

Timeline

- Project start date: April 1st, 2019
- Project end date: March 31st, 2024
- Percent complete: 20%

Budget

- Total project funding: $1.5 million
- Funding for FY 2019: $300 k
- Funding for FY 2020: $300 k

Barriers and Technical Targets

- **Materials:** high-performance bonding materials (Cu or Ag) and assembly technologies (planar, double-side cooling) for making high-temperature (> 200ºC) power modules to enable high converter power density (> 100 kW/L);
- **Gate Driver:** high-temperature (> 200ºC) intelligent gate driver with integrated current sensor;
- **EMI:** EMI mitigation solutions integrated in or on module substrates to enable high converter power density (> 100 kW/L).

Partners

- Virginia Tech - Lead
- Oak Ridge National Laboratory (ORNL)
- National Renewable Energy Laboratory (NREL)
- DOWA
- University of Arkansas

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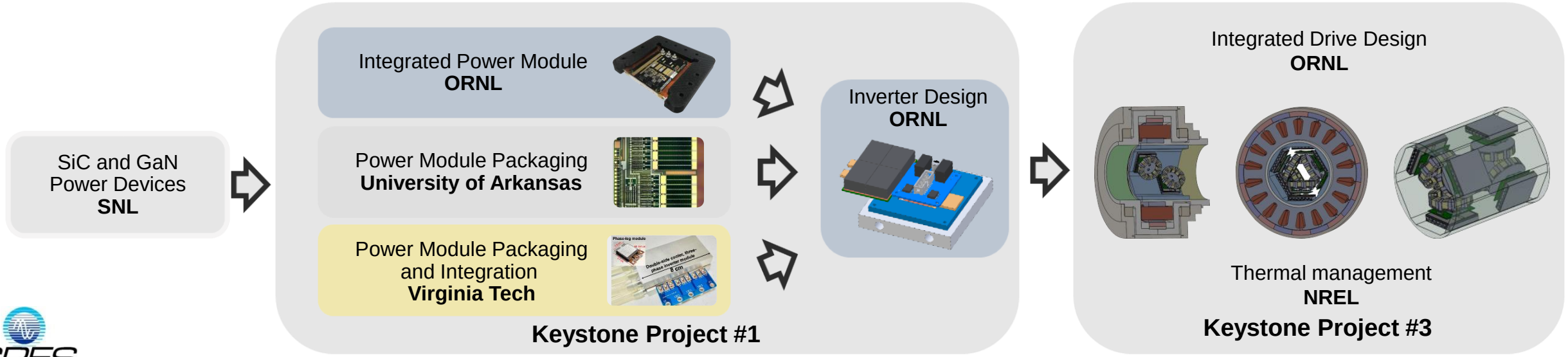
Relevance and Objectives

- **Goal**
  - ✓ Develop packaging materials, assembly processes, and circuit technologies for making WBG power modules with double-side cooling capability, intelligent gate driver, and integrated EMI mitigation solutions.
- **Impact**
  - ✓ Enable the EDT consortium to achieve its targets on performance, cost, power density, and reliability of a 100 kW traction drive system.
- **Overall Objectives**
  - ✓ Develop a low-cost sintered-metal (copper or silver) interconnect technology for working over 200°C;
  - ✓ Develop module designs and fabrication processes with parasitic inductances < 5 nH, heat flux density > 400 W/cm^2, and working junction temperature > 200°C;
  - ✓ Design intelligent gate driver with integrated current sensor and protection for 200°C module;
  - ✓ Design and embed EMI confinement solutions for 20 dB attenuation.
- **Objectives this period**
  - ✓ Coordinate tasks within the VT team and with partners;
  - ✓ Review the state-of-the-art high-temperature module-packaging, current-sensing, and gate-driver technologies;
  - ✓ Simulate, fabricate, and test designs of discrete power modules, current sensors, and gate drivers.



Milestones

Date	Milestones and Go/No-Go Decisions	Status
September 2019	Complete a survey of the state-of-the-art materials and processes for module packaging.	Done
October 2019	Complete an integrated EMI mitigation design and evaluation by simulation.	Done
December 2019	Complete analysis of the state-of-the-art passive materials, substrates, integrated and discrete electronic components, and ancillary components for making high-T gate drivers.	Done
March 2020	Complete a power module design with analyses of electrical, thermal, and thermo-mechanical variables.	Done
April 2020	**Go/No-Go decision:** **Complete one design of power module and one design of gate driver, capable of operation temperature > 200°C with power density > 15 kW/L**	Done
June 2020	Complete a quantitative analysis on effects of processing conditions and high-temperature aging on die-shear strength of the sintered-silver or sintered-copper bond.	On track
October 2020	Fabricate and test high-temperature gate driver with integrated current sensor.	On track
December 2020	Fabricate and test an EMI mitigation circuit integrated in module package.	On track
March 2021	Complete and test a half-bridge power module consisting of four SiC MOSFETs.	
April 2021	**Go/No-Go decision:** **Demonstrate processing feasibility with at least 50% yield for making the planar power modules, gate drivers with current sensors, and EMI mitigation circuit.**	

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Approach

- Survey the literature on the state-of-the-art high-temperature materials, components, and packaging technologies for power switching cells, gate drivers and their power supplies, passive components, and current sensors;
- Establish interconnect material processing (*P, T, t, atm*) and property (σ, Z_{th}) relationships;
- Build structural models of planar modules and simulate distributions of v, i, fields, temperature, and thermo-mechanical stresses to down-select one or two designs for fabrication;
- Design and simulate gate drivers and sensors; select and evaluate high-temperature components; fabricate and test;
- Design and simulate EMI reduction circuits; select and evaluate components; fabricate and test.

Accomplishments - Survey Results on High Temperature Packaging Materials

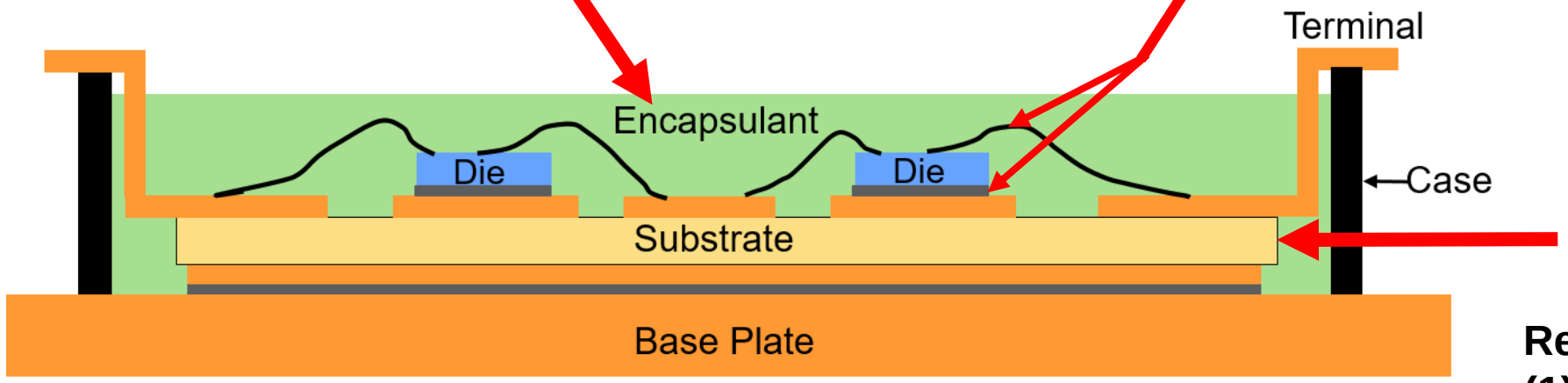
Interconnect
(bond wire and die attach)

Recommendations:

Die attach	Bond wire	Substrate metallization	Die top metallization
Sintered Ag	Al	Ag	Al

Encapsulant

Recommendations:
Organic: silicone, polyimide
Inorganic: lead glass



Substrate

Recommendations:
(1) Si_3N_4 AMB substrate
(2) AlN DBA substrate
with dimples or stepped edge

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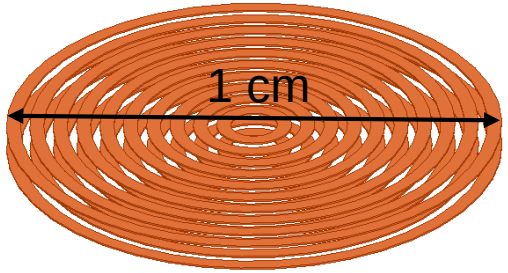
Accomplishments - Survey of High Temperature Components

➢ High temperature gate driver:

- Cissoid chip rated to 175ºC
- Output peak current: 9A at 175ºC
- Propagation delay: 160 ns
- Common mode transient immunity: > 50 kV/ms

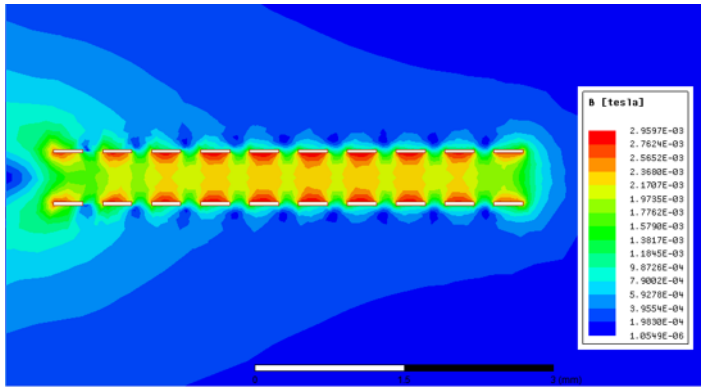
➢ High temperature magnetics:

- Air-core transformers and inductors with PCB winding



Parameter	Value
L	113 nH
M	86 nH

Simulated PCB air-core transformer



Simulated field distribution of PCB air-core transformer

➢ High temperature resistors:

Resistor type	Packaging	Max. Temperature
Metal foil	Through-hole, surface-mount-device (SMD)-chip, flip-chip	240ºC
Metal oxide	Through-hole	275ºC
Thin film	SMD-chip, flip-chip	275ºC
Thick film	SMD-chip, flip-chip	300ºC
Wire-wound	Through-hole	350ºC

➢ High temperature capacitors:

Capacitor type	Max. Temperature	Comments
Tantalum	230ºC	High capacitance value; voltage rating degradation at high temperature
X7R	250ºC	High capacitance value; degraded capacitance above 175ºC
C0G	250ºC	Stable capacitance; Lower capacitance value

✓ **Finished survey of high temperature components and preliminary study of air-core transformer.**

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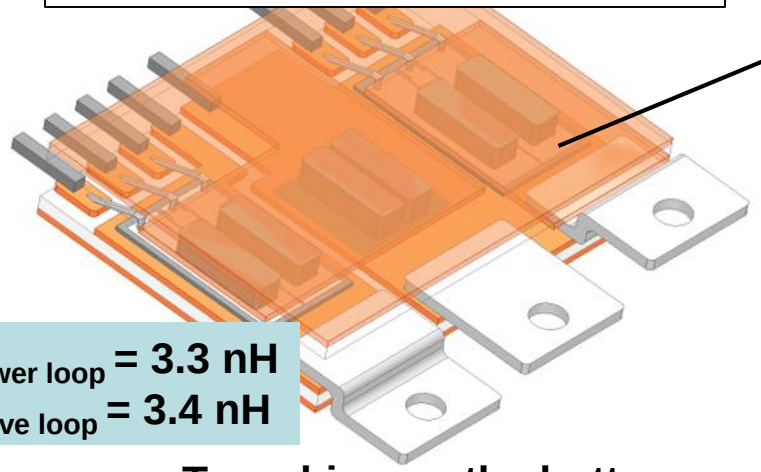
Accomplishments - Layout Designs and Assembly of a Phase-leg SiC Module

Design #1: 27*19*3.6 mm^3



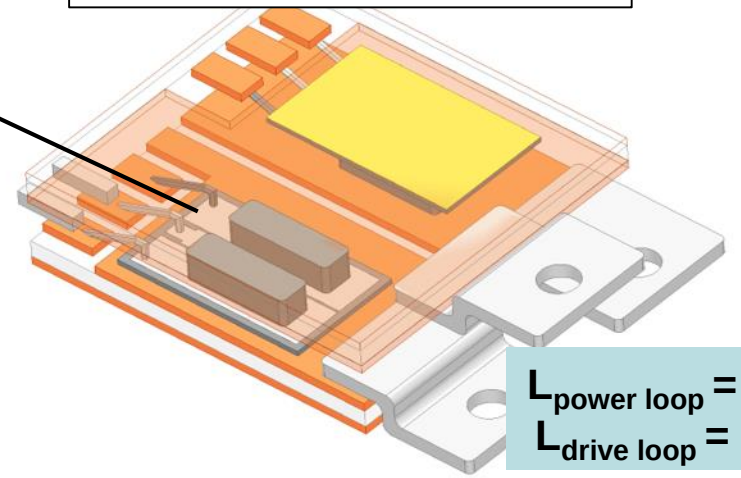
$L_{power\ loop}$ = 3.3 nH
$L_{drive\ loop}$ = 3.4 nH

- Two chips on the bottom

- Serial #: CPM3-1200-0013A
- 1200 V, 149 A, 13 mΩ

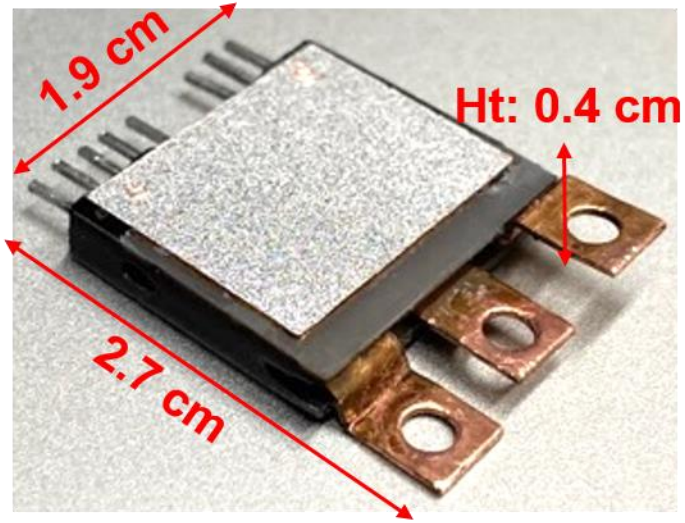
Key features:
- ✓ Sintered Ag joints;
- ✓ Double-side cooling;
- ✓ High density and low profile.

Design #2: 13*19*3.6 mm^3

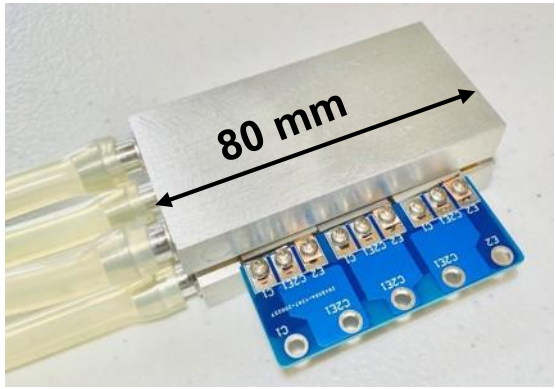


$L_{power\ loop}$ = 2.2 nH
$L_{drive\ loop}$ = 3.4 nH

- One chip on the top, the other on the bottom



A phase-leg module assembly of Design #1



A double-side cooled three-phase inverter: three of the phase-leg modules shown on the left are sandwiched between two water-cooling plates.

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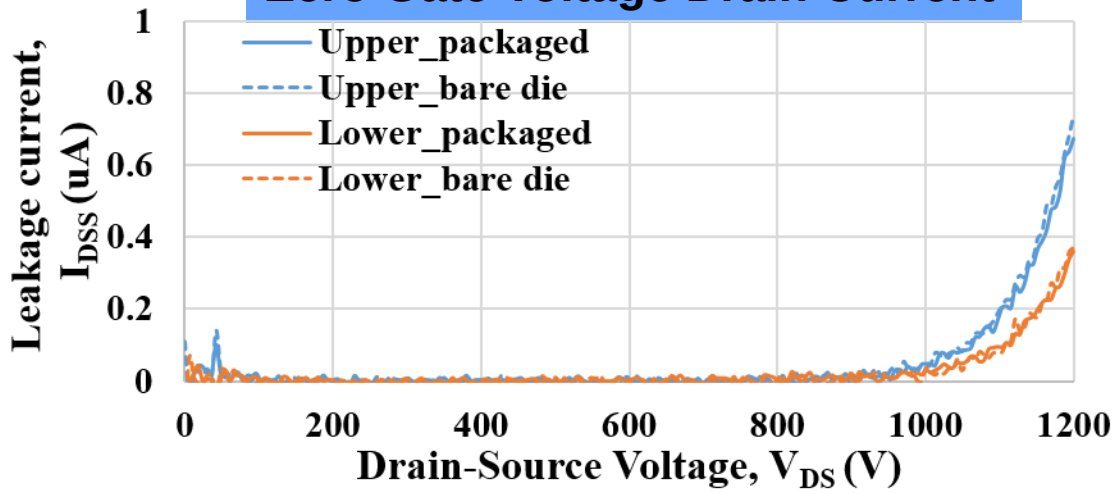
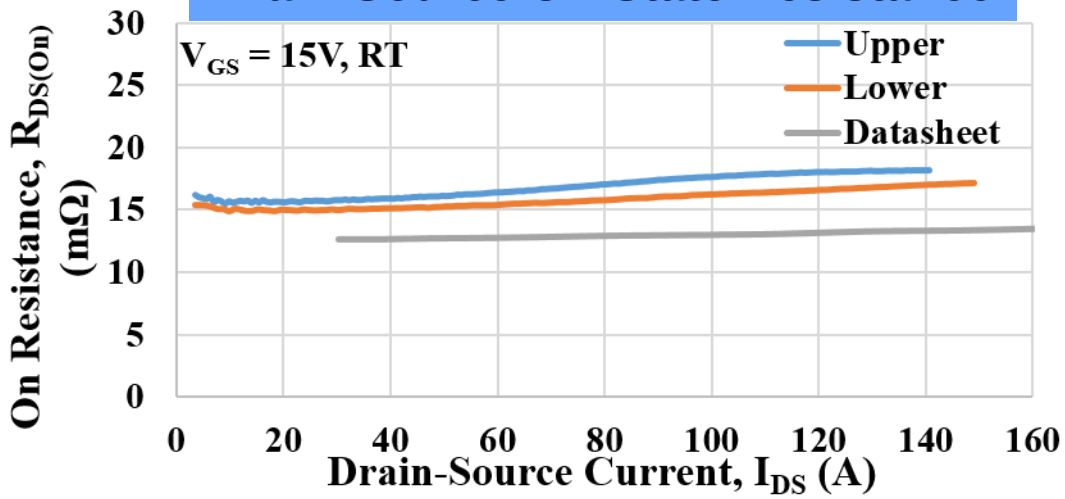
Accomplishments - Static Characterization of a Phase-leg Module

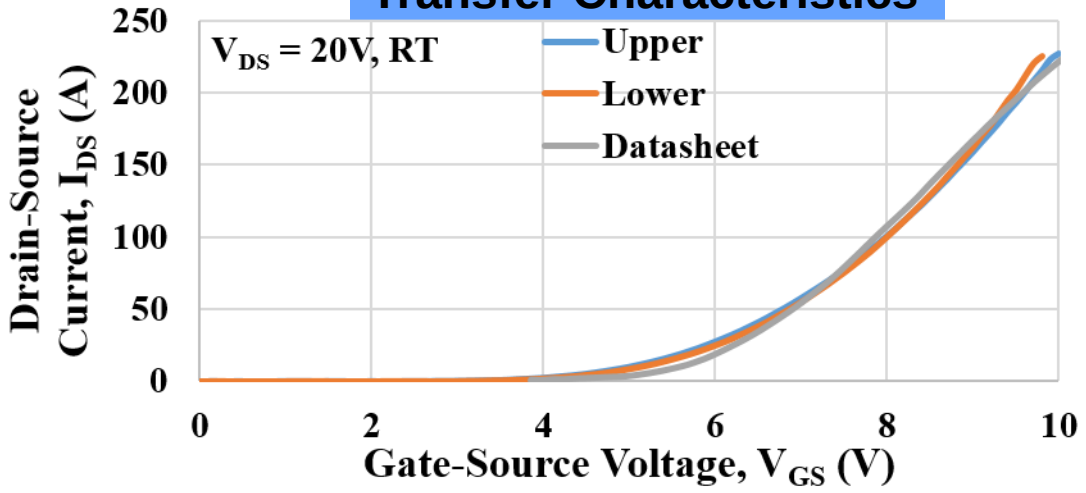
Zero Gate Voltage Drain Current



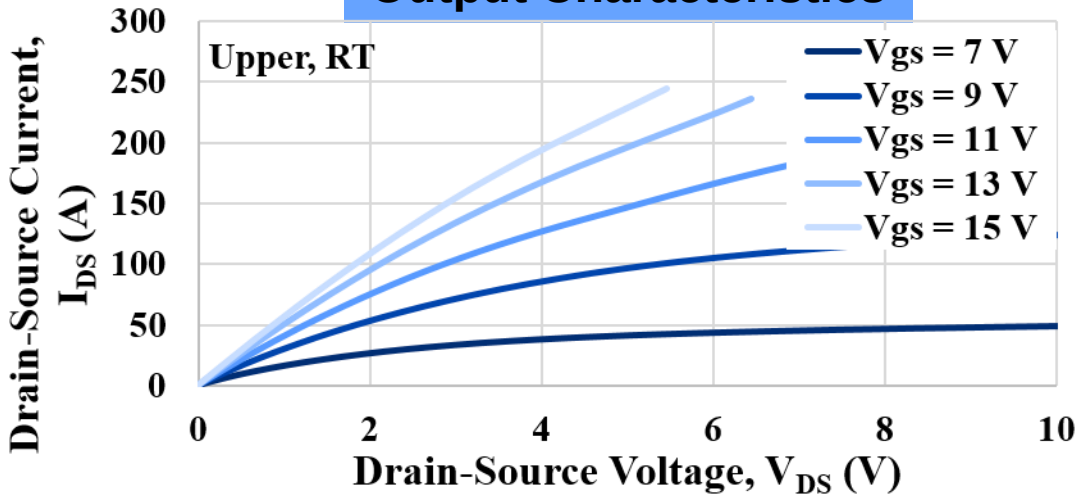
Drain-Source On-State Resistance



Transfer Characteristics



Output Characteristics



✓ The static characteristics of the as-fabricated module are similar to those in the datasheet.

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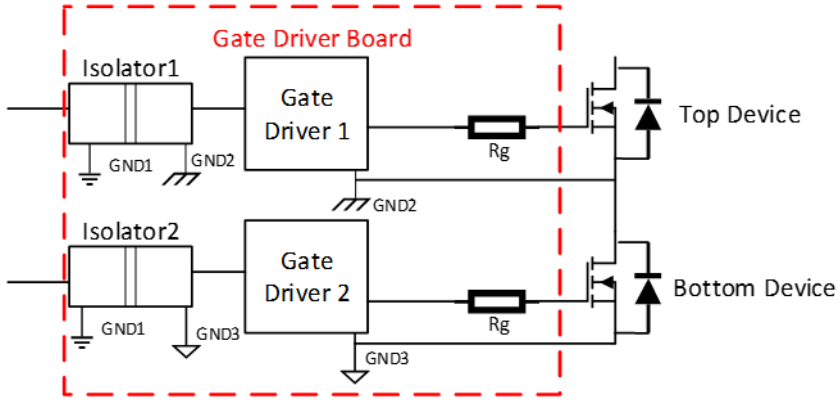
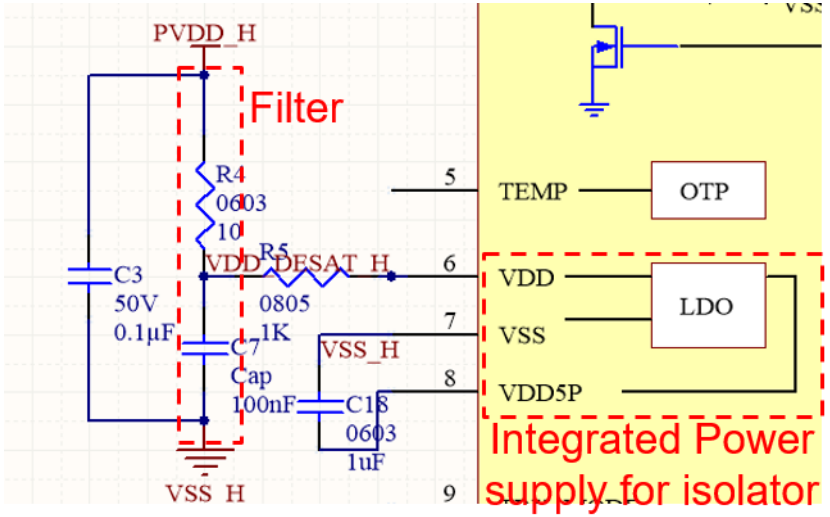
Accomplishments - Preliminary Test of a High-Temperature Gate Driver

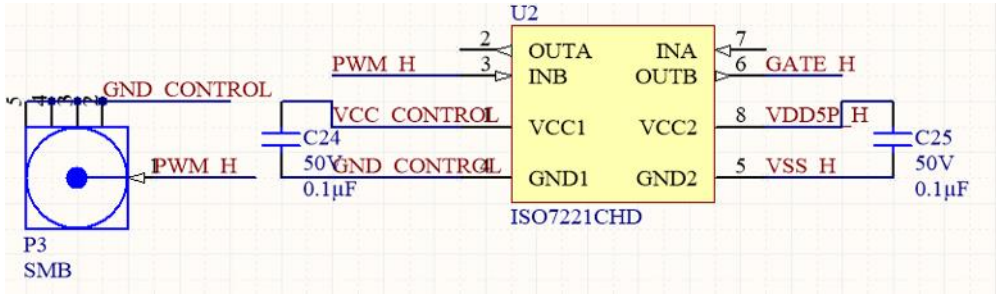
- **Gate driver board structure:**



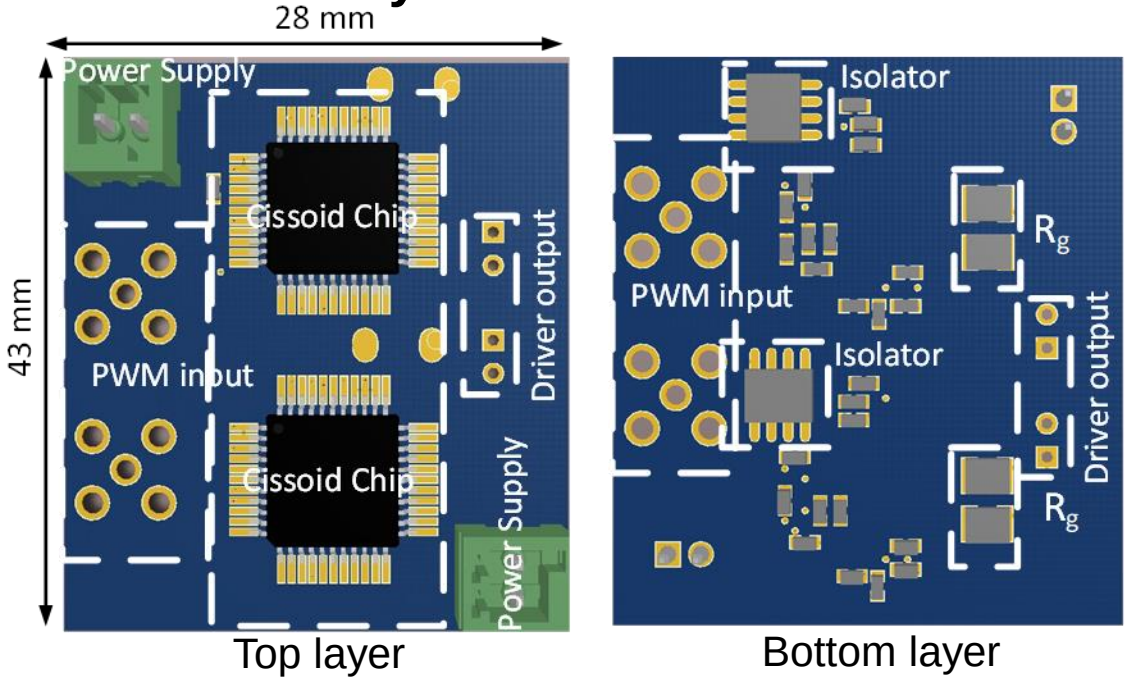
- **Power management circuit:**



- **PWM input circuit with digital isolator:**



- **Final PCB layout:**



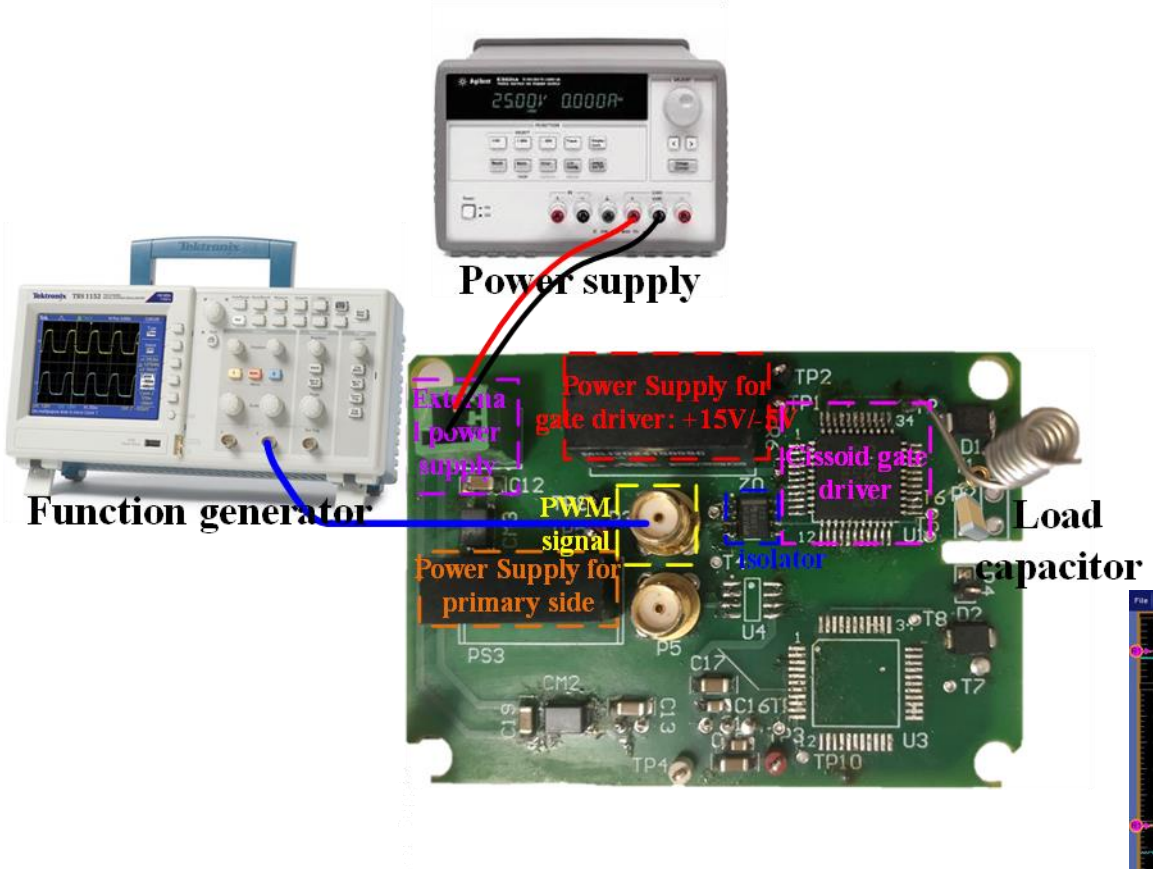
Top layer

Bottom layer

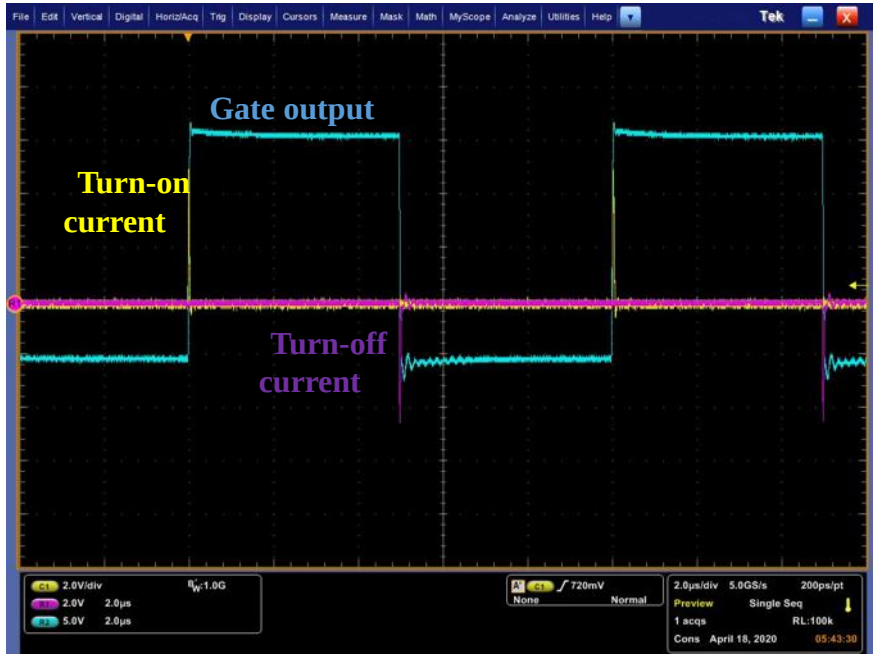
✓ **Completed a gate-driver board design for proof-of-concept testing.**

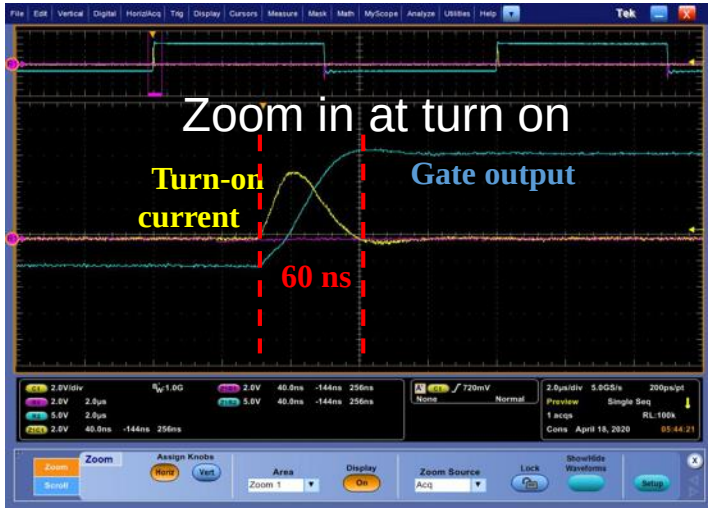
Accomplishments - Gate Driver Board and Testing Results

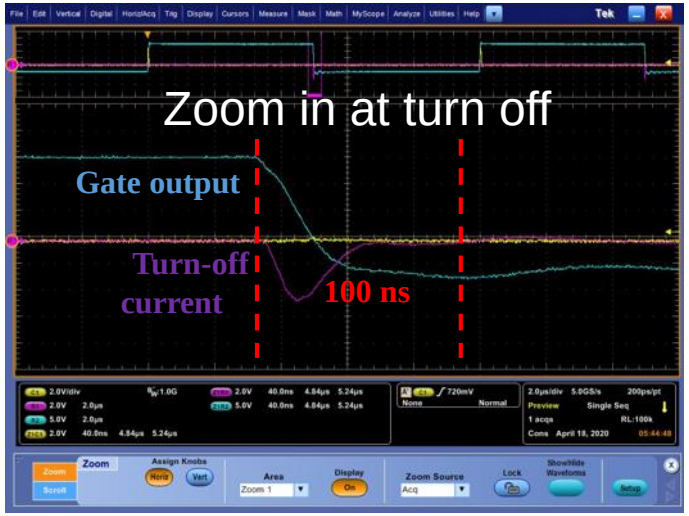
- **Gate driver board with on-board power supplies:**



- **Testing waveforms:**







- ✓ **Gate driver board's function has been verified.**

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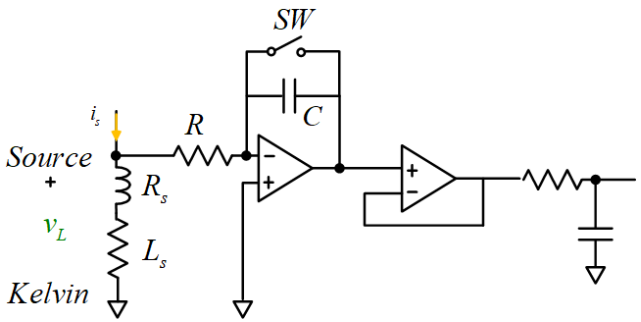
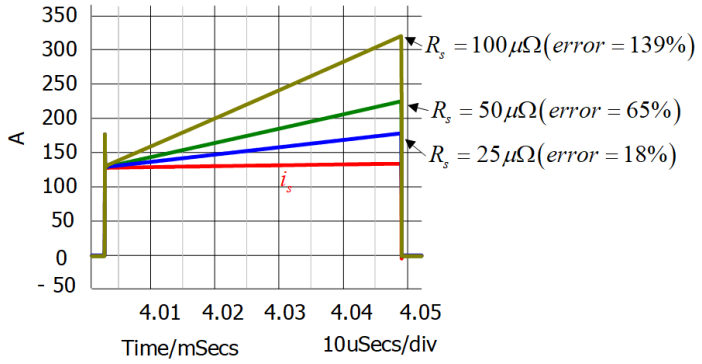
Accomplishments - Current Sensor Scheme with Feedback

- **Effect of the parasitic resistance and compensation algorithm:**

Basic current sensor

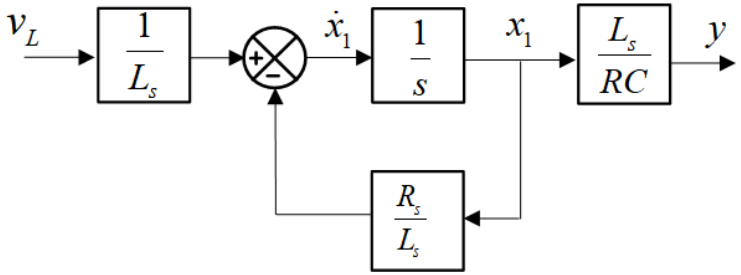


Effect of parasitic resistance



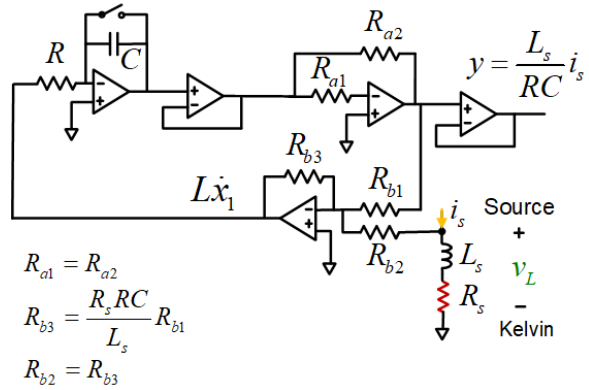
State space model of the compensation algorithm

$$\begin{cases} \dot{x_1} = -\dfrac{R_s}{L_s}x_1 + \dfrac{1}{L_s}v_L \\ y = \dfrac{L_s}{RC}x_1 \end{cases}$$

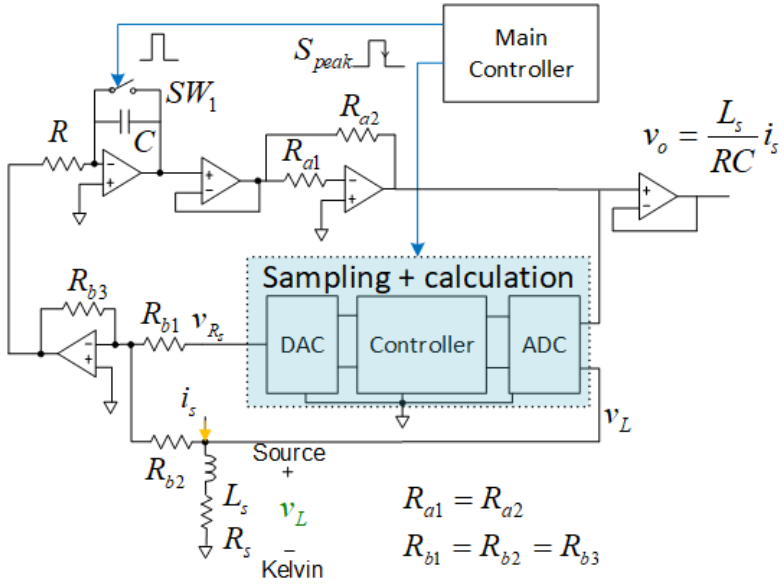


- **Implementation of the compensation method:**

Proposed 1: Current sensor with feedback

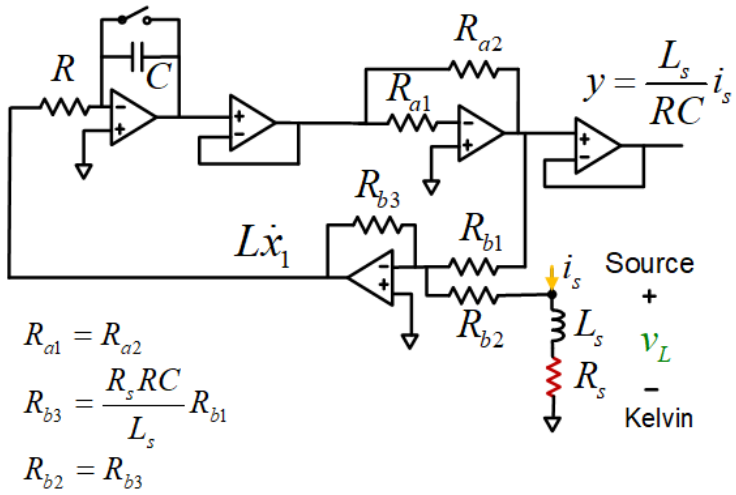


Proposed 2: Current sensor with feedback + online identification of the parasitic resistance

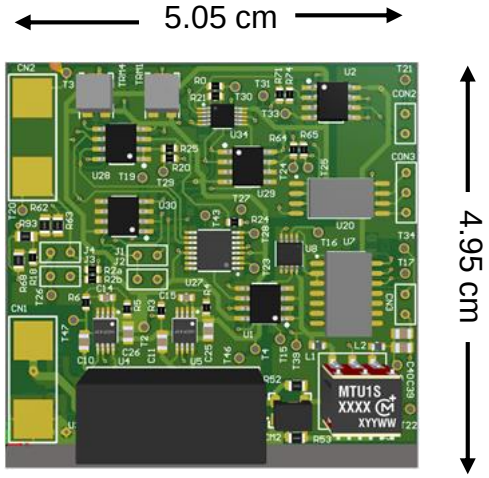


Accomplishments - Design of the Current Sensor

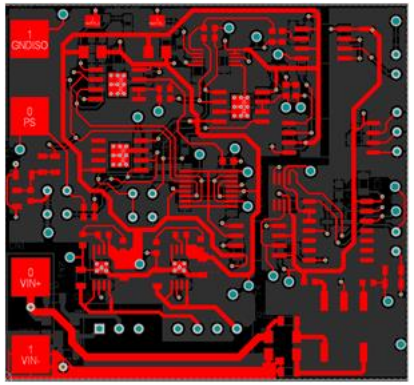
➢ Sensor current with feedback (Proposed 1):



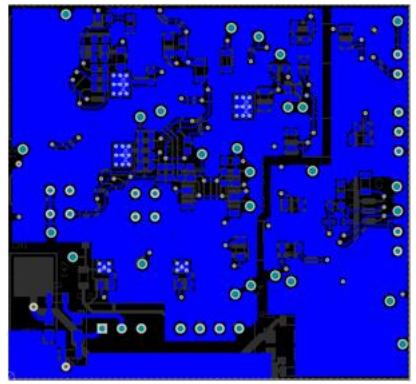
➢ PCB design (2 layers):



Top



Bottom



➢ Main components:

Component	Description	Manufacturer
RS-2409DZ/H3	Isolated DC/DC Converters 2W 9-36VIN ±12VOUT	RECOM
TPS7A4901	Ultralow-Noise, Positive Linear Regulator, 3-36VIN	Texas Instruments
TPS7A3001	Ultralow-Noise, Negative Linear Regulator, 3-36VIN	Texas Instruments
LMH6612	Single Supply 345 MHz Rail-to-Rail Output Amplifiers	Texas Instruments
DG201HSDQ	High-Speed Quad SPST CMOS Analog Switch	Vishay

- **The designed sensor will be tested on commercial power MOSFET;**
- **Input is the Kelvin-source voltage and output is the measured switching current.**

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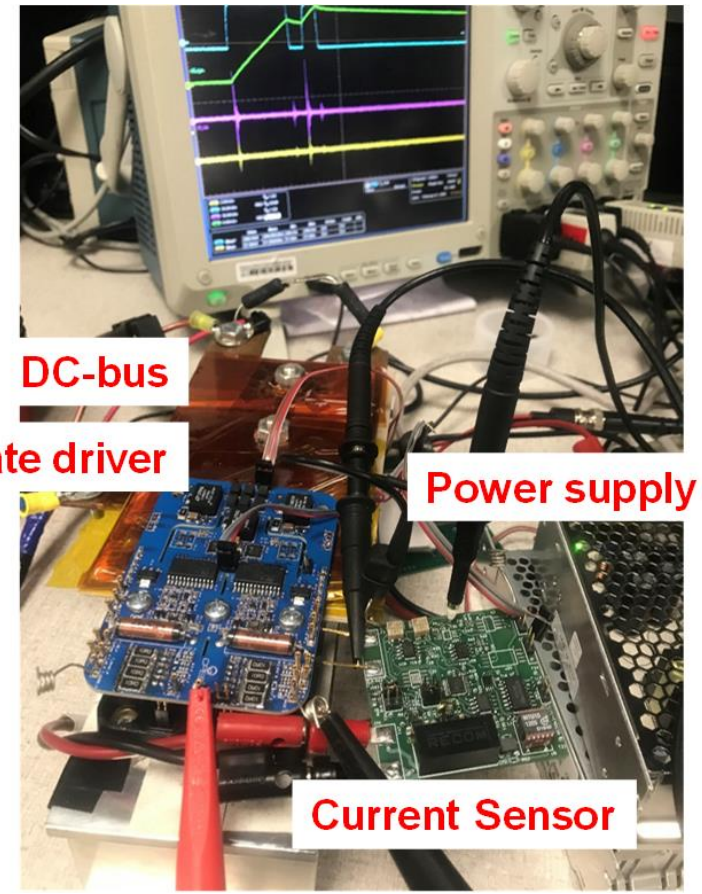
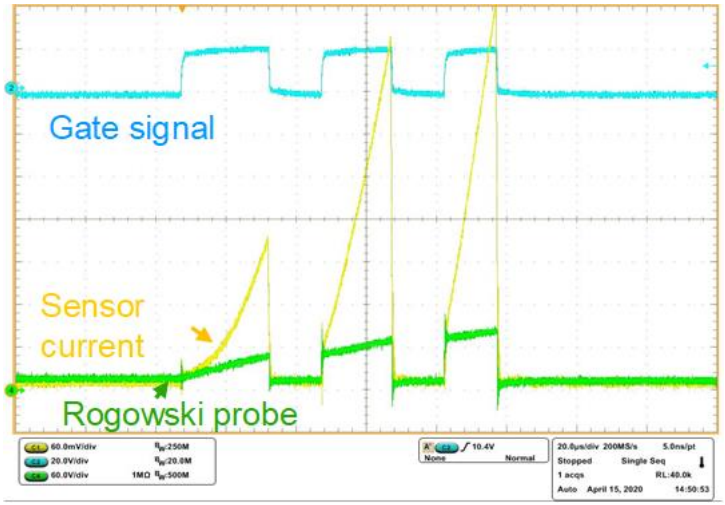
Accomplishments - Test Setup and Experimental Results

➢ **Setup:**

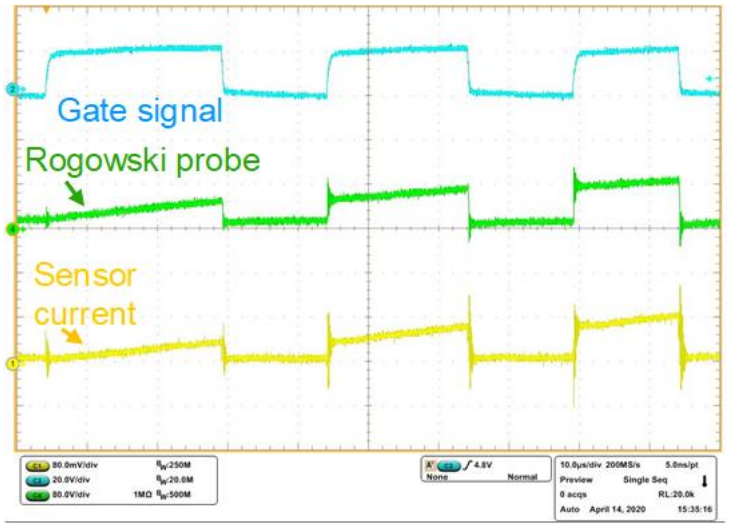


➢ **Experimental results:**

Without feedback



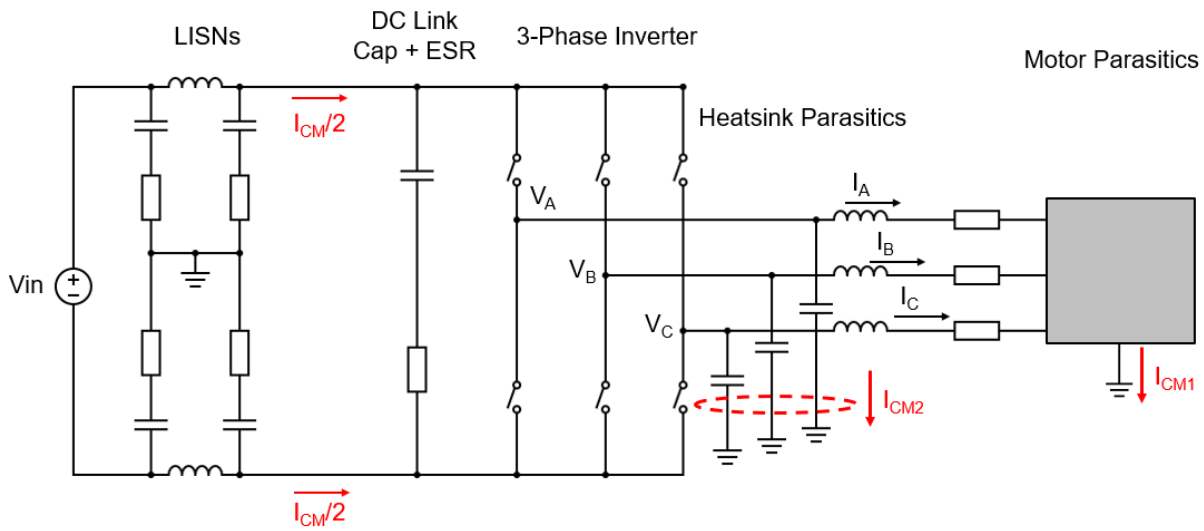
With feedback



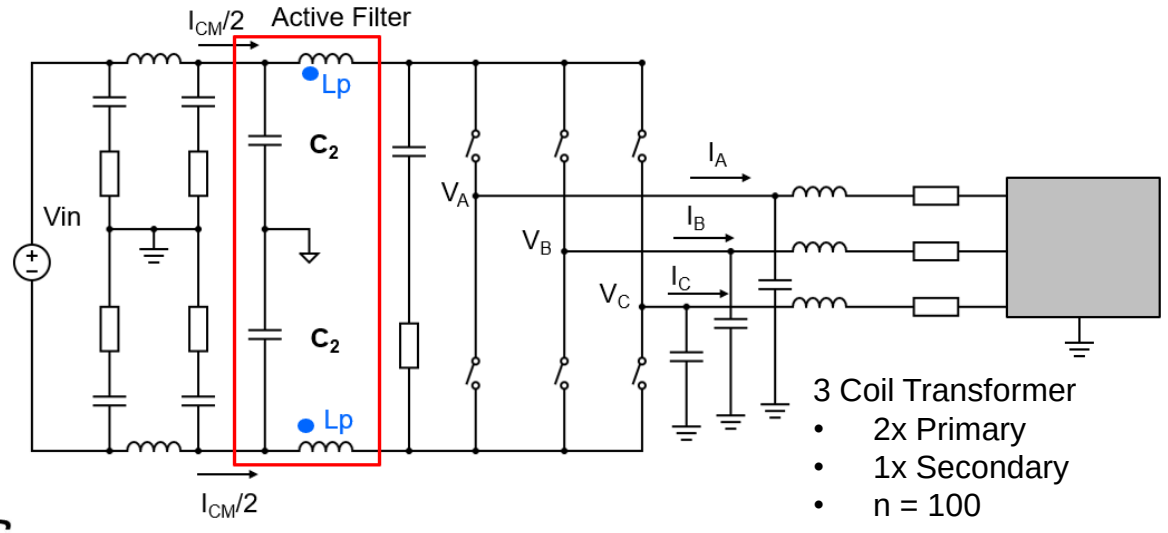
- ✓ **The proposed current sensor with feedback compensation considerably mitigates the effect of the parasitic resistance;**
- ✓ **Waveform of the sensing current is similar to that of the actual switching current;**
- ✓ **There is still an initial error in the sensing current, which needs to be mitigated to further increase the accuracy.**

Accomplishments - Active Filter for CM Current Suppression

- **Motor drive system with circulating CM current:**

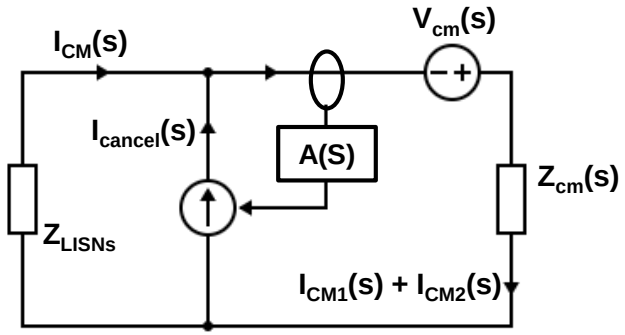


- **Motor drive system with feedforward CM current cancellation:**



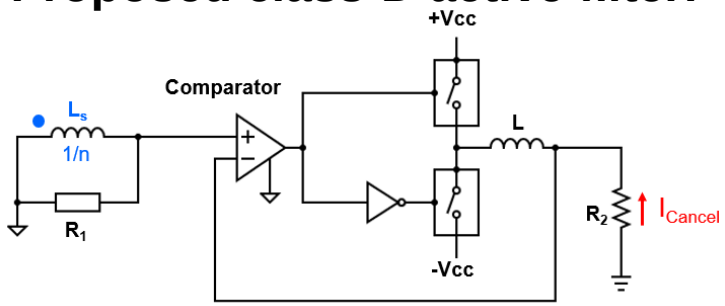
3 Coil Transformer
- 2x Primary
- 1x Secondary
- n = 100

- **Feedforward CM current cancellation:**



Feedforward Cancellation Condition
- If $Z_{CM} >> Z_{LISNs}$
- Then A(s) = 1 for efficient cancellation

- **Proposed class-D active filter:**



- CM current is reconstructed and injected into system ground with opposite magnitude.

✓ **Class-D provides higher bandwidth for CM current reconstruction.**

Responses to Previous Year Reviewers' Comments

- **None. This is the first year of the project and the first time being reviewed.**

Collaboration

ORNL: provide specifications for module design, access to packaging facility, and support on module testing.

NREL: advise on module thermal designs and support C-SAM characterization of sintered-metal joints and their thermo-mechanical reliability testing.

DOWA: custom-design and fabricate integrated substrate/heat sink structures for module cooling.

University of Arkansas: provide high-temperature gate driver chip.

Remaining Challenges and Barriers

- **1st & 2nd Year:** Finding high-temperature components meeting the designs of gate driver and EMI reduction circuits; we may have to design the circuits around available components;

- **2nd & 3rd Year:** Assembling modules with gate driver and EMI reduction circuits by resolving process compatibility issues stemming from different types of materials and their processing limitations.

Proposed Future Research

Ongoing

FY19 – Survey high-temperature packaging materials and components, module designs and fabrication processes, gate driver and current sensor designs for WBG modules, and EMI mitigation solutions **[September Milestone]**; identify available equipment needed for module, gate driver, and EMI circuit fabrication; simulate designs of power module **[Key March 2020 Milestone]**, gate driver **[December Milestone]**, and EMI **[November Milestone]**; and start making bonded samples and building current sensors;

Proposed

FY20 – Develop reliable processing conditions for chip bonding and planar module fabrication **[June Milestone]**; work with NREL on reliability of sintered bonds; fabricate and test gate-driver circuits for high temperature operation **[October Milestone]** and EMI reduction circuits **[December Milestone]**; fabricate and test fully functional planar, double-side cooled SiC power modules **[Key March 2021 Milestone];**

Planned

FY21 – Assemble power modules together with gate driver and EMI circuits to build power converters capable of working at 200°C.

**** Any proposed future work is subject to change based on funding levels.***

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Summary

- **Relevance:** enable the EDT consortium to achieve its targets on performance, cost, power density, and reliability of a 100 kW traction drive system.
- **Approach:** research, develop, and evaluate the integration and packaging technologies for making high-temperature, high-density, and low-profile wide-bandgap (WBG) power electronics modules with intelligent gate driver, current sensor, and EMI mitigation.
- **Technical Accomplishments:**
  - Completed surveys of high temperature packaging materials, gate drivers, and passive components;
  - Designed, fabricated, and tested a 1.2 kV, 100 A SiC MOSFET phase-leg power module;
  - Completed a survey of air-core magnetics and preliminary simulation of planar air-core transformers;
  - Designed a gate driver board for functional test of a high temperature gate driver and finished a preliminary test;
  - Designed a parasitic-inductance-based current sensor with feedback compensation and obtained experimental results off the source parasitic inductance of a commercial power module;
  - Simulated a common-mode current sensor and compensation circuit using Class-D amplifier.
- **Collaborations:** **ORNL**: providing module design specs and supporting on module testing; **NREL**: advising on module thermal management and supporting C-SAM characterization of sintered-metal joints and thermo-mechanical reliability testing; **UArk**: providing high-temperature gate driver chips; **DOWA**: custom-designing and fabricating integrated substrate/heat sink structures for module cooling.
- **Future Work:**
  - Develop reliable processing conditions for chip bonding and planar module fabrication;
  - Work with NREL on reliability of sintered bonds;
  - Fabricate and test gate-driver circuits for high temperature operation and EMI reduction circuits;
  - Fabricate and test fully functional planar, double-side cooled SiC power modules.

CPES

**** Any proposed future work is subject to change based on funding levels.***