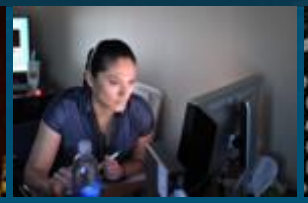
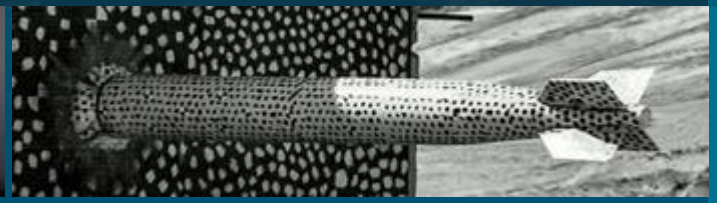
Development of Next-Generation Vertical GaN Devices for High-Power-Density Electric Drivetrain





Greg Pickrell, Co-PI, Power Electronics

Sandia National Laboratories

June 2, 2020

Project ID: elt210

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This presentation does not contain any proprietary, confidential, or otherwise restricted information

Overview

Timeline

- Start – FY19
- End – FY23
- 30% complete

Budget

- Total project funding
  - DOE share – 100%
- Funding received in FY19: $550k
- Funding for FY20: $700k

Goals/Barriers

- Device performance target = 1200 V/100A
- Power Electronics Density = 100 kW/L
- System Power target > 100 kW (~1.2kV/100 A)
- Cost target for Electric Traction Drive system ($6/kW)
- Operational life of Electric Traction Drive system = 300k miles
- Barriers:
  - Conventional SiC-based devices not designed for automotive environment
  - Relative immaturity of GaN-based vertical devices (performance/reliability)
  - Relative immaturity of new passive materials (performance/reliability)

Partners

- ORNL
- NREL
- SUNY – Woongje Sung
- Ohio State – Anant Agarwal
- Jim Cooper
- Jon Wierer – Lehigh University
- Project Lead: Sandia Labs, Team Members: Jack Flicker (Co-PI), Todd Monson, Bob Kaplar

Relevance and Objectives

Objectives

- Develop power electronics components to reach the power density targets of > 100 kW (~ 1.2 kV/100A) and 100 kW/L
- Power electronics performance targets enable overall system performance targets for the Electric Traction Drive system of 33 kW/L, $6/kW, and > 300k mile operation lifetimes
- **Second year objectives**:
  - SiC efforts focused on COTS device evaluation, design improvement and device fabrication for automotive environments
  - GaN efforts focused on device design/simulation, process development, & Gen1 device demonstration

Impact

- Enabling advanced future Electric Traction Drive vehicles which contributes directly to clean energy transportation
- Wide bandgap (SiC and GaN) power devices enable higher power densities (reduced size and weight) and higher operating frequencies
- Higher operating frequencies enable size and weight reduction for passive devices (capacitors and inductors) in power circuits
- Efforts directly address technology barriers for power electronics and Electric Traction Drive power density targets

FY20 Milestones

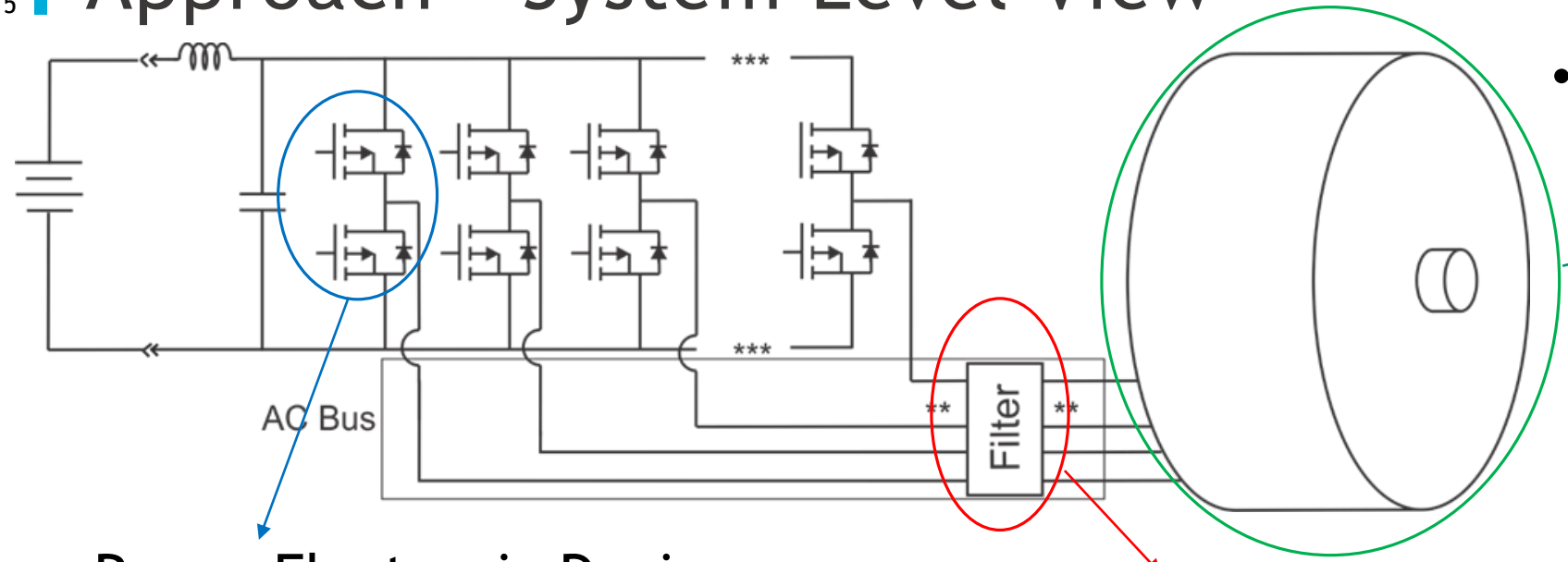
Milestone	Date	Status
Refine vertical GaN MOSFET electro-thermal models. Develop and demonstrate 1st-generation vertical GaN MOSFET gate dielectric process using low-voltage test structures.	9/2020	On Track
Refine vertical GaN Schottky diode and Junction Barrier Schottky diode electro-thermal models. Develop and demonstrate 1st-generation vertical GaN Schottky Barrier and Junction Barrier Schottky diodes and characterize their performance.	9/2020	Complete
Engage in SiC design-for-reliability studies aimed at fabrication of devices specific to automotive environments. Evaluate performance of fabricated SiC devices.	9/2020	On Track
Extend advanced component test-bed capabilities to emulate more realistic usage scenarios. Evaluate commercial devices for automotive applications. Evaluate fabricated GaN devices.	9/2020	On Track

FY21 Milestones (tentative)

Milestone
GaN MOSFET – Demonstrate 100 V reverse holdoff and 0.2 A forward current.
GaN JBS Diode – Demonstrate 600 V reverse holdoff and 0.5 A forward current.
Evaluate 2nd Gen SiC fabricated devices and begin reliability evaluation for new designs
Evaluate SiC and GaN devices in test bed using realistic usage scenarios as appropriate.

Any proposed future work is subject to change based on funding levels.

Approach – System Level View



- Advanced Motor Designs:
  - Increased power density
  - Higher speed operation
    - Reduced size/weight

- Power Electronic Devices:
  - SiC or GaN-based
    - Higher critical elec. field
  - Higher frequency operation
    - Increased power density
    - Reduced size/weight

- Passives for Power Electronics
  - Composite materials for improved inductors
  - Improved capacitor lifetime, operating modes
  - Higher frequency operation
  - Reduced size/weight

- Characterization efforts at each point in the system:
  - Power electronic devices, passives, motors
- Sandia National Labs efforts span multiple levels within system design

Approach – Materials for Power Electronics

Stage 1:
SiC MOSFET + SiC Diode

Device modeling, circuit simulation at each stage.

Stage 2:
SiC MOSFET + GaN Diode

Stage 3:
GaN MOSFET + GaN Diode

Characterization and evaluation of device technology in test bed at each stage.

Any proposed future work is subject to change based on funding levels.

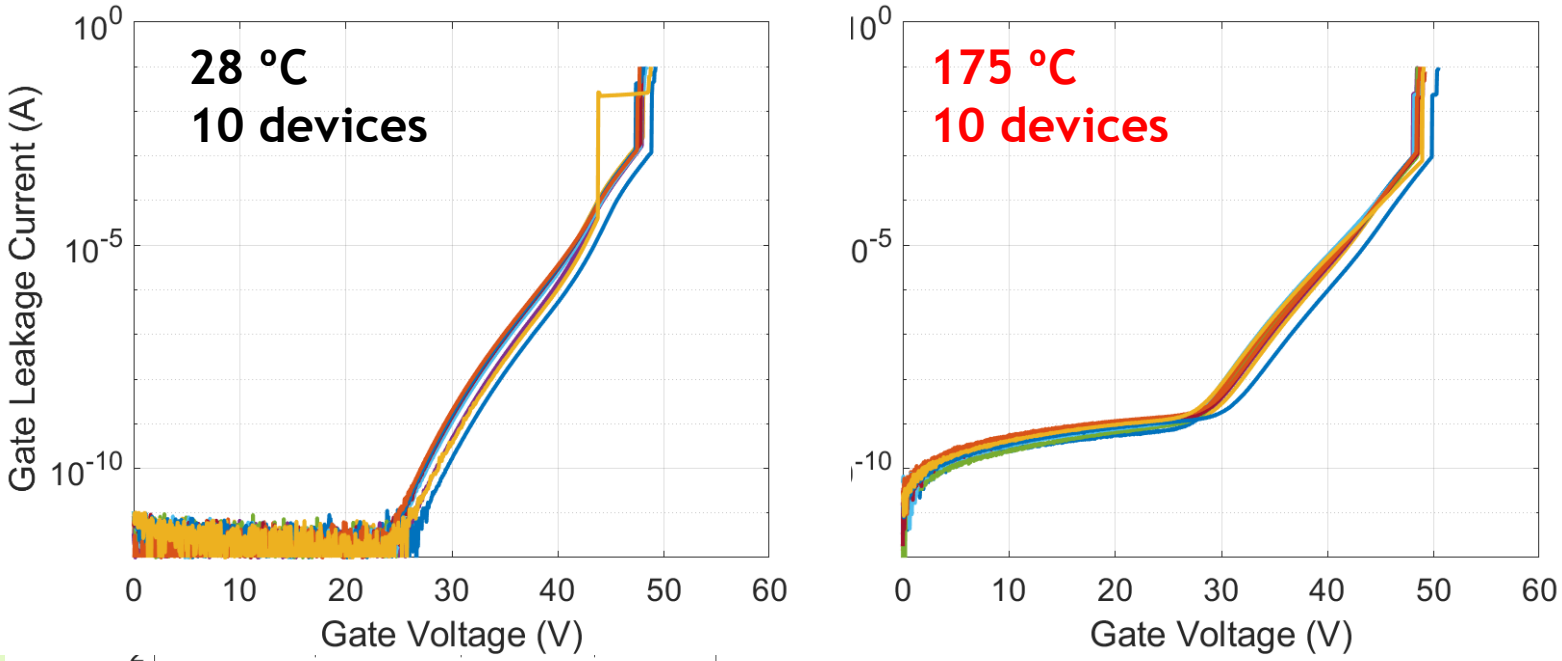
Technical Accomplishments and Progress – SiC COTS

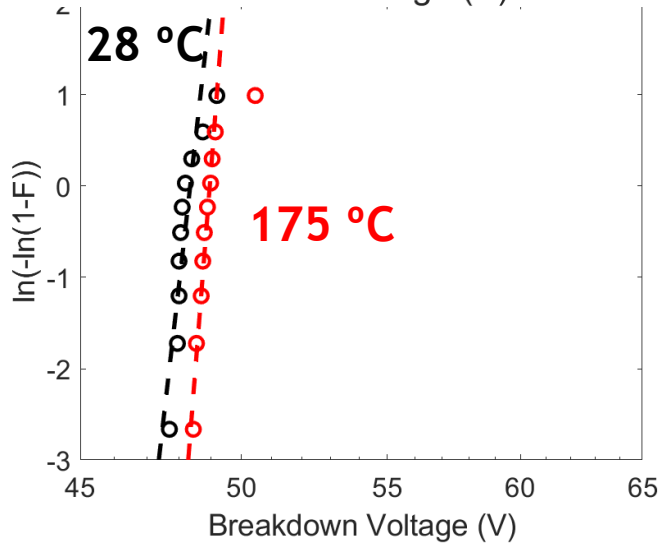
THE OHIO STATE UNIVERSITY

Evaluating COTS SiC MOSFETs under stress to understand performance change for different vendors **(key for automotive applications)**:

- Gate oxide leakage current
- Body diode degradation
- Threshold voltage stability
- Short circuit time
- Avalanche energy

Gate Oxide Leakage Current



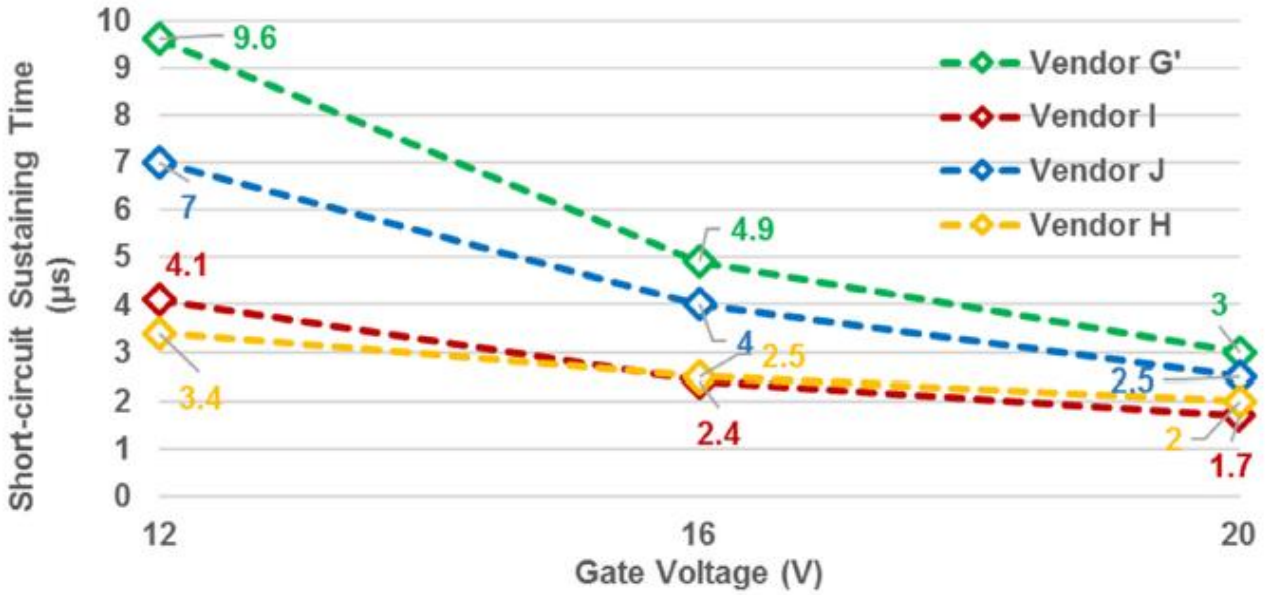


- Evaluated 3 commercial vendors
- 2 of 3 vendors showed stable performance
- Last vendor shows large shift in gate breakdown voltage

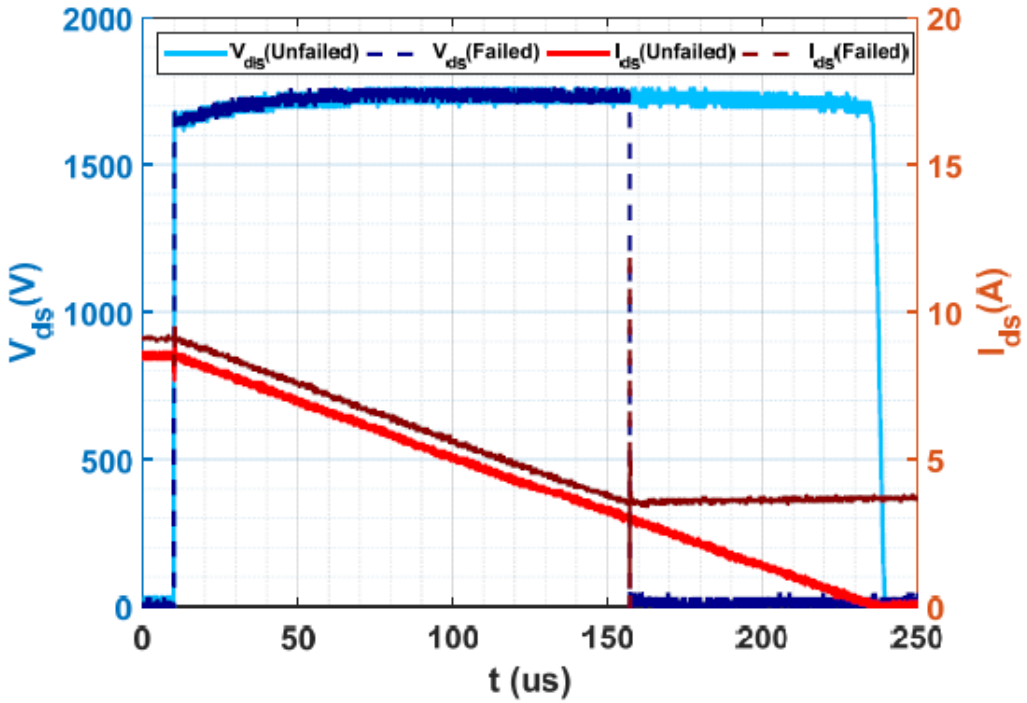
Technical Accomplishments and Progress – SiC COTS

THE OHIO STATE UNIVERSITY

Short-Circuit Time



Avalanche Energy



- Evaluated 4 commercial vendors
- Short-Circuit withstand times decrease with larger gate voltage
- Most commercial vendors have short circuit withstand times significantly < 10 µs (typical Si value)

- Avalanche energy tests for multiple suppliers underway
- Increasing gate pulse lengths until device failure
- Monitor Vds and Ids to determine avalanche energy (Typical Si IGBT ~ 300 mJ, SiC planar MOSFET~ 1000 mJ)

Technical Accomplishments and Progress – SiC Devices

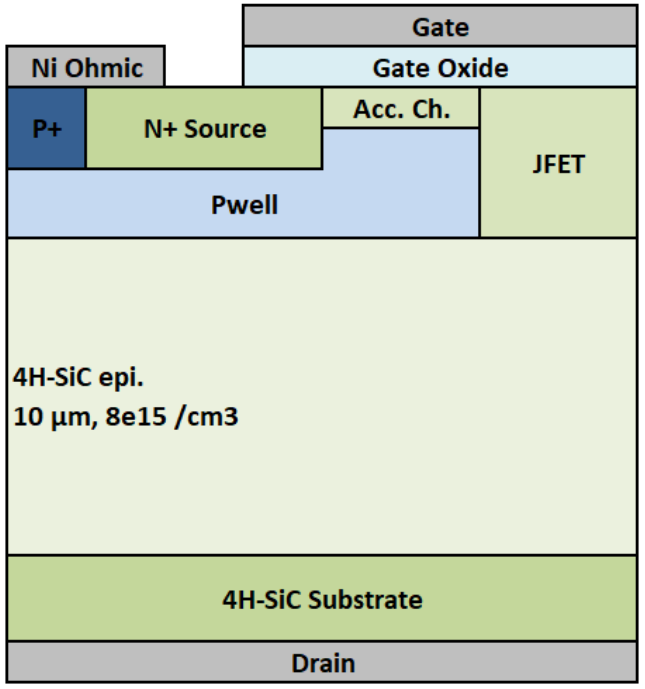
Establishing ability to fabricate custom designs at commercial foundry with SUNY Poly

Design variations include

- Channel length
- JFET depth
- Gate oxide thickness
- Different gate oxide
- Layout variations (Hexagonal)
- Integrated JBS diode/MOSFET

First lot in characterization at SUNY Poly & other consortium partners.
Second lot in fabrication.

Diagram of ½ MOSFET



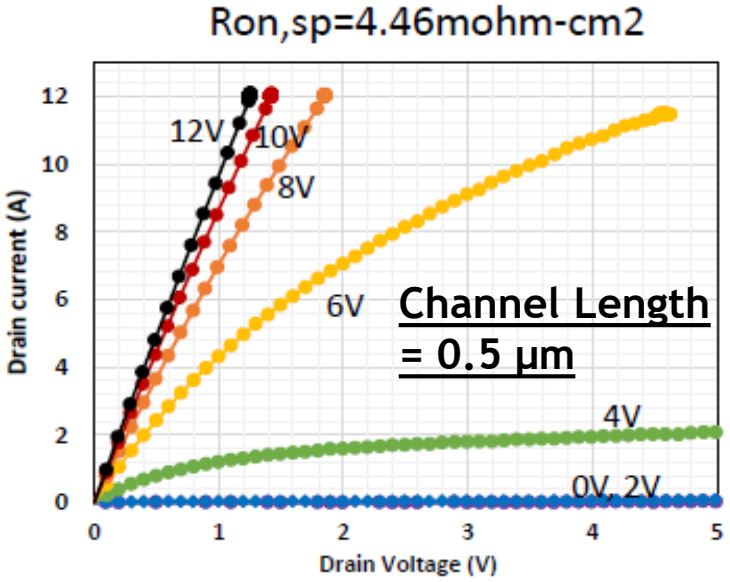
Optical Image of Lot #1 SiC Fabricated Wafer (SUNY Poly)

SUNY Poly Albany Campus

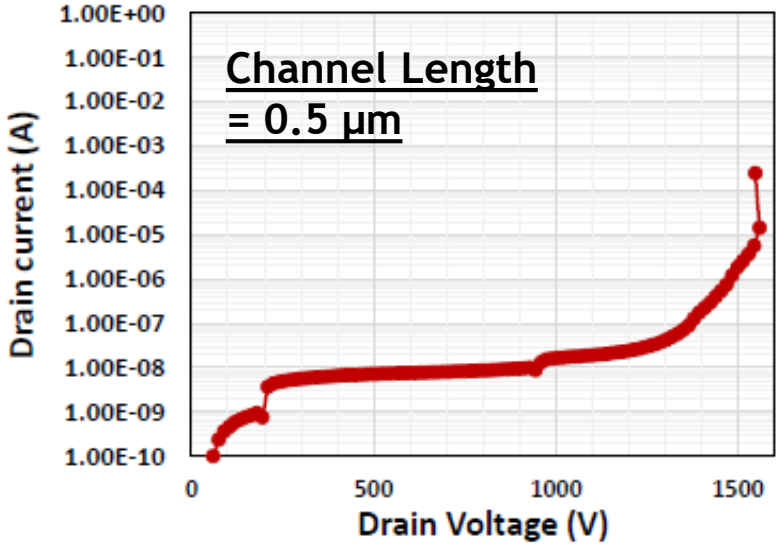
Technical Accomplishments and Progress – SiC Devices

SUNY Poly Albany Campus

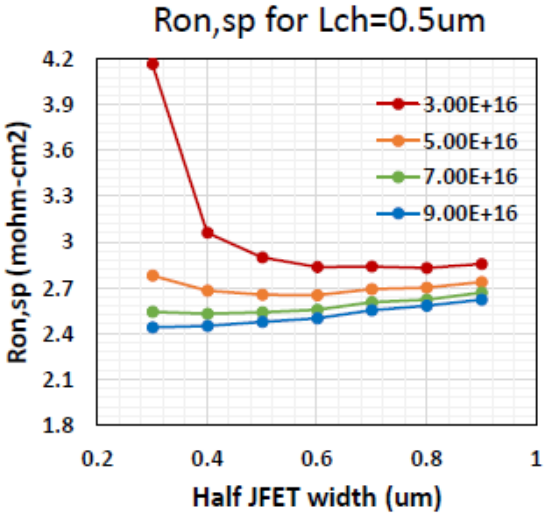
Family of IV curves

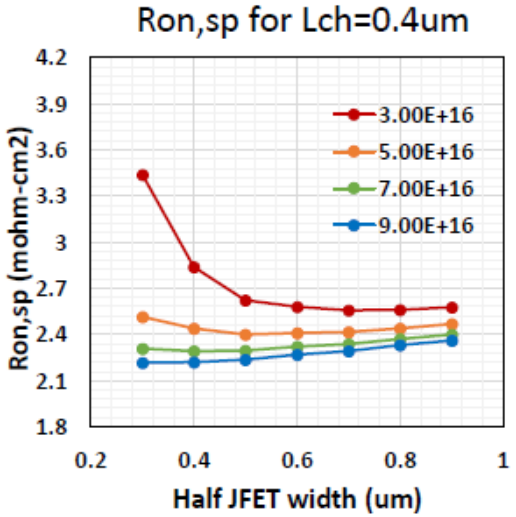


Breakdown (Vbr) Performance



- Representative data from Lot1 wafer characterization
- Ron,sp ~ 4.5 mΩ-cm^2 (including sub.) (target = 6 mΩ-cm^2)
- Ron (total) ~ 100 mΩ (25-30 A current rating)
- Vth = 1.5-3 V (depends on gate oxide thickness) (target = 2 V)
- Vbr ~ 1500 V (target 1500 V)
- Met Year 1 targets on Lot1 wafers





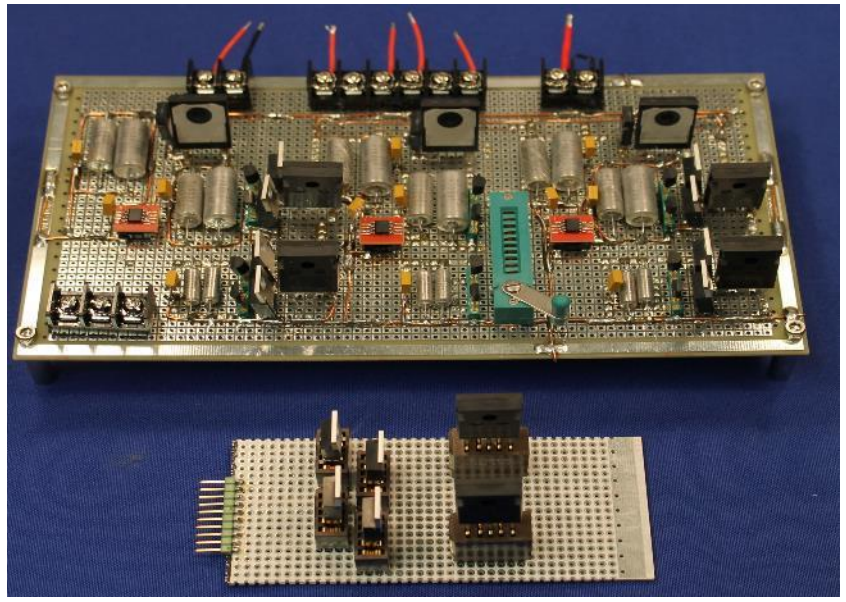
Future testing planned to evaluate:

- Performance sensitivity to different designs for breakdown voltage, threshold voltage, Ron,sp
- Short circuit capability
- Avalanche energy (Si IGBT typical ~ 300 mJ)

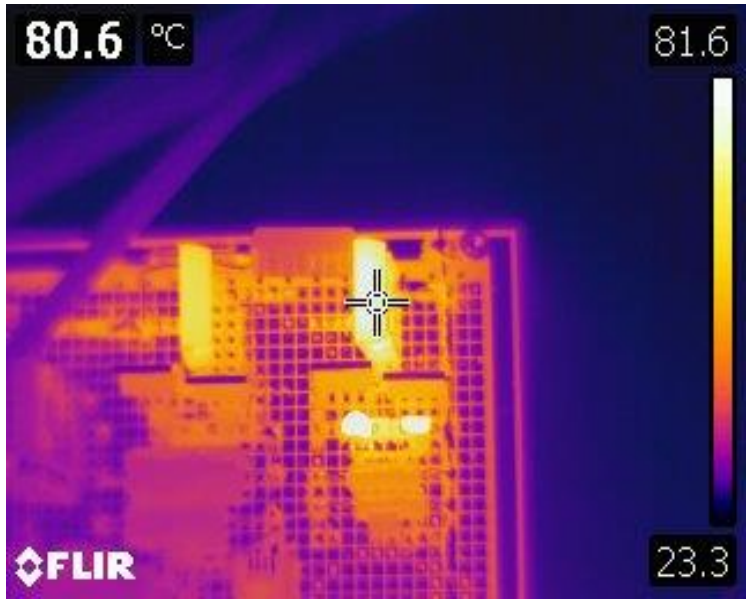
Technical Accomplishments and Progress – Test Bed Development

- Need **rapid prototyping** for R&D devices
- Data on performance and reliability for input in future generations of components
- Realistically emulate operations and stressors that exist in end-use application but can be scaled in parameters (voltage, current, temperature, etc.) to suit intermediate maturity devices
- Developed brushless DC motor drive test-bed to evaluate performance of fabricated devices. Initial test targets:
  - 1000 V, 10 A
  - Fully controllable voltage/current
  - Replicated motor dynamics

Fabricated Test Bed Prototype Boards



Thermal Camera Image of Board



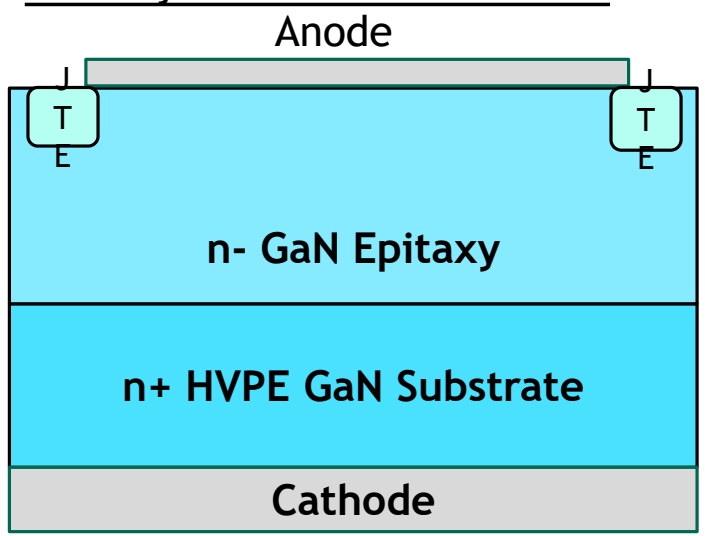
Oscilloscope Traces During Operation

Technical Accomplishments and Progress - GaN

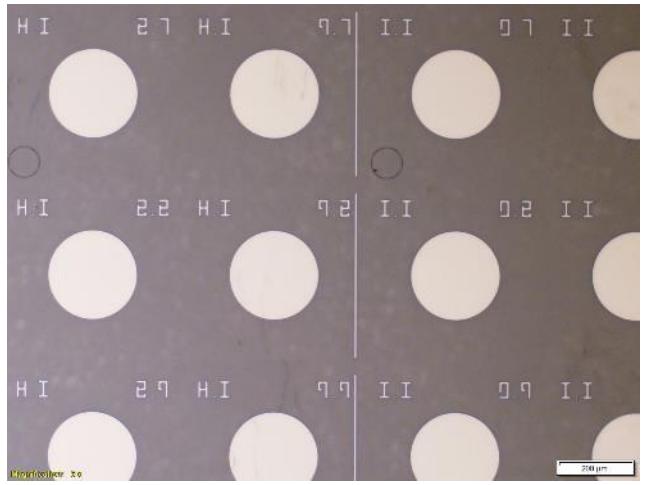
- Vertical GaN devices is another path to Power Electronics target (Long Term)
- Simulated GaN Schottky Barrier (SB) diodes using TCAD
- Grew, fabricated and characterized GaN SB diodes
- MOCVD growth of n-type GaN (c.c. ~ 2E16 cm-3) on conducting n-GaN substrates
- Fabrication process included Schottky metallization (Anode), dielectric passivation, dielectric window, field plate fabrication, and backside ohmic contact metals (cathode)
- Low forward leakage demonstrates good Schottky contact
- Low reverse leakage for reverse voltages of ~ -400 V

FY20 Milestone for SB and JBS Diode demonstration: COMPLETE

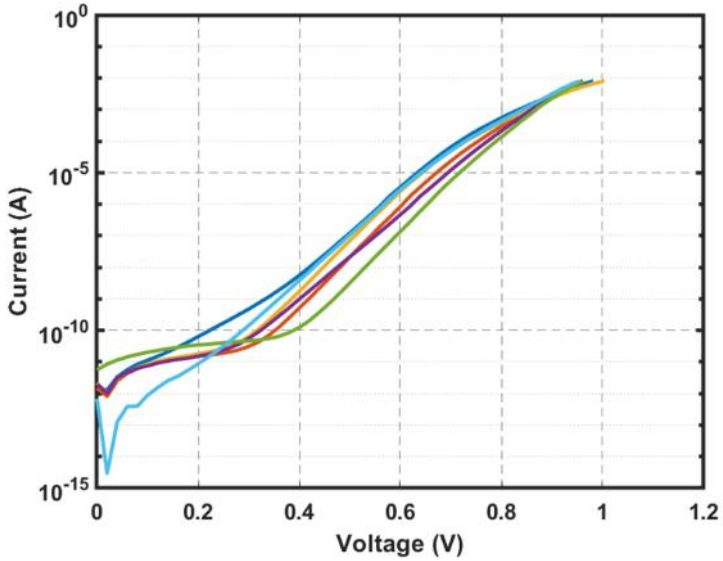
Schottky Barrier Diode Schematic



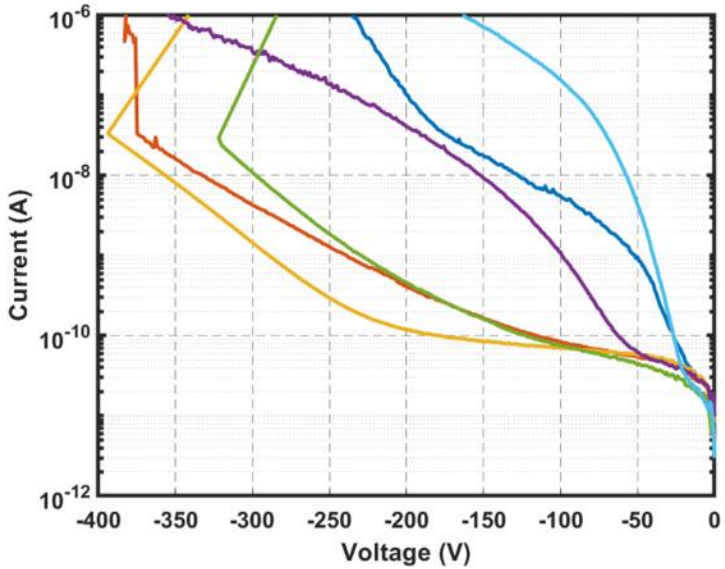
Optical microscope images of fabricated GaN SB Diodes



Forward IV Diode Behavior



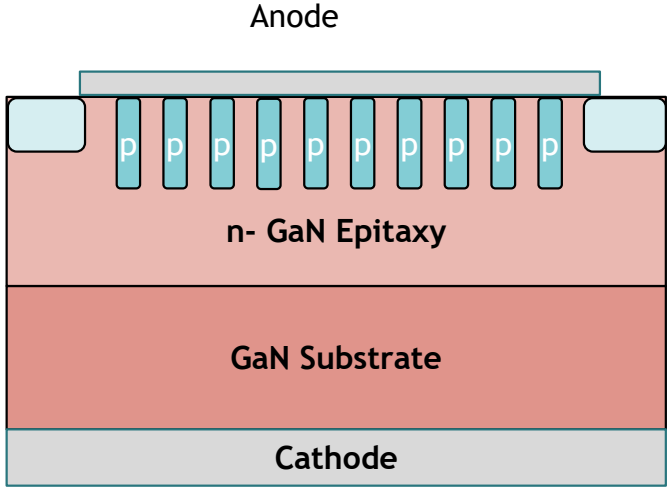
Reverse IV Diode Behavior



Technical Accomplishments and Progress - GaN

LEHIGH UNIVERSITY

- Modeling/Simulation/Optimization of GaN JBS diodes completed

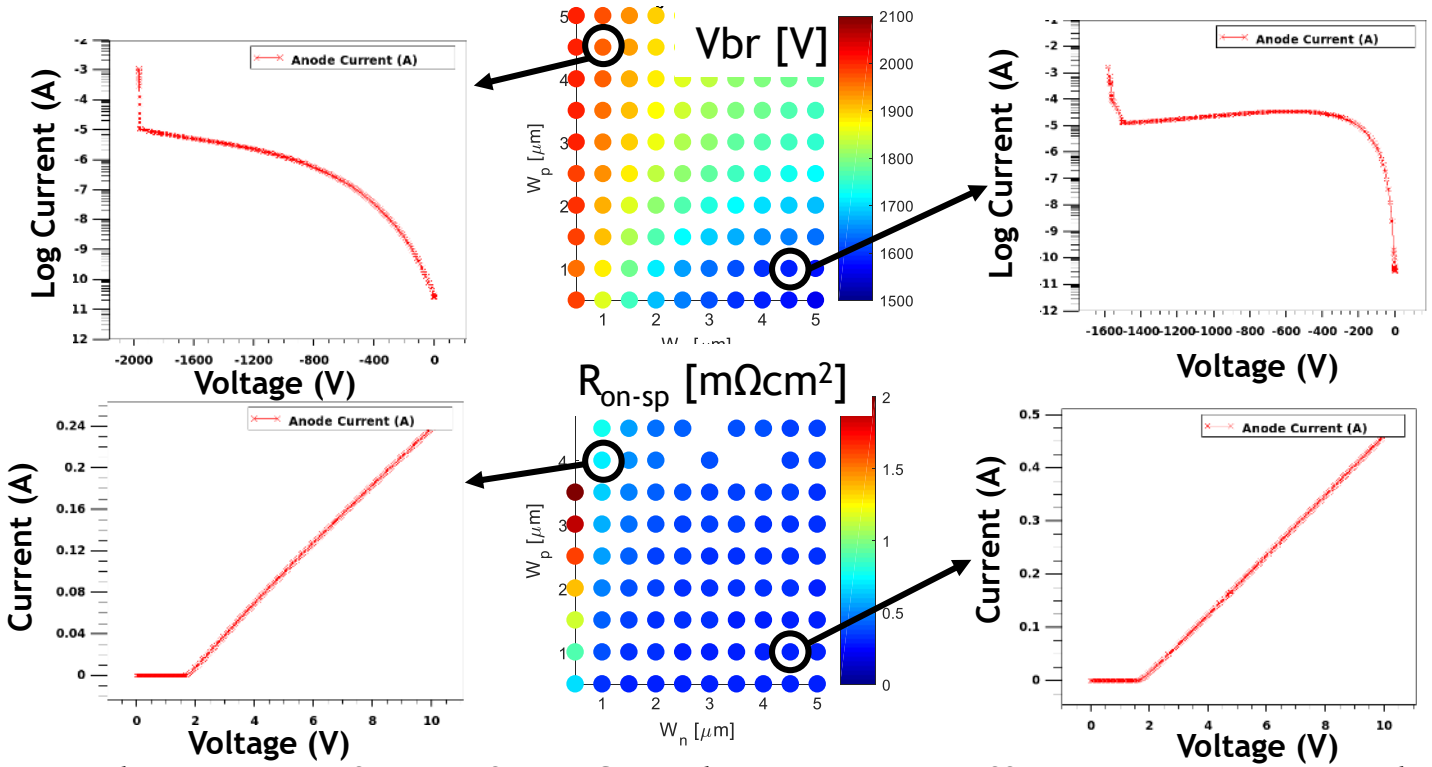


JBS Diode Schematic

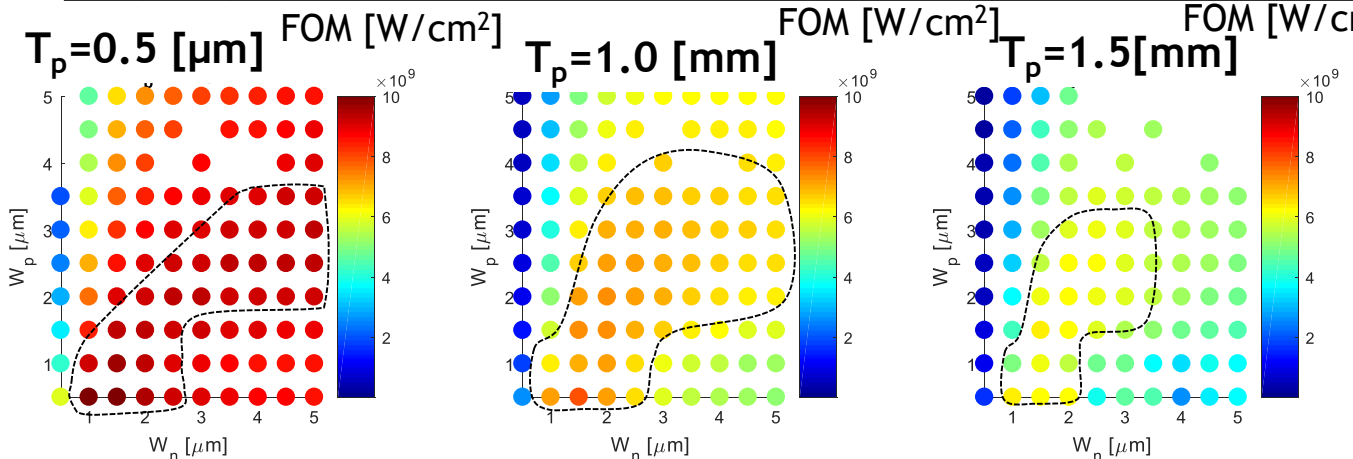
- Calculated Vbr, Ron,sp, and Baliga's FOM(BFOM) ($Vbr^2/Ron,sp$)
- Developed contour areas for different designs with high BFOM to look at process sensitivity
- P-doping ~ 1E18 cm-3 with Tp = 0.5 - 1 µm is target.

FY20 Milestone for SB and JBS Diode simulation: COMPLETE

IV Characteristics for Simulated JBS Diodes



Baliga Figure of Merit for JBS Diode Designs at Different P-Doping Levels

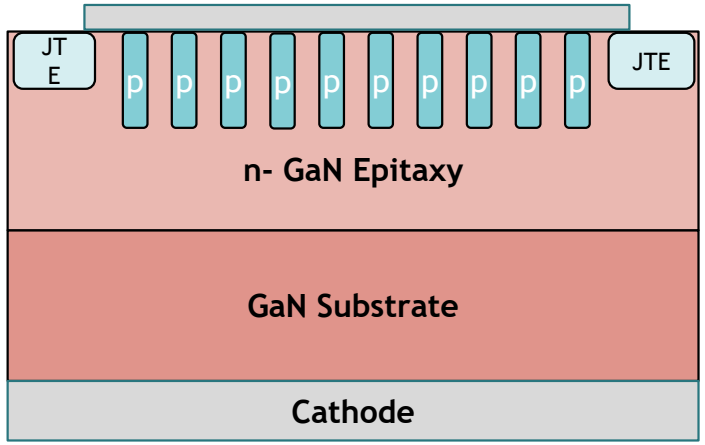


Technical Accomplishments and Progress - GaN

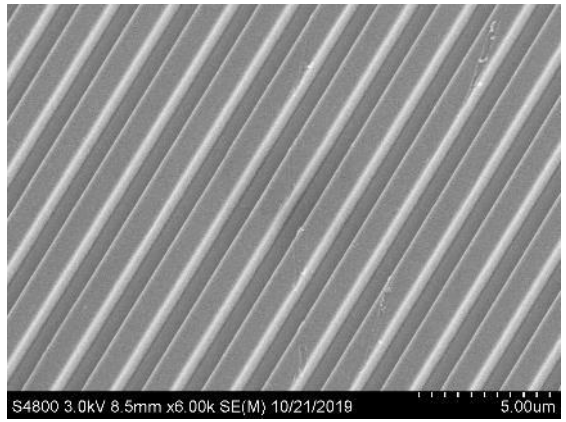
- Process development for GaN JBS diodes underway
- Contact lithography process for 1 µm lines and spaces **demonstrated.**
- Fabricated trench pattern in n-GaN using dry etch process with different trench spacing.
- MOCVD regrowth of p-GaN on trenched surface to fill areas and planarize top surface **demonstrated.**
- Cross-sectional SEM images used to evaluate regrowth quality and planarization. Image shown on right.

FY20 Milestone for SB and JBS Diode process development: COMPLETE

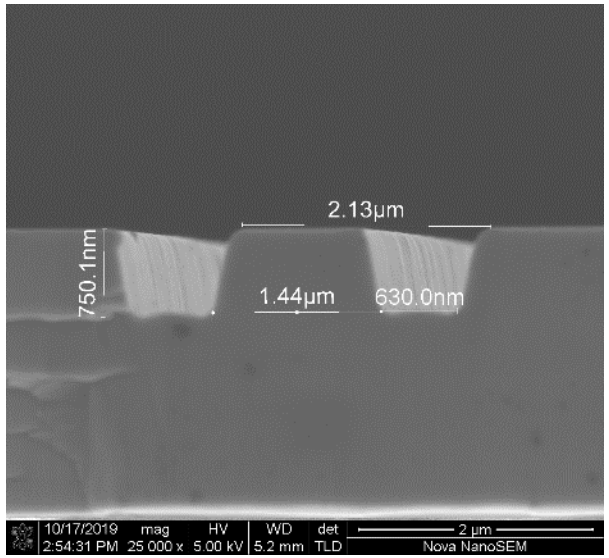
JBS Diode Schematic



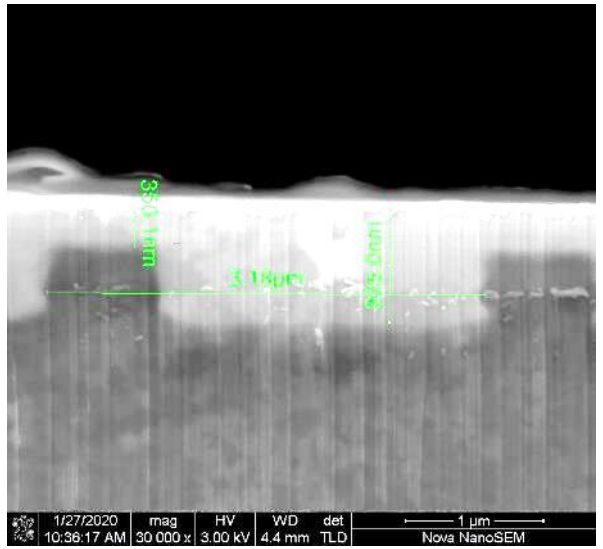
Photoresist Patterns for Trench Process (1 µm lines) for JBS diodes



Cross-section SEM images of etched trenches for JBS Diodes



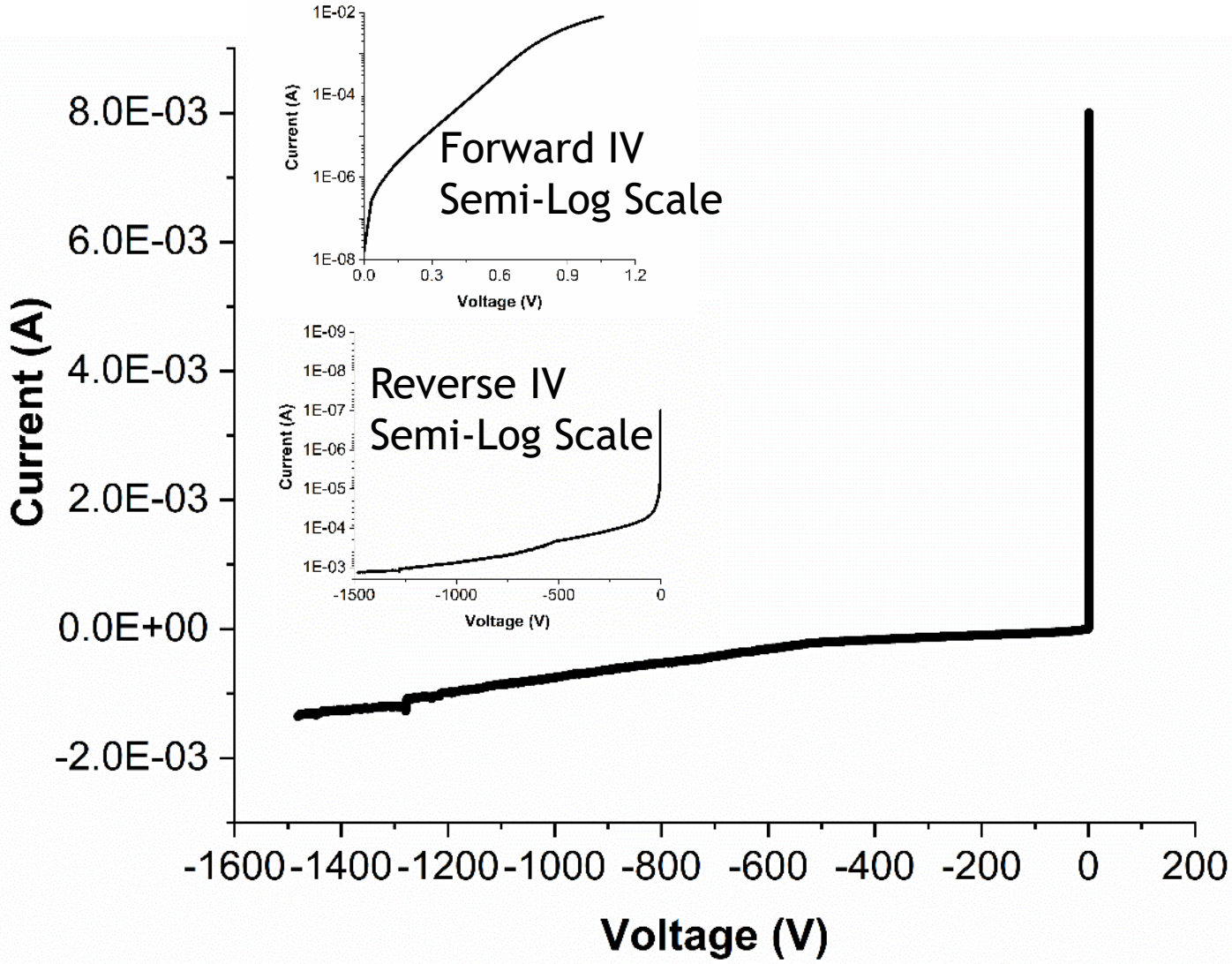
Cross-Section SEM of Regrown GaN JBS Diode



Technical Accomplishments and Progress - GaN

- Gen1 GaN JBS diodes **demonstrated**
- Reverse holdoff to 1.5 k V **(target = 1.2 kV)**
- Tested to low forward current. Future efforts will scale forward current (target = 100 A)
- Trench pattern etched in n-GaN grown on conducting n-GaN substrate
- p-GaN regrown on etched wafers with trench pattern to planarize wafer
- Other device processes including: Schottky contact metals (anode), mesa isolation, dielectric passivation, dielectric window etch, field plate fabrication, backside ohmic metal deposition (cathode)

Forward and Reverse IV Curves for Gen1 GaN JBS Diode



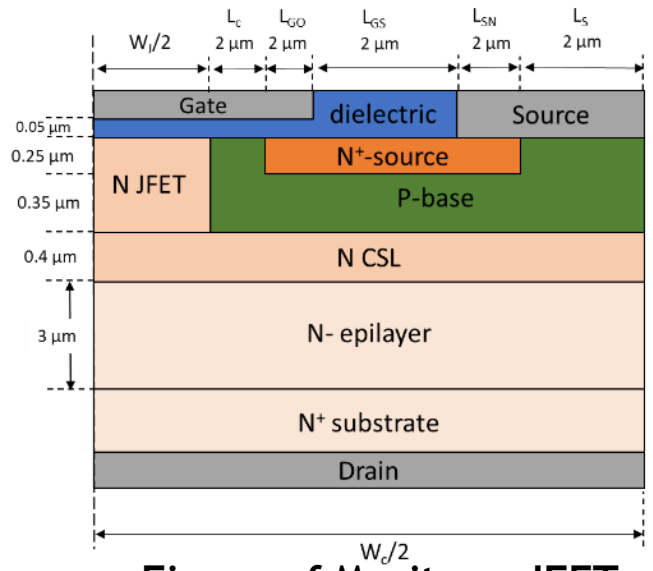
FY20 Milestone for SB and JBS Diode demonstration: COMPLETE

Technical Accomplishments and Progress - GaN

- Double-Well (D) and Trench MOSFET designs simulated in GaN
- Optimizing performance (Vbr, Ron) as a function of doping, layer thickness, and lateral feature dimensions.
- Monitoring peak electric field in semiconductor and dielectric layers to define breakdown.
- Driving designs for performance targets: **1200 V holdoff and 100 A forward current**

FY20 Milestone for GaN MOSFET simulation: COMPLETE

D-MOSFET



Trench MOSFET

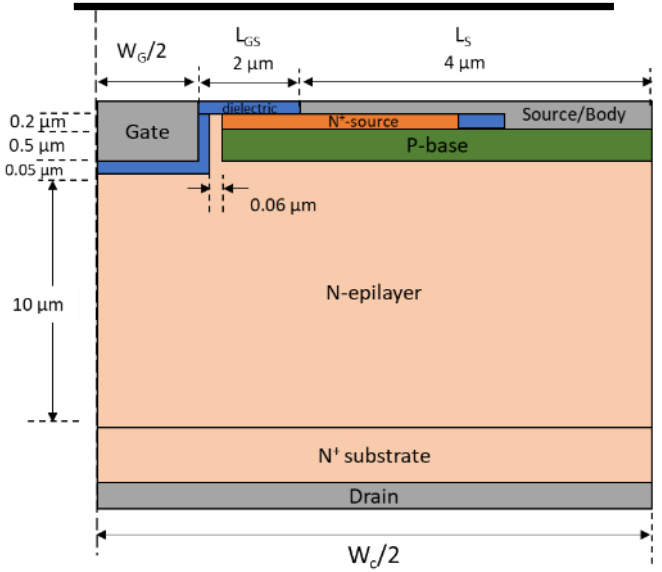
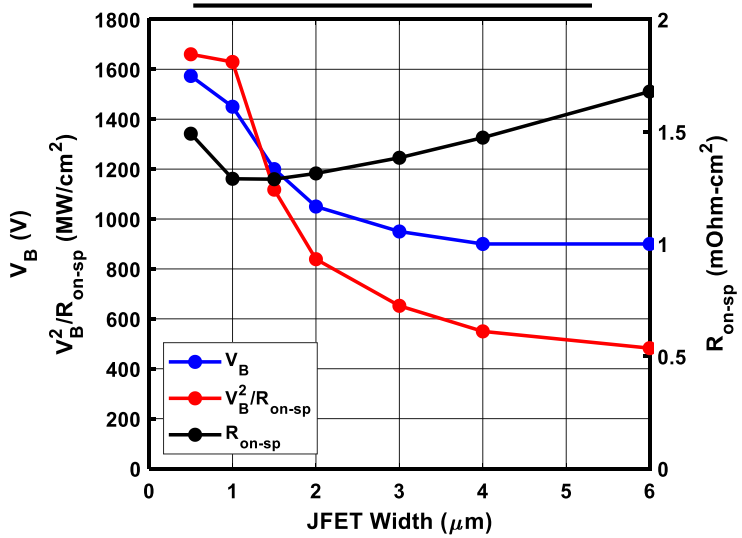
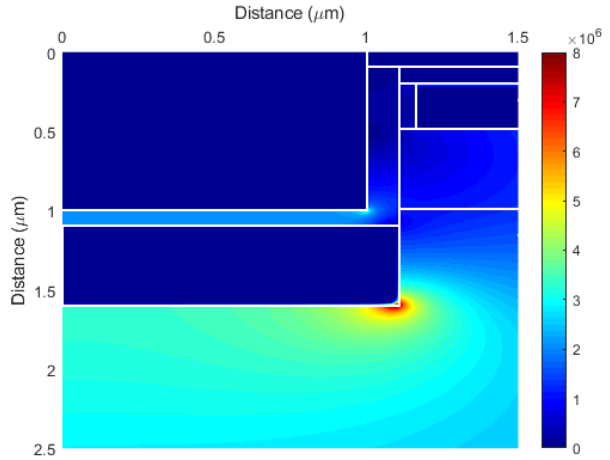


Figure of Merit vs. JFET width for D-MOSFET



Electric Field Simulation for Trench MOSFET

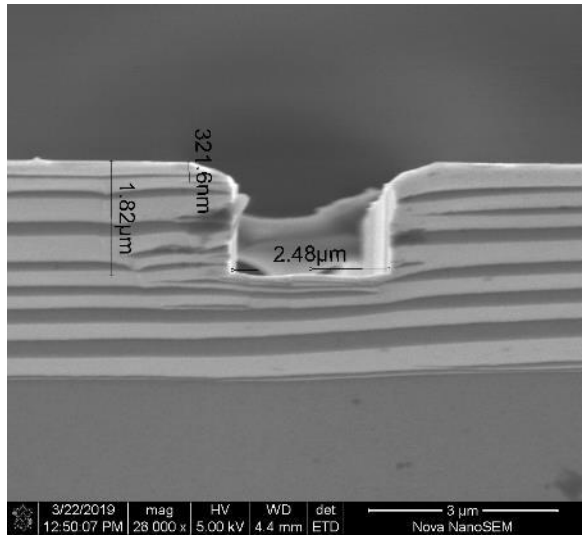


Technical Accomplishments and Progress - GaN

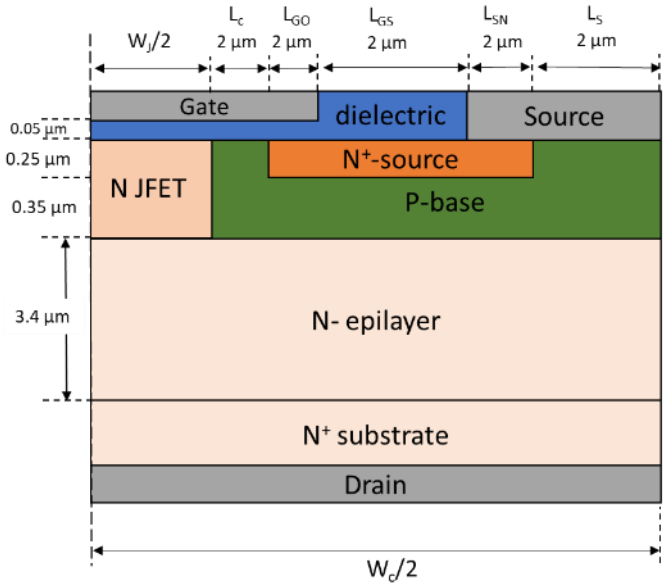
- Trench MOSFET gate structure process development efforts ongoing.
  - Developed hard mask process to results in vertical sidewalls needed for Trench MOSFET
- D-MOSFETs – Si Implant Process Development
  - N+ Source layer needed for D-MOSFET device.
  - P-GaN material implanted with Si (n-type dopant), thermally annealed to activate Si dopants, and fabricated into test structures for process evaluation.
  - Activation experiments have been performed with and without a capping layer (SiN), and at a range of temperatures (900-1100 °C). **Ohmic contacts achieved.**
  - Iterate to reduce ohmic contact resistance and then include in future Gen1 GaN D-MOSFET devices.

FY20 Milestone for GaN MOSFET process development: ON TRACK

Cross-section SEM images of etched gate structures for Trench MOSFETs

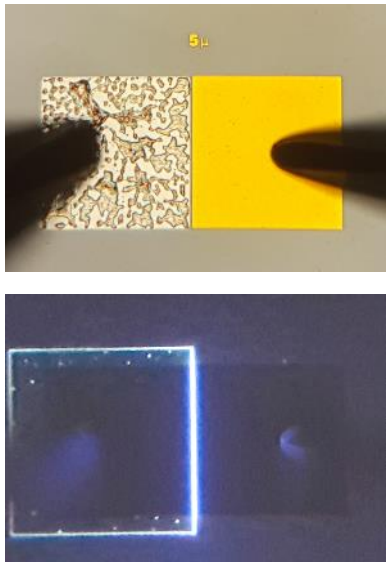


D-MOSFET Schematic

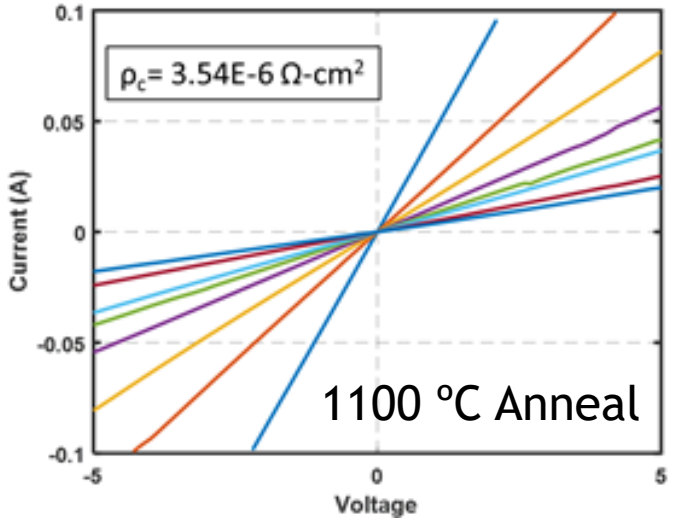


Implanted Lateral PN Diode Test Structure

Under bias Light = electron hole recombination



Si-Implant CTLM with Ohmic Behavior



Responses to Previous Year Reviewers' Comments

- **Multiple reviewer comments asked to define performance targets for power electronic devices**
  - SiC Devices:
    - Slides 7-10 demonstrate focus on evaluation of SiC devices for automotive applications
    - Focus on SiC device failure modes such as gate oxide leakage, threshold voltage shift, short-circuit withstand times
    - Performance targets for SiC devices defined
  - GaN Devices:
    - Slides 14-16 include performance targets for vertical GaN devices
    - Device simulations/designs guiding efforts towards these performance goals.

- **Multiple reviewer comments asked to address future GaN cost/performance for auto applications**
  - Using commercial foundry for SiC devices. Cost models exist that can be used for predicting GaN devices. This will be used to predict GaN device costs in future years.
  - With GaN device maturity, GaN foundries need to be developed/matured for evaluation of GaN for automotive applications.

Collaboration

Oak Ridge National Laboratory – Collaborating partner for Electric Traction Drive integration and evaluation.

National Renewable Energy Laboratory – Collaborating partner for Electric Traction Drive integration and evaluation.

State University of New York (SUNY) (Woongje Sung) – Fabricating SiC JBS diode integrated with MOSFETs. (Subcontractor)

Ohio State University (Anant Agarwal) – Designing for improved reliability for SiC electronics. Evaluate reliability and ruggedness of commercial and fabricated devices using realistic scenarios. (Subcontractor)

Jim Cooper– Working with OSU for SiC device evaluation. Working with Sandia for GaN power electronic device design and characterization. (Subcontractor)

Lehigh University (Jon Wierer) – Working with Sandia for design/simulation/modeling of GaN SB and JBS diodes. (Subcontractor)

Remaining Challenges and Barriers

SiC Devices

- Designs need to be optimized for automotive environments
- Multiple iterations needed to understand performance/reliability/cost tradeoffs

GaN Devices:

- Immaturity of GaN devices requires multiple cycles of learning to develop and optimize device performance
- Need to scale development devices to higher operating currents
- Device reliability needs to be evaluated
- GaN foundry cost models need to be developed

Proposed Future Research

SiC:

- FY20-21:
  - Focus on design and test for automotive reliability
  - Fabricate and test 2nd generation of devices
  - Performance targets 1600 V holdoff, Ron,sp = 5 mΩ-cm^2, Vth = 2 V
- Rest of project:
  - Evaluate performance against Consortium targets
  - Utilize devices in Gen1 prototype Electric Traction Drive

GaN:

- FY20-21:
  - Iterate to improve GaN JBS diode performance to 600 V holdoff voltage, 0.5 A forward current
  - Combine GaN JBS diode with SiC MOSFET in circuit for evaluation
  - Demonstrate GaN MOSFET device performance (100 V holdoff voltage , 0.2 A forward current)
- Rest of project:
  - Iterate to improve GaN SB and JBS diode performance against targets (1200 V/100 A)
  - Iterate to improve GaN MOSFET performance against targets (1200 V/100 A)
  - Combine GaN MOSFET and JBS diode in circuit for evaluation

Any proposed future work is subject to change based on funding levels.

Summary

- Systems level view of the project identified key areas for performance improvement in power electronics:
  - Wide bandgap power devices – evaluate SiC and vertical GaN devices
  - Coordination with passive devices – inductors and capacitors
  - Development of device test platform for realistic EV scenarios
- Pursued multi-path approach for power electronics keystone through development of SiC and GaN devices to meet consortium targets
- SiC method evaluated commercial parts for reliability assessment while starting custom device fabrication at a commercial foundry (University partners). First round showed good device performance. Future designs will focus on automotive requirements.
- GaN device development is underway
  - Extensive device simulations for GaN diodes and MOSFETs completed
  - GaN Schottky diodes and JBS diodes demonstrated. Optimization in process.
  - Process development for GaN MOSFET underway
  - Implanted n-type source contacts for D-MOSFETs demonstrated