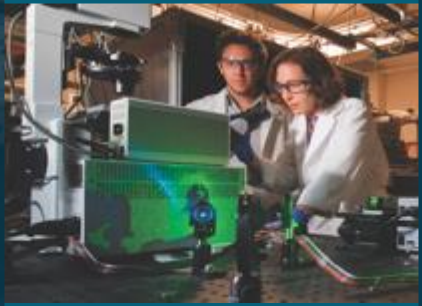
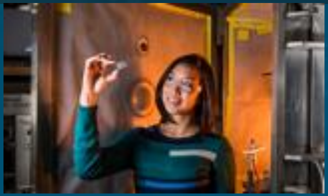
Sandia National Laboratories

Development of Next-Generation Vertical GaN Devices for High-Power-Density Electric Drivetrain





Greg Pickrell, Co-PI, Power Electronics

Sandia National Laboratories

June 11, 2019

Project ID: elt210

U.S. DEPARTMENT OF ENERGY NNSA

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Overview

Timeline

- Start – FY19
- End – FY21
- 25% complete

Budget

- Total project funding
  - DOE share – 100%
- Funding received in FY18: $0
- Funding for FY19: $550k

Goals/Barriers

- Power Density = 100 kW/L
- Power target > 100 kW (~1.2kV/100 A)
- Cost target for Electric Traction Drive system ($6/kW)
- Operational life of Electric Traction Drive system = 300k miles
- Barriers:
  - Conventional SiC-based devices not designed for automotive environment
  - Relative immaturity of GaN-based vertical devices (performance/reliability)
  - Relative immaturity of new passive materials (performance/reliability)

Partners

- ORNL
- NREL
- SUNY – Woongie Sung
- Ohio State – Anant Agarwal
- Jim Cooper
- Jon Wierer – Lehigh University
- Project Lead: Sandia Labs, Team Members: Jack Flicker (Co-PI), Todd Monson, Bob Kaplar

SUNY Poly Albany Campus

Relevance and Objectives

Objectives

- Develop power electronics components to reach the power density targets of > 100 kW (~ 1.2 kV/100A) and 100 kW/L
- Power electronics performance targets enable overall system performance targets for the Electric Traction Drive system of 33 kW/L, $6/kW, and > 300k mile operation lifetimes
- **First year objectives**:
  - SiC efforts focused on COTS device evaluation, design improvement for automotive environments
  - GaN efforts focused on device design/simulation, and process development
  - Passives efforts focused on design of reliability evaluation methods/equipment for capacitors and demonstration of Fe_4N/glass composite inductors

Impact

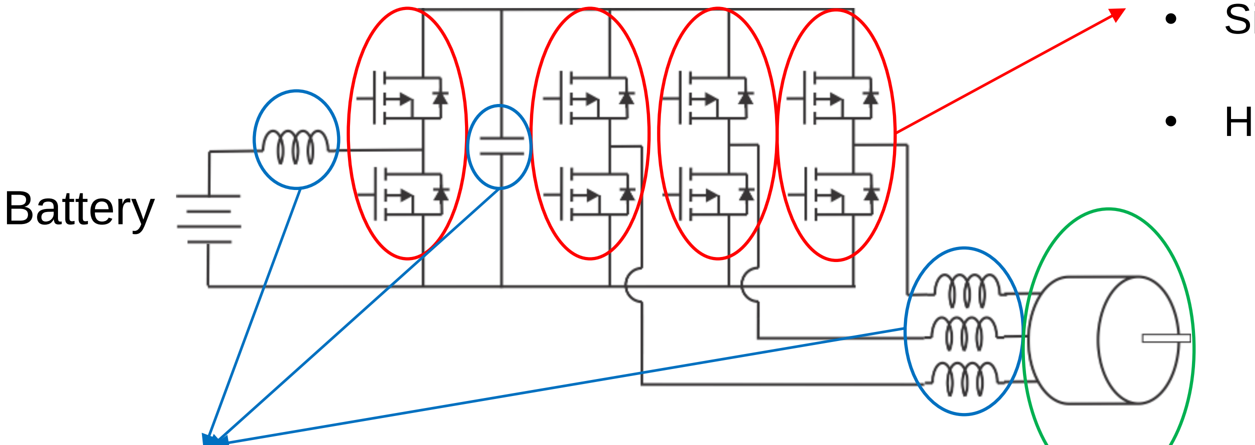
- Enabling advanced future Electric Traction Drive vehicles which contributes directly to clean energy transportation
- Wide bandgap (SiC and GaN) power devices enable higher power densities (reduced size and weight) and higher operating frequencies
- Higher operating frequencies enable size and weight reduction for passive devices (capacitors and inductors) in power circuits
- Efforts directly address technology barriers for power electronics and Electric Traction Drive power density targets

FY19 Milestones

Milestone	Date	Status
Simulate GaN-based diodes (Schottky diode and Junction barrier Schottky (JBS) diode). Demonstrate growth/fabrication processes for realization of devices.	10/2019	On Track
Evaluate state-of-the-art SiC power devices and identify gaps	4/2019	In Progress
Evaluate state-of-the-art passive components and identify gaps	4/2019	In Progress
Design and fabricate advanced test-bed to evaluate components in realistic operating scenarios	10/2019	On Track

Approach – System Level View

- Power Electronic Devices:
  - SiC or GaN-based
    - Higher critical elec. field
  - Higher frequency operation
    - Increased power density
    - Reduced size/weight



- Passives for Power Electronics
  - Composite materials for improved inductors
  - Improved capacitor lifetime, operating modes
  - Higher frequency operation
  - Reduced size/weight

- Advanced Motor Designs:
  - Increased power density
  - Higher speed operation
    - Reduced size/weight

- Characterization efforts at each point in the system:
  - Power electronic devices, passives, motors
- Sandia National Labs efforts span multiple levels within system design

Approach – Materials for Power Electronics

SiC Power Electronics (Short Term)

- 2019: Evaluate reliability and ruggedness of COTS SiC parts. Design for reliability SiC MOSFET.
- 2020: Fabricate improved SiC MOSFETs. Characterize in 10kW, 3Φ inverter system.
- 2021: Iterate design and fabrication learning. Evaluate reliability.

GaN Power Electronics (Long Term)

- 2019: Diode modeling and simulations. Process Development
- 2020: MOSFET Simulations Schottky/JBS Diode Test
- 2021: Schottky/JBS Improvement MOSFET Fab and Test

Passives for Power Electronics

- 2019: Design HALT for capacitors. Demonstrate Fe_4N/glass composite inductor.
- 2020: Demonstrate HALT tester and begin testing. Improve/test inductors
- 2021: Study freq. response of Oxygen vacancies. Evaluate inductors in test bed

2019 2020 2021 2022

Any proposed future work is subject to change based on funding levels.

Approach - SiC based Power Electronics

- SiC is still young … but several Electric Traction Drive products have recently featured SiC devices
- Improving the performance of SiC devices is likely to increase its adoption
- Achieve interim project goals within project timeline

PD550 Si IGBT Inverter
9 kW/L

Gen-1 SiC Inverter
18 kW/L
- **Requires 1/3 the space**

Approach: GaN-Based Power Electronics

Follow successful commercial model of **staged** device integration from Si + SiC development

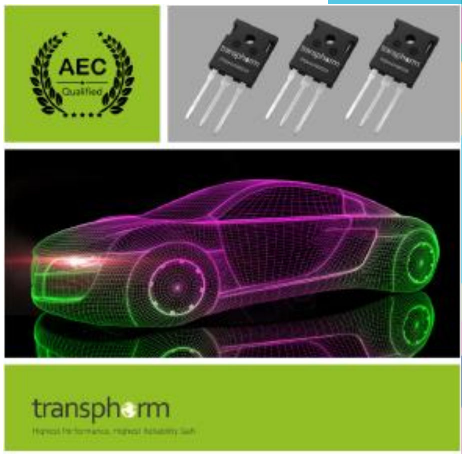
Stage 1: SiC MOSFET + SiC Diode

Device modeling, circuit simulation at each stage.

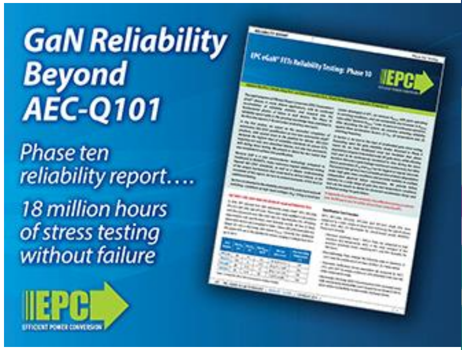
Stage 2: SiC MOSFET + GaN Diode

Characterization and evaluation of device technology in test bed at each stage.

Stage 3: GaN MOSFET + GaN Diode



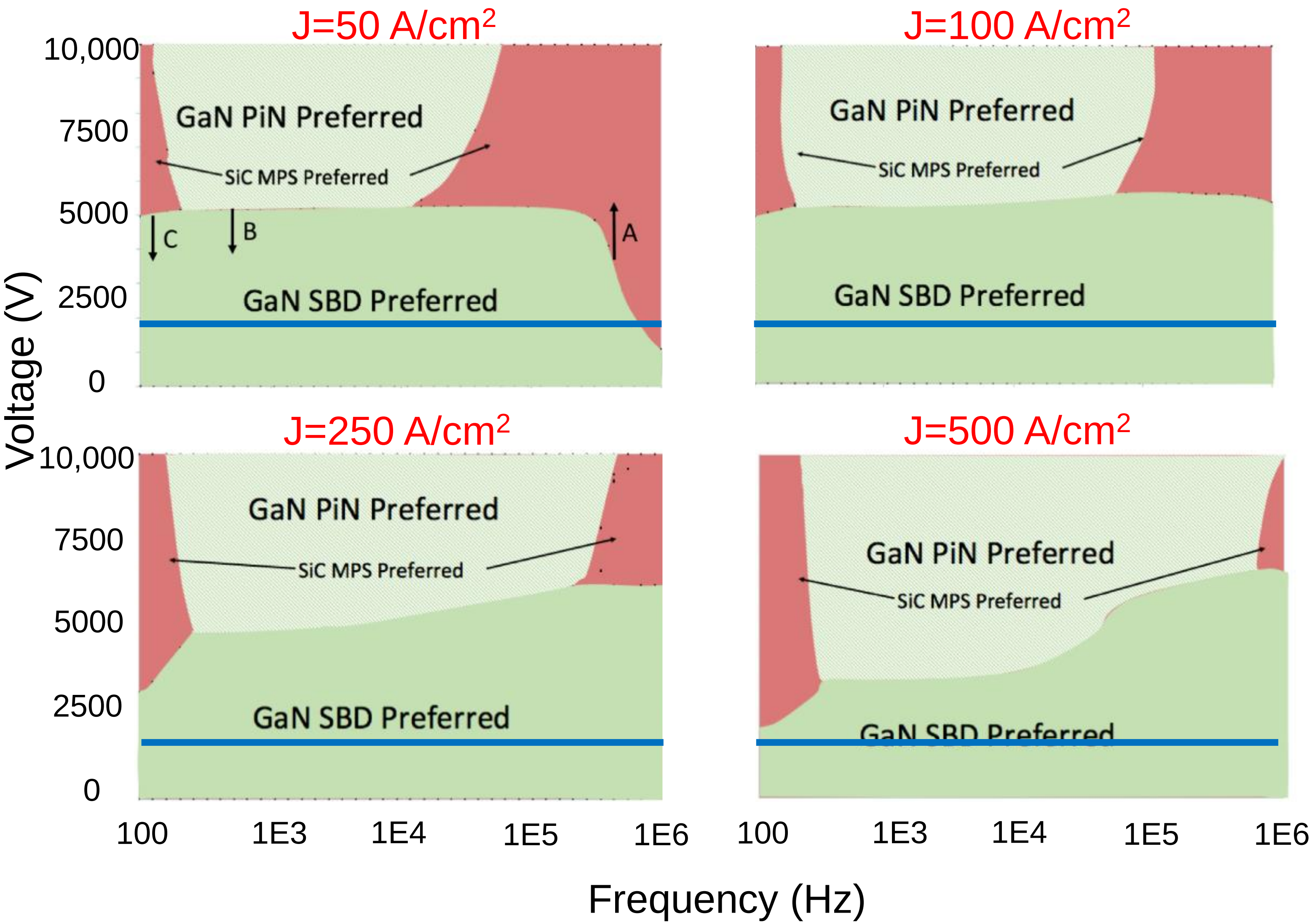
Second Line of AEC-Q101-qualified GaN FETs Now Offered at 175°C



EPC GaN FETs show excellent device reliability (AEC-Q101 qualified)

Approach: GaN-Based Power Electronics

System evaluation of **diode power dissipation vs. diode type** for given operating regime (reverse voltage, forward current density, frequency), T=300K



Lower Ron for GaN SBD and JBS diodes drive expected performance benefits

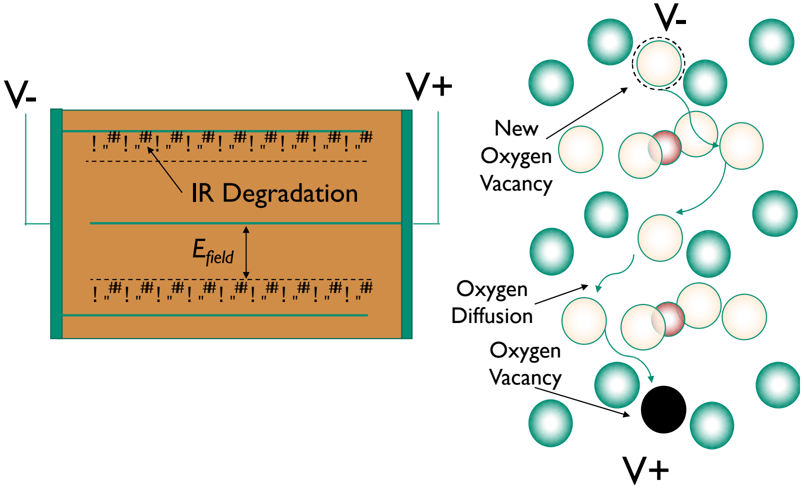
Target operating regime for power electronics: 1200 V/100 A (blue line)

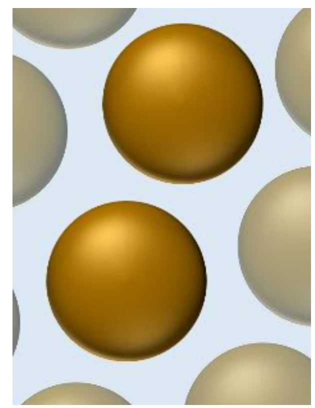
J. Flicker and R. Kaplar, IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Albuquerque, NM, 2017.

Approach: Passive Materials for Power Electronics

Innovate passive materials for high frequency power electronics systems

- Improve ceramic capacitor performance and reliability
- Increase frequency and reduce size of inductors
- Increase power density through integration (vs. discrete components)





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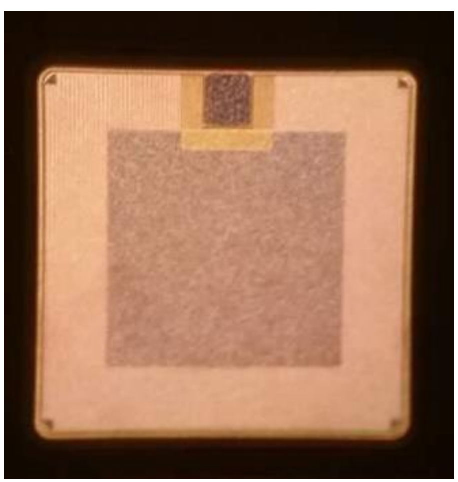
- **Ceramic capacitors aging caused by oxygen diffusion toward anode and accumulation of oxygen vacancies at cathode**
- **Bipolar switching at ~10x the rated voltage and 125°C above the rated temperature can increase the time to failure**

- **Inductor designs improved with designed Fe_4N composites**
  - **Smaller size**
  - **Higher frequency operation**
  - **Operating temperatures up to 200 C**

Technical Accomplishments and Progress - SiC

- SiC is one path to Power Electronics target **(short term)**
  - SiC has some commercial maturity and a larger manufacturing base
- SiC device designs currently not targeting automotive applications
  - Cost emphasized over reliability
  - High temp. operation causes issues with threshold voltage < 1 V at 150C (junction temp.)
  - Gate oxides designs, channel length designs not optimized for automotive environment
- Change focus to ***"design for reliability"*** within cost targets
- Design Advanced Component Test-Bed – Ongoing at Sandia (poster)
  - Characterize new device designs with relevant use scenarios

MOSFET Die



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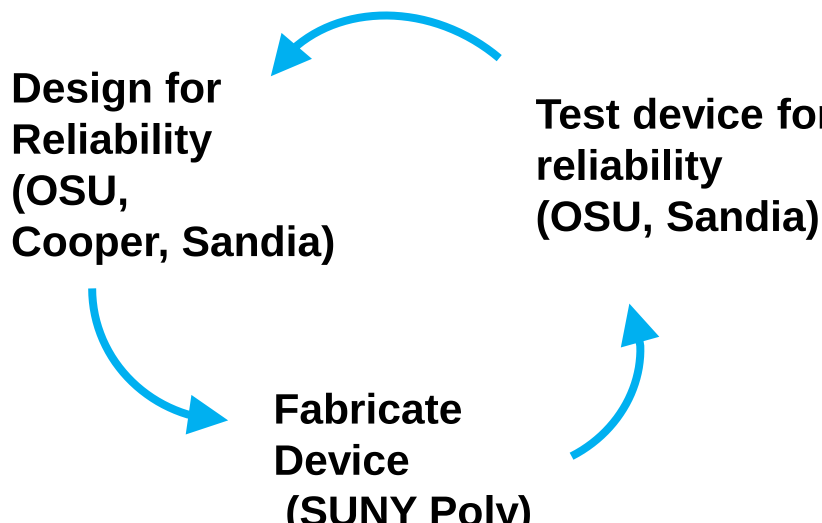
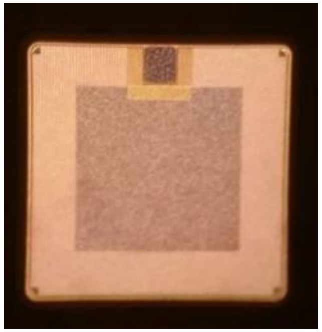


Technical Accomplishments and Progress - SiC

COST and RELIABILITY GOALS are achievable by 2025

Estimates of chip cost for a 1.2 kV/100 A MOSFET with an integrated JBS diode (chip size 6 mm × 6 mm)



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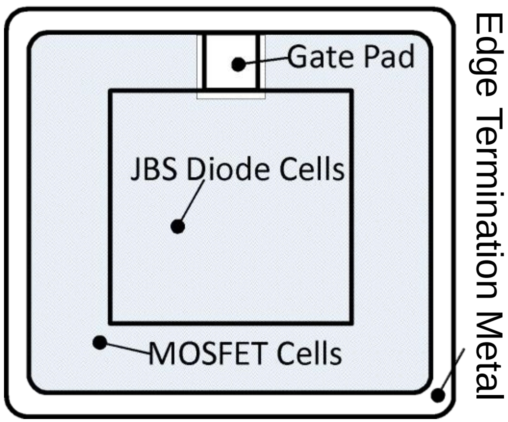
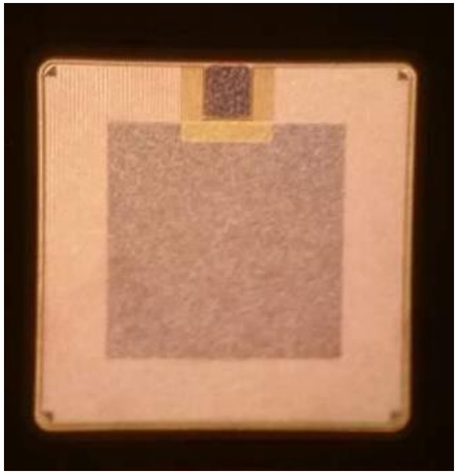
	R&D Phase (2018)	Low volume (2020) 10,000 chips per year	Moderate volume (2023) 1 million chips per year	200mm substrate with Moderat volume (2023~)
Cost per Amp	27¢/Amp	10¢/Amp	2.8¢/Amp	1.85¢/Amp
Cost of 150 mm SiC substrate	$2500	$1700	$500	$750
Process cost per wafer	$5000	$1500	$500	$500
Cost per 100 A die	$27	$10	$2.8	$1.85
Total number of chips on a wafer excluding a 2 mm zone around the substrate	400	400	400	750
Yield	70%	80%	90%	90%
Number of functional die per wafer	280	320	360	675

Technical Accomplishments and Progress - SiC

SiC device manufacturing: SUNY Poly

- Reliability/Ruggedness evaluation of COTS and SUNY Poly devices
  - Ohio State University
- Evaluate devices in 10kW, 3 phase inverter system
  - Stress devices in realistic drive cycle scenario (e.g. 10 min hill climb)
- Devices fabricated by State University of New York Polytechnic Institute (SUNY Poly)
  - High performance, highly reliable 900-1700 V SiC JBS diode integrated MOSFETs
  - Devices to be fabricated at commercial foundry





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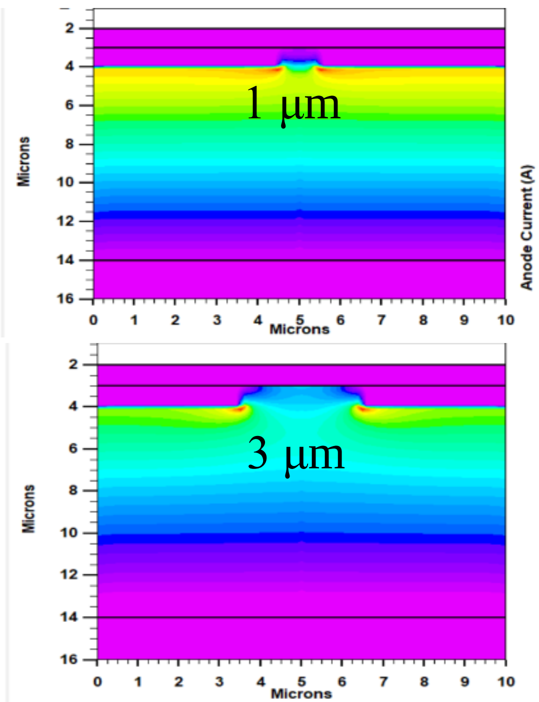
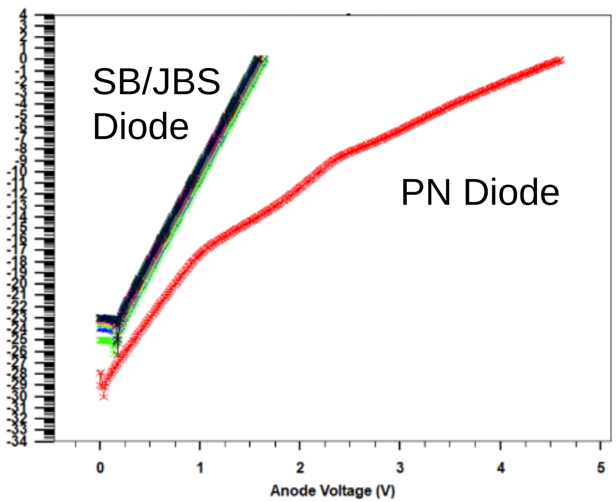
Technical Accomplishments and Progress - GaN

- Vertical GaN devices is another path to Power Electronics target (Long Term)
  - **Higher Performance and Larger Design Space**
- Decision to focus resources in first year on the vertical GaN diode
  - Allows staged combination with SiC transistors.
  - Schottky Barrier (SB) diodes and Junction Barrier Schottky (JBS) diodes
- Modeling/Simulation is underway
  - Developed SB diode models in Silvaco simulation software
  - JBS diode models are under development

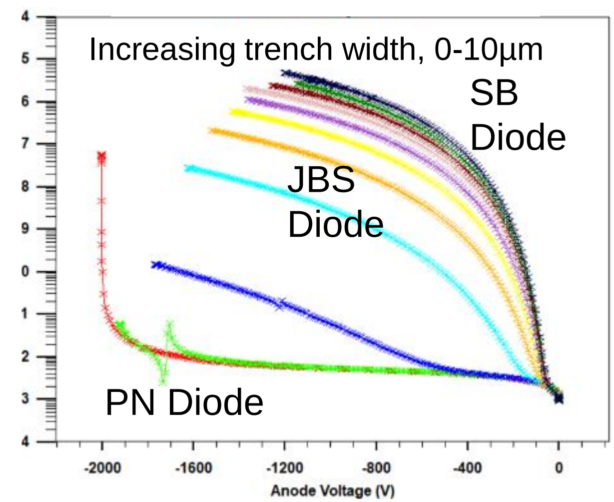
E-field – Planar JBS



JBS - Forward IV



JBS - Reverse IV

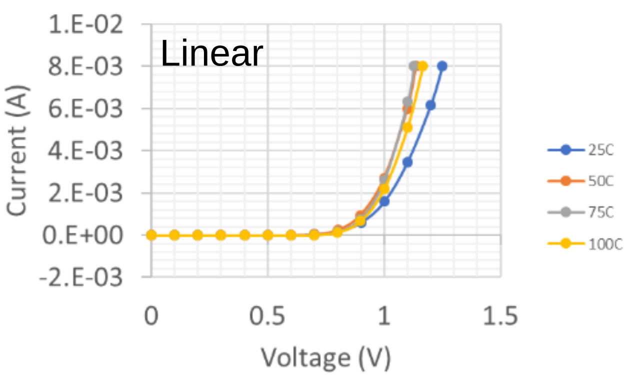


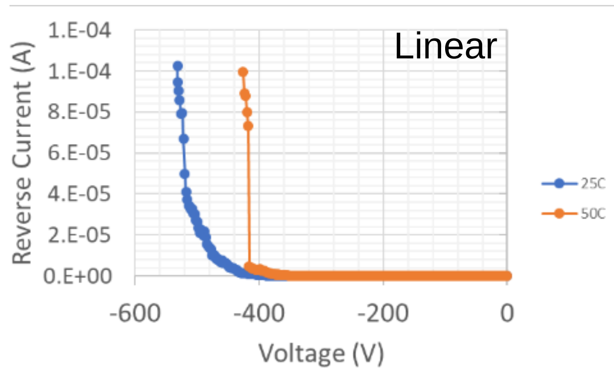
FY19 Milestone for SB and JBS Diode simulation: ON TRACK

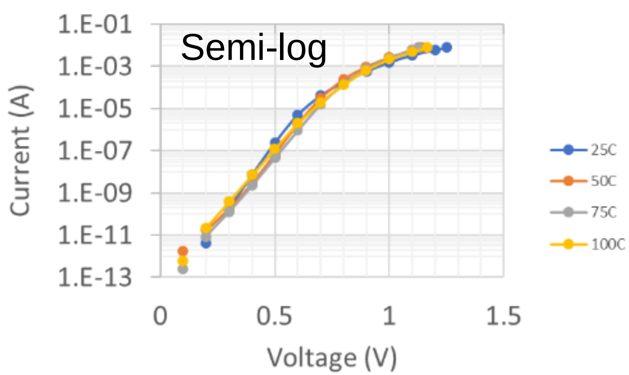
Technical Accomplishments and Progress - GaN

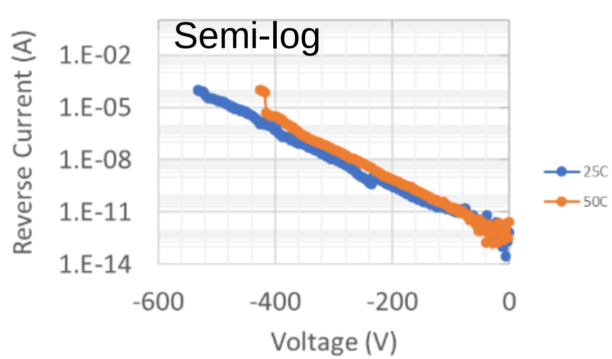
- Gen1 GaN SB Diodes **demonstrated**
  - SB diodes being characterized and used to calibrate models
  - Focus on good Schottky/Metal interface on Gen1 devices, not on breakdown voltages
- Mask designs for JBS diode development **completed**
  - Exploring different design strategies
  - Using SiC devices to understand current scaling methods

SB Diode IV over Temperature

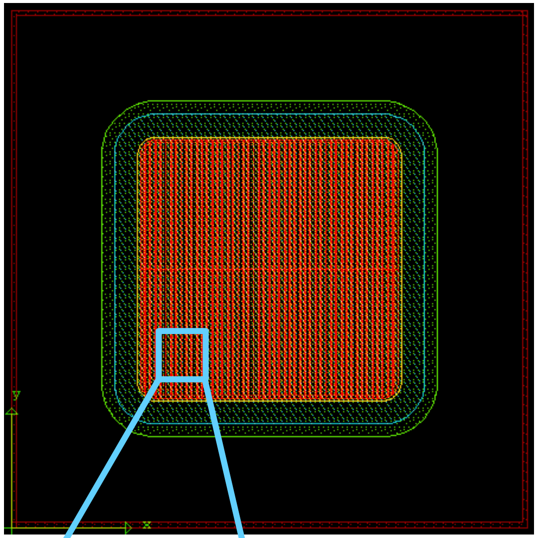


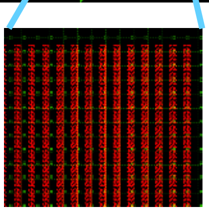






JBS Diode Mask





Trench design for alternating p- and n-GaN layers

FY19 Milestone for GaN Process Development: ON TRACK

Responses to Previous Year Reviewers' Comments

- Sandia's first year on this program
- No previous comments

Collaboration

SUNY Poly Albany Campus

Oak Ridge National Laboratory – Collaborating partner for Electric Traction Drive integration and evaluation.

National Renewable Energy Laboratory – Collaborating partner for Electric Traction Drive integration and evaluation.

State University of New York (SUNY) (Woongie Sung) – Fabricating SiC JBS diode integrated with MOSFETs. (Subcontractor)

Ohio State University (Anant Agarwal) – Designing for improved reliability for SiC electronics. Evaluate reliability and ruggedness of commercial and fabricated devices using realistic scenarios. (Subcontractor)

Jim Cooper– Working with OSU for SiC device evaluation. Working with Sandia for GaN power electronic device design and characterization. (Subcontractor)

Lehigh University (Jon Wierer) – Working with Sandia for design/simulation/modeling of GaN SB and JBS diodes. (Subcontractor)

Remaining Challenges and Barriers

SiC Devices

- Designs need to be optimized for automotive environments
- Multiple iterations needed to understand performance/reliability/cost tradeoffs

GaN Devices:

- Immaturity of GaN devices requires multiple cycles of learning to develop and optimize device performance
- MOSFET development to follow behind JBS diode development

Passives

- Immaturity of technology requires further development and understanding

Proposed Future Research

SiC:

- FY19-20:
  - Evaluate COTS devices for reliability and ruggedness
  - Initiate "design for reliability" efforts
  - Initiate SiC device fabrication and evaluation
- Rest of project:
  - Focus on Design and Test for Reliability
  - Fabricate devices based on Design for Reliability
  - Evaluate performance against Consortium targets
  - Utilize devices in Gen1 prototype Electric Traction Drive

Passives:

- FY19-20:
  - Design and build HALT tester for capacitors.
  - Demonstrate Fe_4N/Glass composite inductor
- Rest of project:
  - Refine materials for passives for highly integrated, high frequency solution
  - Evaluate reliability of capacitors and inductors
  - Develop path for production of passive components

GaN:

- FY19-20:
  - Refine SB and JBS diode modeling efforts
  - Improve SB GaN diode performance
  - Demonstrate GaN JBS diodes
  - Initiate GaN MOSFET modeling and process development
- Rest of project:
  - Iterate to improve GaN SB and JBS diode performance against targets (1200 V/100 A)
  - Combine with SiC MOSFET in circuit for evaluation
  - Demonstrate GaN MOSFET device performance
  - Iterate to improve GaN MOSFET performance against targets (1200 V/100 A)
  - Combine GaN MOSFET and JBS diode in circuit for evaluation

Any proposed future work is subject to change based on funding levels.

Summary

- Systems level view of the project identified key areas for performance improvement in power electronics:
  - Wide bandgap power devices – evaluate SiC and vertical GaN devices
  - Passive devices

- SiC device improvement will be driven through “design for reliability” approach with performance metrics for reliability and cost in mind

- GaN device development is underway
  - GaN diode simulation and modeling in process
  - Schottky Barrier (SB) diodes demonstrated and used to refine models
  - GaN process development underway for JBS diode fabrication

- Passive component (capacitors and inductor) development is underway
  - Reliability evaluation of ceramic capacitors with different operation modes is in design.
  - Fe_4N/Glass composite inductor materials are in development.