Advanced Power Electronics Designs – Reliability and Prognostics

(Keystone Project 1)

PI: Douglas DeVoto
National Renewable Energy Laboratory
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DOE Vehicle Technologies Program
2019 Annual Merit Review and Peer Evaluation Meeting

ELT218

Overview

Timeline

- Project start date: FY19
- Project end date: FY21
- Percent complete: 15%

Barriers

- Barriers addressed
  - Cost
  - Performance
  - Reliability and Lifetime

Budget

- Total project funding: $175K
  - DOE share: $175K
- Funding for FY19: $175K (new start)

Partners

- Interactions/collaborations
  - Oak Ridge National Laboratory (ORNL)
  - Indiana Integrated Circuits (IIC)
  - DuPont
- Project lead
  - National Renewable Energy Laboratory (NREL)

Relevance

- Wide bandgap (WBG) packaging designs must thermally allow for:
  - Higher operating temperatures
  - Higher heat fluxes/power densities
  - Hot spots
- Coefficient of thermal expansion (CTE) mismatch between layers of the module will impose stresses that can initiate and propagate defects:
  - Attach layer fatigue
  - Interconnect fatigue
- **New package designs must address thermal and reliability concerns and be evaluated under accelerated conditions that approximate real-world conditions**

Approach

- **New package designs must address thermal and reliability concerns and be evaluated under accelerated conditions that approximate real-world conditions**
- NREL is closely working with ORNL and industry partners to evaluate new packaging materials and manufacturing techniques for wide-bandgap (WBG)-based traction inverters

IIC: Quilt packaging via a chip-to-chip edge interconnect technology

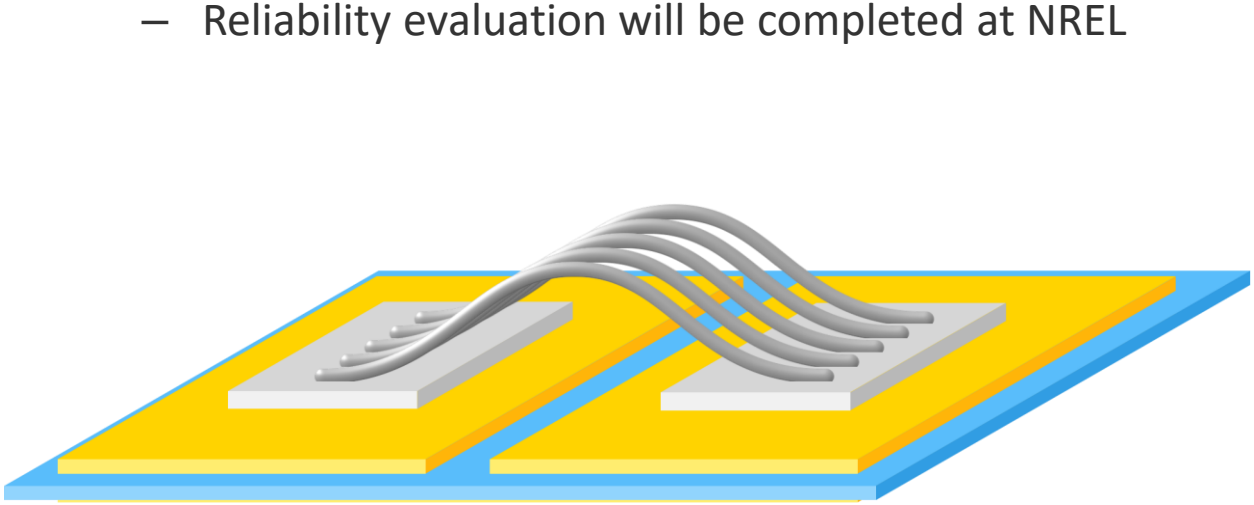
D: DuPont: Organic direct-bond-copper (ODBC) substrate as a replacement of ceramic substrates

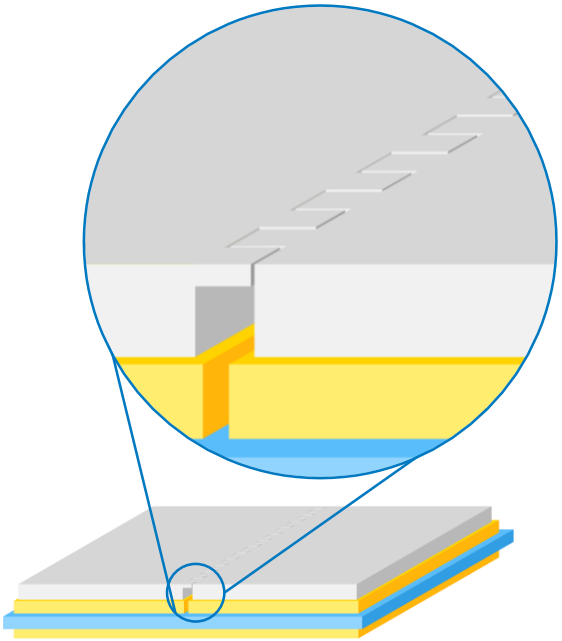
N: Prognostics work at NREL will continue to develop a remaining useful lifetime (RUL) tool that uses drive cycle input data for fatigue models for existing and future packaging designs

Approach

IIC

- Alternative interconnect designs are required as devices are reduced in size and spacing between devices is minimized
- **Traditional wire interconnects or etched substrates for topside electrical connections will be replaced with direct chip-to-chip connection**
- Devices are joined with quilt packaging, eliminating the need for wire bonds or other external electrical connection technology
  - Experimental samples have been designed in collaboration with IIC and ORNL
  - Reliability evaluation will be completed at NREL





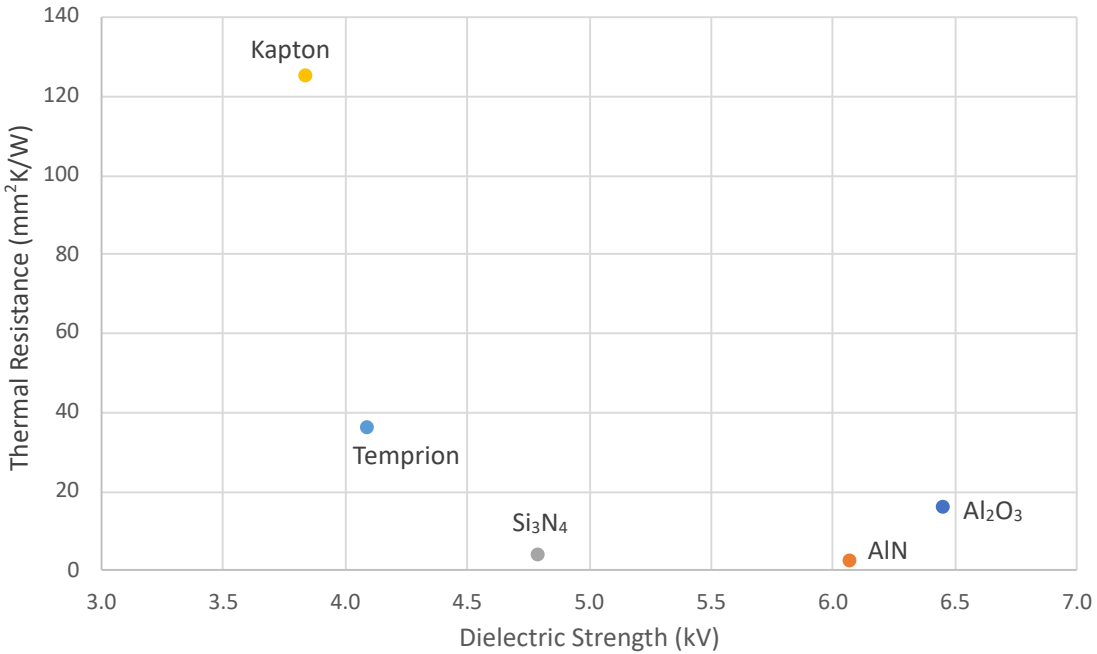
Approach

D

- **Alternative electrically insulated substrate designs are required to enable reliable packages that operate with higher power densities and higher temperatures**
- Traditional substrate technologies
  - Direct bond copper (DBC)
    - Oxidation of copper (Cu) foils during bonding lowers melt temperature from 1,083°C to 1,065°C
    - Maximum metallization thickness of 1 mm
    - Must have metallization layers on both sides of the ceramic
    - Examples include aluminum oxide (Al_2O_3), aluminum nitride (AlN), and zirconia (ZrO_2)-doped high-performance substrates (HPS)
  - Active metal bonding (AMB)
    - Brazing process with silver-copper (Ag-Cu) alloy between Cu and ceramic at 850°C in vacuum
    - Requires more processing steps and is more expensive than DBC
    - Silicon nitride (Si_3N_4) substrate is an example
- ODBC
  - A polyimide dielectric is bonded with metal through elevated temperature and pressure
  - No limitations in metal material or metallization thickness

Approach

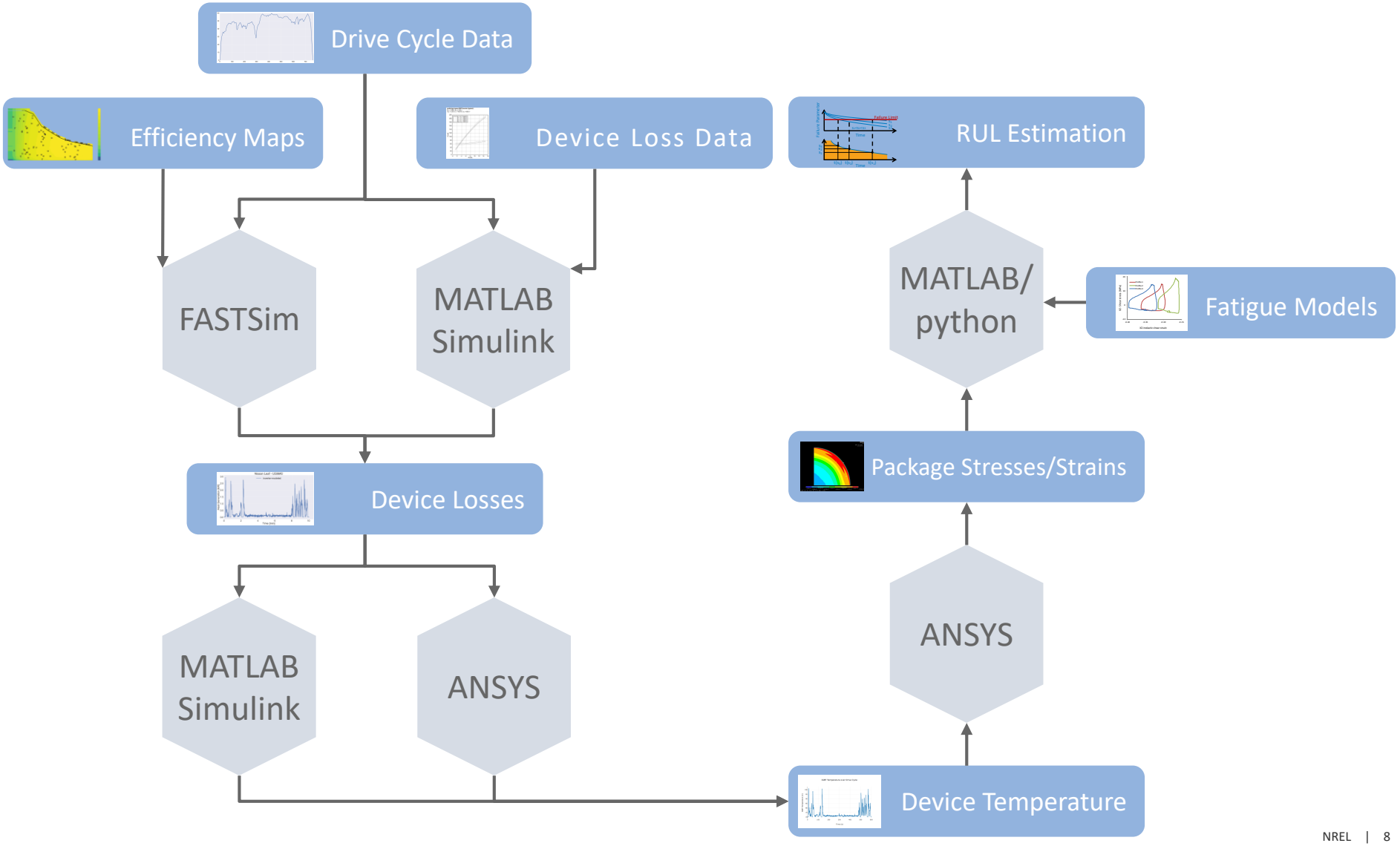
D



Insulator	Thickness (µm)	Dielectric Strength (kV/mm)	Dielectric Strength (kV)	Thermal Conductivity (W/mk)	Thermal Resistance (mm^2K/W)
Al_2O_3	380	17	6.5	24	16
AlN	380	16	6.1	180	2
Si_3N_4	320	15	4.8	90	4
Kapton	25	154	3.9	0.2	125
Temprion	25	164	4.1	0.7	36

Approach

- RUL tool will evaluate failure mechanisms using drive cycle inputs



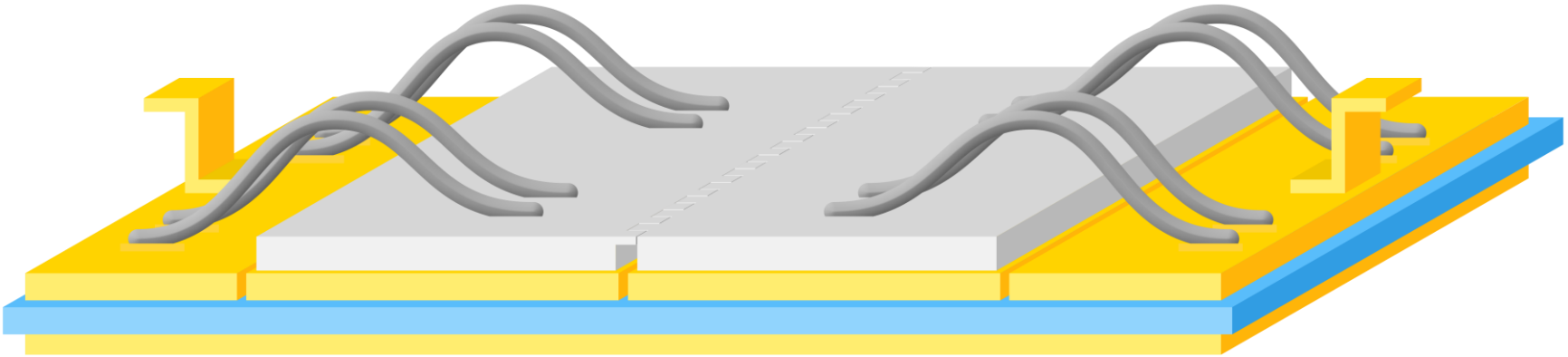
Milestones

Date/Status	Description
December 2018 *(complete)*	Milestone • With project partners, define new packaging technologies for evaluation, including thermal benefits/reliability risks.
March 2019 *(complete)*	Go/No-Go • Complete thermal modeling evaluation of select packaging technologies.
June 2019 *(in progress)*	Milestone • Characterize devices/packages under thermal aging and cycling conditions and monitor component health through electrical precursor measurements.
September 2019 *(in progress)*	Milestone • Prepare report on research results.

Technical Accomplishments and Progress

IIC

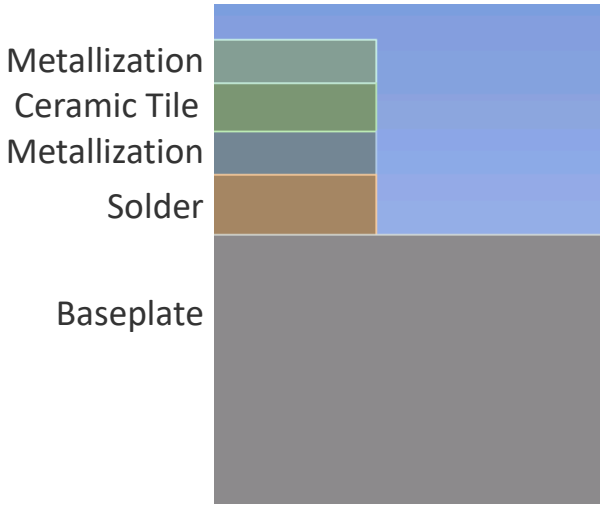
- In collaboration with ORNL and IIC, initial device geometry has been designed
- Devices will be mounted to substrates, and reliability of connections will be evaluated



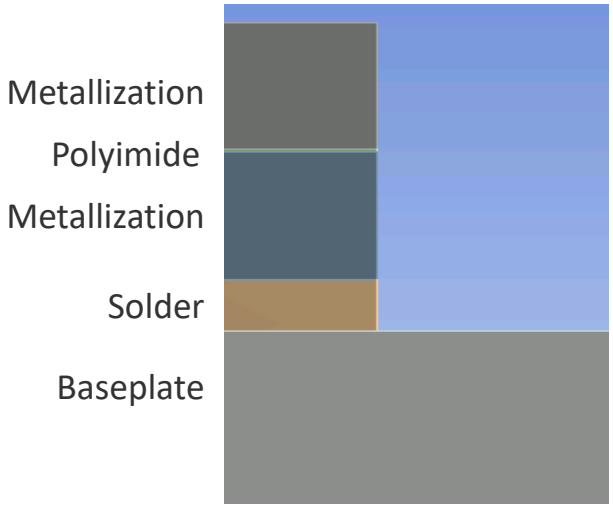
Technical Accomplishments and Progress

D

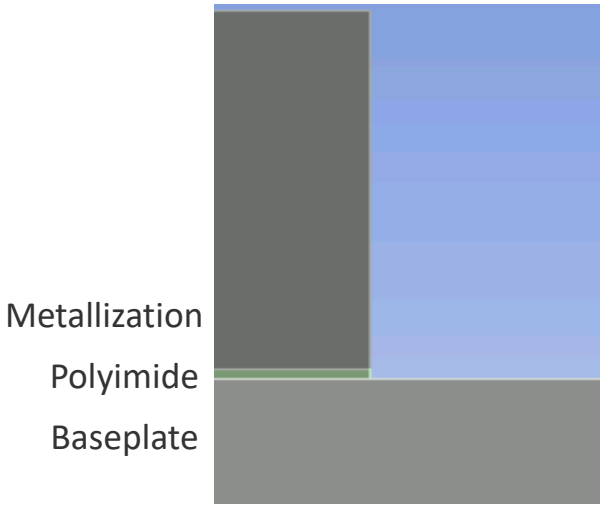
- Thermal impact of alternative DuPont ODBC substrate designs has been modeled



Industry Standard



ODBC Substrate



ODBC Simplified Substrate

Technical Accomplishments and Progress

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- Substrates placed between diode and cold plate
- A transient power pulse was applied to the package, and the decay of the temperature in the diode was monitored over time to establish the resistance-capacitance network for the package
- ODBC thermal performance similar to AlN

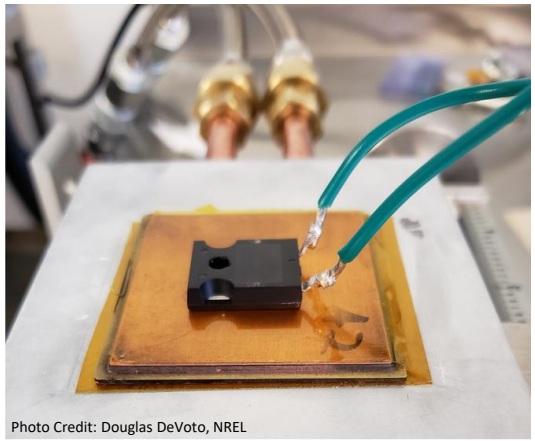
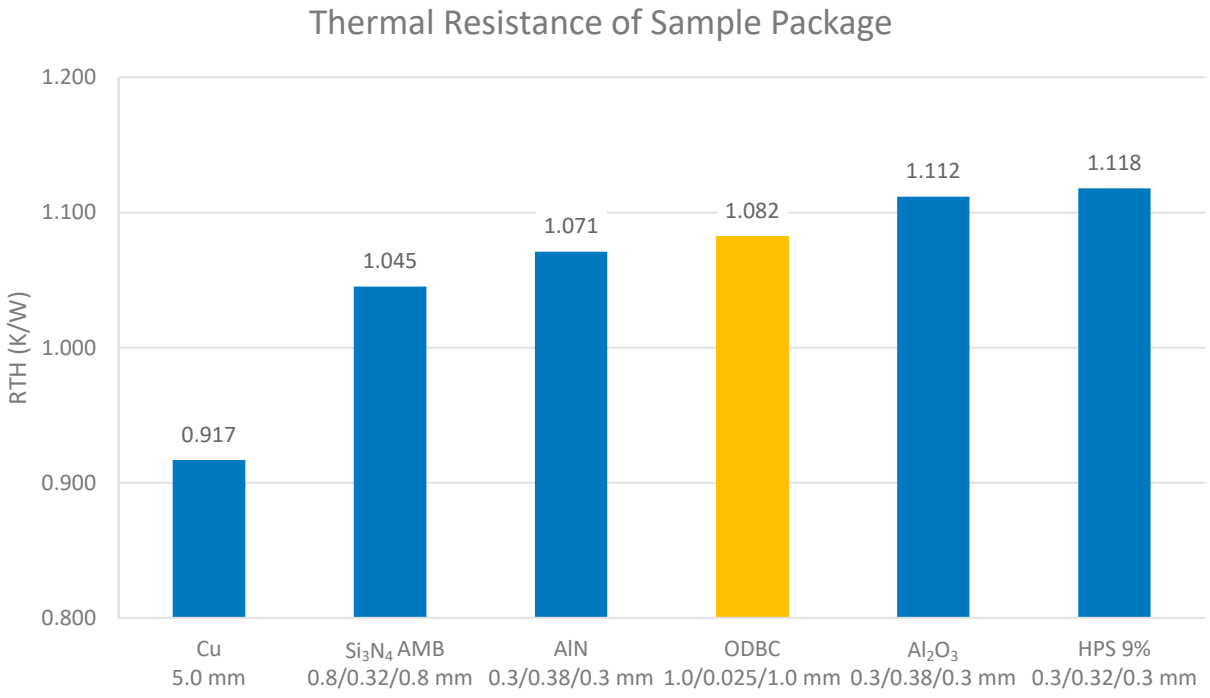
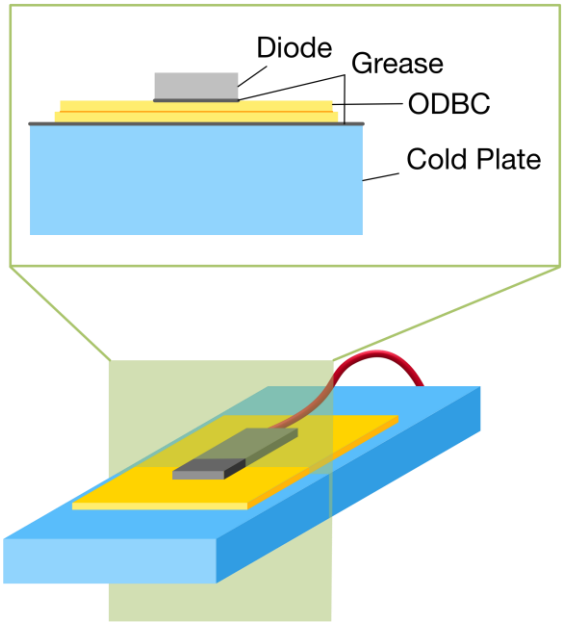


Photo Credit: Douglas DeVoto, NREL





T3ster Test Setup

Technical Accomplishments and Progress

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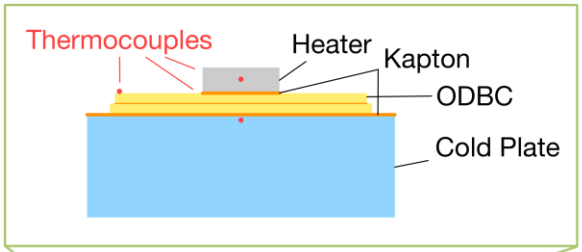
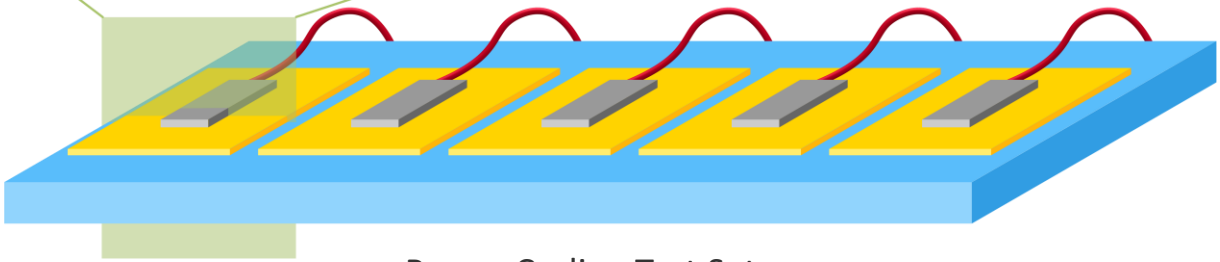
- Thermal Shock: -40°C to 200°C, 5-minute dwells
- Thermal Aging: 175°C
- Power Cycling: 40°C to 200°C
- ODBC substrates have reached 5,000 thermal shock cycles, 1,900 thermal aging hours, and 2,200 power cycles
- No significant decrease in electrical or thermal performance has been observed

Substrates Undergoing Aging





Power Cycling Test Setup

Technical Accomplishments and Progress

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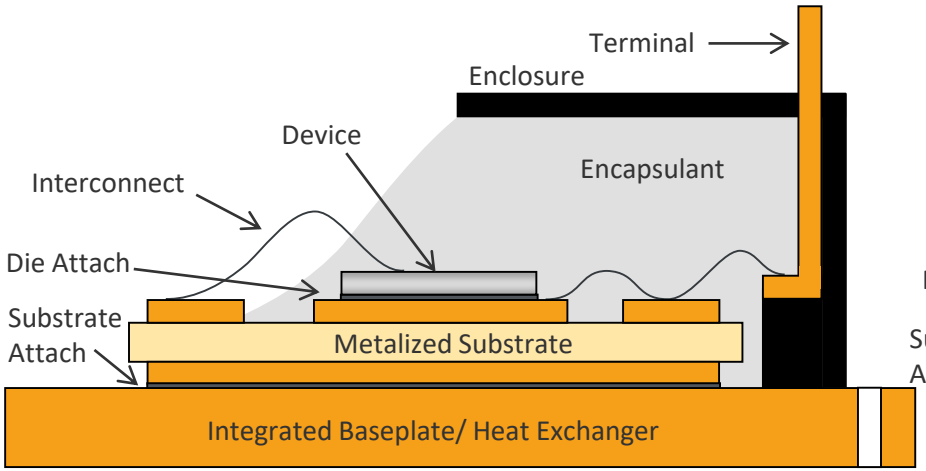
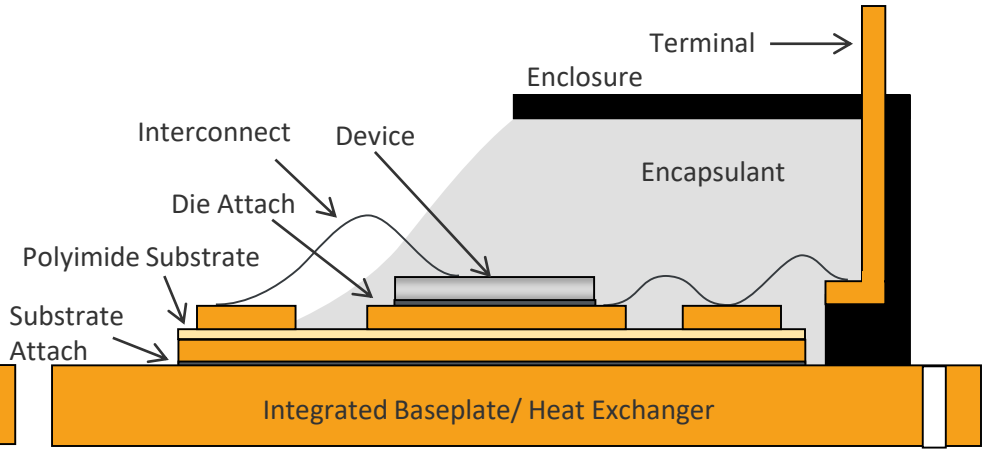
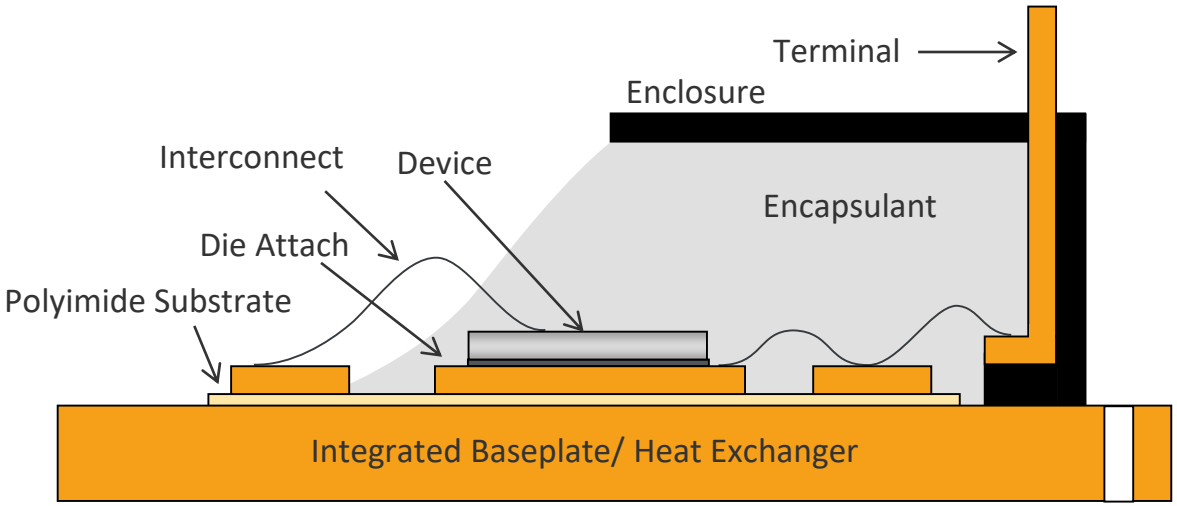
- Integration of ODBC substrate into a power module can enable thicker metallization layers or the elimination of the bottom metallization layer and the substrate-attach layer



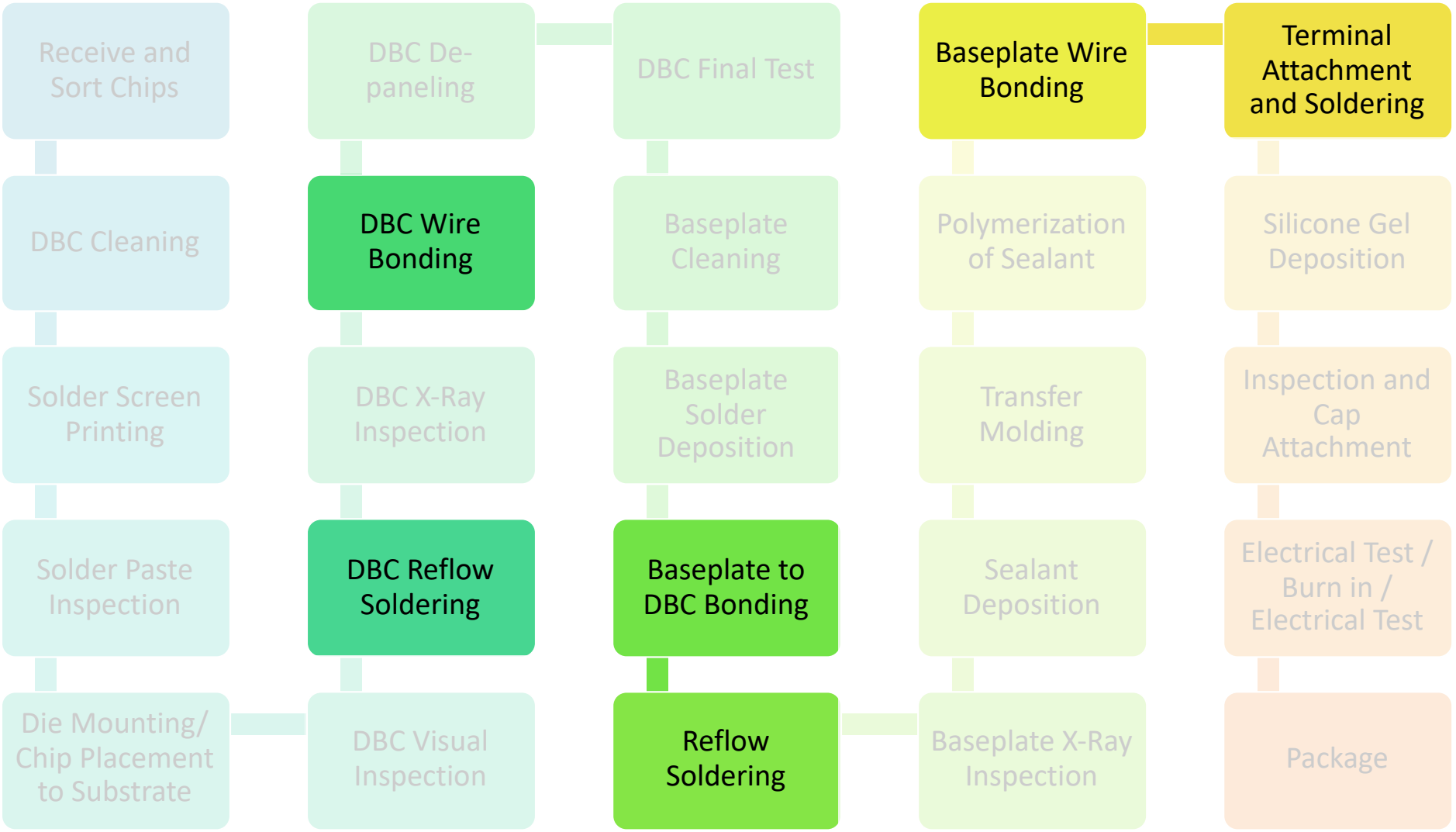




Technical Accomplishments and Progress

D

- Existing manufacturing process includes multiple bonding steps

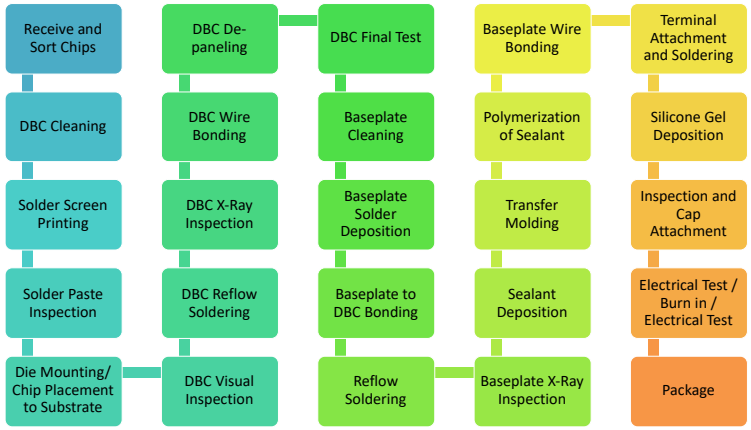


Horowitz, K., Remo, T., Reese, S. (2017). A Manufacturing Cost and Supply Chain Analysis of SiC Power Electronics Applicable to Medium-Voltage Motor Drives. Technical Report TP-6A20-67694, National Renewable Energy Laboratory. doi:10.2172/1349212.

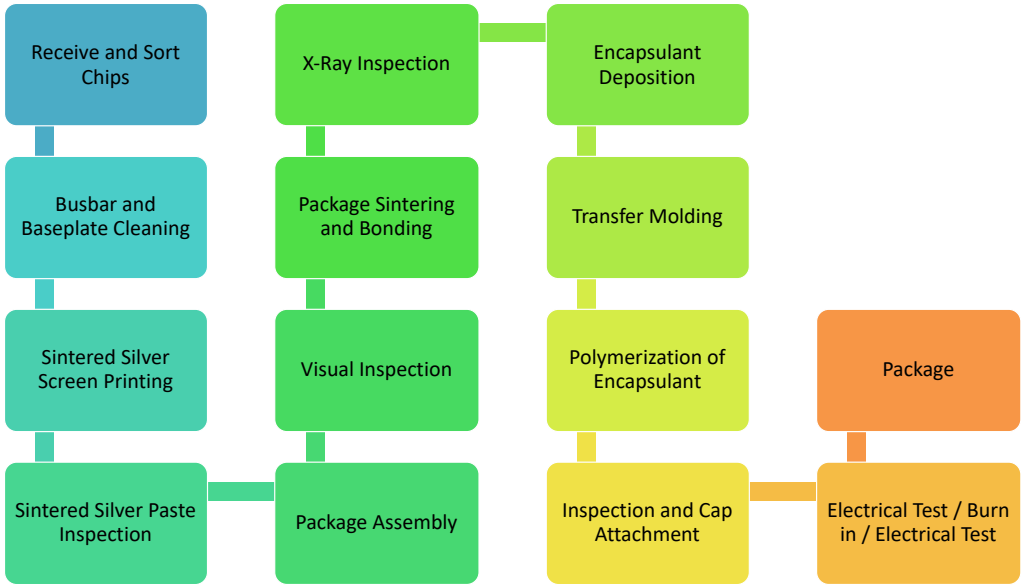
Technical Accomplishments and Progress

D

- Existing manufacturing process can be simplified and several assembly steps can be completed simultaneously with the new process

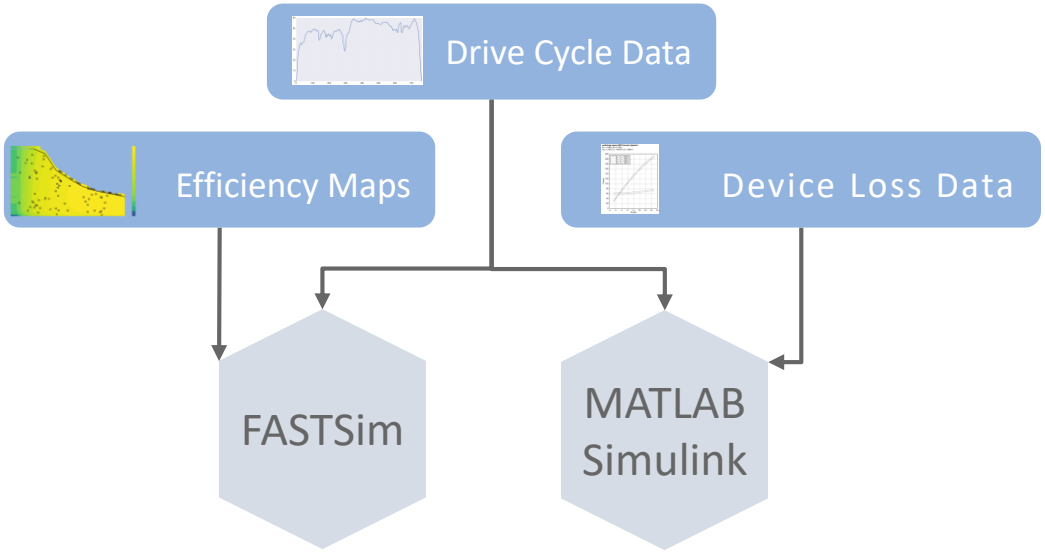


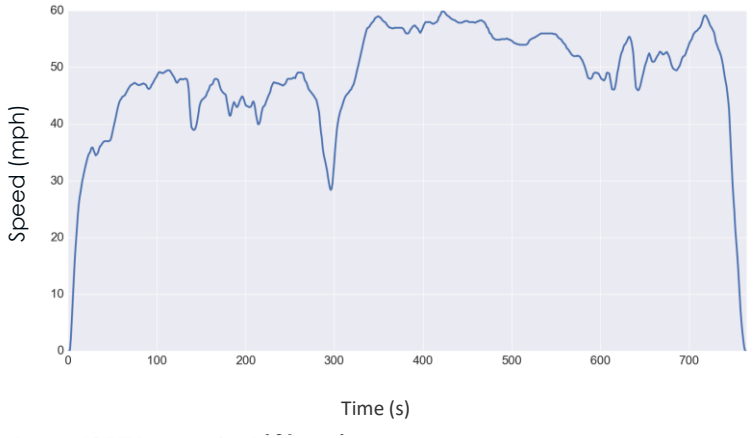
Existing Process

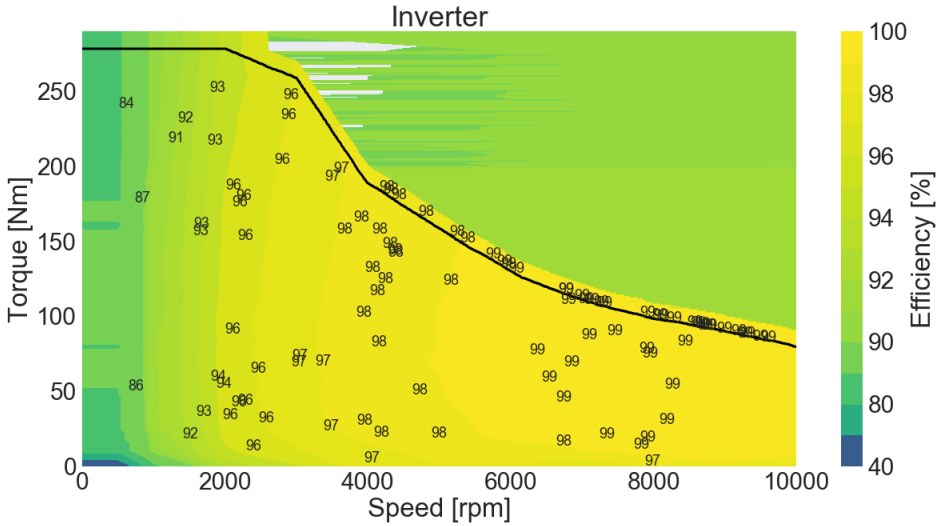


New Process

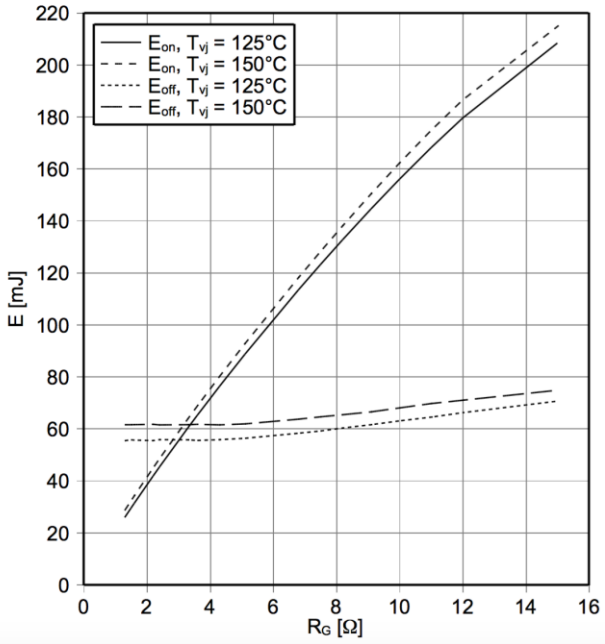
Technical Accomplishments and Progress







switching losses IGBT,Inverter (typical)
$E_{on} = f(R_G)$, $E_{off} = f(R_G)$
$V_{GE} = \pm 15$ V, $I_C = 450$ A, $V_{CE} = 600$ V



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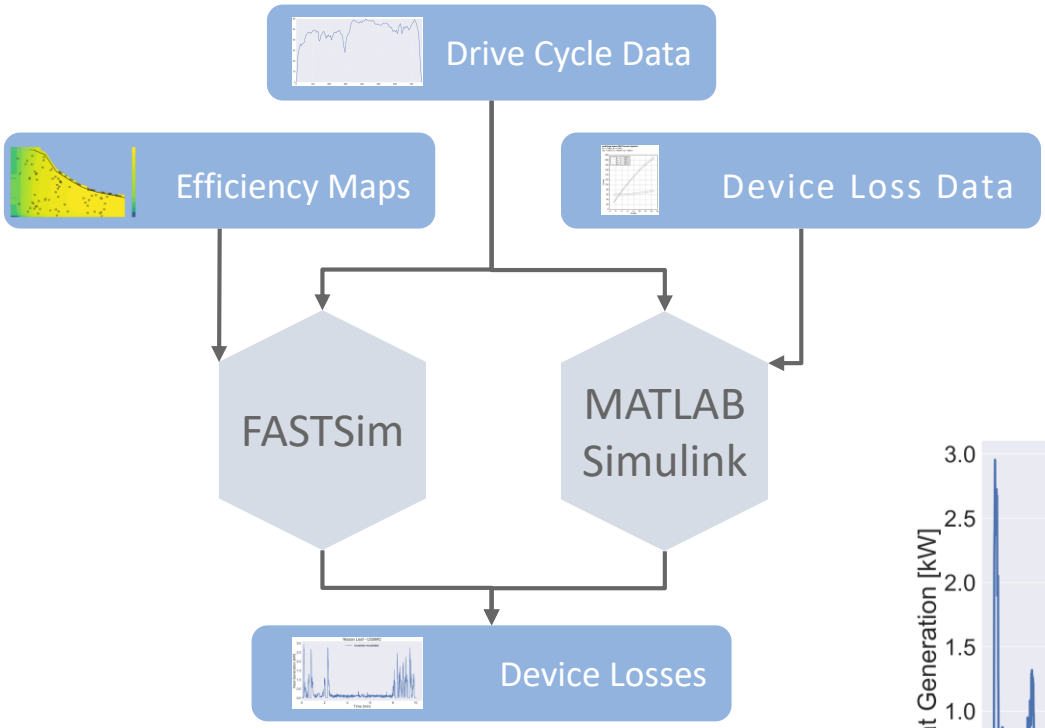

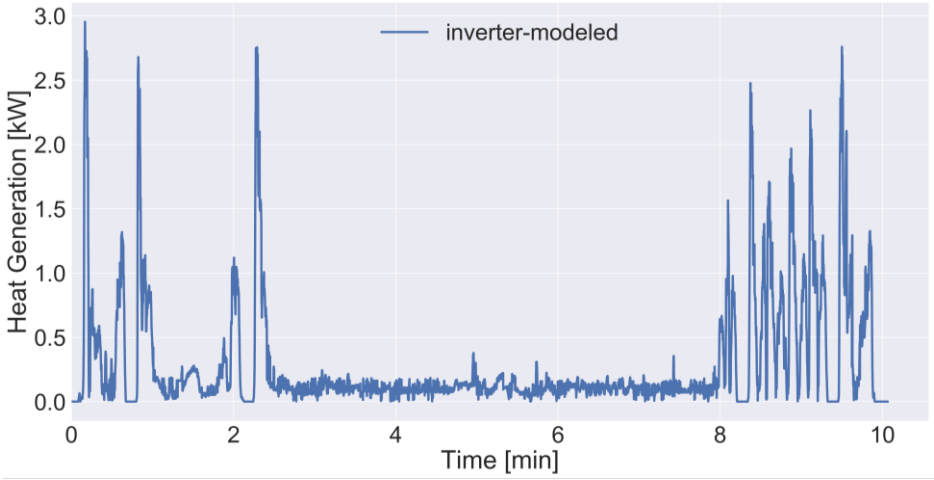

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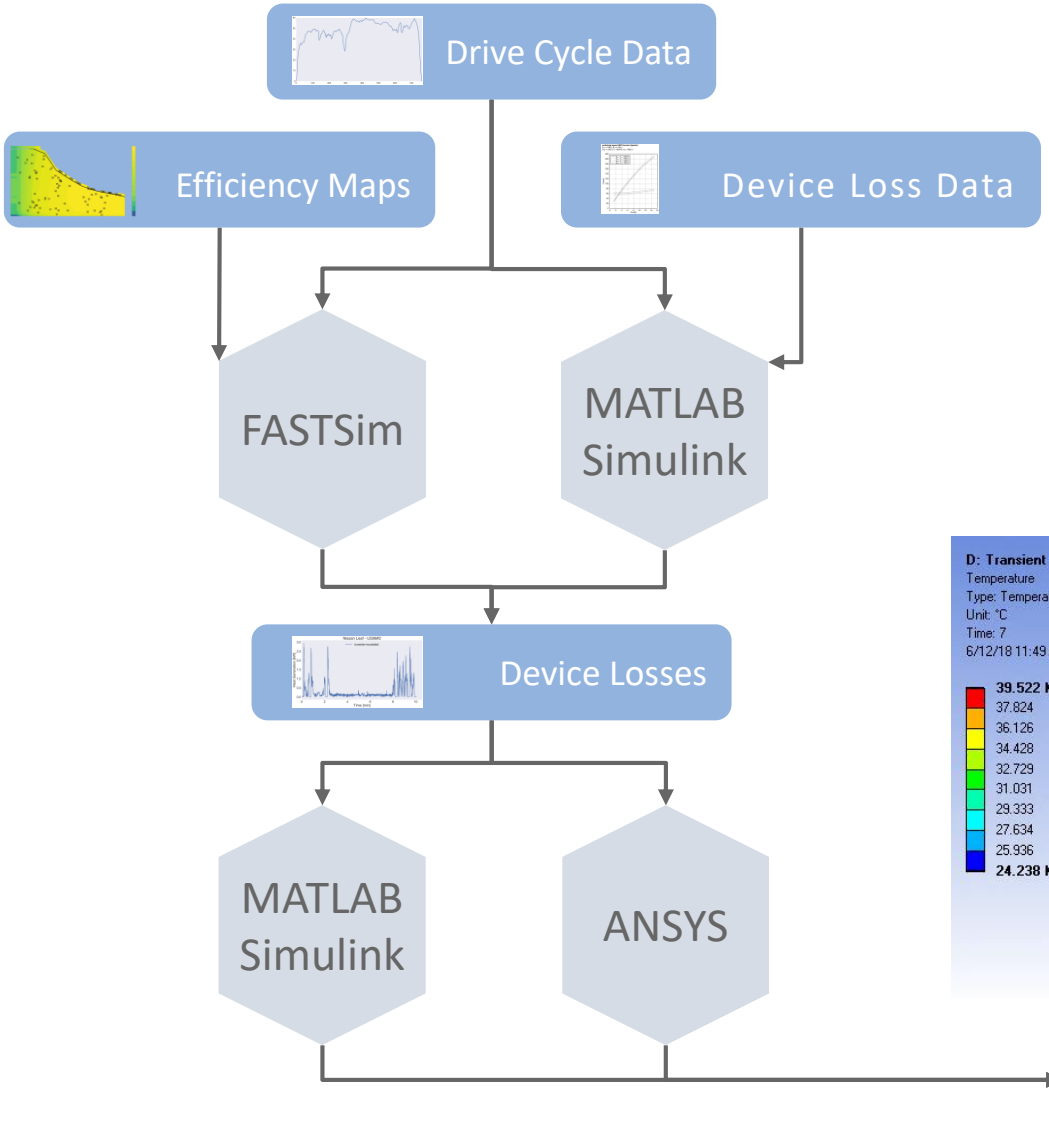

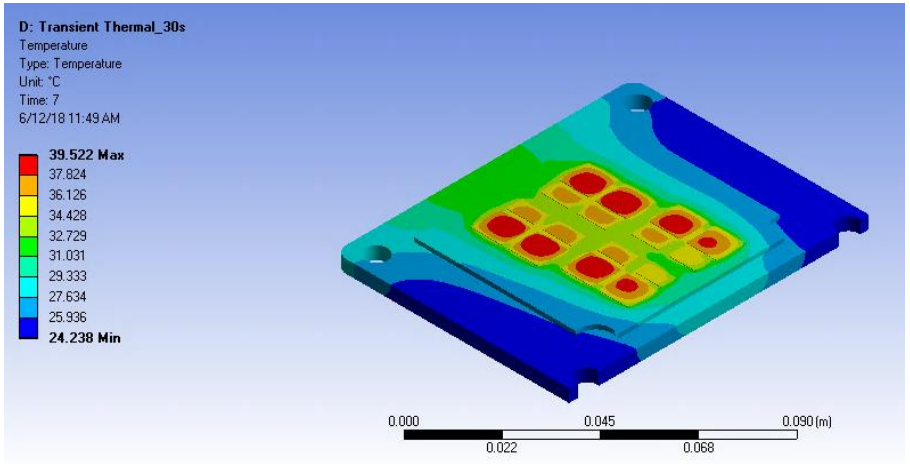

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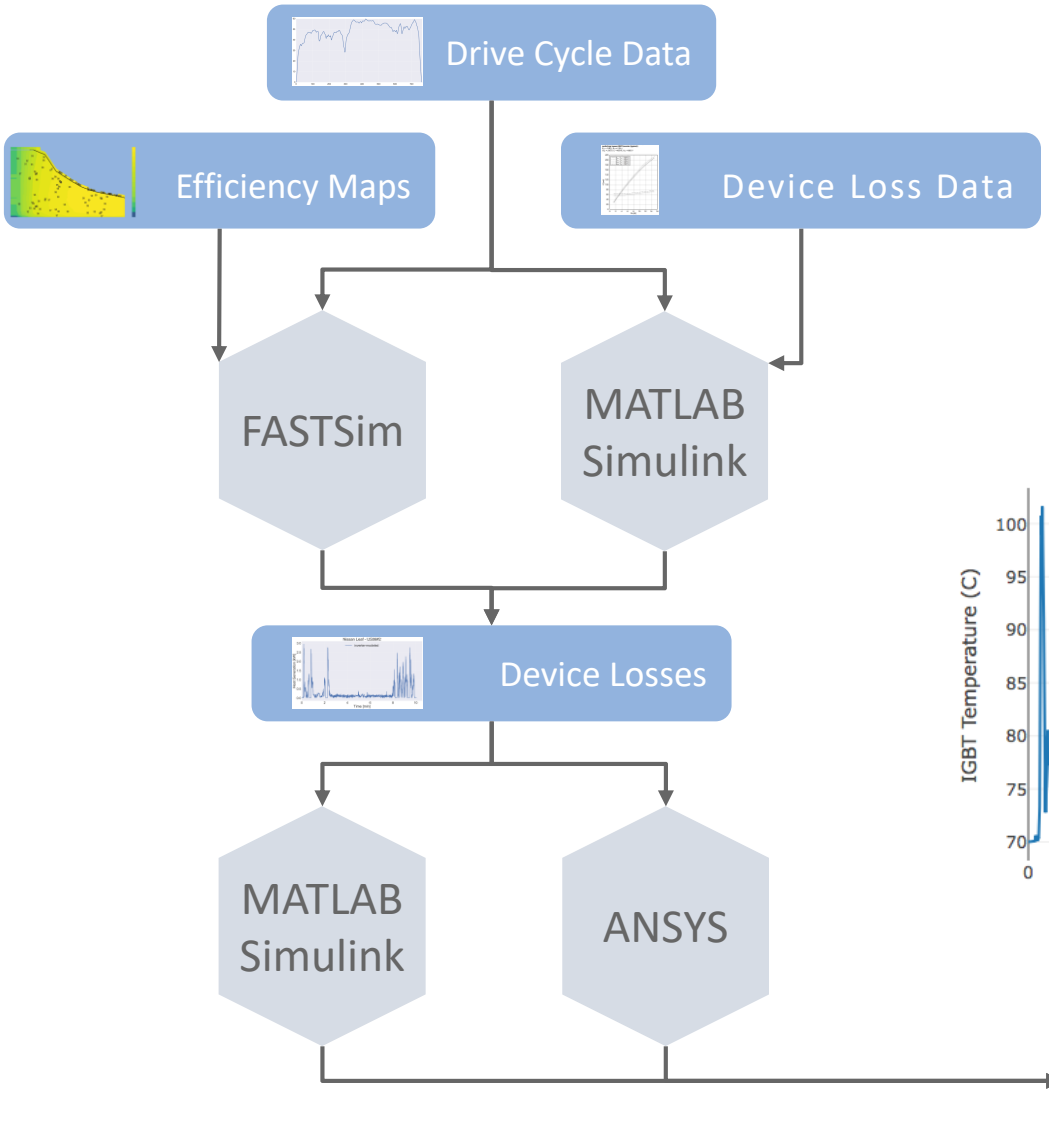

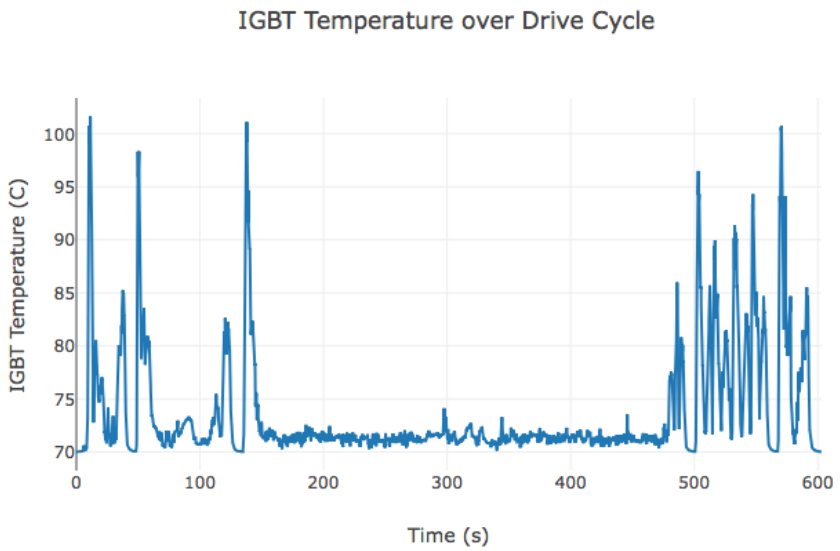

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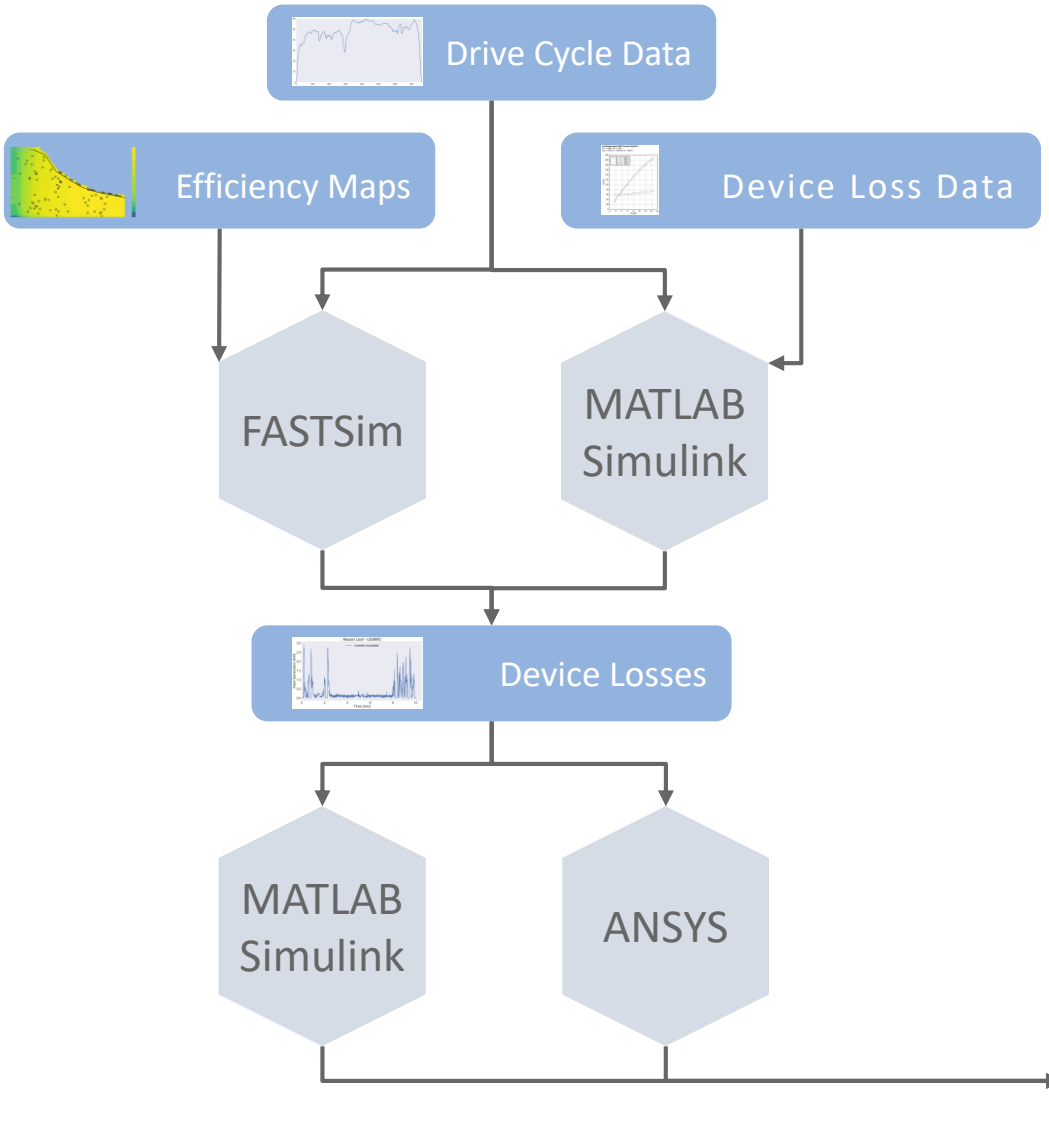

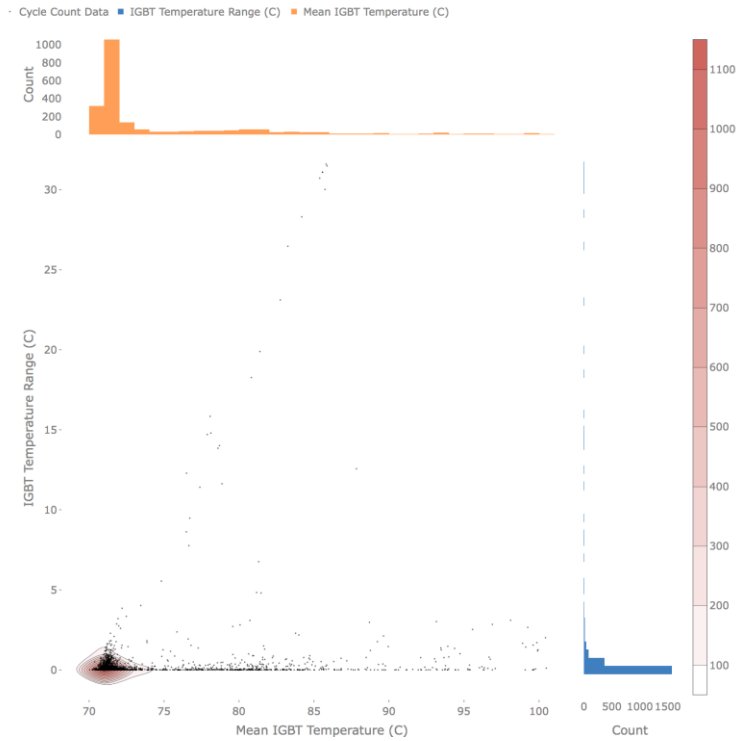

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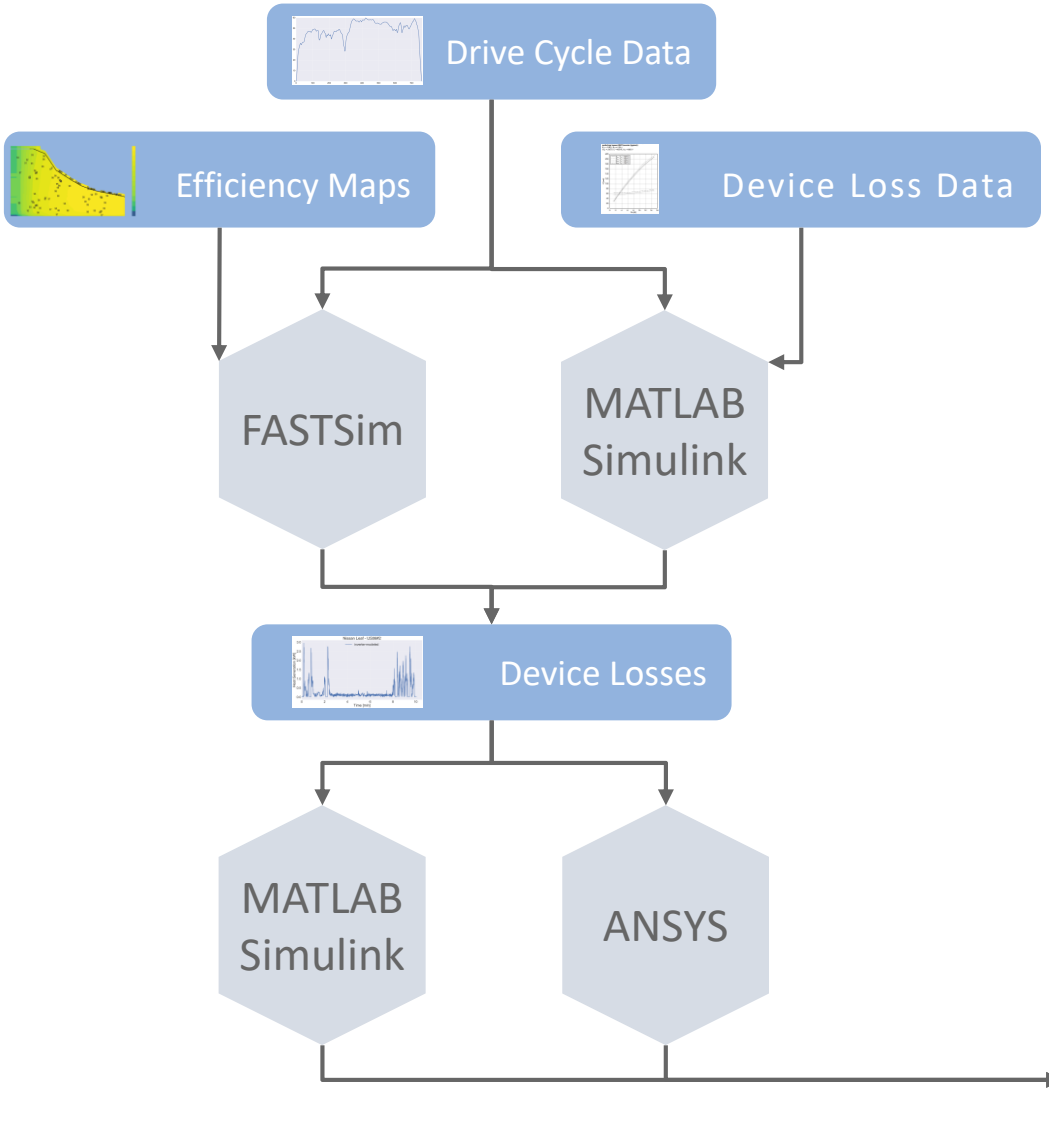

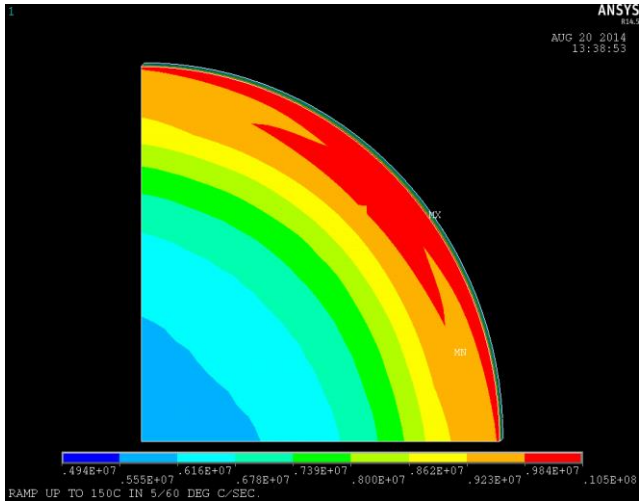

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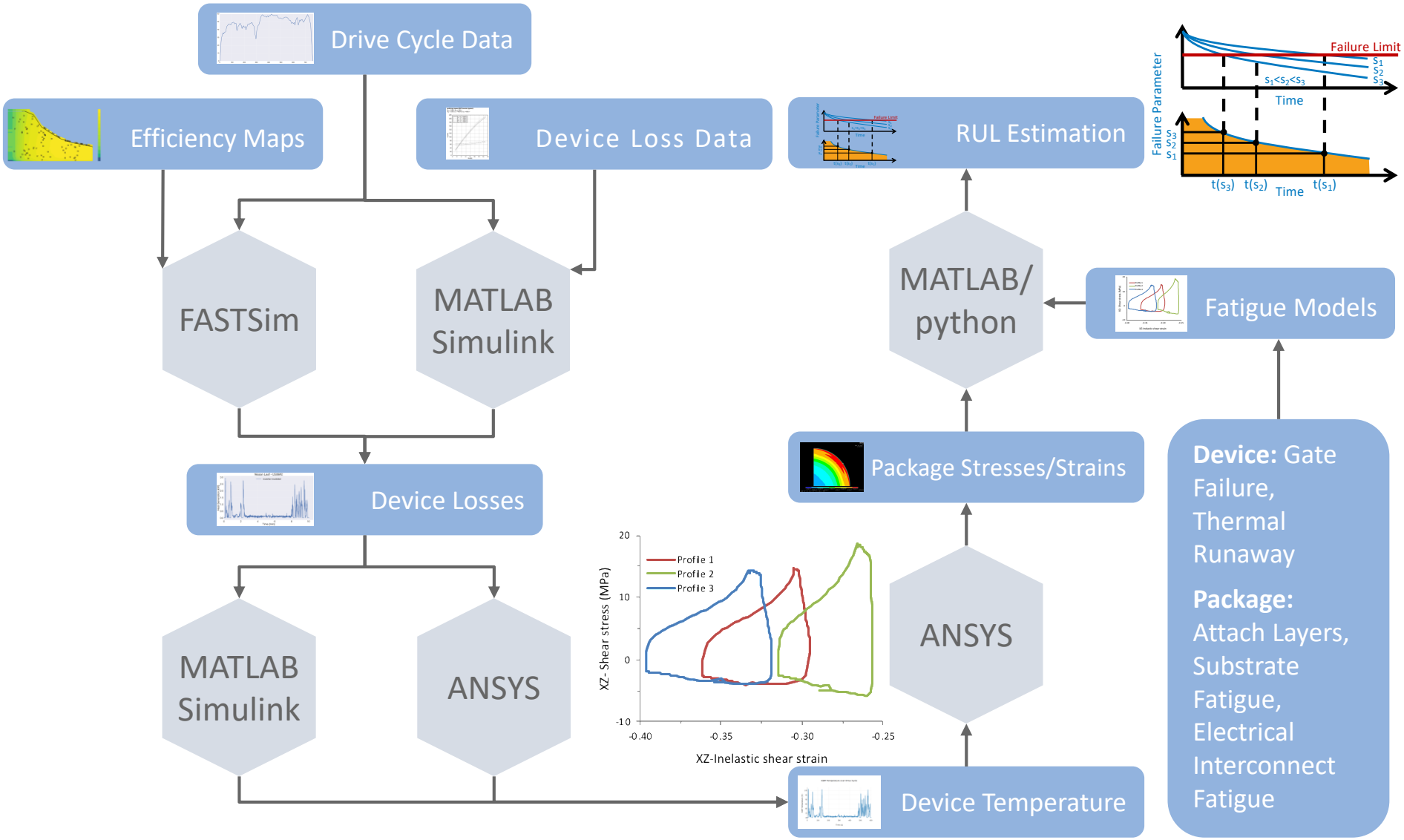

Responses to Previous Year Reviewers' Comments

- This project is a new start in FY19

Collaboration and Coordination

- ORNL
  - Laboratory partner for design and assembly of power electronics modules
- IIC
  - Industry partner for quilt packaging technology
- DuPont
  - Industry partner for ODBC technology

Remaining Challenges and Barriers

- Thermal and reliability concerns of new electrical connect technology must be experimentally evaluated
  - Thermal modeling will determine impact of positioning devices more closely to each other
  - Experimental characterization will evaluate nodule reliability under power and thermal cycling
- New substrate technologies may be susceptible to unforeseen failure mechanisms
  - Past reliability evaluation of ODBC substrates has been promising but full module assembly and evaluation in collaboration with ORNL is needed
- RUL estimation accuracy is dependent on quality of drive cycle input data and validation
  - NREL is working closely with several industry partners to utilize quality drive cycle data

Proposed Future Research

- FY19
  - Complete thermal modeling of packages integrating devices with quilt packaging technology and ODBC substrates
  - Evaluate quilt packaging reliability under power and thermal cycling
- FY20
  - Evaluate thermal and reliability performance of assembled half bridge module in collaboration with ORNL, IIC, and DuPont

**Any proposed future work is subject to change based on funding levels.*

Proposed Future Research

- FY20: Validate RUL tool with experimental results from Accelerated Drive Cycle Platform

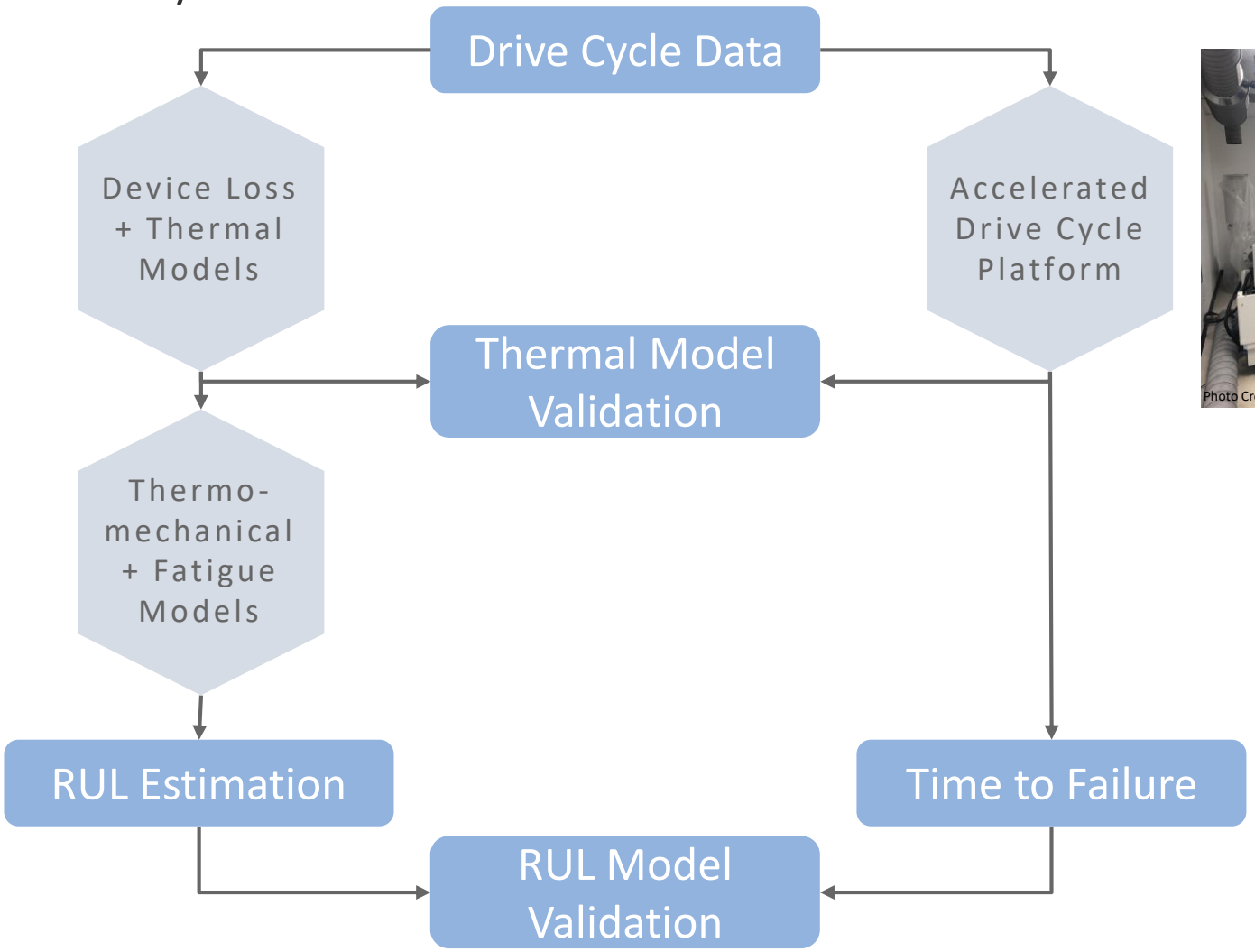


Photo Credit: Douglas DeVoto, NREL

**Any proposed future work is subject to change based on funding levels.*

Summary

Relevance

- New package designs must address thermal and reliability concerns and be evaluated under accelerated conditions that approximate real world conditions

Approach

- Collaborate with ORNL and industry partners to evaluate new packaging materials and manufacturing techniques for WBG based traction inverters
- Continue to develop an RUL tool that uses drive cycle input data for fatigue models for existing and future packaging designs

Technical Accomplishments

- Completed design of devices connected by quilt packaging
- Completed thermal and reliability evaluation of ODBC substrates
- Demonstrated RUL tool

Collaborations

- ORNL
- IIC
- DuPont

Acknowledgments

Susan Rogers, U.S. Department of Energy

NREL EDT Task Leader

Sreekant Narumanchi
Sreekant.Narumanchi@nrel.gov
Phone: (303)-275-4062

Team Members

NREL: Joshua Major, Gilbert Moreno, Paul Paret
ORNL: Emre Gurpinar
IIC: Jason Kulick, Jackson Lu, Edit Varga
DuPont: Gregory Blackman, Rajesh Tripathi, Claire Wemp
Flex Power Control: Greg Smith

For more information, contact

Principal Investigator:
Douglas DeVoto
douglas.devoto@nrel.gov
Phone: (303)-275-4256

Thank You

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