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annual progress report

Annual Progress Report for Advanced Power Electronics and Electric Motors

U.S. Department of Energy
Vehicle Technologies Program
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Annual Progress Report for Advanced Power Electronics and Electric Motors

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Contents

Acronyms and Abbreviations

3-D	three-dimensional
3G	third generation
A/C	air conditioning
ac	alternating current
Al	aluminum
AlN	aluminum nitride
APEEM	Advanced Power Electronics and Electric Machines (ORNL)
AWG	American wire gauge
BJT	bipolar junction transistor
Cds	drain-to-source capacitance
CF-trans-qZSI	current-fed trans-quasi-ZSI
CF-trans-ZSI	current-fed trans-ZSI
CFM	cubic feet per minute
Cgd	gate-to-drain capacitance
Cgs	gate-to-source capacitance
CMOS	complementary metal-oxide semiconductor
CSI	current source inverter
CTE	coefficient of thermal expansion
Cu	copper
DBA	direct bonded aluminum
DBC	direct bonded copper
dc	direct current
DMOS	double diffused metal-oxide semiconductor
DOE	U.S. Department of Energy
DPT	double pulse test
DUT	device under test
ECU	electronic control unit
ECVT	electronically controlled continuously variable transmission
EETT	Electrical and Electronics Technical Team
EV	electric vehicle
EVSE	electric vehicle supply equipment
FEA	finite element analysis
FSCW	fractional slot concentrated winding
FSM	front surface metallization
f_{sw}	switching frequency
GaN	gallium nitride
GCD	greatest common devisor

GUI	graphical user interface
HV	high voltage
IC	integrated circuit
ICE	internal combustion engine
IGBT	insulated gate bipolar transistor
IMMD	integrated modular motor drive
JFET	junction field-effect transistor
LCM	least common multiple
Ld	direct axis inductance
Lq	quadrature axis inductance
LED	light emitting diode
LVDS	low voltage differential signaling
MG	motor-generator
MMF	magnetic motive force
MOSFET	metal-oxide semiconductor field-effect transistor
mph	miles per hour
Nm	Newton meter
OEM	original equipment manufacturer
op-amp	operational amplifier
ORNL	Oak Ridge National Laboratory
PCU	power converter unit
PE	power electronics
PEV	plug-in electric vehicle
PF	power factor
PM	permanent magnet
PMSM	permanent magnet synchronous motor
PSIM	Powersim (circuit simulation software)
PWM	pulse width modulation
R&D	research and development
R-C	resistance-capacitance
R-L	inductor-resistor
RB	reverse-blocking
regen	regeneration
rms	root mean square
SAE	Society of Automotive Engineers
SCP	short circuit protection
Si	silicon
SiC	silicon carbide

SMC	soft magnetic composite
SOA	state-of-the-art
SOI	silicon-on-insulator
SPICE	Simulation Program with Integrated Circuit Emphasis
SPM	surface permanent magnet
SPP	slot/phase/pole
SRM	switched reluctance motor
T_{amb}	ambient temperature
TCIL	thermal conductive insulation layer
TIM	thermal interface material
$T_{initial}$	initial temperature
T_{inlet}	inlet temperature
Tj	junction temperature
TPM	transfer-molded power module
UVLO	undervoltage lockout
Vdc	volts of direct current (operating voltage)
Vgs	gate-source voltage
VSATT	Vehicle Systems Analysis Technical Team
VSI	voltage source inverter
VTP	Vehicle Technologies Program
Wb	weber (SI unit of magnetic flux)
WBG	wide bandgap
WEG	water-ethylene glycol
ZCSI	Z-source current source inverter
ZSI	Z-source inverter

1. Introduction

The U.S. Department of Energy (DOE) and the U.S. Council for Automotive Research (composed of automakers Ford, General Motors, and Chrysler) announced in January 2002 a new cooperative research effort. Known as FreedomCAR (derived from "Freedom" and "Cooperative Automotive Research"), it represents DOE's commitment to developing public-private partnerships to fund high risk, high payoff research into advanced automotive technologies. Efficient fuel cell technology, which uses hydrogen to power automobiles without air pollution, is a very promising pathway to achieve the ultimate vision. The new partnership replaces and builds upon the Partnership for a New Generation of Vehicles initiative that ran from 1993 through 2001.

Advanced Power Electronics and Electric Machines (APEEM) subprogram within the DOE Vehicle Technologies Program (VTP) provides support and guidance for many cutting-edge automotive technologies now under development. Research is focused on developing revolutionary new power electronics (PE) and electric motor technologies that will leapfrog current on-the-road technologies. The research and development (R&D) is also aimed at achieving a greater understanding of and improvements in the way the various new components of tomorrow's automobiles will function as a unified system to improve fuel efficiency.

In supporting the development of advanced vehicle propulsion systems, the APEEM subprogram has enabled the development of technologies that will significantly improve efficiency, costs, and fuel economy.

The APEEM subprogram supports the efforts of the FreedomCAR and Fuel Partnership through a three phase approach intended to

- identify overall propulsion and vehicle related needs by analyzing programmatic goals and reviewing industry's recommendations and requirements and then develop the appropriate technical targets for systems, subsystems, and component research and development activities;
- develop and validate individual subsystems and components, including electric motors and PE; and
- determine how well the components and subsystems work together in a vehicle environment or as a complete propulsion system and whether the efficiency and performance targets at the vehicle level have been achieved.

The research performed under this subprogram will help remove technical and cost barriers to enable the development of technology for use in such advanced vehicles as hybrid electric vehicles (HEVs), plug-in HEVs (PHEVs), battery electric vehicles, and fuel-cell-powered automobiles that meet the goals of the VTP.

A key element in making these advanced vehicles practical is providing an affordable electric traction drive system. This will require attaining weight, volume, and cost targets for the PE and electrical machines subsystems of the traction drive system. Areas of development include

- novel traction motor designs that result in increased power density and lower cost;
- inverter technologies involving new topologies to achieve higher efficiency, with the ability to accommodate higher temperature environments while achieving high reliability;
- converter concepts that use methods of reducing the component count and integrating functionality to decrease size, weight, and cost;
- new onboard battery charging concepts that result in decreased cost and size;

- more effective thermal control through innovative packaging technologies; and
- integrated motor/inverter concepts.

The following report discusses those projects carried out in FY 2010 and conveys highlights of their accomplishments. Numerous project reviews, technical reports, and papers have been published for these efforts, and they are indicated at the end of each section for readers interested in pursuing details of the work.

Major Accomplishments for Technical Projects

Wide Bandgap Materials

- Acquired, tested, and characterized silicon carbide (SiC) junction field-effect transistors (JFETs), metal-oxide semiconductor field-effect transistors, bipolar junction transistors, and diodes.
- Developed a SPICE model for a 1200 V, 10 A, SiC JFET.
- Developed a traction drive model to simulate the performance of wide bandgap devices over different drive cycles.

Direct Water-Cooled Power Electronics Substrate Packaging

- Finalized a design and performed finite element analysis simulations.
  - Validated results by comparing to experimental results.
  - Achieved agreement between 10% and 15%.
- Confirmed through simulations and tests that the maximum junction temperature could be maintained below 165°C using 105°C coolant at 30 kW continuous power.

High Temperature, High Voltage Fully Integrated Gate Driver Circuit

- Designed, fabricated, and packaged a silicon-on-insulator chip for operation at 200°C. The device completed this year incorporates the following features.
  - On-chip voltage regulator.
  - Undervoltage lockout, short circuit, desaturation, and thermal shutdown protection.
  - Gate current monitoring.
  - Low voltage differential signaling circuit.
  - Drive current capability greater than 5 A at 200ºC.
  - Switching frequency greater than 100 kHz.
  - 100% high side duty cycle with charge pump.

Inverter Using Current Source Topology

- Developed two new Z-source current source inverters (ZCSIs) with a reduced component count, a current-fed trans-Z-source inverter (CF-trans-ZSI) and a current-fed trans-quasi-ZSI (CF-trans-qZSI). The new ZCSIs have a higher voltage boost ratio of 3 vs 2 for the previous ZCSIs.
- Completed a design for a 55 kW ZCSI based on the CF-trans-qZSI using first generation reverse blocking (RB) insulated gate bipolar transistor (IGBT) technology. The design yields a specific power of 4.89 kW/kg and a power density of 15.5 kW/L.
- Confirmed through simulation the feasibility of using the ORNL V-I converter-based current source inverter (CSI) topology in series and power-split series-parallel HEV configurations. The CSI dual-motor-drive using RB-IGBTs provides significant performance improvements over the Camry PE:

- 49% increase of specific power (6.4 vs 4.3 kW/kg),
- 60 % increase of power density (9.9 vs 6.2 kW/kg), and
- 34% reduction of cost ($15.4/kW vs $23.2/kW).

Segmented Drive Inverter Topology with a Small dc Bus Capacitor

- Designed, built, and successfully tested a 55 kW segmented inverter prototype achieving a 60% reduction in direct current (dc) bus capacitance with an inductor-resistor load and an induction motor. Test results show significant reductions of
  - 55%~75% in capacitor ripple current,
  - 70%~90% in battery ripple current, and
  - 60%~80% in motor ripple current.

Novel Packaging to Reduce Stray Inductance in Power Electronics

- Developed a new packaging method based on P- and N-cells to reduce the stray inductance between the active switch (IGBT) and diode.
- Completed electromagnetic and circuit simulations showing the reduction of parasitic inductance (20% reduction) and resistance and corresponding improvement in overshoot voltage in a proposed package module (15% reduction).
- Developed a 10 kW phase leg power module that incorporates the novel circuit layout.

High Temperature Air-Cooled Traction Drive Inverter Packaging

- Completed a parametric study to determine the feasibility and boundary conditions required for an air-cooled 55 kW peak/30 kW continuous power rated inverter.
- Performed simulations for steady state and under drive cycle conditions to determine design and junction temperature effects with varying parameters.

Power Device Packaging

- Benchmarked multiple state-of-the-art commercial packaging technologies and assessed advanced packaging approaches.
- Developed and simulated an innovative device module packaging concept.
- Designed and outfitted a state-of-the-art packaging laboratory.

New Class of Switched Reluctance Motors Without Permanent Magnets

- Verified through simulations that the design meets 2015 performance targets with less than 5% torque ripple.
- Designed entire assembly, prepared drawings for fabrication, received all parts, and began assembling prototype motor.

Novel Flux Coupling Motor Without Permanent Magnets

- Finalized a mechanical design which will allow the rotor to safely operate at 14,000 RPM.
- Initiated fabrication of the prototype motor.

Benchmarking Competitive Technologies

- Completed evaluation of the 2010 Prius, including
  - efficiency mapping of subcomponents and system,
  - packaging and manufacturing analysis, and
  - component performance assessment.

High-Power-Density Integrated Traction Machine Drive

- Identified a six-phase, 10-pole permanent magnet (PM) machine as the most promising configuration.
- Investigated a heterarchical control architecture for achieving fault tolerant operation.
- Characterized high temperature static and switching behaviors of candidate silicon devices.
- Designed and simulated performance of a baseline 10 kW phase leg power module with 105°C cooling.

Demonstrated significant heat transfer improvement with enhanced surfaces

- Demonstrated up to a 100% enhancement in heat transfer coefficients for submerged single-phase jets impinging on the Wolverine MicroCool enhanced surface, up to a 130% increase in heat transfer coefficients for free jets impinging on a 3M microporous coating, and up to a 500% enhancement in pool boiling heat transfer coefficients with reduced boiling incipience superheat for a 3M microporous coating compared to a plain surface.

Validated analytical techniques for assessing thermal performance and integration

- Validated newly developed modeling techniques for characterizing power electronic thermal performance and tradeoffs between package configuration and thermal management.
- Results of the analysis approach were published at the IMAPS 2nd Advanced Automotive Workshop on Automotive Microelectronics and Packaging in April 2010, and they were submitted as part of a DOE milestone report for 2010.

New cooling loops and capabilities implemented in NREL's power electronics laboratory

- Developed a wide range of new and unique laboratory capabilities for investigating advanced thermal management and packaging technologies.
  - air cooling technology characterization test bench
  - high pressure two-phase cooling test loop for studying novel refrigerants
  - single phase water-ethylene glycol cooling test loop
  - system for air and liquid cooling flow visualization
  - hot press for synthesizing bonded interfaces
  - thermal shock chamber
  - liquid coolant reliability test loop for evaluating erosion/corrosion of enhanced surfaces

Applied system approach to air cooling research and development

- Developed and applied a system level approach to air-cooled power electronics thermal management that addresses cooling technology, package mechanical design, balance of system, and vehicle application.
- A system level modeling tool framework was created to study and understand the interactions of these four components.

Developed reliability model framework for bonded interfaces

- Implementation of fatigue failure models within the ANSYS Finite Element Software for the purpose of evaluating how solder joint fatigue is affected by new packaging designs and/or cooling methodologies.

Assessment of Motor Technologies

For the past several years, the interior PM (IPM) motor has been considered the obvious choice for electric traction drive systems. However, with the rapidly increasing costs of magnets and the possibility of a future shortage of rare earth metals, the IPM motors may not continue to be the economic or technical favored option. Because of this it is timely to consider other options for motor types.

To provide a basis for deciding which research topics should be pursued, an assessment of motor technologies has been undertaken to determine which, if any, of various motor technologies is *potentially* capable of meeting FreedomCAR 2015 and 2020 targets. Input to the assessment was obtained primarily from interviews with experts and follow-on technical briefs that focused on critical topics identified during the interviews. The list of experts includes original equipment manufacturers, automotive suppliers, leading researchers in academia, and consultants. In addition, past ORNL reports, previous assessments, and magnet literature were reviewed. For each technology, discussions focused on the current state-of-the-art performance and cost, recent trends in the technology, inherent characteristics of the motor that either limit the ability of the technology to meet the targets or aid in meeting the targets, the R&D that would be needed to meet the targets, and the potential for the technology to meet the targets.

The motor technologies considered in the assessment are all brushless and include both PM motors and motors without PMs.

Four types of PM motors were considered. *IPM motors* were treated in detail and form the baseline against which other types of motors were compared. *Surface-mounted PM motors* were treated only briefly because they have no apparent advantage over IPM motors. *Wheel motors* were treated only briefly because they are not a high priority among the automotive manufacturers and are not a major emphasis in the FreedomCAR program. *Multiple-rotor motors* also were treated only briefly because previous research indicated that there are significant challenges that would require extensive R&D with a questionable probability of success.

Three types of motors without PMs were considered. Although inferior to IPM motors in performance and being a relatively mature technology, *induction motors* were treated in detail because they are relatively inexpensive and they were considered seriously before the introduction of IPM motors. If rare earth PMs become unavailable or too expensive in the future, induction motors may be the preferred option for many applications. Although there are problems with torque ripple and noise with *switched reluctance motors*, they were considered in detail because they are rugged and relatively inexpensive. *Motors with external excitation* were considered in detail because it is a relatively new technology with unknown but possibly exciting potential.

No new concepts emerged during the interviews conducted in FY 2010.

During FY 2010 interviews were conducted with Chrysler, Ford, GM, five suppliers, four consultants, and various researchers at Ames Laboratory and ORNL. Several additional interviews will be conducted early in FY 2011, and then a final report will be prepared.

Plug-In Hybrid Electric Vehicle Assessment

More battery powered electric vehicles (EVs) and PHEVs will be introduced to the market in 2011 and beyond. Because these vehicles have large batteries that need to be charged from an external power source or directly from the grid, their batteries, charging circuits, charging stations/infrastructures, and grid interconnection issues are garnering more attention. This report summarizes information regarding the batteries used in PHEVs, different types of chargers, charging standards and circuits, comparing different topologies. It also includes a list of vehicles that are going to be in the market soon together with a list of different charging stations and manufacturers. A summary of different standards governing charging circuits and charging stations concludes the report.

There are several battery types that are available for PHEVs, but the most popular ones have nickel-metal hydride and lithium ion (Li ion) chemistries. The former one is being used in current HEVs, but the latter will be used in most of the PHEVs and EVs because of its higher energy densities and higher efficiencies.

The chargers that can be used to charge these vehicles can be classified based on the circuit topologies (dedicated or integrated), location of the charger (either on or off the vehicle), connection (conductive, inductive/wireless, and mechanical), electrical waveform [dc or alternating current (ac)], and direction of power flow (unidirectional or bidirectional). The first PHEVs typically will have dedicated onboard unidirectional chargers that will have conductive connections to the charging stations and will be charged using either dc or ac. In the near future, bidirectional chargers might also be used in these vehicles once the benefits of practical vehicle to grid applications are realized.

The terms charger and charging station cause terminology confusion. To prevent misunderstandings, the more descriptive term of “electric vehicle supply equipment” (EVSE) is used instead of charging station. The charger is the power conversion equipment that connects the battery to the grid or another power source, while EVSE refers to external equipment between the grid or other power source and the vehicle, and it might include conductors, connectors, attachment plugs, microprocessors, energy measurement devices, transformers, etc. Currently there are around a dozen companies that are producing EVSEs.

There are several standards and codes regarding conductive and inductive chargers and EVSEs from the Society of Automotive Engineers (SAE), Underwriters Laboratories, the International Electrotechnical Commission, and the National Electric Code. The two main standards from SAE describe the requirements for conductive and inductive coupled chargers and the charging levels. Three levels are specified for inductive coupled charging: Level 1 (120 V and 12 A, single phase), Level 2 (208–240 V and 32 A, single phase), and Level 3 (241–600 V and 400 A, three phase). The standard for the conductive coupled charger also has similar charging levels for Levels 1 and 2, but it allows higher current levels for Level 2, charging up to 80 A. Level 3 charging for this standard is still under development and considers dc charging instead of three phase ac.

2. Power Electronics Research and Technology Development

2.1 Wide Bandgap Materials

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Objectives

- To keep up-to-date with the state-of-the-art wide bandgap (WBG) power devices and acquire, test, and characterize newer WBG power devices.
- To assess the system level impact of WBG semiconductor devices on hybrid electric vehicles.

Approach

- Evaluate device performance: Acquire, test, and characterize newer WBG power devices, including
  - static characteristic tests,
  - dynamic characteristic tests, and
  - behavioral modeling.
- Develop behavioral SPICE (Simulation Program with Integrated Circuit Emphasis) models for packaging projects.
  - Specific device tests will be performed to extract the parameters required for behavioral SPICE models.
  - These models will be used to study the parasitic parameters in a package.
- Perform inverter simulations with selected device models. The inverter simulations will be performed to evaluate the impact of the device performance at system level.
- Prepare a summary report for incorporation in the Vehicle Technologies Program annual report that includes the device test results and SPICE modeling results.

Major Accomplishments

- Acquired, tested, and characterized silicon carbide (SiC) junction field-effect transistors (JFETs), metal-oxide semiconductor field-effect transistors (MOSFETs), bipolar junction transistors (BJTs), and diodes.
- Developed SPICE model for a 1,200 V, 10 A, SiC JFET.
- Developed a traction drive model to simulate the performance of the WBG devices over different drive cycles.

Future Direction

- Acquire, test, and characterize state-of-the-art and newer technology WBG power devices.

- Develop SPICE models of the devices.
- Continue to optimize drive model for determining system level performance of devices.

Technical Discussion

1. Device Testing

The WBG devices acquired this year are "normally off" SiC JFETs, SiC BJTs, SiC MOSFETs, and SiC junction barrier Schottky (JBS) diodes. On-state characteristics and switching energy losses of the devices were obtained, and the voltage blocking capability of the devices over a wide temperature range was tested. The test results for these devices will be presented in the following sections. All the devices obtained were experimental samples.

1.1 Normally Off 1,200 V, 50 A, SiC JFET

Static characteristics of a 1,200 V, 50 A, normally off SiC JFET at different operating temperatures are shown in Fig. 1. Normally off devices are the preferred type of device in power converters for fail-safe operation. The forward characteristics were obtained for a gate voltage of +3 V. The forward voltage drop of the device at 15 A increased from 0.7 V at 25°C to 2.2 V at 175°C. This shows that the power dissipation of the device would limit the device operation to 15 A at higher temperatures. The leakage current of the device was obtained over the temperature range of 25°C to 150°C and up to 600 V (Fig. 2).

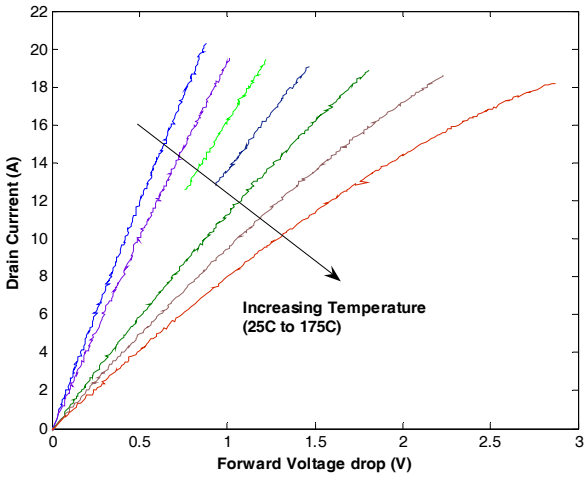

Fig. 1. i-v curves of a 1,200 V, 50 A, SiC JFET.

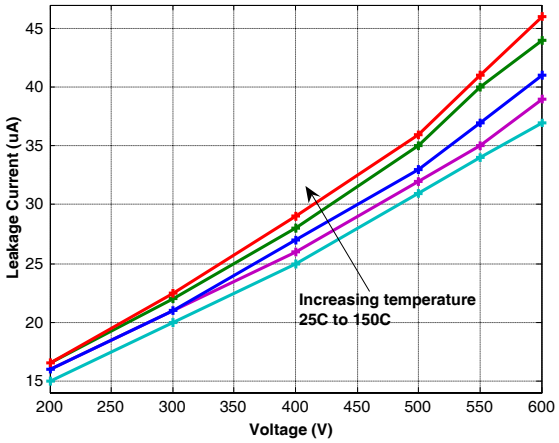

Fig. 2. Leakage current vs voltage of 1,200 V, 50 A, JFET.

The "turn-on" and "turn-off" energy losses of the JFET were obtained using the double pulse circuit with a load inductance of 360 µH, and a 1,200 V, 30 A, SiC JBS diode was used as the clamping diode in the circuit. The gate driver used for this testing was a commercial gate driver board SGDR600P1. The device requires constant current for the device to remain switched on, and this features demands more power from the gate driver. The data were obtained at 600 V and 400 V dc for various currents at 25°C and 175°C. The total energy losses increase with increase in current; however, not significantly (Figs. 3 and 4).

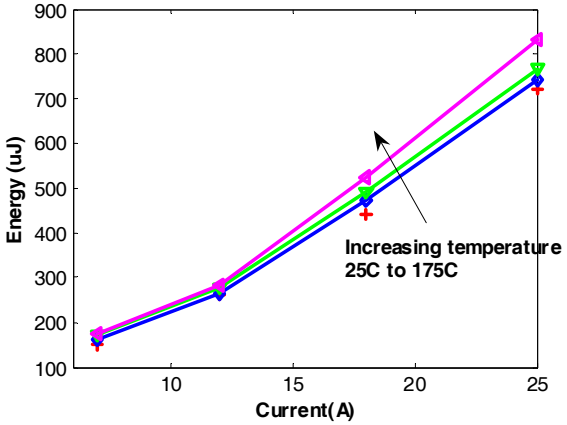

Fig. 3. Total switching energy losses of a 1,200 V, 50 A, SiC JFET at 600 V.

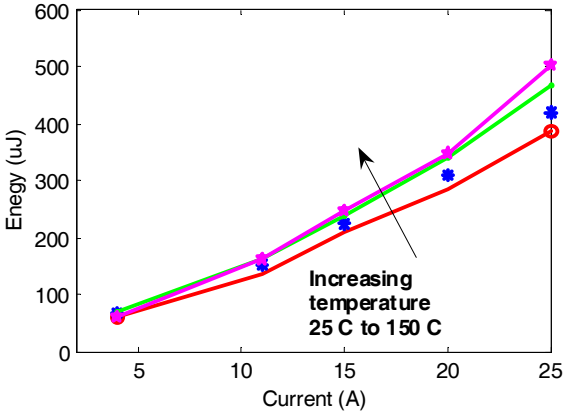

Fig. 4. Total switching energy losses of a 1,200 V, 50 A, SiC JFET at 400 V.

1.2 Normally Off 1,200 V, 100 A, SiC JFET

A 1,200 V, 100 A, normally off SiC JFET in an experimental half bridge module was tested. The on-state characteristics were obtained at +3 V gate-source voltage (Vgs). Static characteristics of the JFET are shown in Fig. 5 for different operating temperatures. The leakage current of the JFETs in the module was measured over the temperature range of 25°C to 150°C. The measured leakage current did not change with temperature (Fig. 6). It should be noted that the module had a snubber across the dc link inside the module and part of the current could be driving the capacitor in the snubber.

The module had a wire bonding issue and the gate of the upper device could not block at high voltages. However, the devices in the module were still functional. The turn-on and turn-off energy losses of the JFET were obtained using the double pulse circuit with a load inductance of 110 µH. An external 600 V, 75 A, Schottky diode was used as the clamping diode in the circuit. The gate drive used for the test was a commercial IDD409 IXYS chip with 35 V, 9 A, output drive capability similar to the single JFET device. The data were obtained at 600 V dc for various currents and for 25°C and 175°C. The total energy losses increase with increase in current; however, not significanltly. (Fig. 7).

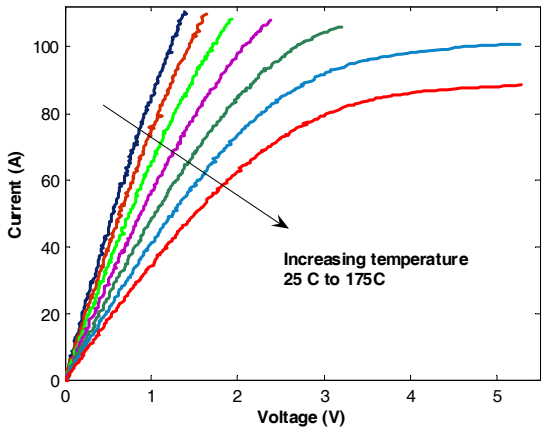

Fig. 5. i-v curves of a 1,200 V, 100 A, SiC JFET.

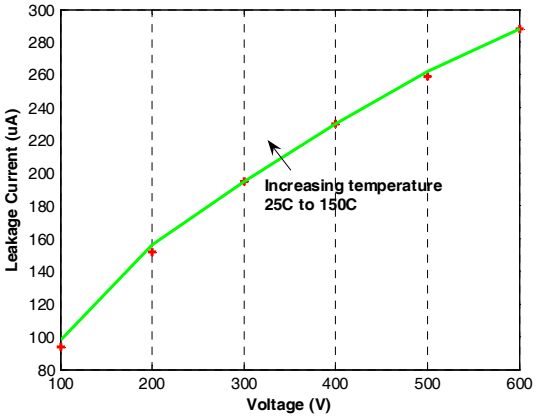

Fig. 6. Leakage current vs voltage of a 1,200 V, 100 A, JFET.

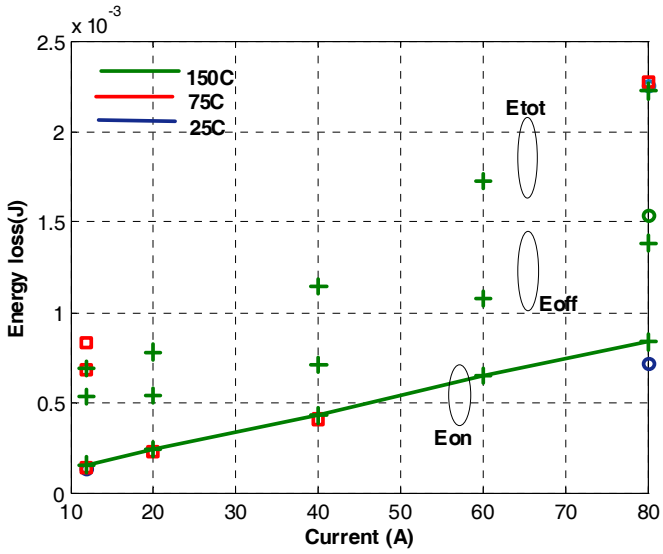

Fig. 7. Switching losses of 1,200 V, 100 A, SiC JFET.

1.3 SiC BJT (1,200 V, 6 A)

The SiC BJT is a current controlled device unlike the voltage controlled FET devices. Experimental samples (1,200 V, 6 A) were obtained and tested. The static characteristics of the SiC BJT were obtained at 350 mA of base current and over a temperature range of 25°C to 175°C (Fig. 8). The low forward voltage drop at 6 A shows that this device could be operated up to 10 A at 175°C. The leakage current at different voltages over a temperature range of 25°C to 150°C is shown in Fig. 9. The leakage current at 600 V increases from 1.5µA at 25°C to 3.6 µA at 150°C. Because the gate drive requirements are very similar, the BJT was tested with the same gate driver as the normally off SiC JFET. The BJT was tested with the 1,200 V, 8 A, SiC JBS diode in the chopper circuit. The total switching energy losses of the BJT at 400 V and 600 V at different temperatures are shown in Fig. 10. The losses do not change much with temperature.

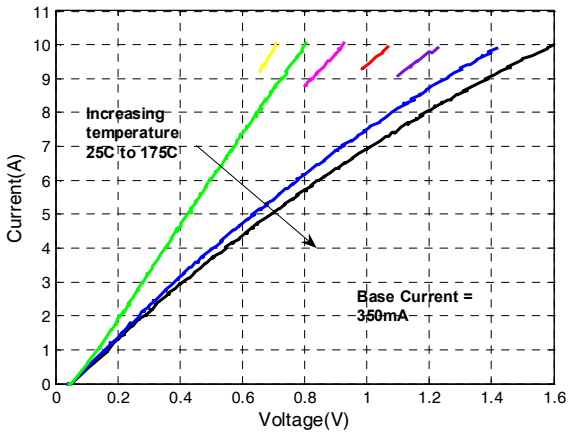

Fig. 8. i-v curves of a 1,200 V, 6 A, SiC BJT.

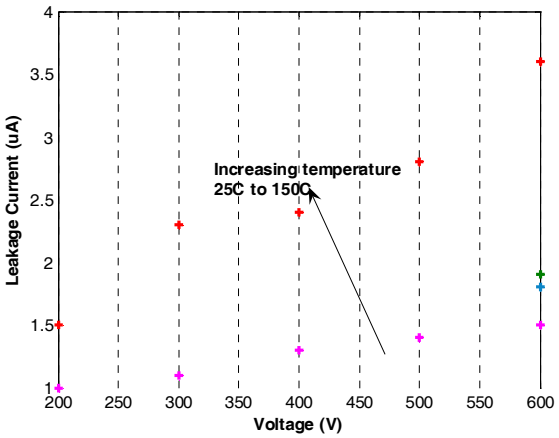

Fig. 9. Leakage current vs voltage of a 1,200 V, 6 A, SiC BJT.

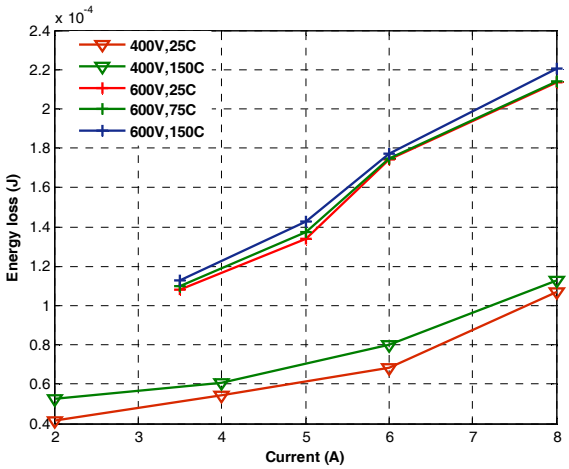

Fig. 10. Total switching energy losses of 1,200 V, 6 A, SiC BJT at 400 V and 600 V.

1.4 SiC JBS Diode (1,200 V, 30 A)

The static characteristics of a 1,200 V, 30 A, SiC JBS diode were obtained over a wide temperature range (25°C–225°C) (Fig. 11). The diodes were specifically designed for high temperature operation. The leakage current of the diode at a blocking voltage of 600 V is about 0.5 µA at 25°C and increases to 3.7 µA at 200°C (Fig. 12). This clearly shows that the device can block higher voltages at higher temperatures. The SiC JBS diode was tested in the same chopper circuit as the SiC 50A normally off SiC JFET with double pulse switching to obtain its dynamic characteristics. The turn-off energy losses of the JBS diode at 200 V, 400 V, and 600 V over a wide temperature range are shown in Fig. 13. The turn-off losses do not change much with temperature or current, exhibiting temperature independent switching loss behavior. However, the loss increases as the voltage increases.

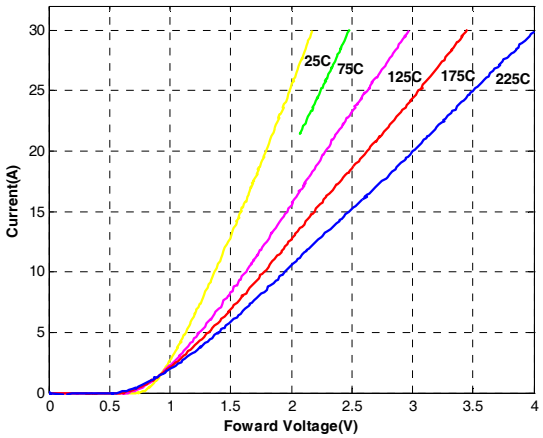

Fig. 11. I-v curves of a 1,200 V, 30 A, SiC JBS diode.

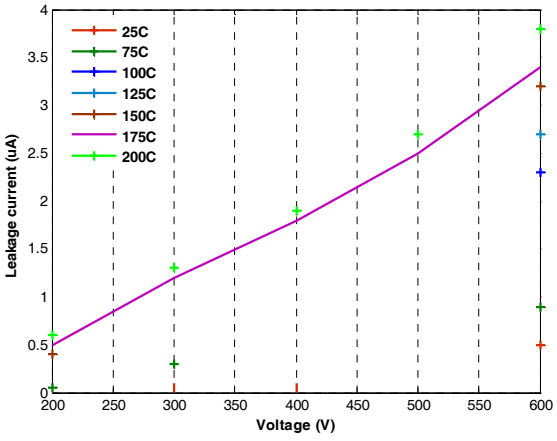

Fig. 12. Leakage current vs voltage for a 1,200 V, 30 A, SiC JBS diode.

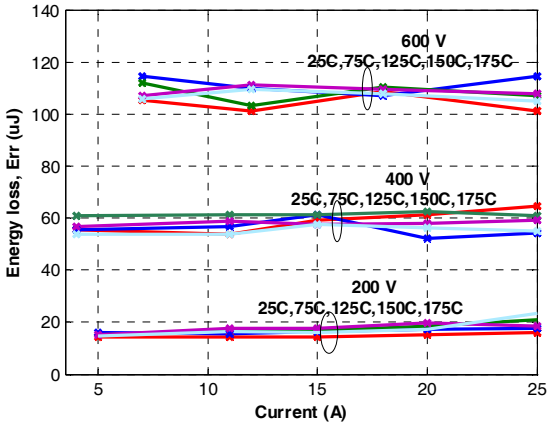

Fig. 13. Switching energy losses of 1,200 V, 30 A, SiC JBS diode at 200 V, 400 V, and 600 V.

1.5 SiC JBS Diode (1,200 V, 8 A)

The static characteristics of a 1,200 V, 8 A, SiC JBS diode were obtained over a wide temperature range (25°C–225°C) (Fig. 14). The diodes were specifically designed for low leakage currents at high temperaturesn. The leakage current of the diode at a blocking voltage of 600 V is about 0.05 µA at 25°C and increases to 4.3 µA at 200°C (Fig. 15). This clearly shows that the device can block higher voltages at higher temperatures. The SiC JBS diode was tested in the same chopper circuit as the 1,200 V, 6 A, SiC BJT with double pulse switching to obtain its dynamic characteristics. The turn-off energy losses of the JBS diode at 400 V and 600 V at different temperatures are shown in Fig.16. The turn-off losses do not change much with temperature or current, exhibiting temperature independent switching loss behavior. However, the loss increases as the voltage increases.

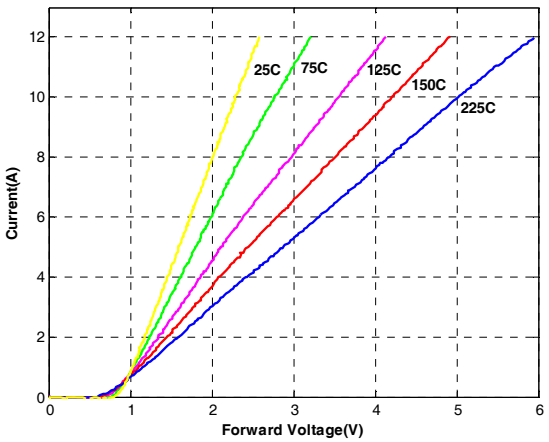

Fig. 14. i-v curves of a 1,200 V, 8 A, SiC JBS diode.

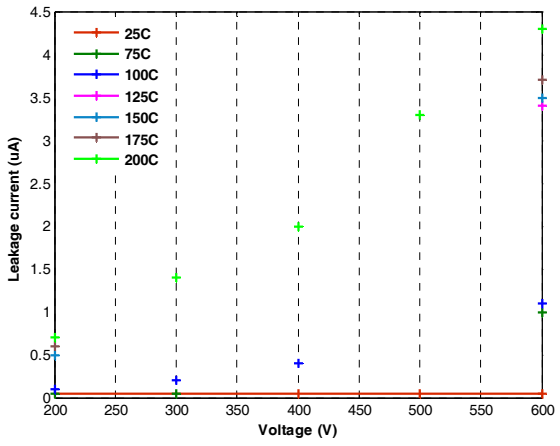

Fig. 15. Leakage current vs voltage of a 1,200 V, 8 A, SiC JBS diode.

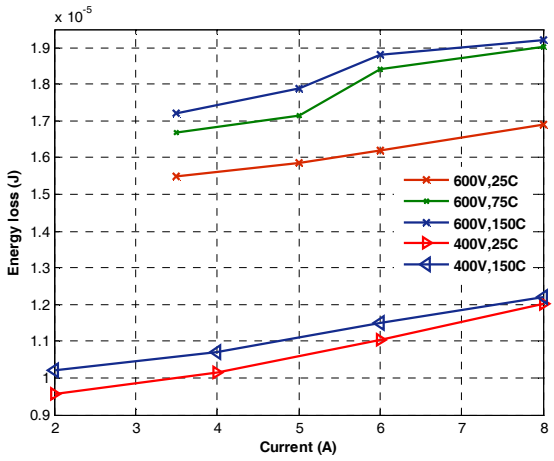

Fig. 16. Switching energy losses of a 1,200 V, 8 A, SiC JBS diode at 400 V and 600 V.

1.6 SiC MOSFET (1,200 V, 100 A)

Static characteristics of a 1,200 V, 100 A, SiC MOSFET in a half bridge module for different operating temperatures at 20 V Vgs are shown in Fig. 17. This module was built using the commercial Si CM100DY-24A half bridge module package. The SiC MOSFET was tested in a chopper circuit with double pulse switching to observe its dynamic characteristics. The gate driver used for obtaining the dynamic characteristics is a commercial gate driver (HCPL 316J). The gate voltage was switched from +15 V Vgs to −5V. The diode in the half bridge module was used as the clamping diode with a 110 µH inductor as the load. The total switching energy losses of the MOSFET at 600 V and 400 V are shown in Fig.18. The switching losses increase with an increase in current and do not change much with temperature.

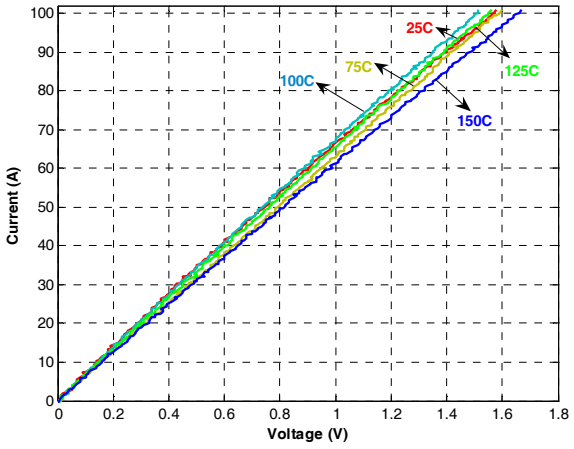

Fig. 17. i-v curves of a 1,200 V, 100 A, SiC MOSFET.

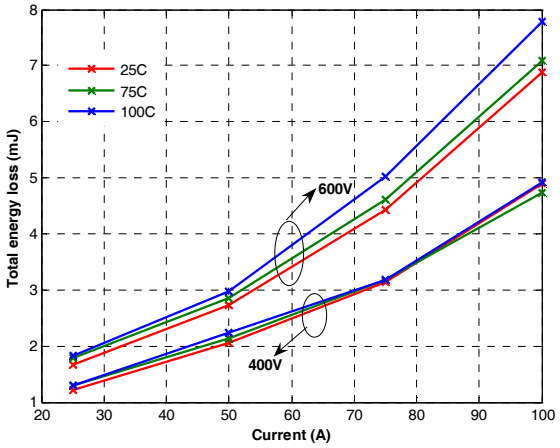

Fig. 18. Switching energy losses of a 1,200 V, 100 A, SiC MOSFET at 400 V and 600 V.

1.7 SiC JBS Diode (1,200 V, 100 A)

The static characteristics of a 1,200 V, 100 A, SiC JBS diode in the SiC MOSFET module were obtained across a wide temperature range (25°C–150°C) (Fig. 19). The diode has negative temperature coefficient below 10 A current and positive temperature coefficient above 10 A. The SiC JBS diode was tested in the

same chopper circuit as the SiC MOSFET with double pulse switching to observe its dynamic characteristics. The turn-off energy losses of the JBS diode at 600 V and 400 V are shown in Fig. 20. The turn-off losses do not change much with temperature, exhibiting temperature independent switching loss behavior. Also, the turn-off losses do not change much with an increase in current; however, the losses increase with increasing voltage.

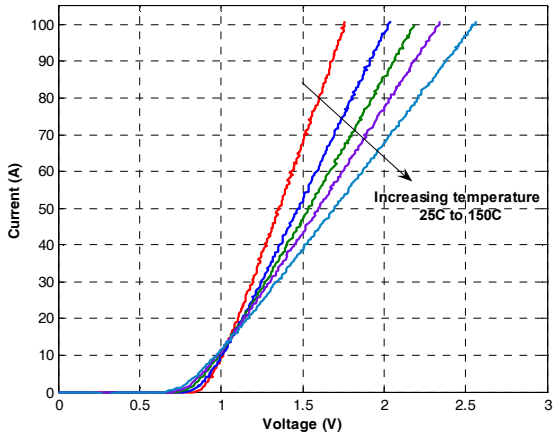

Fig. 19. i-v curves of a 1,200 V, 100 A, SiC JBS diode.

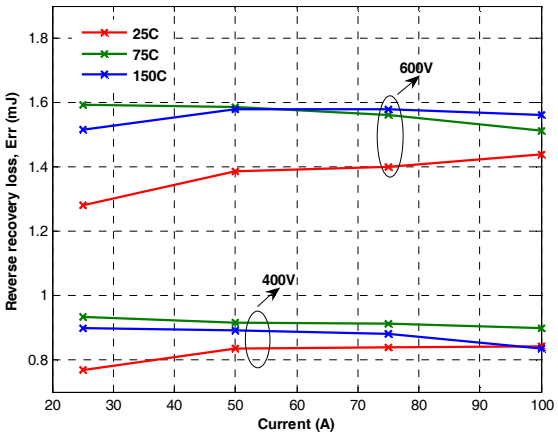

Fig. 20. Switching energy losses of a 1,200 V, 100 A, SiC JBS diode at 400 V and 600 V.

2. Traction Drive Model

The model consists of two parts: (1) an electric motor/generator model that computes the current, voltage, and phase angle that will optimally produce 100% of the torque required at each time step and (2) an inverter loss model that computes the temperature dependent device losses associated with the voltages, currents, and frequencies demanded by the motor.

For this study, the speed and power required for the drive were generated using Camry-like reference vehicle characteristics. The driving profile followed by the vehicle was the standard US06 Supplemental Federal Test Procedure—a 20 minute, 8-mile-long combination of urban and highway driving with 80 miles per hour (mph) peak and 52 mph average moving speeds. Assuming a flat terrain and no atmospheric wind, the average and peak road-power demands placed on the vehicle's motor were 25.1 kW/100 kW for propulsion and 19.7 kW/68.6 kW for braking.

2.1 Internal Permanent Magnet Motor Model

The motor model emulates a typical Camry-like eight-pole internal permanent magnet machine, characterized by parameters extracted from testing done at ORNL. The motor model follows the classic d-q (direct-quadrature) transformation approach. The model allows for regenerative recovery of the vehicle's excess kinetic energy that is conventionally wasted in the brakes by friction. When the vehicle's power demand is negative, the motor acts as a generator. The motor model takes all or part of the road-power demand as input and computes the frequency, current, voltage, and phase angle that will optimally produce the torque required at each time step. In a pure electric power mode the full road-demand is placed on the electric motor. In a hybrid configuration the fraction of power allocated to the motor can vary from 0% to 100% of the required road power depending on the hybridization power sharing scheme.

In this study it is assumed that most of the power demand of the drive cycle will be supplied by the electric drivetrain, and in the regions where the demand is more than the maximum power of the motor, the engine will generate the power. The available maximum terminal voltage limits the output power of the motor, which is dependent on the dc bus voltage with maximum boost. The terminal voltage is calculated assuming a six-step inverter mode of operation. The maximum current and voltage demands on the motor are 240 A and 300 V.

2.2 Inverter Model

The inverter loss model was implemented with a conduction loss model developed using averaging techniques described in [1] and switching loss equations derived based on switching energy loss data. The temperature dependent conduction loss parameters, on-state resistance and voltage drop, and switching losses were obtained from testing the 1,200 V, 100 A, SiC MOSFET module. The module test data were presented in Sects. 1.6 and 1.7. In addition to the power, current, power factor, and voltage demands computed by the motor model, the conduction loss model requires the modulation index as input. This index was calculated as the ratio of the terminal voltage required by the motor and the dc-link voltage provided by the boost converter. The boost factor as a function of torque and speed was empirically derived from test data for a Camry drive system following the US06 drive cycle. The boost function shown in Fig. 21 was obtained by curve fitting the test data. The test data were provided by Argonne National Laboratory. The battery voltage and the bus voltage are shown in Fig. 22.

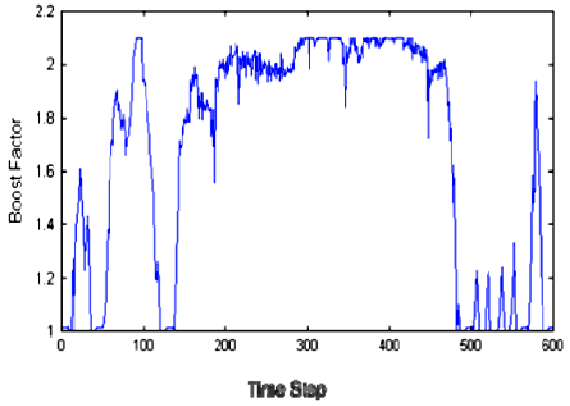

Fig. 21. Boost factor calculated from vehicle test data.

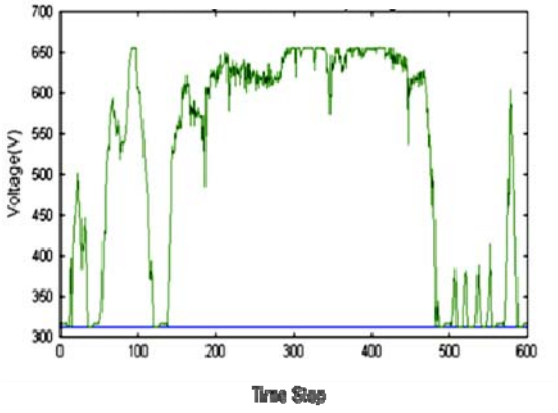

Fig. 22. Bus voltage (green) and battery voltage (blue).

The maximum boost factor is about 2.1 for the US06 drive cycle. The computation of the temperature dependent power losses in switches and diodes iterates with a thermal model that computes the junction temperatures from the power losses assuming a constant heat sink temperature. The devices tested were a MOSFET and a JBS diode in a 1,200 V, 100 A, half bridge SiC module prototype. The SiC module has two SiC MOSFETs and two JBS diodes. The inverter for this study was simulated with three switch–diode pairs (300 A rating) per phase in a full bridge configuration to accommodate the maximum current of 240 A for the drive cycle.

2.3 Simulation Results

The drive model was simulated for the US06 drive cycle with SiC MOSFET and diode models at switching frequencies of 10 kHz and 20 kHz and two different coolant temperatures: 70°C and 105°C. The drive model outputs time dependent, cycle average, and cumulative values of interest for all pertinent parameters. The simulated efficiencies of an all-SiC (SiC MOSFET/SiC Schottky diode) inverter are

shown in Table 1. The table shows the average inverter efficiency and inverter losses over the drive cycle for 10 and 20 kHz operation with both 70°C and 105°C cooling .

Table 1. Simulation Results of Traction Drive for US06 Drive Cycle

Coolant temperature (°C)	Operating frequency	
	10 kHz	**20 kHz**
Inverter efficiency (%)		
70	97.43	95.41
105	97.39	95.34
Inverter energy loss (kJ)		
70	338.9	617.6
105	344.3	626.7

The inverter efficiency corresponds to the switching and conduction losses of devices in the inverter only, and the losses in the boost converter are not included. For 10 kHz operation, the efficiency of the SiC inverter decreased by only 0.1% from 70°C to 105°C coolant temperature condition because of the temperature independence of its switching losses. However, when the switching frequency was increased from 10 kHz to 20 kHz the efficiency of the SiC inverter decreased by 2.02% and 2.05%, respectively, at 70°C and 105°C coolant temperatures.. This illustrates that the low losses and high temperature capability of SiC devices will certainly improve the system efficiency and increase the power density of the inverter.

3. SPICE Model

In FY 2010, one of the tasks was to develop behavioral SPICE models of WBG devices. The device chosen this year was a 1,200 V, 10 A, normally on SiC JFET. The model was developed using the parameters obtained using the test data. The forward and dynamic behavior of the device was simulated and compared to the measured data. The details of the modeling are described below.

3.1 Equivalent Circuit of JFET

The equivalent circuit of the JFET is shown in Fig. 23. The circuit elements include gate resistance and inductance (Rg, Lg); drain series inductance (Ld); source series inductance (Ls); and the junction capacitances between the three terminals, gate-to-source (Cgs), gate-to-drain (Cgd), and drain-to-source (Cds). The values of Rg, Lg, Ld, and Ls were obtained from the device manufacturer [2] (Rg = 6 Ohms, Lg = 5 nH, Ld = 1nH, and Ls = 1 nH). The junction capacitance values were extracted from the test data as shown in Figs. 24, 25, and 26. The data were curve fitted and the equations were derived as shown below.

$$C_{gd} = 10^{-12} * (72.61 * exp(-0.05 * V_{dg}) + 45.2 * exp(-0.002648 * V_{dg})) \quad . \tag{3.1}$$

$$C_{gs} = 10^{-12} * (0.005 * V_{gs}^4 + 0.3321 * V_{gs}^3 + 7.543 * V_{gs}^2 + 78.13 * V_{gs} + 1082) \quad . \tag{3.2}$$

$$C_{ds} = 10^{-12} * (587.9 * exp(-0.105 * V_{ds}) + 159.1 * exp(-0.0051 * V_{ds})) \quad . \tag{3.3}$$

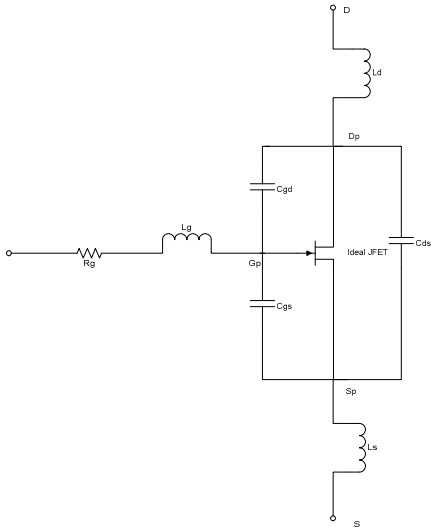

Fig. 23. Equivalent circuit of a SiC JFET.

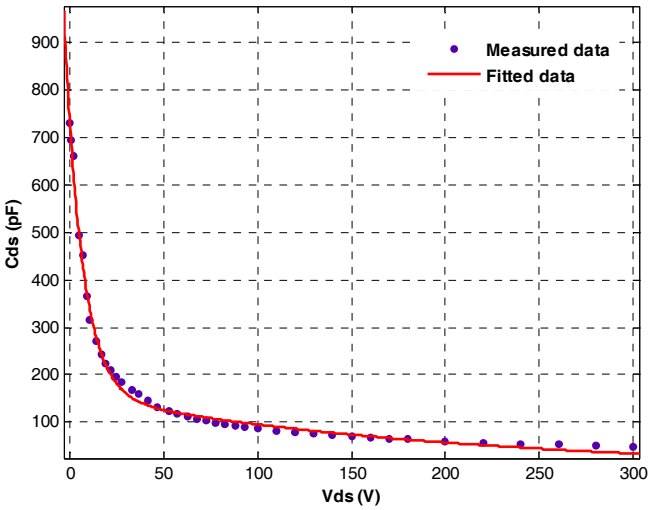

Fig. 24. Drain to source capacitance (Cds) vs drain to source voltage (Vds).

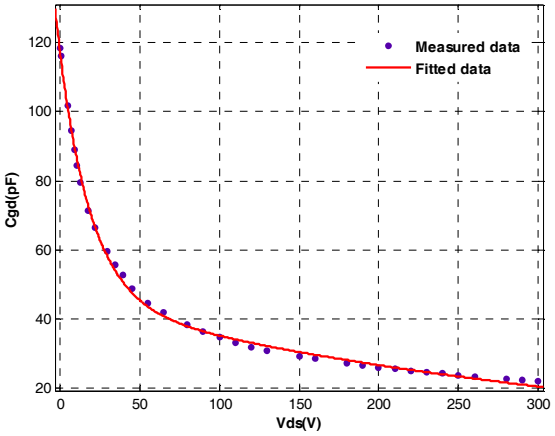

Fig. 25. Gate to drain capacitance (Cgd) vs Vds.

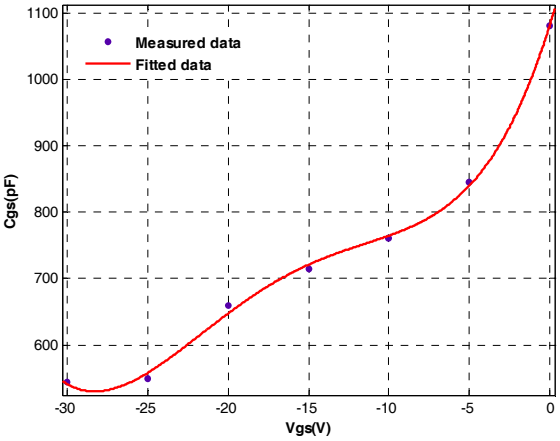

Fig. 26. Gate to source capacitance (Cgs) vs gate-source voltage (Vgs).

The current through the device can be represented as

$$I_D(T, Vgs, Vds) = I_s(T, Vgs) * \left(1 - e^{-c(T,Vgs)*Vds}\right) , \tag{3.4}$$

where I_D is the current going through the device, *Is* is the saturation current, and *c* is the speed at which the current reaches its saturation value. The temperature dependence of the current was modeled using the forward characteristics obtained over the range of temperatures. *Is* and *c* are a function of both gate-to-source voltage (Vgs) and the junction temperature (T). The equations for forward characteristics over different temperatures can be described as follows.

$$I_s(T, Vgs) = I_{s0}(T) + I_{s1}(T) * Vgs + I_{s2}(T) * V_{gs}^2 . \tag{3.5}$$

$$I_{s0}(T) = 0.000512 * T^2 - 0.1832 * T + 37.65 . \tag{3.6}$$

$$I_{s1}(T) = 0.0001467 * T^2 - 0.04011 * T + 4.278 \ . \quad (3.7)$$

$$I_{s2}(T) = -0.0005475 * T + 0.09581 \ . \quad (3.8)$$

$$C(T, V_{gs}) = C_2(T) * V_{gs}^2 + C_1(T) * V_{gs} + C_0(T) \ . \quad (3.9)$$

$$C_2(T) = 5.829 * 10^{-8} * T^2 - 1.117 * 10^{-8} * T - 0.001683 \ . \quad (3.10)$$

$$C_1(T) = 1.039 * 10^{-6} * T^2 - 0.0002609 * T - 0.01116 \ . \quad (3.11)$$

$$C_0(T) = -0.1211 \ . \quad (3.12)$$

3.2 Validation of the Model

The SPICE model of the SiC JFET was validated using two different test circuits, one for static characteristics and one for dynamic characteristics. The static characteristics of the device were obtained using a 371B curve tracer, and the simulation results were obtained by sweeping the current to saturation at different gate voltages and different temperatures. The forward characteristics obtained from simulation at 25°C are shown in Fig. 27. The comparison of simulation and tests results for a gate voltage of −10 V at different temperatures is shown in Fig. 28. The device current in the saturation region and the linear region matches the test results very closely. The dynamic characteristics of the test data were obtained from the double pulse test circuit at 300 V and 5 A using a 600 V, 6 A, Schottky diode. The SPICE model of the diode was obtained from Cree for a similar diode and used in the simulation. The switching curves in Figs. 29 and 30 show an excellent match between the simulation and test results for both the current and the voltage.

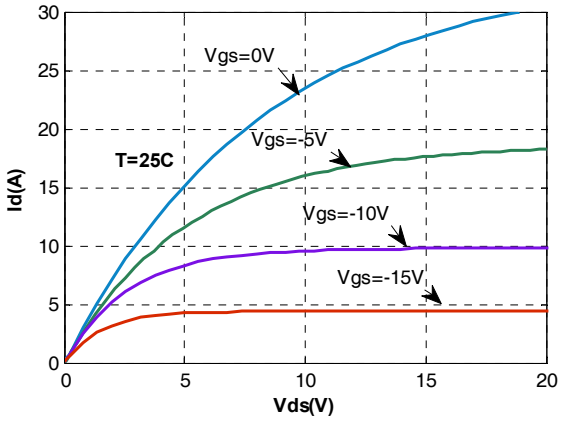

Fig. 27. Simulated forward characteristics of the SiC JFET.

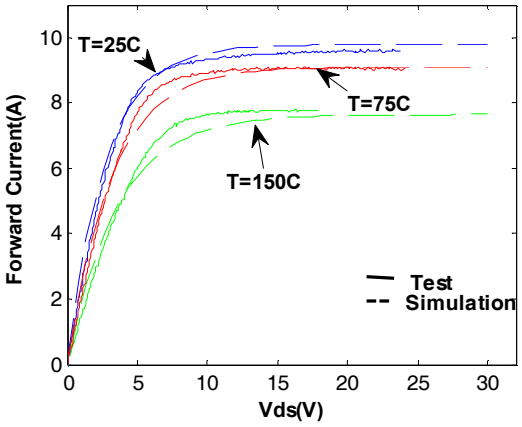

Fig. 28. Comparison of simulation and test results for forward characteristics at various temperatures and −10 V Vgs.

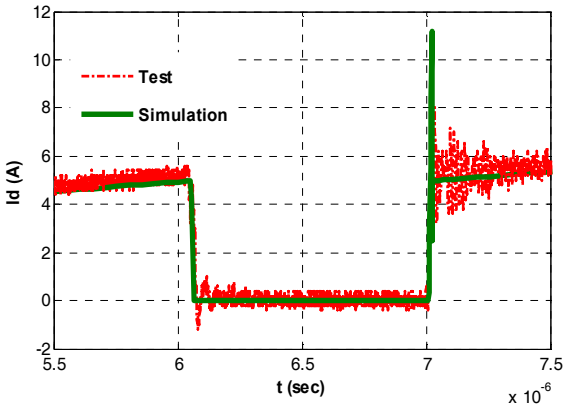

Fig. 29. Comparison of current waveforms of the JFET.

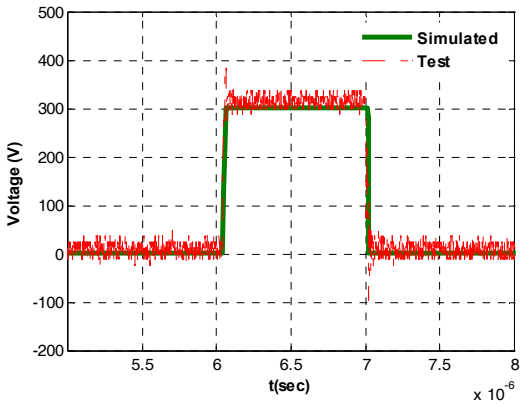

Fig. 30. Comparison of voltage waveforms of the JFET.

Conclusion

Several new SiC JFETs, MOSFETs, Schottky diodes, and JBS diodes were acquired, tested, and modeled. The traction drive model was sucessfully completed and the simulation results for the SiC inverter, developed based on 1,200 V, 100 A, SiC MOSFET testing, were presented. A behavioral SPICE model of a 1,200 V, 10 A, normally on SiC JFET was developed by obtaining the critical model parameters from testing the device. The SPICE model was validated with the actual test data.

Publications

1. M. S. Chinthavali, et al., "High Power SiC Modules for HEVs and PHEVs," IEEE International Power Electronics Conference 2010 (IPEC), June 21–24, 2010, Sapporo, Japan.
2. M. S. Chinthavali, P. J. Otaduy, and B. Ozpineci, "Performance Comparison Study of SiC and Si Technology for an IPM Drive System," International Conference on Silicon Carbide and Related Materials (ICSCRM) 2009, October 11–16, 2009, Nurnberg, Germany.

References

1. B. Ozpineci, et al., "Effects of Silicon Carbide (SiC) Power Devices on PWM Inverter Losses," *The 27th Annual Conference of the IEEE Industrial Electronics Society*, November 29–December 2, 2002, Denver, Colorado, pp. 1061–1066.
2. http://siced.com/download/CY11cb9072X1225e4d14d8X3eae/JFET_INF06_1200V_V1a.lib.

2.2 Direct Water-Cooled Power Electronics Substrate Packaging

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Objectives

- Achieve a reduction in the size and weight of power electronic inverters while operating with a high temperature coolant.
  - Volume reduction—the proposed ORNL structure allows for the maximum cooling surface area to be used within the smallest geometrical volume.
  - Weight savings—Weight reduction of about 17% as compared to the 2007 Toyota Camry by the removal of the traditional baseplate and heat sink.
- Achieve system cost reductions through
  - elimination of auxiliary cooling loop,
  - removal of the baseplate and heat sink, and
  - use of silicon switches with high temperature coolant.
- Achieve a reliable substrate design while using 105°C water-ethylene glycol (WEG) coolant.

Approach

The strategy of this research effort was to reduce the size and weight of the power electronic inverter by

- directly cooling the substrate package,
- eliminating the cold plate and the heat spreader, and
- removing the thermal interface material (TIM).

Major Accomplishments

- Completed metallization of the second generation ceramic substrate.
- Evaluated metallization, which was shown to have excellent bond strength.
- Selected and fabricated an octagonal design containing eight coolant channels. This design produced the following results.
  - — Inverter design volume of 3.6 L.
  - — Coolant temperature of 105°C WEG with a copper cladding thickness of 0.012 in.
  - — Projected power density of 15 kW/L.
  - — Maximum steady state temperatures for 30 kW continuous loads as follows.
    - ► Insulated gate bipolar transistor (IGBT)—164.5°C
    - ► Diode—154.2°C
    - ► Coolant fluid—127.8°C

- Completed flow header finite element analysis (FEA) and achieved a balanced coolant flow design to supply the substrates.
- Optimized buss structures within the design inverter performance.

Future Direction

- This project will conclude in FY 2010.

Technical Discussion

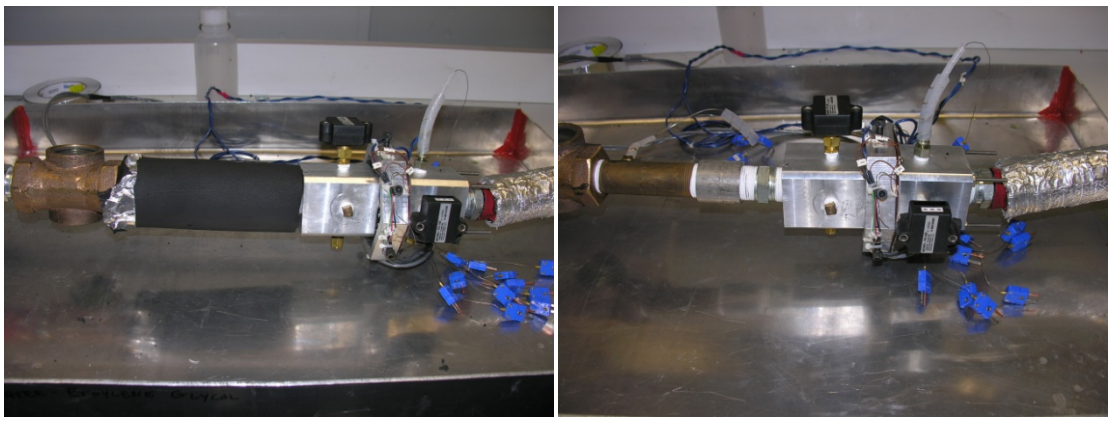
The scope of this project for FY 2010 was to complete the second generation half leg module and test this module's copper plating process. The testing results were then compared to the final FEA results to see whether any improvement in thermal conductivity was achieved with the new plating. Additionally, the complete inverter design was to be finalized, including any module modifications that may have been required, and the necessary components for a complete inverter package fabricated.

Component fabrication consisted of fabricating the alumina substrates; having the substrates metalized, plated, and chips sintered/soldered into position; and wire bonding the completed module. The gate cards and their associated hardware were to be designed and fabricated. The capacitor with its specific direct current (dc) connection points was to be fabricated, and the flow headers and any additional miscellaneous components were to be completed this year.

Completing and Testing Second Generation Module

The second generation half lag module was completed using the new copper plating process. To ensure consistency between FY 2009 and FY 2010 test and model validation, the setup contained power resistors just as in FY 2009. Figures 1 and 2 show the several layers of insulation material and how this insulation was built up, in stages, to isolate the module from the outside environment.

Figure 3 shows the assembled module and the new configuration of the thermocouples. A groove the same size as the diameter of the thermocouple was cut in the ceramic base of the power resistor. Once the thermocouples were installed in this groove, the resistors were then installed in position on the module holder. This assembled configuration provided a more accurate junction temperature reading between the power resistor and the copper base.



(a) **(b)**

Fig. 1. Beginning (a) and intermediate (b) stages of module insulation.

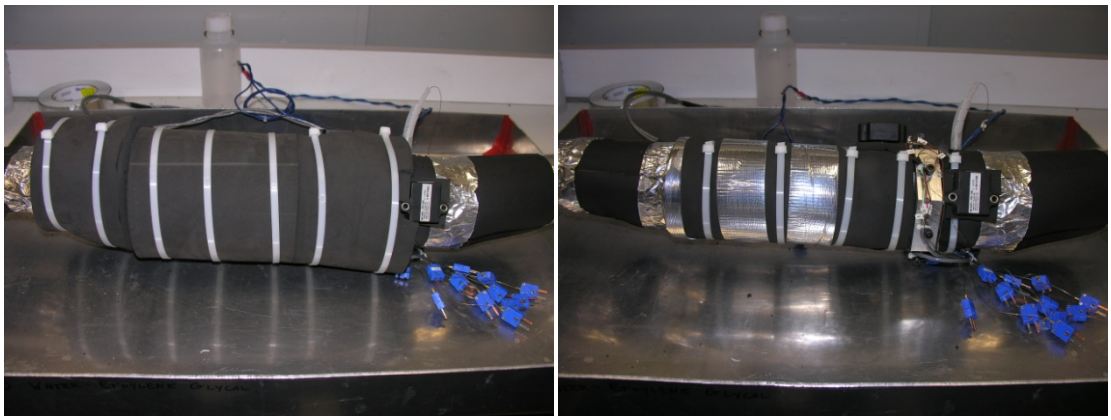
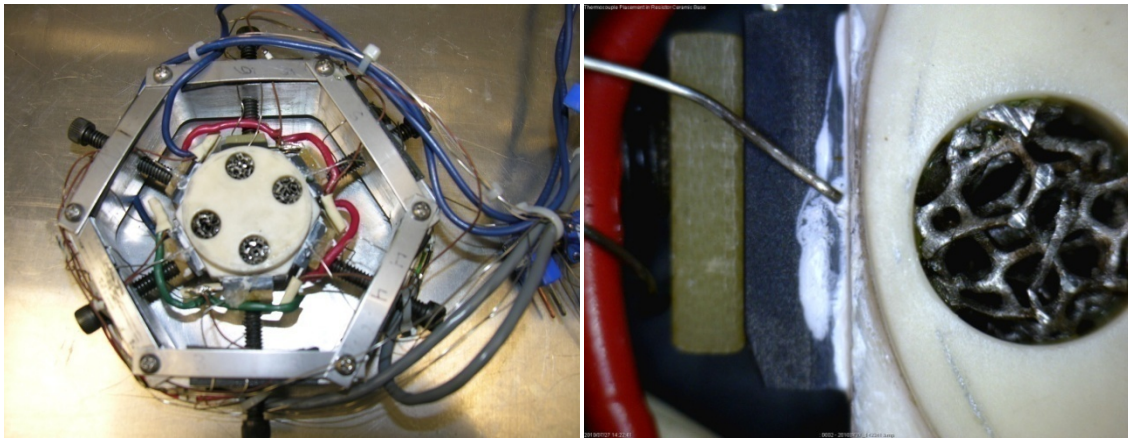


Fig. 2. Final stages of module insulation.



(a) **(b)**

Fig. 3. Assembled module (a) and new configuration of the thermocouples (b).

Figure 4 shows the FEA output for the four-hole design and the locations where the temperature data were taken. As stated previously, the power resistors contained a thermocouple groove cut into the ceramic base for installation of the thermocouple. This placed the measurement device at the closest point to the junction temperature as possible. Table 1 shows a comparison of the test data to the FEA data with the results matching within a 10–15% margin of error.

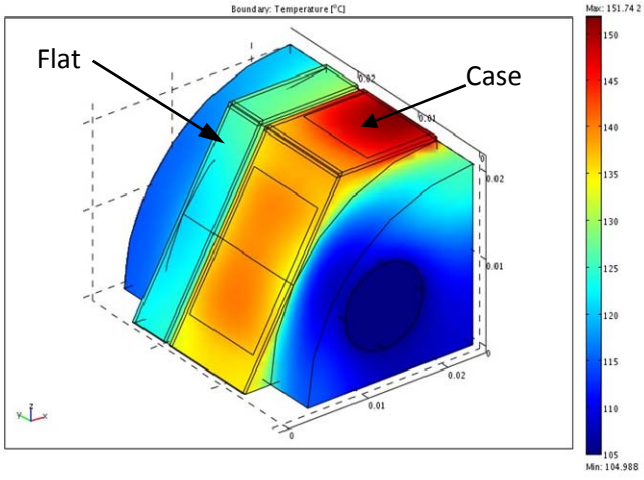


Fig. 4. FEA output for four-hole design.

Finalizing Design Requirements for a Complete Inverter

Results from FY 2009 tests indicated that IGBT and diode temperatures would only rise between 2° and 3°C when operated at the peak performance values of 55 kW from the steady state performance value of 30 kW for 18 s. Taking into account this temperature rise information, a two-

chip-deep octagonal substrate design was produced and FEA results obtained. This design required fewer ceramic modules, produced a more compact design, and allowed for minimal buss connection points. Each octagonal module could operate as a phase of the three phase system; thus the final design only needed three modules. This two-chip-deep octagonal design contained eight coolant channels, each channel located directly under the chips. This arrangement provided the best cooling structure for chip heat dissipation.

Table 1. Comparison of Experimental and Simulated Data for Four-Hole Structure

Nominal inlet temperature (°C)	Electrical power (W)	Heat added to fluid (W)	Results	Average case temperature (°C)	Average flat temperature (°C)
50	331.3	250	Experimental	72.3	37.5
			COMSOL[a]	63.5	32.6
			Error	-12.20%	-13.10%
75	332.25	253.3	Experimental	73.6	35.6
			COMSOL	62.8	30.5
			Error	-14.60%	-14.30%
90	294.9	238.8	Experimental	68.9	29.9
			COMSOL	59.2	25.9
			Error	-14.10%	-13.50%
105	210.4	186.5	Experimental	43.9	21.5
			COMSOL	39.1	19.1
			Error	-10.90%	-11.20%

[a]Simulation software used.

The inverter volume was projected to be 3.6 L with this design. Using a WEG coolant temperature of 105°C and a copper cladding thickness of 0.012 in., the design was projected to achieve a power density of 15 kW/L. This meets the 2020 FreedomCAR target. The maximum steady state temperatures for 30 kW continuous loads were as follows.

- IGBT—164.5°C
- Diode—154.2°C
- Coolant fluid—127.8°C

Figure 5 shows the FEA results for the simulated octagonal module. Figure 6 is an exploded view showing all of the components specified for the Direct Water-Cooled Power Electronics Substrate Inverter Package.

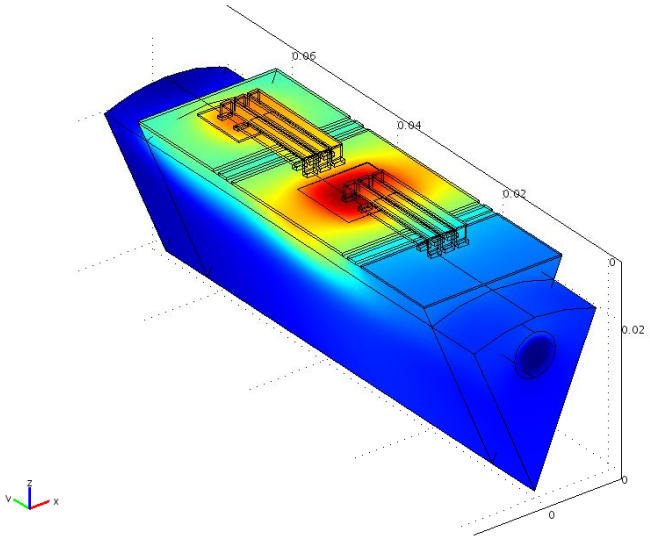


Fig. 5. FEA results of the simulated octagonal model.

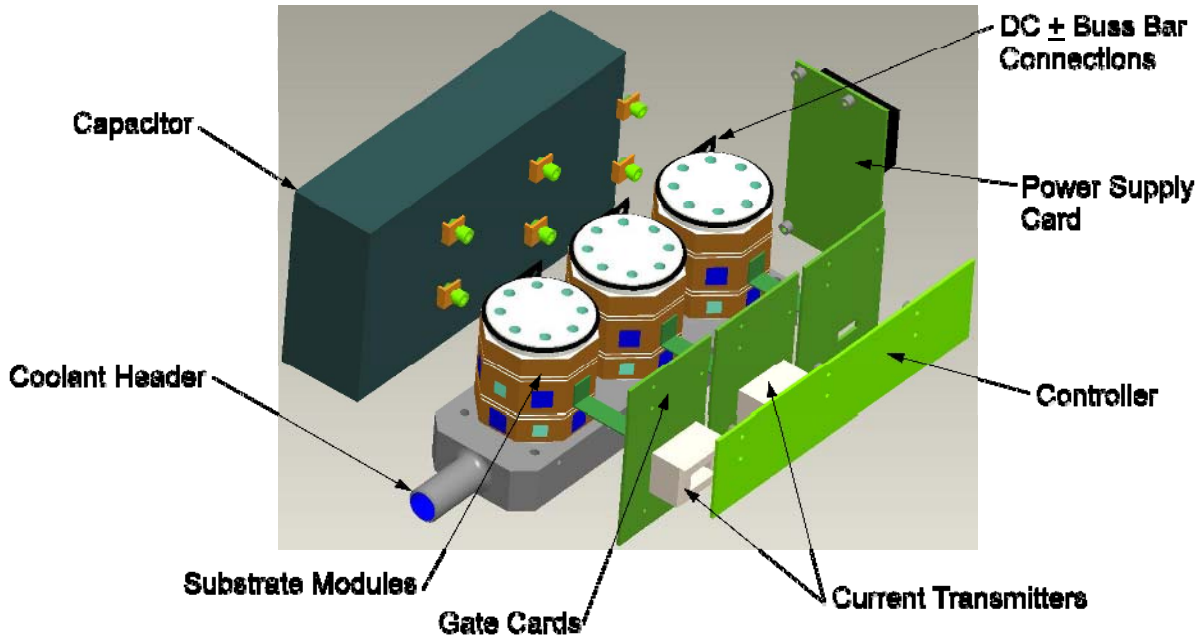


Fig. 6. Exploded view of complete Direct Water-Cooled Power Electronics Substrate Inverter Package (upper coolant header removed for clarity).

3. FABRICATION OF INVERTER COMPONENTS

To evaluate the copper to alumina substrate bond, one of the alumina four-hole substrates was sent to Stellar Industries, Inc., to be copper plated. This process involves plating the part with molybdenum/manganese and firing at a high temperature so the molybdenum/manganese bonds molecularly with the alumina. Then this surface can be plated with copper for an extremely intimate bond between the copper and the alumina substrate. Once a test piece was received from Stellar Industries, the substrate was sectioned and polished so the bond area between the copper and the alumina could be

evaluated under an electron microscope. Figure 7 shows the sectioned part, and Fig. 8 shows the bond area. The plating process used by Stellar Industries produces an excellent bond area, free of voids.

Fig. 7. Sectioned part used for copper bond evaluation.

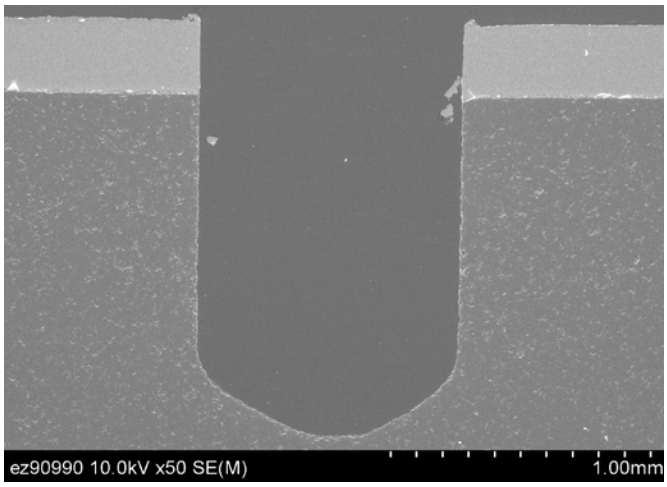


Fig. 8. Magnified bond area shows an excellent bond between the alumina and copper.

After the initial copper plating evaluation, fabrication of the octagonal alumina substrates was completed by CoorsTek, Inc. The parts were initially produced as green parts, rough machined to shape, and fired to their final densification. After firing, the parts were machined to their final dimensional shape. The octagonal flats were checked for flatness, and all parts met the required specification. Figure 9 shows the finished alumina octagonal substrate.

Fig. 9. Finished alumina octagonal substrate fabricated by CoorsTek.

The finished octagonal substrates were shipped to Stellar Industries to be copper plated. Figure 10 shows a final component bonded with copper.

Fig. 10. Final component bonded with copper by Stellar Industries.

Before plating, Stellar Industries performed a dye penetrant test on the substrates to determine the integrity of the parts. This was done to ensure that the parts could withstand high temperature firing without failure. Some of the parts were determined to have fine stress cracks that could possibly affect them during the plating process. Figure 11 shows the cracks revealed by the dye penetrant test.

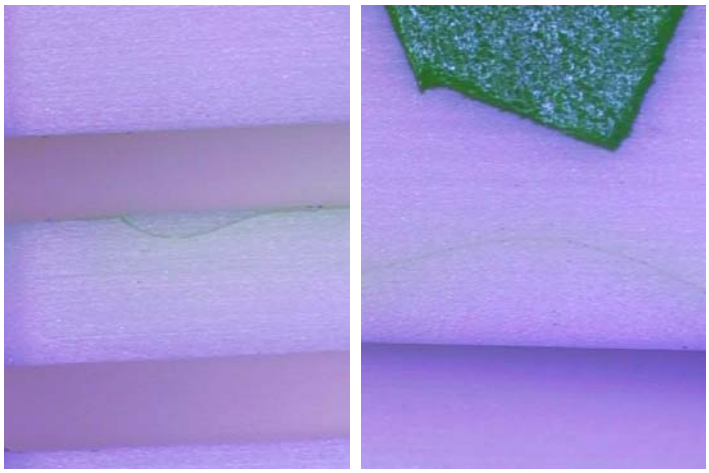


Fig. 11. Cracks revealed by dye penetrant testing.

CoorsTek was contacted concerning the nature of these stress cracks and indicated that the final firing process combined with the final machining process could have produced these fine stress cracks. The CoorsTek process of firing to a final densification of the octagonal substrate and final machining process can be modified to eliminate this problem.

However based on this experience, it was necessary to ensure that if some of the substrates developed fine stress cracks during high volume manufacturing, the plating process would not cause the cracks to propagate to the point of substrate failure. Therefore, the copper plating process was applied to one of the stress cracked parts to determine whether the crack in the substrate would be affected by the high temperature firings of the plating process. Upon completion of the plating process, it was determined that the high temperature firing process had no detrimental effect on the cracked component.

Fig. 12. Nickel-/silver-plated part with IGBTs and diodes sintered into position.

Once the copper plated octagonal structures were received from Stellar Industries, the modules were shipped to NBE Technologies, LLC, to be plated with nickel/silver and then have the IGBTs and diodes sintered into position. Figure 12 shows one of the completed modules. The IGBTs and diodes have been sintered into position and are ready for wire bonding. Also note that the dc connection tabs have been soldered into position.

Flow headers were designed to be multifunctional. The primary purpose of the headers was to be the transport medium for the WEG coolant. The headers also provide structural support for the inverter assembly, the gate cards, the control card, and the power supply card. An FEA analysis was performed on the flow header to ensure a balanced flow between the three supply areas for each of the three modules. Figure 13 shows the balanced FEA result.

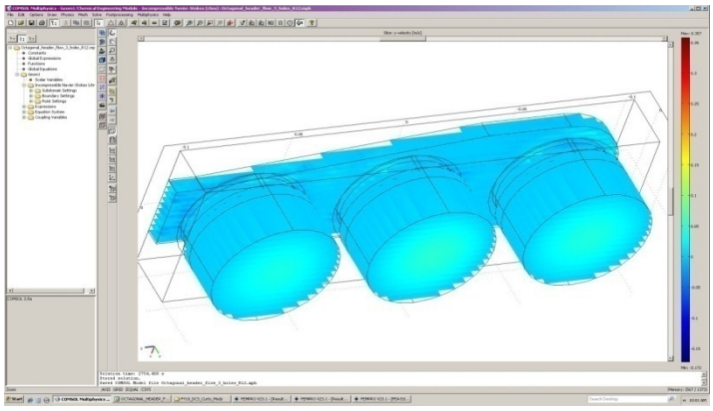


Fig. 13. FEA results of header flow analysis showing a balanced flow.

A flow test was completed and the flow measured between the three output areas to confirm that the flow was balanced. A slight modification was needed to the first flow output area to bring it into balance with the middle and last output area. Figure 14 shows the completed header assembly with the cover removed so the internal flow output areas can be seen. Figure 15 shows the assembly buildup as of September 24, 2010.

Fig. 14. Inverter flow header.

Fig. 15. Inverter assembly buildup as of September 24, 2010 (top flow header removed).

Gate cards were designed to fit within the dimensional specifications necessary to ensure a compact overall volume as well as the electrical requirements for use in high temperature environments. The gate drive board design is capable of driving three 200 A IGBT dies in parallel and plugs directly into the

digital signal processing controller. Figure 16 shows a completed gate drive board which has been populated with the necessary components for high temperature operation.

Fig. 16. Completed gate drive board.

Capacitors necessary to complete the inverter build were fabricated by Electronic Concepts, Inc., in Eatontown, New Jersey. The capacitors were built to a specification of 600 µF and 500 Vdc. The dc connection tabs were specifically placed so it would bolt directly to the tabs on the modules and still remain within the specified volume of the design. Figure 17 shows a completed capacitor.

Fig. 17. Completed capacitor from Electronic Concepts.

Conclusion

The Direct Water-Cooled Power Electronics Substrate Packaging concept developed at ORNL substantially improves upon the established packaging concepts used today through the following.

- Elimination of the auxiliary cooling loop, resulting in a system cost savings of $175.00.
- Removal of the baseplate and heat sink.
- Use of silicon switches with high temperature (105°C) coolant.
- Removal of the TIM or thermal grease, which vastly improves waste heat removal in the system.
- Elimination of the copper baseplate and the aluminum heat exchanger, which results in additional weight, volume, and cost savings.
- Flowing coolant directly through the ceramic substrate, which delivers cooling more directly to the semiconductor dies.

This innovative design and thermal stack reduction is expected to achieve higher inverter power densities and significantly reduce system costs. Results from this program indicate that a 175°C rated silicon IGBT

could work using 105°C WEG coolant. The current design also shows the potential to exceed the 2020 FreedomCAR target of 14.1 kW/kg with the use of 105°C coolant.

Patents

1. R. H. Wiles, et al., *Direct Cooled Power Electronics Substrate,* U.S. Patent 7796388, awarded on September 14, 2010.

2.3 High Temperature, High Voltage Fully Integrated Gate Driver Circuit

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Objectives

- Increase the current drive of the preceding high temperature gate driver circuit design.
- Improve the gate driver design to make it more robust against temperature variation.
- Enhance some gate driver circuitry to improve functionality [e.g., voltage regulator, undervoltage lockout (UVLO)].
- Incorporate additional protective features with the core gate driver circuit (e.g., desaturation detection and gate current monitoring circuitry).
- Integrate a charge pump with the core gate driver to enable a 100% high-side duty cycle.
- Include a low voltage differential signaling (LVDS) circuit.
- Design input-isolation test circuitry as a step toward an input-isolation solution.
- Move all capacitors necessary for full functionality on-chip.
- Rework gate driver layout to increase space use and reliability.

Approach

- Make as much use of the bipolar complementary metal-oxide semiconductor–double diffused metal-oxide semiconductor (DMOS) on silicon-on-insulator (SOI) process features to optimize the gate driver design for high ambient temperature operation.
- Test different types of wide bandgap semiconductor power switches with the driver circuit.

Major Accomplishments

- Designed and sent the fourth generation (Corinth) gate driver circuit for fabrication.
- Made refinements to the LM723 based voltage regulator.
- Integrated the charge pump with the core gate driver.
- Incorporated desaturation detection and gate current monitoring circuitry in the gate driver chip.
- Designed input-isolation test circuitry and placed on the chip.
- Integrated LVDS circuit with the gate driver.
- Integrated capacitors on-chip.
- Reworked gate driver layout.

Future Direction

- Use results from Corinth to improve the gate driver design, if necessary.
- Develop an input-isolation solution.

- Integrate the gate driver with WBG power switches in a smart power module.
- Work with industry to achieve product commercialization.

Technical Discussion

The goal of this project is to develop an SOI based high temperature, high voltage gate driver integrated circuit with high drive current capability for WBG power switches, such as silicon carbide (SiC) and gallium nitride (GaN). Power electronics in future electric vehicles (hybrid, plug-in hybrid, and full electric) are expected to use WBG based power devices which are capable of working at much higher ambient temperatures than the conventional silicon based power switches. Implementation of WBG based power modules in automotives will allow the use of air cooling for electronics under the hood. To obtain the full advantage of the high temperature capability of WBG devices, the associated control electronics (such as gate driver circuits) also need to operate at higher temperatures with minimal thermal management. By placing the gate driver circuit close to the power switches, system reliability as well as performance can be improved.

Third Generation Gate Driver Measurement Results

Figure 1 shows the test setup used for characterizing the prototype third generation (3G) gate driver chips. A polyimide test board with the gate driver chip was placed inside the environmental chamber. Chamber temperature was varied to test the gate driver circuit at different ambient temperatures. For both resistance-capacitance (R-C) load and SiC power switch tests, the actual load was kept outside the chamber. A 600 V, 16 A, direct current (dc) power supply unit was used for the SiC power switch tests.

Fig. 1. High temperature gate driver test setup.

The chip was first tested with the on-chip current limiting resistor R_G connected in series with an external 10 nF capacitive load at different ambient temperatures by placing the test board inside the temperature chamber. Figure 2 shows the 30 V peak-to-peak (−15 V to +15 V), 20 kHz, gate pulse signal generated by the chip at 200ºC ambient temperature with a nominal R_G value of 3.4 Ω. The drive current wave shape is presented in Figure 2. At 200°C, the peak sourcing and sinking currents were 2.5 A and 2.2 A, respectively.

Figure 3 presents the measured source and sink current peaks at different ambient temperatures for three different integrated circuits (ICs) with the same R-C load (R_G = 3.4 Ω and C =10 nF). Small chip-to-chip variations in drive current were observed.

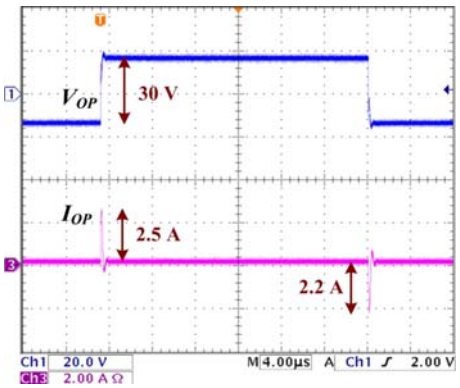

Fig. 2. R-C load test results at 200°C with R_G =3.4 Ω and C_{Load} = 10 nF.

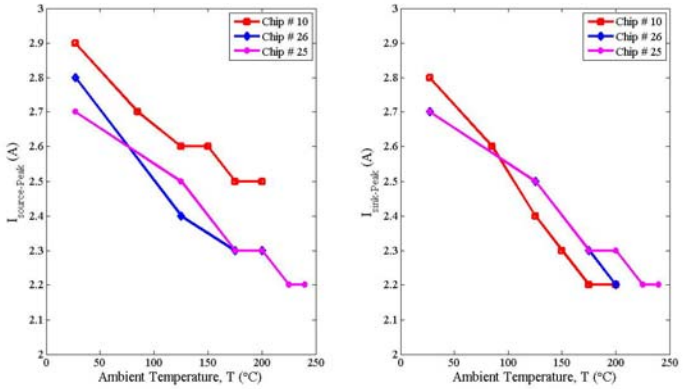

Fig. 3. Measured source and sink current peaks at different ambient temperatures for three different ICs with same R-C load (R_G= 3.4 Ω and C=10 nF).

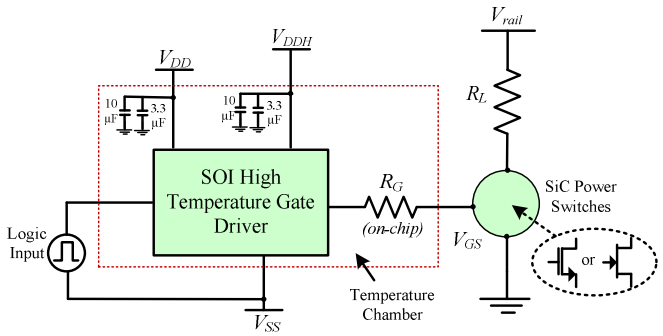

Fig. 4. Schematic of test setup for MOSFET (VDDH = 15 V, VSS = −5 V) and for normally ON JFET module (VDDH = 3 V, VSS = −5 V).

A SiC powered metal-oxide semiconductor field-effect transistor (MOSFET) (1,200 V, 10 A) prototype device developed by Cree was tested with this gate driver chip. An 80 Ω, 250 W load resistor (in series with the drain terminal) was used with the SiC MOSFET in a common-source configuration. Figure 4 shows the test connection for the SiC powered MOSFET test with the gate driver circuit.

Rail voltage was set at 560 V using a 600 V, 16 A, dc power supply. A 7 A peak load current was passed through the MOSFET when it was turned "ON" by the gate driver chip. A 20 V peak-to-peak (+15 V to −5 V) drive signal was applied to the gate terminal of the SiC MOSFET through the 3.4 Ω on-chip current limiting resistor (R_G). The test board was placed inside the temperature chamber, and the SiC MOSFET was kept outside the chamber as it was not packaged for high temperature applications. Starting from room temperature, the chip was tested up to 200ºC. Switching frequency was set at 20 kHz, and the duty cycle was 5%.

Figure 5 shows the gate voltage (pink), MOSFET drain terminal voltage (blue), and load current (cyan) waveforms at 200°C. The temperature of the chamber was raised from room temperature to 200°C in three steps (27°C, 125°C, and 200°C). The ringing effect observed in the wave shapes was due to the added parasitic inductances of the connection wires that ran from inside the temperature chamber to the outside load. A 10% to 90% rise time and a 90% to 10% fall time for both the gate drive voltage signals and the MOSFET drain voltage at each temperature level are recorded in Table 1. These readings show that this high temperature gate driver circuit maintains a fairly constant driving strength over the entire test temperature range.

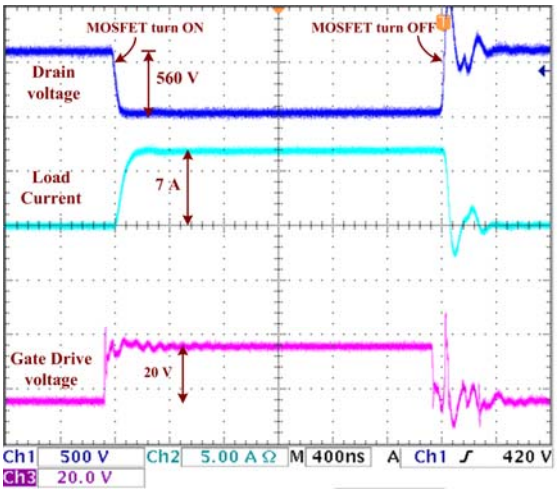

Fig. 5. Prototype circuit's test results at 200°C when driving a 1200 V, 10 A, SiC MOSFET.

Table 1. Rise Time and Fall Time at Different Ambient Temperatures

Ambient temperature (°C)	Drain voltage (V_{DS})		Gate voltage (V_{GS})	
	t_{rise} (ns)	t_{fall} (ns)	t_{rise} (ns)	t_{fall} (ns)
27	15.7	33.4	2.8	3.6
125	15.7	35.1	3.1	4.0
200	20.2	41.0	4.0	5.6

The prototype high temperature gate driver IC was also tested with an SiC normally "ON" junction field-effect transistor (JFET) (1,200 V, 50 A) power module developed by Microsemi using SemiSouth's normally "ON" SiC JFET. A gate driver circuit was biased to generate an 8 V peak-to-peak (−5 V to

+3 V) gate signal to control the JFET module which was connected to a 560 V rail voltage through an 80 Ω load resistor. Figure 6 shows the test result at 200°C ambient temperature with 1 kHz switching frequency.

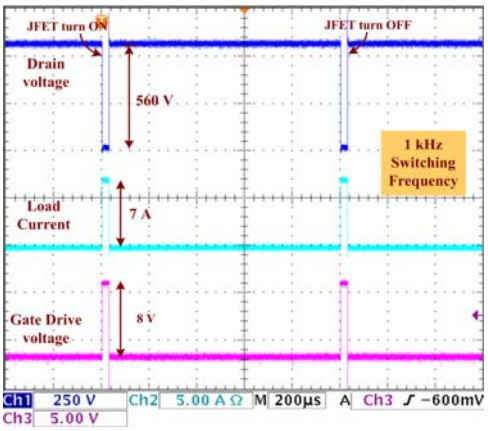

Fig. 6. SiC normally ON JFET module (1200 V, 50 A) test results.

The wide temperature on-chip voltage regulator exceeds the operating range and temperature stability performance of commercially available voltage regulators, including the LM723 Zener reference based voltage regulator design upon which it is based. The measured parabolic temperature curve of the new SOI voltage regulator indicates minimal output voltage variation over the entire temperature range thanks to the reference voltage temperature compensation scheme used in this design. The voltage regulator is capable of operating in environments up to 250°C. The regulated voltage over temperature is shown in Fig. 7.

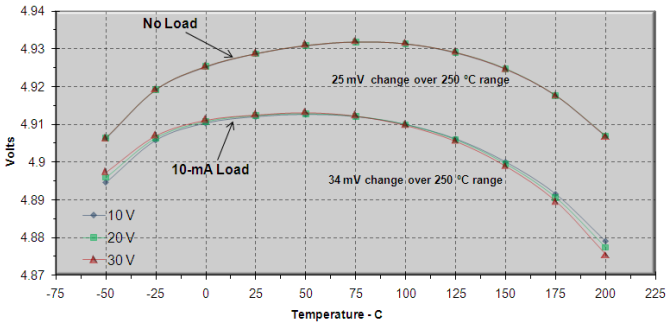

Fig. 7. Regulated voltage over temperature.

This 3G gate driver also contained several protection circuits that will send a fault signal to the gate driver logic if operational boundaries are exceeded. These circuits included a temperature sensor, UVLO circuit, and short circuit protection (SCP) circuit. The temperature sensor is designed to have nearly zero quiescent power loss until it approaches high temperature, unlike traditional sensors that have nearly constant power dissipation over temperature [1]. Several temperature cycles were carried out to measure the upper and lower triggering temperatures for this sensor circuit. Figure 8 shows the results of these temperature cycle tests for several chips.

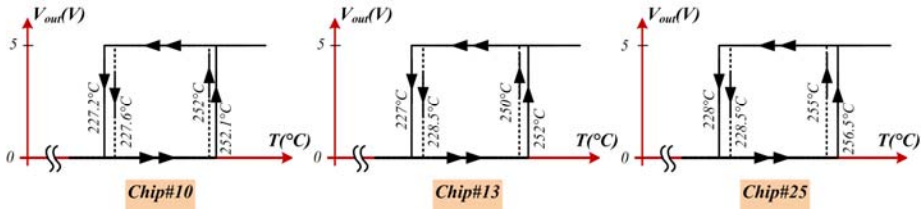

Fig. 8. Temperature sensor output in response to temperature cycling.

The SCP circuit measures the current through the power device driven by the gate driver and sends a fault if this value exceeds the limits set by the user. Figure 9 demonstrates the SCP circuit in action at 175°C detecting a high current event and sending a fault signal and recovery from the fault. After detecting a high current incident, the SCP shunts voltage from the gate of the power device to reduce the fault current before sending the fault signal that deactivates the gate driver.

(a) **(b)**

Fig. 9. SCP test results at 175°C of current fault: (a) fault "ON"; (b) fault "OFF."

The UVLO circuit monitors the supply (VDD and VDDH) power rails and sends a fault signal if they drop below 10% of their rated value. Figure 10 shows measurement results at 200°C for the 5 V power rail switching between undervoltage and nominal voltage conditions.

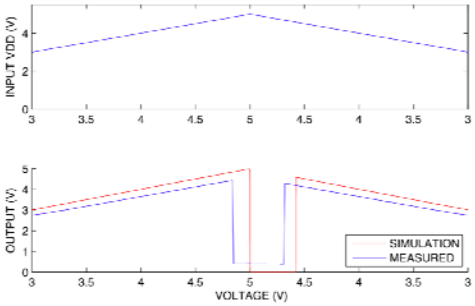

Fig. 10. UVLO detecting an undervoltage at 200°C on the 5 V rail.

Fourth Generation (Corinth) Gate Driver

Circuit design, simulation, layout, post-layout simulation, and submission for fabrication for the Corinth gate driver circuit have been completed. Figure 11 shows the block diagram schematic of the Corinth gate driver circuit. Compared to earlier prototypes, this version of the gate driver comprises several modifications and improvements in the core driver circuit.

Fig. 11. Block diagram of Corinth.

Charge Pump

The charge pump was designed to replace the bootstrap capacitor and diode used in previous revisions of the gate driver. The bootstrap circuit was used to provide a 5 V floating supply rail to power the high-side circuitry that drives the current sourcing output transistor, M_H. It necessitated periodically turning the gate driver output "OFF" to allow the bootstrap capacitor to recharge. This effectively limited the lower frequency bound for the operation of the gate driver to no less than 1 kHz for reliable operation.

The charge pump in Fig. 12, based on [2], removes the recharge cycle limitation by providing charge independent of the gate driver's switching state. This is accomplished by continually refreshing the charge of capacitor C2. A logic signal, V_{SWITCH}, drives switches S1 and S2. When this signal is high, S1 is "ON," allowing current to flow through diode D1 and charging the boost capacitor C1. At the same time S2 is "ON," maintaining switch S3 in an "OFF" state. When switches S1 and S2 are turned "OFF," the charge on capacitor C1 begins to charge the gate of switch S3 through resistor R1, eventually activating switch S2. With switch S2 "ON," capacitor C1 is connected to C2, and charge is exchanged. When switches S1 and S2 are activated again, switch S3 is pulled low and deactivated, while capacitor C1 is again placed in charging mode. With continuous cycling, based on the logic control signal V_{SWITCH}, charge is maintained on capacitor C2, and power is constantly available to the high-side circuitry of the gate driver, allowing for 100% high-side duty cycle operation.

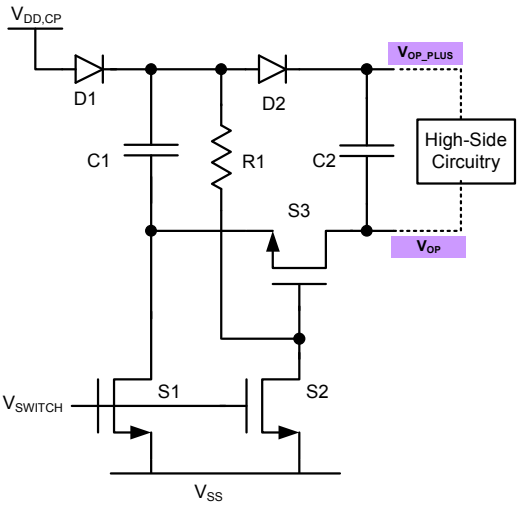

Fig. 12. Basic charge pump schematic.

$V_{DD,CP}$, the power supply used to charge capacitor C1, is supplied by a version of the voltage regulator modified to provide a particular voltage curve of 6.7 V to 6.2 V across 27°C to 200°C. This is done to offset the change in the diode's voltage drop for the same temperature range and allow for a supply voltage of about 5 V to be available to the high-side circuitry for the entire temperature range.

Output Drivers

As observed in Fig. 3, showing test results from the 3G gate driver, the maximum output current drive at 200°C was not as high as expected. While drive current is greater than 2.2 A at 200°C, maximum current was expected to be about 5 A. The source of the lower current drive is believed to be related to self-heating of the output drivers. The output driver arrays were made up of eight hundred 45 V lateral DMOS devices, each on the 3G design. These devices were placed at minimum spacing from each other, which would create the worst case self-heating effects. Several steps have been taken to alleviate this condition: the devices have been spaced further apart; heat pipes (metal traces tied to ground and pads) were added to help remove heat from the output driver area of the chip; and wider metal traces were used for all high current wires (and elsewhere where possible), as shown in Fig. 13.

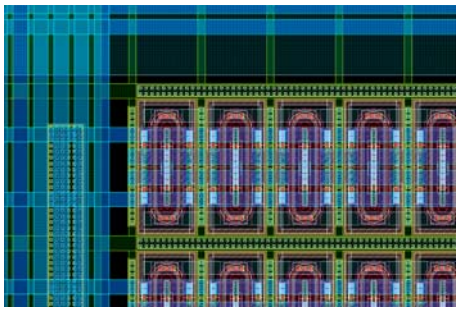

Fig. 13. Corner of output driver on Corinth.

Voltage Regulator

The Corinth voltage regulator design implements the same basic LM723 topology seen in the 3G voltage regulator [3]. The impressive temperature performance and supply rejection found in the 3G design is once again used while 3G test data allow for significant design improvements. The most significant improvements of the Corinth voltage regulator result from modifications to the operational amplifier output stage. As seen in Fig. 14, the output stage of the Corinth voltage regulator has been implemented as a class-AB source follower. The class-AB output stage significantly reduces the output impedance and allows for symmetrical sinking and sourcing of output current. An output capacitor is used to supply load

current during transient events, as these load transients greatly exceed the bandwidth of the op-amp (operational amplifier). To ensure the pole generated by the output capacitor occurs beyond the unity-gain frequency, the output stage requires a low output impedance and therefore a large quiescent current (about 2 mA). With this arrangement, the output capacitor of the voltage regulator is able to supply charge to the gate driver circuits during load current transients without inducing instability.

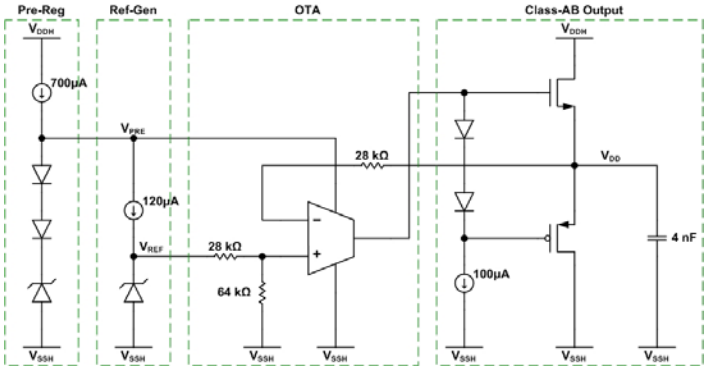

Fig. 14. Voltage regulator topology.

The preregulator and reference generator of the Corinth voltage regulator are relatively unchanged with only slight changes in biasing and temperature compensation schemes to accommodate the changes made in the op-amp design. The Corinth voltage regulator also improves on the offset voltage found in the 3G voltage regulator. Because device matching is impossible for laterally-diffused bipolar junction transistor (BJT) devices, the bias point of the differential input pair is set to minimize the effects of input bias current at the output. Figure 15 shows a simulation of the voltage regulator's output voltage for the fully integrated gate driver during a transient event, the switching of the gate driver output. The output of the voltage regulator is maintained within 125 mV of the nominal value during all transient events. This modest variation in output voltage is within the requirements of the gate driver circuits and allows for reliable operation without the requirement of an external capacitor.

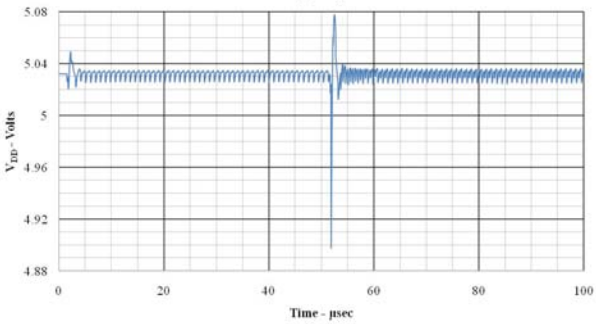

Fig. 15. Corinth voltage regulator transient event simulation.

Undervoltage Lockout

The integrated UVLO circuit used in the gate driver monitors V_{DDH}–V_{SSH} and provides an enable signal when usable supply voltages are available. The Corinth UVLO uses a current-sourced Zener diode to provide the reference voltage for the UVLO comparator, shown in Fig. 16. This reference voltage is compared to resistively-divided V_{DDH}–V_{SSH}, where the resistors R_1 and R_2 are set according to the value of V_{DDH}–V_{SSH} via external jumpers. The 3G UVLO used a resistively loaded Zener diode reference that failed due to large diode currents. In addition to providing a more robust architecture, the reference circuit used in the Corinth UVLO provides improved supply rejection for more accurate UVLO performance [4].

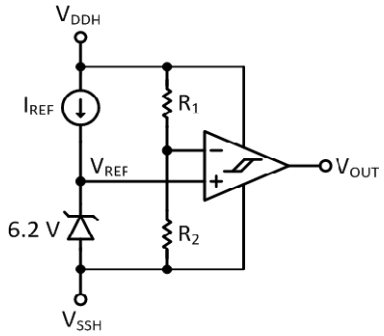

Fig. 16. UVLO topology

Low Voltage Differential Signaling Receiver

The Corinth gate driver circuit is designed to allow the use of LVDS for input signal transmission. This signaling method provides low noise, high speed signaling capabilities to increase reliability of gate

driver operation. To properly use LVDS, the Corinth chip requires an on-chip LVDS receiver circuit (Fig. 17) to convert the LVDS signal into a usable single ended 5 V signal.

This circuit design consists of a positive feedback decision circuit (M5–M8), an output buffer (M9–M12), and two inverter stages (M13–M16). The decision circuit inherently incorporates hysteresis into the threshold characteristic of the LVDS receiver. This hysteresis aids in reducing the effects of differential and common-mode noise injected into the input signal. The LVDS input signal is a 350 mV_{p-p} square wave with a 1.25 V common-mode voltage. Figure 18 shows the LVDS receiver simulation performance for a 1 MHz input signal with a 10 pF load capacitance. Simulations over temperature reveal modest delay time changes that lie well within LVDS and Corinth requirements.

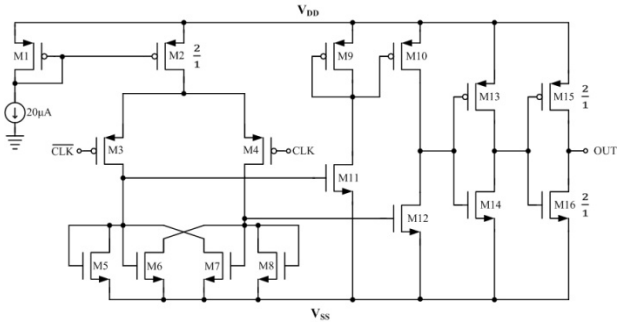

Fig. 17. Corinth LVDS receiver.

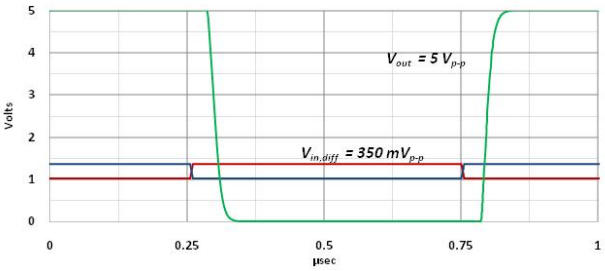

Fig. 18. Corinth LVDS receiver simulation at 200°C.

Photodetector

Among the input isolation test circuitry on Corinth is a photodetector for testing an in-package optical isolation approach using an on-chip photodetector and in-package light emitting diode (LED) to provide the electrical isolation required to operate the gate driver in bridge configurations (Fig. 19). To withstand the harsh temperature of the application environment an LED similar to a GaN LED will be used.

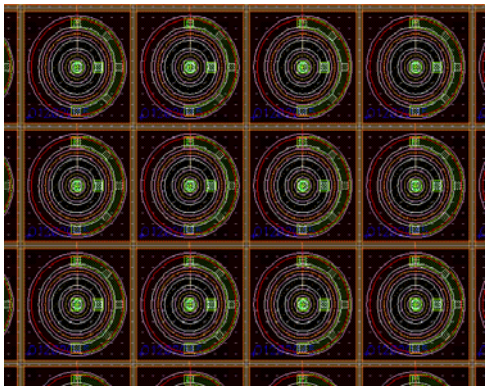

Fig. 19. Array of open-base NPN BJTs.

The photodetector is composed of an array of NPN BJTs in which the photosensitive base is left open and has no electrical connection. When a photon is incident on the base, electron hole pairs generated in the reverse biased base-collector junction are swept out of the space charge region giving rise to a photocurrent. This photocurrent is injected into the base, forward biasing the base-emitter junction. This leads to normal transistor action. The photocurrent in the base is multiplied by the transistor current gain β. To increase the current driving capacity, multiple phototransistors will be used in an array configuration. The depletion region of the collector has a high carrier generation efficiency, so a metal window will be placed across the collector junctions of the transistors. The transistors are biased to operate in the forward-active region, and a current mirror will duplicate the photodetector's current across a resistor to create a detectable voltage. This configuration is shown in Fig. 20.

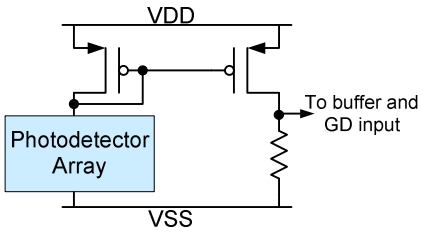

Fig. 20. Photodetector configuration.

Transformer Based Isolation Circuitry

The transformer based input isolation test circuitry is designed to give an impression of how an on-chip transformer based solution might perform. It uses an on-chip transformer to isolate the logic-level control signal from high voltage transient signals of the gate driver. Because the on-chip transformer is designed and optimized at a specific frequency, any noise at other frequencies will be decoupled from the gate driver side. Even for noise near the operating frequency of the transformer, the isolation will be significant such that the input control sections are isolated from the gate driver circuits.

The transformer based input isolation is shown in Fig. 21. It operates by modulating the input signal with the high frequency output from an oscillator. The modulated or chopped differential high frequency signal is then buffered to match the transformer's low input impedance. On the output of the transformer the signal is fed into a differential envelope detector composed of a full-wave rectifier and RC load, which is partially the parasitic impedance of the input gate of driver circuits.

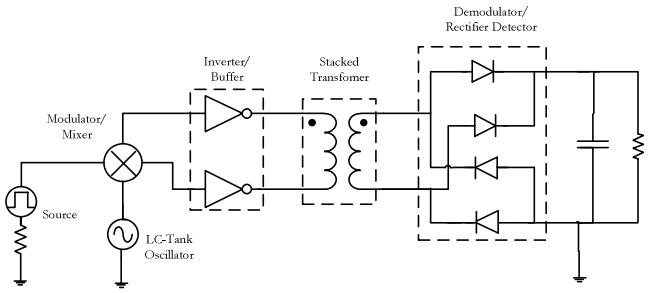

Fig. 21. Block diagram of transformer based input isolation.

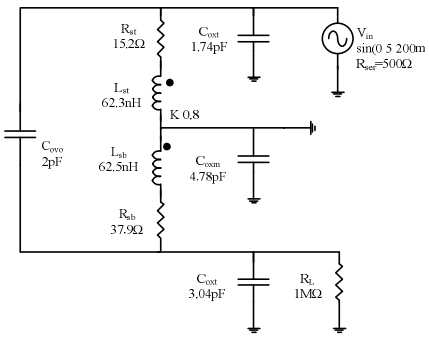

Fig. 22. Lumped analytical model for stacked transformer.

A stacked architecture was chosen for the on-chip transformer. Stacked transformers provide higher coupling efficiency but larger parasitic capacitance, which leads to a lower resonant frequency compared with planar types. However, for an operating frequency of 200 or 300 MHz, a stacked transformer with a resonant frequency of more than 1 GHz can be implemented without parasitics being a concern [5–7]. As no support for transformers is provided by the SOI process, the transformer design was accomplished by using a lumped transformer model. Based on process parameters, a stacked transformer with an outer diameter of 700 µm, 10 turns, a winding width of 20 µm, and a winding space of 2 µm was chosen. The lumped analytical model is shown in Fig. 22.

The oscillator used for generating the 200 MHz high frequency carrier signal is shown in Fig. 23. It is an LC-tank oscillator commonly used in RF circuits. One of the key components of an LC-tank oscillator is the parallel inductor and capacitor and their associated parasitic capacitance and resistance. Based on the inductors designed for the transformer, an inductor constructed for one side of the transformer with an inductance no less than 130 nH was designed. The associated series resistance, interwinding, and ground coupling capacitance are estimated following the methods used in the transformer design. The PMOS and NMOS transistors have large width-to-length ratios to facilitate the oscillation, providing strong positive feedback.

The simulation results for the complete system are shown in Fig. 24. The oscillator signal is the 200 MHz output of the LC tank. This signal is then modulated with the gate driver's input signal to produce a modulated input signal which is fed into the transformer through buffers. The output of the transformer is connected to the input of the rectifier. The rectifier's output is a close reproduction of the original input signal.

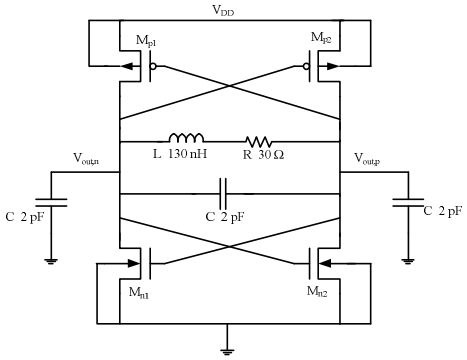

Fig. 23. LC-tank oscillator.

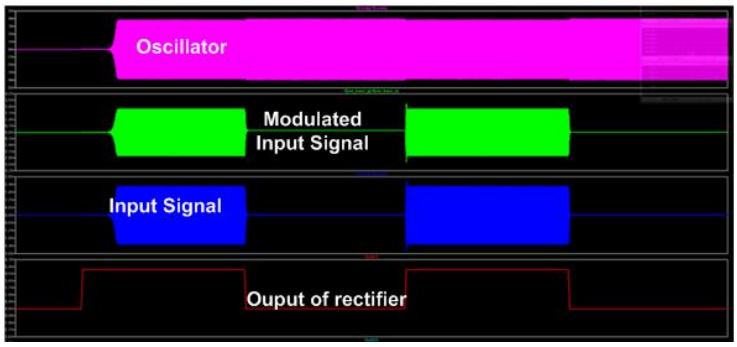

Fig. 24. Transformer based isolation simulation.

Short Circuit Protection

High temperature testing (up to 200°C) has been conducted on the 3G short circuit protection (SCP) circuit. The SCP circuit operates by monitoring the source current of the power device and sending a fault signal if the value moves beyond set parameters. The measurement results, Fig. 9, match well with simulations. In the measurements, V_{ref} is set to 400 mV, while V_{sense} is 1 Hz square wave from 0.3 V to 0.5 V. The gate driver input signal is set to 10 kHz square wave, with no load at the output.

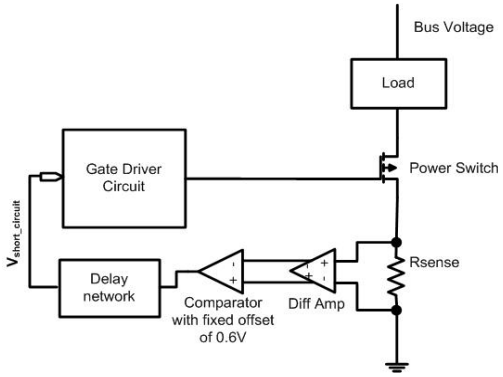

Fig. 25. Circuit diagram for SCP.

The improved Corinth version of the SCP has been altered to include a differential amplifier, Fig. 25, similar to the amplifier used in the new gate current monitoring circuitry. The amplifier helps to reduce noise from the sense resistor input signals by canceling out the common-mode noise present in the signals.

Desaturation Short Circuit Protection

Desaturation SCP is used to detect when a power switch is "ON" but is not operating within the saturation region, a high V_{CE} or V_{DS} event (a potential high or short circuit current condition). The schematic for the circuit is shown in Fig. 26. Under normal load the power switch is "ON." Diode D2 turns on with the power switch to provide $Va = V_{CE} + V_{D2}$ and $V_{C1} = [R2/(R2+R3)] \times (Va - V_{D4})$. Here, V_{D2} is the anode to cathode forward-bias voltage for diode D2, and V_{CE} is the voltage drop across the power switch (power switch load not shown). In this case, there is no fault signal. When a short circuit occurs, V_{CE} and Va increase due to the increase in current. As a result, C1 is charged to a higher voltage. When V_{C1} reaches V_{ref}, a fault signal is generated to shut "OFF" the power switch. The power switch will remain "OFF" until the SCP situation is removed externally.

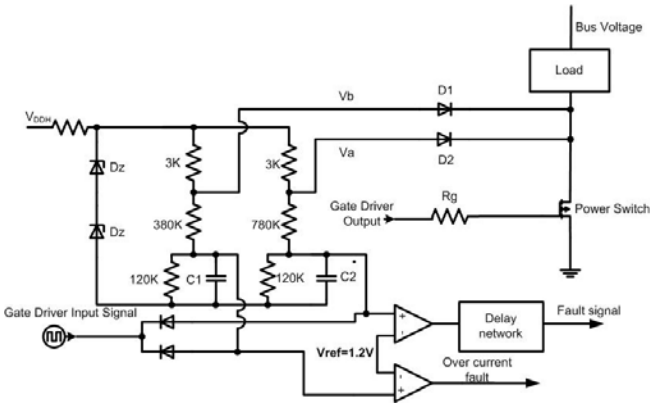

Fig. 26. Desaturation SCP.

Gate Current Monitoring

Gate current monitoring is necessary to protect the gates of the power switches. Transient gate current usually exists during the transient switching of the power devices as the gate drive quickly charges and discharges (less than 10 ns) the gate capacitance. However, under certain situations, such as a short circuit or excessive device wear, the gate current can become higher or last longer and become unsafe to the device or system. This can cause irreversible damage to the power device. Excess and continuous gate current is usually due to a short between the gate and the source while longer duration gate current is mainly due to the dielectric wear of the power device [8].

The gate current monitoring circuit, Fig. 27, uses a sense resistor placed in series with the gate resistor to detect the fault current. Any current outside of the expected range or lasting longer than expected will be detected as a fault by the circuit. It operates as follows.

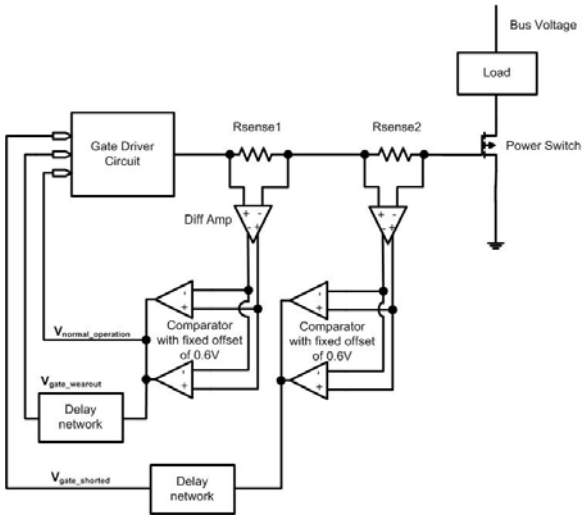

Fig. 27. Gate current monitoring.

- The gate current is converted to a voltage by the *Rsense* resistor.
- Normal switching current will be detected by reference *Vref2*; thus signal *Vnormal_operation* is sent to the gate driver core circuit.
- If the gate current lasts longer than expected, it will be detected by the delay network block and fault signal *Vgate_wearout* is sent to the gate driver circuit.
- Excess high and persistent gate current will be recognized by *Vref1* and trigger the *Vgate_shorted* signal.

Extensive simulations have been conducted across temperature as the gate driver output voltage can swing 30 V peak to peak within 10 ns. A brief look at simulation results is provided in Figs. 28 and 29, with a 30 V supply at room temperature. Figure 28 shows the normal operation of the gate driver chip as a pulse of *Vnormal_operation* is generated during each switching transient. Figure 29 illustrates both gate degradation and shorted situations where the signals *Vgate_wearout* and *Vgate_shorted,* respectively, will be triggered.

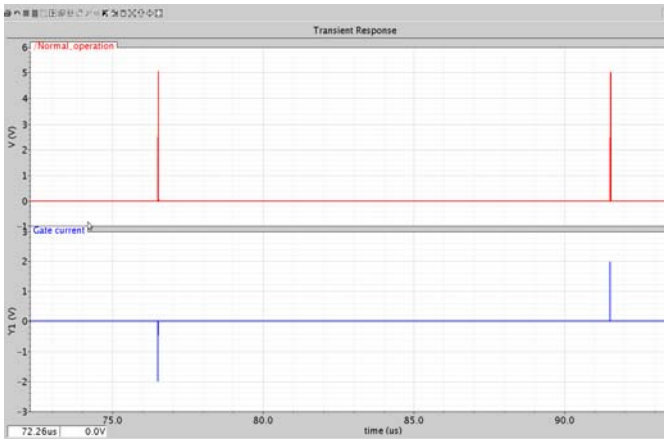

Fig. 28. Normal operation of gate driver.

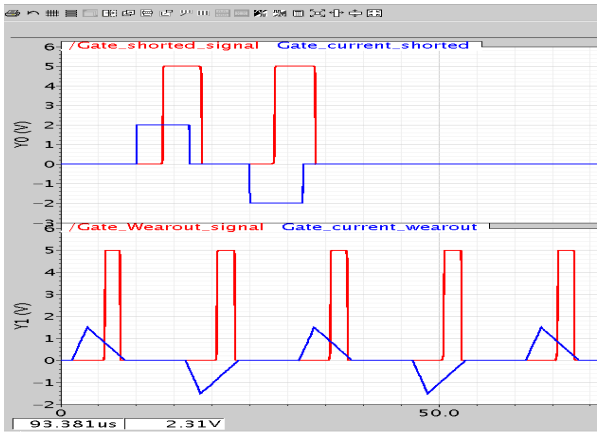

Fig. 29. Gate wear and gate shorted situation.

Conclusion

This challenging project involves the development and demonstration of a high temperature, high voltage gate driver circuit with large current sourcing/sinking capability to drive different types of WBG power switches. Successful integration of this gate driver circuit with WBG power switches will result in smart power converter modules with reduced volume and weight compared to the conventional all silicon based topologies. The 3G gate driver chip designed in 2009 has been shown to operate at 200°C with a current drive strength greater than 2.2 A at frequencies greater than 100 kHz with no active or passive cooling mechanism.

The improved version of the gate driver, Corinth, is currently being fabricated. Its enhancements include a higher output drive current, refined voltage regulator, charge pump for 100% high-side duty cycle, and LVDS circuit. The new protection features, gate current monitoring and desaturation SCP, augment the previously available on-chip circuits. Also, the input isolation test circuitry is a step toward an on-chip or in-package integrated approach to input isolation.

Publications

1. M. A. Huque, et al., "SOI-Based High-Voltage, High-Temperature Integrated Circuit Gate Driver for Sic-Based Power FETs," *IET Proceedings on Power Electronics,* Vol. 3, 2010 (in press).
2. Liang Zuo, et al., "A Universal BCD-on-SOI Based High Temperature Short Circuit Protection for SiC Power Switches," IMAPS International Conference on High Temperature Electronics (HiTEC 2010), May 11–13, 2010, Albuquerque, New Mexico.
3. Liang Zuo, et al., "A Universal SOI Based High Temperature High Voltage Gate Driver Integrated Circuit for SiC Power Switches with Short Circuit Protection," accepted for poster presentation at IEEE Lester Eastman Conference, August 3–5, 2010, Troy, New York.
4. Chiahung Su, et al., "A High-Temperature, High Voltage Linear Regulator in 0.8µm SOI BCDMOS," IMAPS International Symposium on Microelectronics, November 1–5, 2009, San Jose, California.
5. M. A. Huque, et al., "A High-Temperature, High-Voltage SOI Gate Driver IC with High Output Current and On-Chip Low-Power Temperature Sensor," 42nd International Symposium on Microelectronics (IMAPS 2009), November 1–5, 2009, San Jose, California.

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8. L. Chen, F.Z. Peng, and D. Cao, "A smart gate drive with self-diagnosis for power MOSFETs and IGBTs," *2008 IEEE Applied Power Electronics Conference and Exposition*, February 24–28, 2008, Austin, Texas, pp.1602–1607 (2008).

2.4 Inverter Using Current Source Topology

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Objectives

- Overall project objectives
  - Develop new Z-source current source inverter (ZCSI) topologies that combine the benefits of ORNL's current source inverter (CSI) efforts and Michigan State University's work on Z-source inverters (ZSIs) to significantly reduce cost and volume through the integration of voltage boost, inverter, regeneration (regen), and plug-in electric vehicle (PEV) charging functions.
- Objectives for FY 2010 effort
  - Perform a simulation study on selected ZCSI topologies.
  - Produce a design for a 55 kW ZCSI based on the selected topology.
  - Perform a feasibility assessment of using the ORNL voltage to current source (V-I) converter based CSI topology for hybrid electric vehicle (HEV) configurations with more than one motor.

Approach

- Use ORNL's CSI with a quasi-Z network (ZCSI) of passive components to enable
  - single stage voltage buck and boost power conversion,
  - battery charging, and
  - safe operation in open circuit events.
- Eliminate antiparallel diodes with reverse-blocking (RB) insulated gate bipolar transistors (IGBTs).
- Reduce total capacitance.
- Provide sinusoidal voltages and currents to the motor.
- Demonstrate tolerance of phase leg shoot-through conditions.
- Extend constant-power speed range without using a dc-dc boost converter.

Major Accomplishments

- Developed two new ZCSIs with a reduced component count: a current-fed trans-ZSI (CF-trans-ZSI) and a CF-trans-quasi-ZSI (CF-trans-qZSI). Simulation study indicates the new ZCSIs have a voltage boost ratio of 3 in contrast to 2 for the previous ZCSIs.
- Completed a design for a 55 kW ZCSI based on the CF-trans-qZSI using first generation RB-IGBT technology. The design yields a specific power of 4.89 kW/kg, a power density of 16.6 kW/L, and an efficiency of 93.8% in boost mode and 94% in buck mode. With next generation RB-IGBT technology, the efficiency numbers can be increased to 96% and 96.7%, respectively.
- Confirmed through simulation the feasibility of using the ORNL V-I converter based CSI topology in series and power-split series parallel HEV configurations. The CSI dual-motor-drive power

electronics (PE) using RB-IGBTs provides significant performance improvements over the 2007 Camry PE:
- 49% increase of specific power (6.4 vs 4.3 kW/kg),
- 60% increase of power density (9.9 vs 6.2 kW/kg), and
- 34% reduction of cost ($15.4/kW vs $23.2/kW).

Future Direction

- Further improve the specific power and power density of the ZCSIs by reducing the size and weight of the passive components.
- Investigate by simulation and experiment performances of the two new ZCSIs for charging batteries in PEVs.
- Design, fabricate, and test a 55 kW ZCSI prototype.
- Design, build, and test a 55 kW V-I converter based CSI dual-motor-drive inverter prototype.

Technical Discussion

Background

Current electric vehicles (EVs) and HEVs use inverters that operate off a voltage source. They are called voltage source inverters or VSIs [Fig. 1(a)] because the most readily available and efficient energy storage devices, batteries, are inherently voltage sources. The VSI, however, possesses several drawbacks that make it difficult for it to meet the FreedomCAR goals for inverter volume, lifetime, and cost established by the U.S. Department of Energy and its industrial partners [1]. The VSI requires a very high performance direct current (dc) bus capacitor to maintain a near ideal voltage source and absorb the ripple current generated by the switching actions of the inverter. The root mean square (rms) value of the ripple current can reach 50% to about 80% of the motor current. Concerns about the reliability of electrolytic capacitors have forced HEV makers to use film capacitors, and currently available film capacitors that can meet the demanding requirements of this environment are costly and bulky, taking up one-third of the inverter volume and making up one-fifth of the cost. The reliability of the inverter is also limited by the capacitors and further hampered by the possible shoot-throughs of the phase legs making up a VSI [S_1–S_2, S_3–S_4, and S_5–S_6 in Fig. 1(a)]. Steep rising and falling edges of the pulse width modulated output voltage generate high *dv*/*dt* related electromagnetic-interference noises, cause motor insulation degradation due to the voltage surges resulting from these rapid voltage transitions, produce high frequency losses in the windings and cores of the motor, and generate bearing-leakage currents that erode the bearings over time. Furthermore, for the VSI to operate from a low voltage battery, a bidirectional boost converter is needed.

All these problems can be eliminated or significantly reduced by the use of another type of inverter, the CSI [Fig. 1(b)]. The CSI requires no dc bus capacitors and uses only three alternating current (ac) filter capacitors of a much smaller capacitance. The total capacitance of the ac filter capacitors is estimated to be about one-fifth that of the dc bus capacitors in the VSI. In addition, the CSI offers many other advantages important for EV/HEV applications: (1) it does not need antiparallel diodes in the switches, (2) it can tolerate phase leg shoot-throughs, (3) it provides sinusoid-shaped voltage output to the motor, and (4) it can boost the output voltage to a higher level than the source voltage to enable the motor to operate at higher speeds. These advantages could translate into a significant reduction in inverter cost and volume, increased reliability, a much higher constant-power speed range, and improved motor efficiency and lifetime. Furthermore, by significantly reducing the amount of capacitance required, the CSI based inverter with silicon IGBTs will be able to substantially decrease the requirements for cooling systems and, further, could enable air-cooled power inverters in the future when silicon carbide based switches become commercially viable.

Two factors, however, have so far prevented the application of CSIs in HEVs. The first is the difficulty of incorporating batteries into a CSI as energy storage devices and controlling the motor at low speeds; the

second is the limited availability of power switches that can block voltages in both forward and reverse directions. However, IGBTs with RB capability are being offered as engineering samples, and the technology is rapidly reaching the maturity needed for commercial production. This project aims to take advantage of the latest technologies to remove the remaining hurdles and bring the CSI to HEV applications by offering new inverter topologies based on the CSI but with novel schemes to incorporate energy storage devices. Two approaches are being examined: one uses a V-I converter and the other uses a passive Z-network of inductors, capacitors, and diodes. The former, although it requires switches, has the advantage of being able to be applied in multiple-motor traction drive systems.

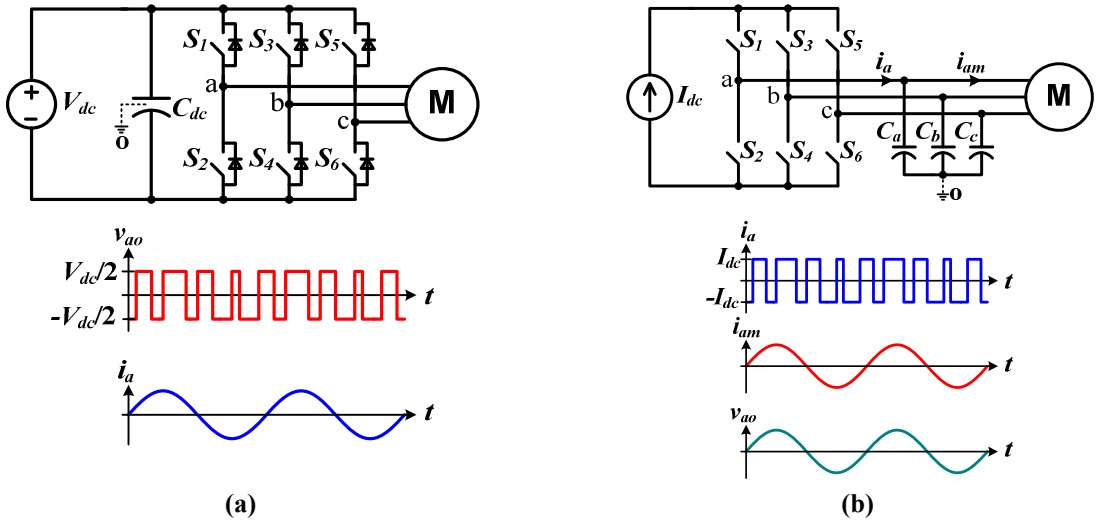


Fig. 1. Schematics of the two types of inverters and typical output voltage and current waveforms: (a) VSI; (b) CSI.

V-I Converter Based CSI

Figure 2 shows a schematic of a V-I converter based CSI for a dual-motor drive system for series or power-split series parallel HEV applications with two CSI bridges connected back-to-back through a V-I converter. The V-I converter includes two switches, S_a and S_b; two diodes, D_1 and D_2; and a dc choke, L_{dc}. The V-I converter transforms the voltage source of the battery into a current source for the inverters, CSIB1 and CSIB2, by providing the capability to control and maintain a constant dc bus current, I_{dc}. The V-I converter also enables the inverters to charge the battery during dynamic braking without the need for reversing the direction of the dc bus current.

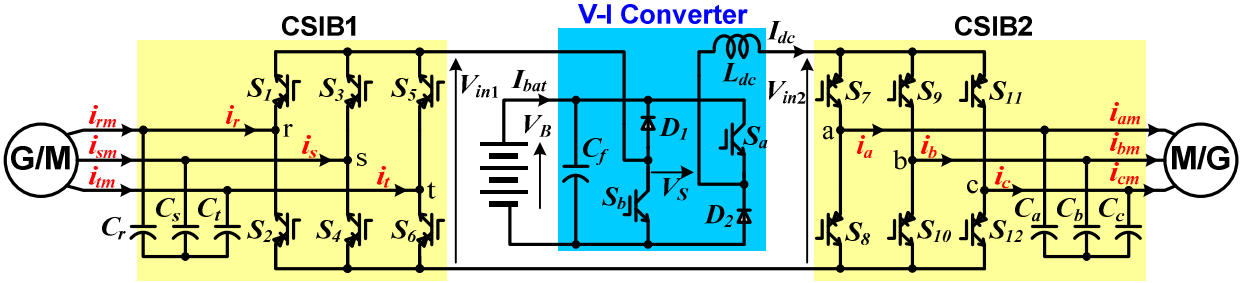


Fig. 2. V-I converter based CSI for a dual-motor drive system for series or power-split series parallel HEV applications.

The CSI based dual-motor drive system provides the following advantages: (1) sharing a single dc link inductor and battery interface circuit (V-I converter); (2) enabling three operation modes: (a) both motors/generators in motoring, (b) both in regen, and (c) one in motoring and one in regen; and (3) producing even higher output voltages for the motor compared to a single CSI drive, as shown in Fig. 3. Table 1 summarizes the performance improvements of the CSI dual-motor-drive PE over the Camry PE.

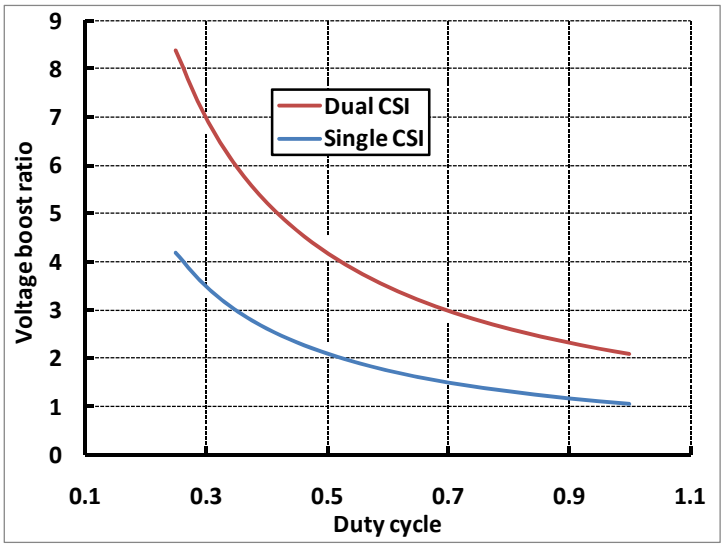


Fig. 3. Voltage boost ratio vs CSI duty cycle.

Table 1. Performance Improvements of the CSI Dual-Motor-Drive PE Over the Camry PE

	Camry PE			CSI dual-motor-drive PE with regular IGBT[a]			CSI dual-motor-drive PE with RB-IGBT[b]		
	Weight (kg)	Volume (L)	Cost ($)	Weight (kg)	Volume (L)	Cost ($)	Weight (kg)	Volume (L)	Cost ($)
Bus Cap	3.57	2.6	$260.00	0.36	0.26	$26.00	0.36	0.26	$26.00
Side housing	1.2	0.98	$1,040.00	1.20	0.98	$1,040.00	1.20	0.98	$728.00
Power module	5	4.3		5.00	4.30		2.75	2.37	
Boost/V-I converter	6.6	3.5	$325.00	6.60	3.50	$325.00	6.60	3.50	$325.00
Subtotal	16.37	11.38	$1,625.00	13.16	9.04	$1,391.00	10.91	7.11	$1,079.00
Reductions in weight, volume, and cost				**20%**	**21%**	**14%**	**33%**	**38%**	**34%**
Performance metrics	4.3 (kW/kg)	6.2 (kW/L)	23.2 ($/kW)	5.3 (kW/kg)	7.7 (kW/L)	19.9 ($/kW)	6.4 (kW/kg)	9.9 (kW/L)	15.4 ($/kW)
Performance improvement				**23%**	**24%**		**49%**	**60%**	
Reduction in cost/kW						**14%**			**34%**

[a]Assumptions: (1) 90% reduction of capacitance and (2) 20% of inverter cost from capacitor.

[b]Assumptions: (1) 90% reduction of capacitance, (2) 20% of inverter cost from capacitor, (3) 30% reduction in diode cost of the inverter switch module, (4) 45% reduction in diode volume and weight of the inverter switch module, and (5) no changes between the boost converter in the Camry PE and V-I converter in the CSI.

Z-Network Based Current Source Inverter

Two new Z-network based current source inverter (ZCSI) topologies have been developed. Figure 4 shows a schematic drawing of the CF-trans-qZSI, and Fig. 5 depicts the CF-trans-ZSI. Both topologies use a Z-network consisting of a diode, D_1; a capacitor, C_1; and a coupled inductor-transformer, L_1 and L_2. Compared to previous ZCSIs, the new topologies eliminate one capacitor and can extend the constant-power speed range by increasing the transformer turns ratio to provide a higher voltage boost ratio. Compared to the traditional CSI, the ZCSIs can buck and boost the output voltage in a single stage, charge the battery during regen operation, and tolerate open circuit conditions in the CSI bridge.

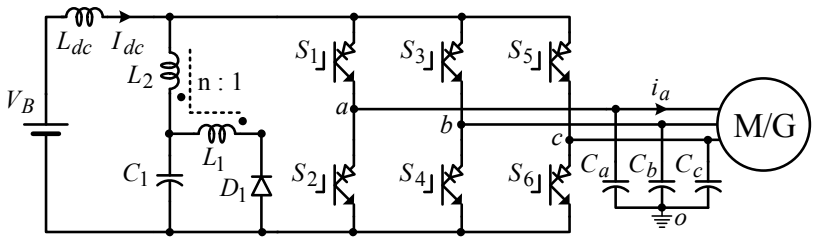


Fig. 4. CF-trans-qZSI.

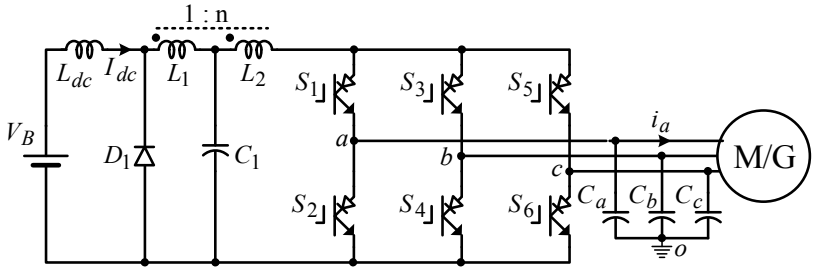


Fig. 5. CF-trans-ZSI.

In addition to the traditional CSI control method, two open circuit–zero state references are added to the current references, as shown by the shaded intervals in Fig. 6. During these intervals, the shoot-through zero states, in which both switches, S_1 and S_2, are conducting, are changed to open circuit zero state by turning off both switches.

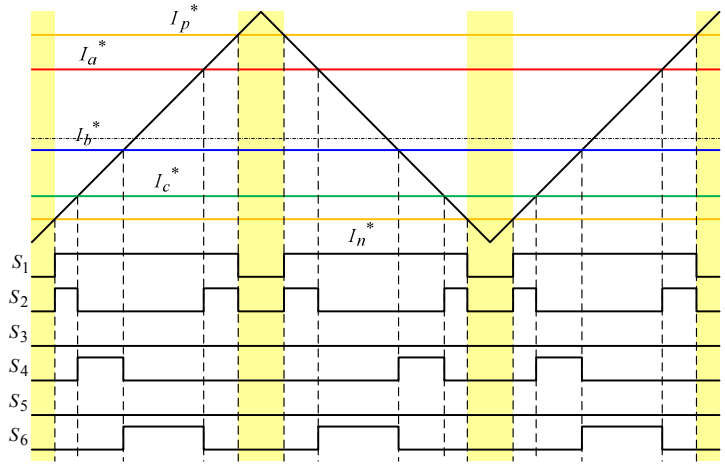


Fig. 6. Pulse width modulated control method with open circuit–zero state references inserted.

Depending on how the open circuit–zero state reference is generated, there are three ways to insert it: (1) simple boost control, in which two straight lines are added as the open circuit–zero state reference; (2) maximum boost control, which uses the envelop of the three-phase current references; and (3) constant boost control, in which the reference is produced by injecting a third harmonic into the current commands, as shown in Fig. 7. The maximum boost control transfers the entire shoot-through zero state interval to open circuit zero state, while the simple boost and constant boost control have the same open-state duty cycle over every switching cycle.

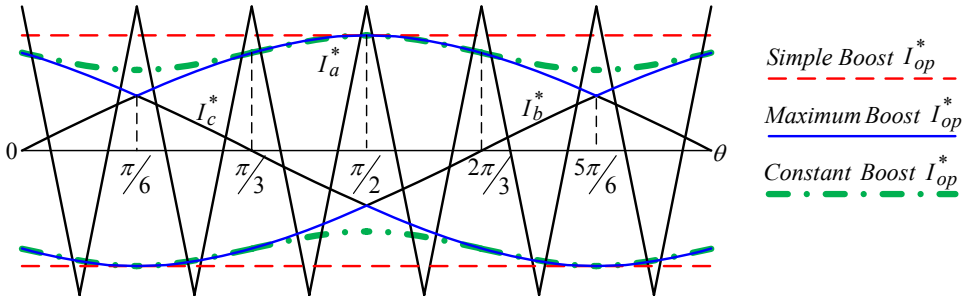


Fig. 7. Pulse width modulated control methods using three different open circuit–zero state references.

Figure 8 shows the equivalent circuits of the CF-trans-ZSI. There are three dc operation states: active, shoot-through zero state, and open circuit zero state. Figure 8(a) shows the active state, in which the inverter operates in one of the six active states and the diode, D_1, (ref Fig 5) is not conducting. Figure 8(b) shows the shoot-through zero state, in which one of the inverter legs is short-circuited and the diode, D_1, is not conducting. Figure8(c) shows the open circuit zero state, in which all the switches of the inverter are off and the motor is disconnected from the battery. The diode, D_1, is conducting during this state. Figure 9 shows the three similar dc equivalent circuits for the CF-trans-qZSI.

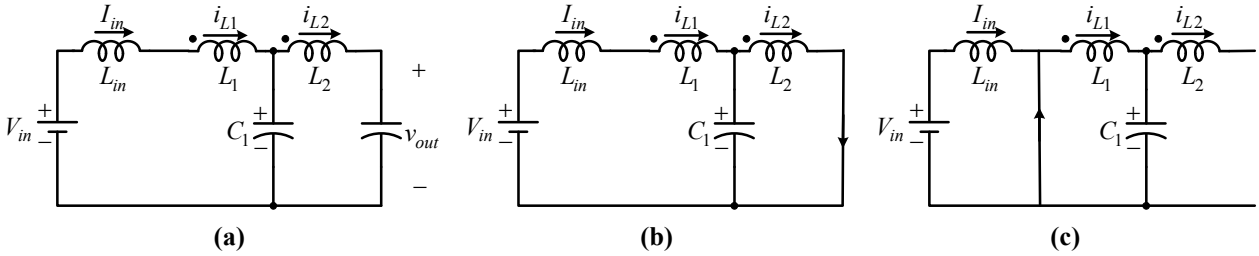


Fig. 8. CF-trans-ZSI equivalent circuit: (a) active state, (b) shoot-through zero state, and (c) open circuit zero state.

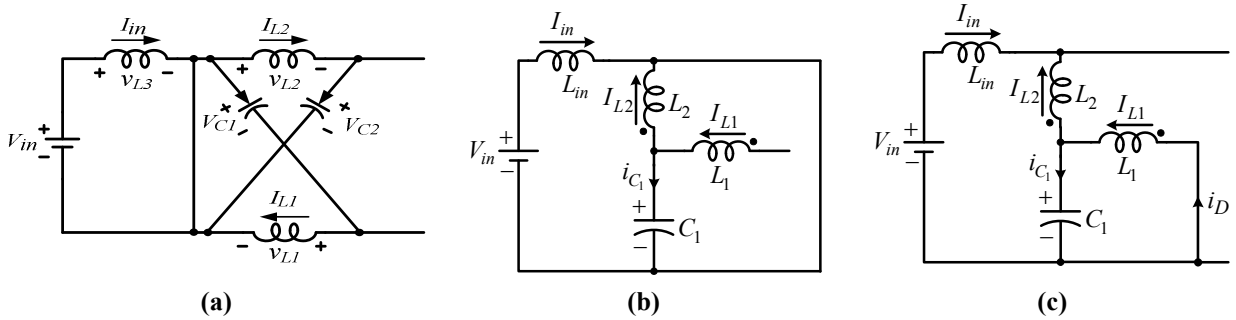


Fig. 9. CF-trans-qZSI equivalent circuit: (a) active state, (b) shoot-through zero state, and (c) open circuit zero state.

The dc voltage gain of the CF-trans-ZSI and CF-trans-qZSI can be derived from the equivalent circuits as

$$\frac{V_{out}}{V_{in}} = \frac{1 - D_{op}(1 + \frac{n_2}{n_1})}{D_A} .$$

For a turns ratio of 2 (i.e., $n_2/n_1 = 2$), the above equation becomes

$$\frac{V_{out}}{V_{in}} = \begin{cases} \frac{1}{D_A} & \text{if } D_{op} = 0 \\ \frac{3D_A - 2}{D_A} & \text{if } D_{sh} = 0 \end{cases} ,$$

where n_2/n_1 is the turns ratio of the coupled inductor and D_A, D_{op}, and D_{sh} represent the duty cycles for the active, open circuit, and short circuit zero states, respectively.

Figure 10 shows the dc output voltage gain of the CF-trans-ZSI and CF-trans qZSI. There are three operation regions, A, B, and C. In region B the inverter operates in the motoring mode and can produce an equivalent dc output voltage in the range of 0 to about 3 Vin. Region C is the regen region as indicated by the negative output voltage gain. In this region, the inverter can operate as a pulse width modulated rectifier to charge the battery. Region A is a prohibited region because the diode of the Z-network will conduct automatically, interrupting the proper operation of the inverter. The output voltage will get distorted due to the unwanted conduction of the diode. If it is desired to extend the motoring operation region, the diode will have to be replaced with an RB switch. Alternatively, increasing the transformer turns ratio can also extend the motoring operation region. In addition, the line marked "Mode 1" represents the motoring operation region boundary on which no open circuit zero states are introduced and the highest voltage gain is achieved. The line marked "Mode 2" is the regen region boundary line where all the shoot through zero states are replaced by open circuit zero states. During this mode, the inverter produces the lowest possible voltage.

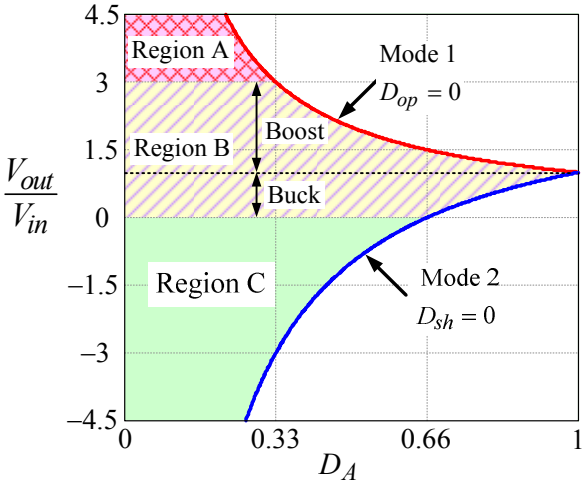


Fig. 10. CF-trans-ZSI and CF-trans-qZSI dc output voltage gain.

Table 2 summarizes the open circuit duty cycle, D_{op}, voltage and current gains corresponding to the modulation index, M, for the three control strategies. In the table, n is the turns ratio of the coupled inductor and $\cos\delta$ is the power factor (PF) of the motor.

Table 2. Comparison of the Three Different Control Strategies

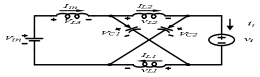
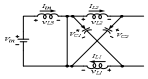
Control method	D_{op}	Voltage gain	Current gain
Simple boost	$1-M$		
Maximum boost	$1-\frac{3\sqrt{3}M}{2\pi}$	$\frac{4}{3M\cos\delta}\left(\frac{3\sqrt{3}M}{2\pi}(1+n)-n\right)$	$\frac{2\pi M}{3\sqrt{3}M(n+1)-2\pi n}$
Constant boost	$1-\frac{\sqrt{3}M}{2}$	$\frac{4}{3M\cos\delta}\left(\frac{\sqrt{3}M}{2}(1+n)-n\right)$	$\frac{2M}{\sqrt{3}M(n+1)-2n}$

Figure 11 plots the output line-to-line peak voltage gain of the CF-trans-ZSI and CF-trans-qZSI versus the modulation index at n = 2 and PF = 1 for the three control methods. The simple boost method produces the narrowest operation area while the maximum boost method leads to a slightly wider regen area than that of the constant boost scheme.

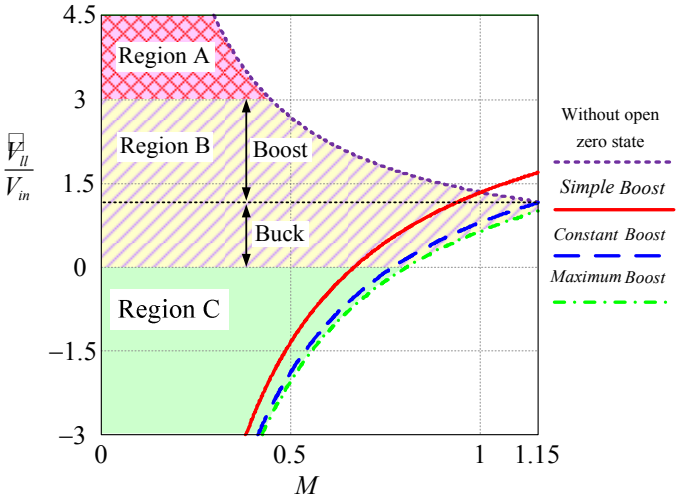


Fig. 11. Output voltage gain at *n* = 2 vs modulation index for the three control methods.

55 kW CF-trans-qZSI Design

A design for a 55 kW CF-trans-qZSI (Fig. 4) was produced for the following conditions.

- Peak power rating: 55 kW
- Battery voltage, V_{in}: 260 V
- Output line-to-line voltage: 0~500 V
- Switching frequency: 10 kHz
- Coupled inductor turns ratio: 2

Based on the calculated voltage stress of 780 V and current stresses of 243 A peak and 70 A average for the switches, an RB-IGBT rated at 1,200 V and 200 A should be chosen. However, because RB-IGBTs with those ratings are not available at the present, the conduction and switching loss data of the 1,200 V–100 A RB-IGBT from Fuji will be used to estimate the losses and efficiency of the inverter design. At $V_{ce(sat)}$ = 2.8 V and an average switch current of 70 A, conduction losses of the six switches are estimated to be 1,176 W (6 × 2.8 × 70). Assuming the RB-IGBT switching loss of 200 A would be twice that of the 100 A devices, the total switching loss of the six devices under 10 kHz switching would be 1,800 W (6 × 30 mJ × 10 kHz). The estimated volume and weight of the RB-IGBT module are 0.308 L and 0.85 kg, respectively, based on the current 100 A RB-IGBT modules.

Based on the calculated diode voltage stress of 390 V and current stresses of 626 A peak and 211 A average, a diode rated at 600 V and 600 A could be sufficient for the design. The readily available diode from Powerex (QRS0680T30, rated at 600 V and 800 A) was, however, chosen for the design. The weight and volume of the diode are 0.22 kg and 95.88 mL, respectively. The diode conduction and reverse recovery losses are estimated at 358.7 W and 13.0 W, respectively.

Requirements for the Z-network capacitor are 300 V, 450 Arms, and 300 μF. To meet the ripple current requirement, four Electronic Concepts film capacitors, UL34Q157K, in parallel were chosen for the design, resulting in a total capacitance of 600 μF, a total volume of 0.87 L, and a total weight of 1.2 kg. The loss due to the electric series resistance is 24.3 W.

Requirements for the Z-network inductors, L_1 and L_2, are 15 μH/367 Arms and 60 μH/300 Arms, respectively. With the selected amorphous core, AMCC500, and 6 turns for L_1 and 12 turns for L_2, the resulting coupled inductor has L_1 = 12.6 μH, L_2 = 50.4 μH, core weight of 2.89 kg, core loss of 393 W, copper loss of 202 W, copper weight of 1.9 kg, and a total inductor volume of 0.75 L.

Requirements for the input inductor, L_{dc}, are 212 A and 69 μH. With the selected amorphous core, AMCC320, and 11 turns, the resulting inductor has L_{dc} = 60.5 μH, core weight of 2.17 kg, core loss of 295 W, copper loss of 70 W, copper weight of 0.649 kg, and a total inductor volume of 0.72 L.

The voltage stress of the output ac filter capacitors is around 500 Vrms, and the required capacitance is 30 μF per phase. By connecting the output capacitors in delta, the required per-phase capacitance value will be reduced to one-third (i.e., 10 μF). The Electronic Concepts film capacitor, 5MPA2106J, rated at 530 VAC and 10 μF, was selected, resulting in a total volume of 0.265 L and weight of 0.408 kg.

A water-cooled heat sink about twice the size of the switch module was chosen for the design. The volume and weight of the heat sink are 0.308 L and 0.974 kg, respectively.

Table 3 provides a summary of component volumes and weights and the resulting power density. Figure 12 shows inverter volume breakdown by component; the Z-network capacitor and inductors are the major volume-contributing parts, constituting 71% of the total inverter volume. Figure 13 illustrates weight breakdown by component; the Z-network inductor contributes the most to the inverter weight (42%). Figures 14 and 15 show loss breakdown in boost mode and buck mode. The estimated efficiency is 93.8% in boost mode and 94% in buck mode.

Table 3. Summary of Component Volume, Weight, and Power Density for the 55 kW Inverter Design

	Switches	Diode	Z-network capacitor	Z-network inductor	Input inductor	Output capacitor	Heat sink	Total	Power density
Weight (kg)	0.85	0.22	1.2	4.79	2.816	0.408	0.9735	**11.2575**	**4.89 kW/kg**
Volume (L)	0.308	0.09588	0.87	0.75	0.72	0.265	0.308	**3.317**	**16.6 kW/L**

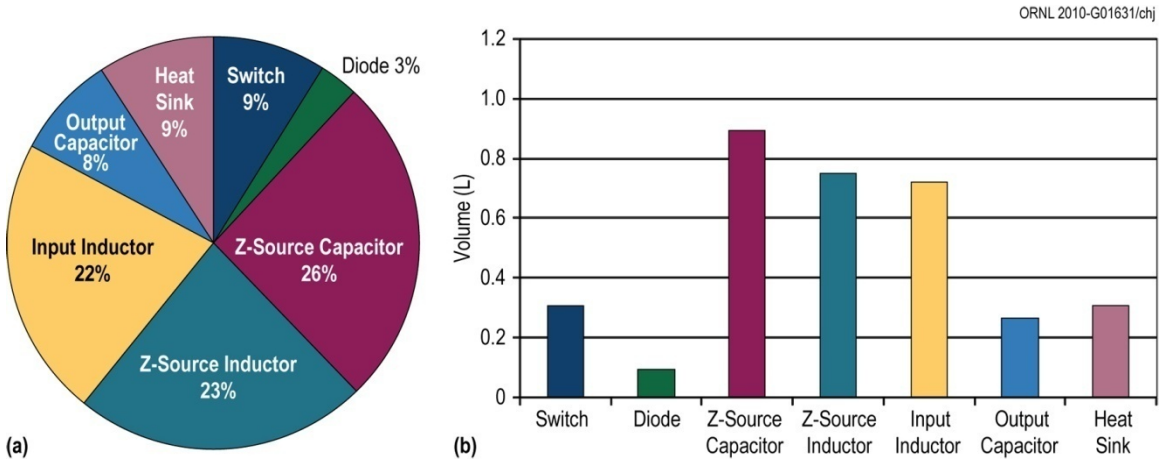


Fig. 12. Volume breakdown by component for the 55 kW CF-trans-qZSI design: (a) component percentage of total; (b) component volume in liters.

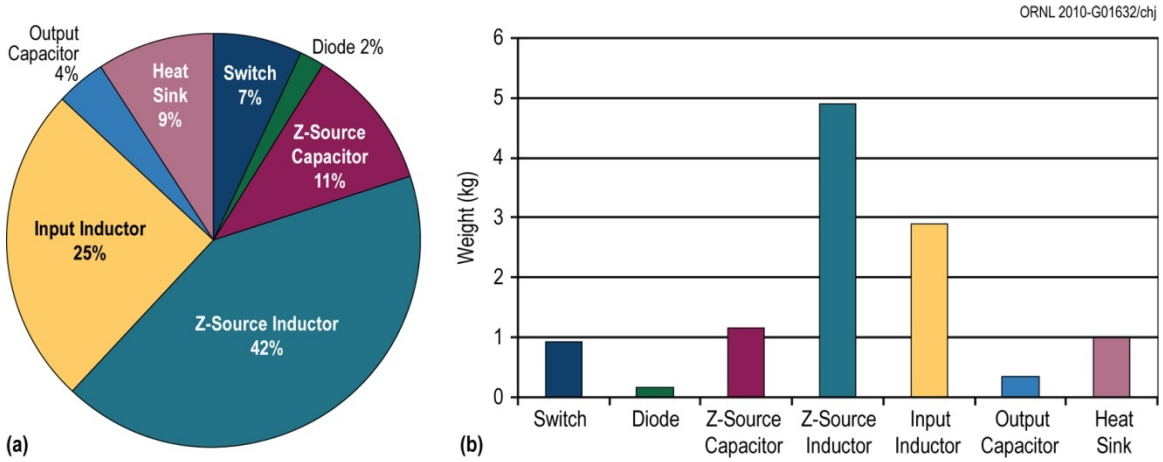


Fig. 13. Weight breakdown by component for the 55 kW CF-trans-qZSI design: (a) component percentage of total; (b) component weight in kilograms.

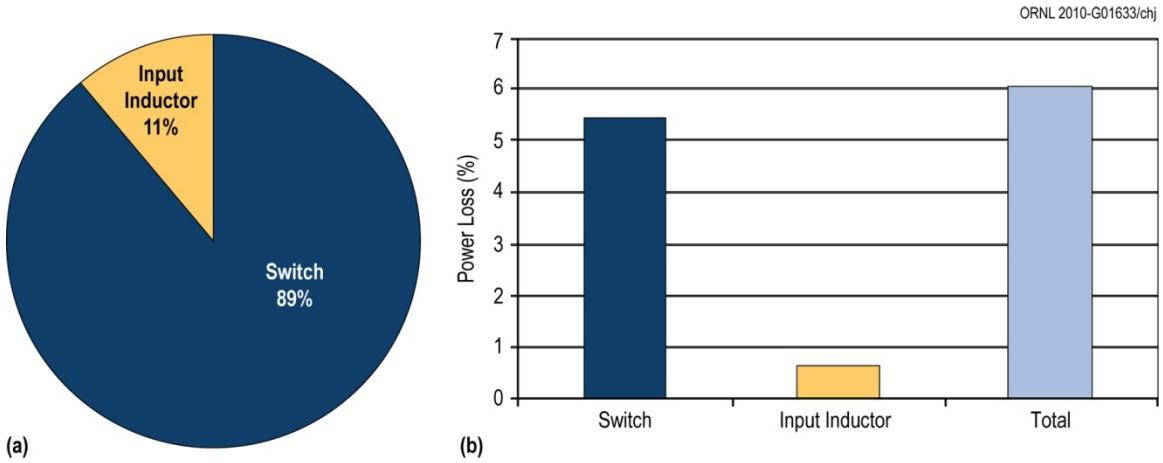


Fig. 14. Boost mode loss breakdown by component for the 55 kW CF-trans-qZSI design: (a) component loss as a percent of the whole; (b) individual component power loss.

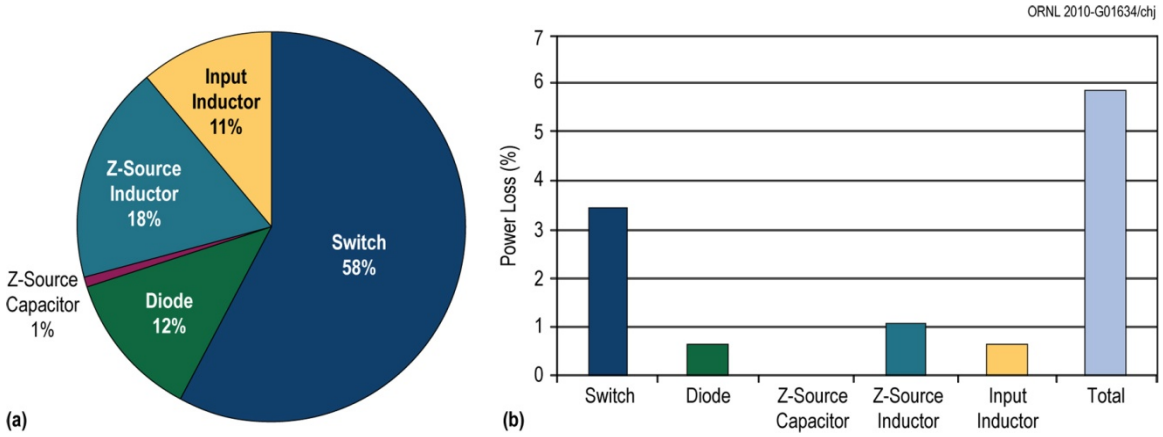


Fig. 15. Buck mode loss breakdown by component for the 55 kW CF-trans-qZSI design: (a) component loss as a percent of the whole; (b) individual component power loss.

The switching device loss is the major contributor to the total loss. To achieve higher power density and reduce the size of the inductor, the switching frequency should be increased. But the device switching loss will also increase, negatively impacting the converter efficiency. Currently available first generation RB-IGBT technology was used in this design. With anticipated 100% reductions in switching and conduction losses with next generation RB-IGBTs, the boost mode and buck mode efficiency numbers can be increased to 96% and 96.7%, respectively, as shown in Fig. 16. Further, future wide bandgap based devices, which can switch at high frequencies while still maintaining low switching losses, can be used to shrink the size of the inductors and improve the power density and efficiency.

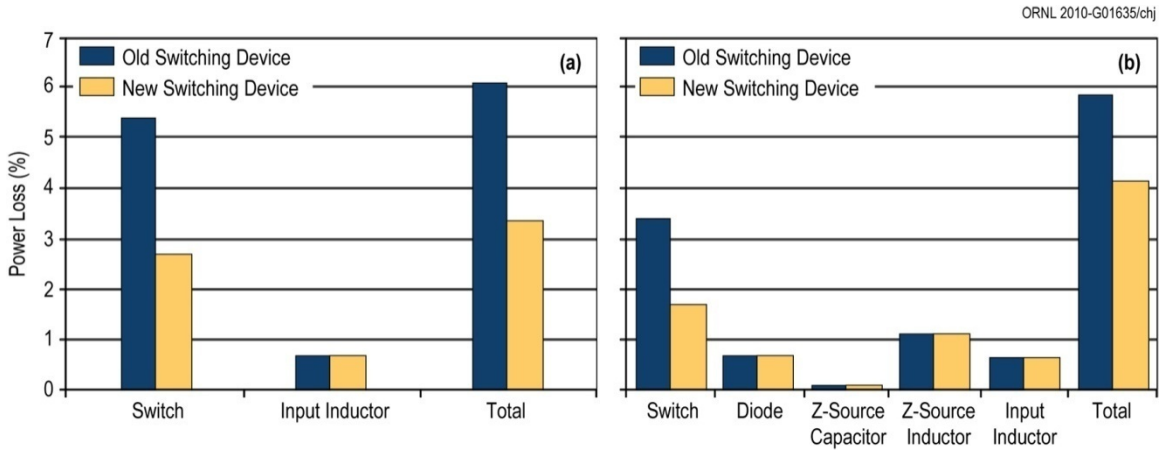


Fig. 16. Power loss comparisons showing anticipated loss reductions with next generation RB-IGBTs for (a) boost mode and (b) buck mode.

Figures 17–19 show simulated waveforms of three-phase motor voltages, Vab, Vbc, and Vca; motor currents, ia, ib, and ic; battery current, Iin; and battery voltage, Vin, for the 55 kW ZCSI design operating in boost, buck, and regen modes.

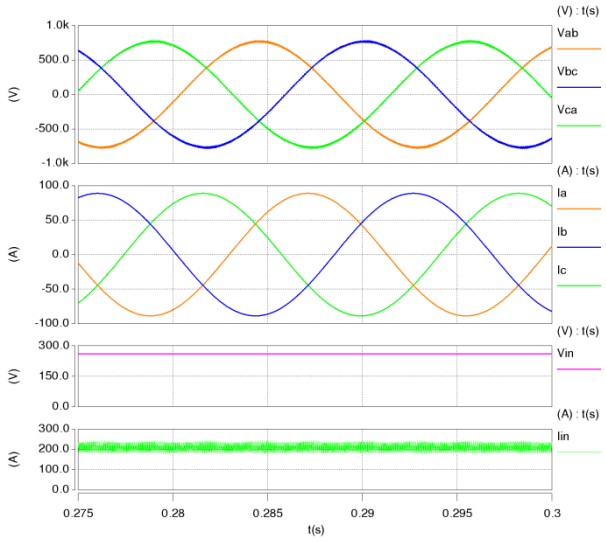


Fig. 17. Simulated waveforms in boost mode.

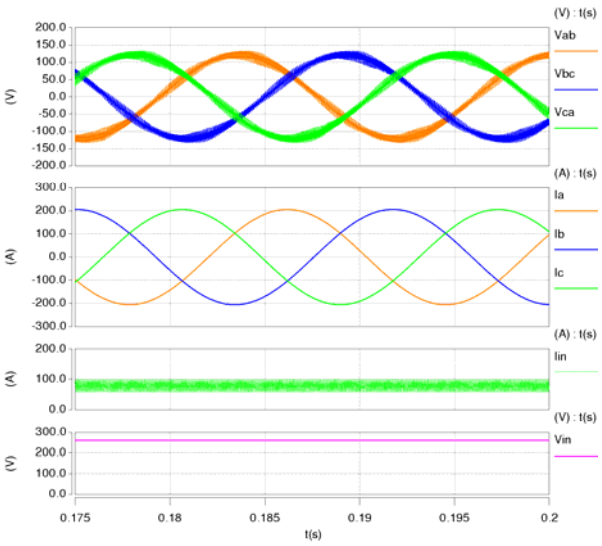


Fig. 18. Simulated waveforms in buck mode.

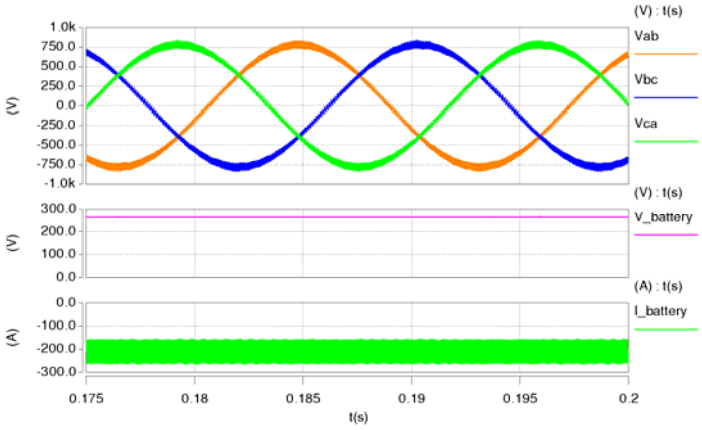


Fig. 19. Simulated waveforms in regen mode.

Conclusion

Two new ZCSIs with a reduced component count, CF-trans-ZSI and CF-trans-qZSI, were developed. Simulation study indicates the new ZCSIs have a voltage boost ratio of 3 in contrast to 2 for the previous ZCSIs.

A design for a 55 kW ZCSI based on the CF-trans-qZSI was completed using first generation RB-IGBT technology. The design yields a specific power of 4.89 kW/kg, a power density of 16.6 kW/L, and efficiency of 93.8% in boost mode and 94% in buck mode. With next generation RB-IGBT technology, it is estimated the efficiency numbers can be increased to 96% and 96.7%, respectively.

Simulation results confirmed the feasibility of using the ORNL V-I converter based CSI topology in series and power-split series parallel HEV configurations. The CSI dual-motor-drive PE using RB-IGBTs provides significant performance improvements over the Camry PE: 49% increase in specific power (6.4 vs 4.3 kW/kg), 60% increase in power density (9.9 vs 6.2 kW/kg), and 34% reduction in cost ($15.4/kW vs $23.2/kW).

Publications

1. L. Tang and G. J. Su, "Boost Mode Test of a Current-Source-Inverter-Fed Permanent Magnet Synchronous Motor Drive for Automotive Applications," in Proceedings of *the 12th IEEE Workshop on Control and Modeling for Power Electronics* (COMPEL 2010), June 28–30, 2010, Boulder, Colorado.
2. G. J. Su, L. Tang, and Z. Wu, "Extended Constant-Torque and Constant-Power Speed Range Control of Permanent Magnet Machine Using a Current Source Inverter," in *Proceedings of the 5th IEEE Vehicle Power and Propulsion Conference* (VPPC '09), pp. 109–115, Sept. 7–11, 2009, Dearborn, Michigan.
3. Z. Wu and G. J. Su, "High-Performance Permanent Magnet Machine Drive for Electric Vehicle Applications Using a Current Source Inverter," in *Proceedings of the 34th Annual Conference of the IEEE Industrial Electronics Society* (IECON '08), pp. 2812–2817, November 10–13, 2008, Orlando, Florida.

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1. M. Takei, Y. Harada, and K. Ueno, "600V-IGBT with reverse blocking capability," pp.413–416 in *Proceedings of IEEE ISPSD '2001*, 2001.
2. E. R. Motto, et al., "Application Characteristics of an Experimental RB-IGBT (reverse blocking IGBT) Module," in *Proceedings of IEEE IAS 2004 Annual Meeting*, pp. 1504–1544 (2004).

Patents

1. Gui-Jia Su, "Power Conversion Apparatus and Method," application US12/399,486, March 6, 2009, patent pending.

2.5 A Segmented Drive Inverter Topology with a Small dc Bus Capacitor

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Objectives

- Overall project objectives
  - Significantly reduce the amount of inverter direct current (dc) bus capacitance through reducing the ripple current by 60%.
- Objectives for FY 2010 effort
  - Demonstrate a 55 kW segmented inverter prototype that is capable of operating with an amount of bus capacitance reduced by 60% compared to a standard voltage source inverter (VSI).

Approach

- Use a segmented drive system topology that does not need additional switches or passive components but can significantly reduce the dc link ripple current and the capacitance.
- Perform simulation study of various pulse width modulation (PWM) schemes using PSIM circuit simulation software to assess their impact on the capacitor ripple current.
- Design, build, and test a 55 kW inverter prototype to experimentally validate the simulation study.

Major Accomplishments

- Demonstrated a 55 kW segmented inverter prototype with a 60% reduction of dc bus capacitance compared to a standard VSI.
  - Prototype test results show
  - (a) a significant reduction of 55% to about 75% in capacitor ripple current and
  - (b) a significant reduction of 70% to about 90% in battery ripple current.
  - Estimated performance improvements when the technology is applied to the Toyota Camry motor inverter include
    (a) 40% increase in specific power to 12.9 kW/kg,
    (b) 35% increase in power density to 15.9 kW/L,
    (c) 11% decrease in $/kW to $11.6/kW, and
    (d) exceeding the DOE 2015 target for specific power and the 2020 target for power density.

Future Direction

- Design, build, test, and characterize a 55 kW prototype of an integrated segmented inverter-motor drive to reduce drive system cost.

Technical Discussion

Background

The dc bus capacitor is an essential component for maintaining a stable dc bus voltage for the VSI based traction drive systems in electric vehicles, hybrid electric vehicles (HEVs), and plug-in HEVs. Figure 1 is a schematic of the standard VSI based drive system. The VSI, mainly comprising six power semiconductor switches—typically insulated gate bipolar transistors (IGBTs)—and a dc bus filter capacitor, switches the battery voltage according to a chosen PWM scheme to control the motor torque and speed through regulating the motor current and voltage. In doing the switching operations, it generates large ripple currents in the dc link, necessitating the use of the dc bus filter capacitor to absorb the ripple currents and suppress voltage transients, which occur on the dc bus at every instant of inverter switching and are detrimental to the battery life and reliability of the semiconductor switches in the inverter.

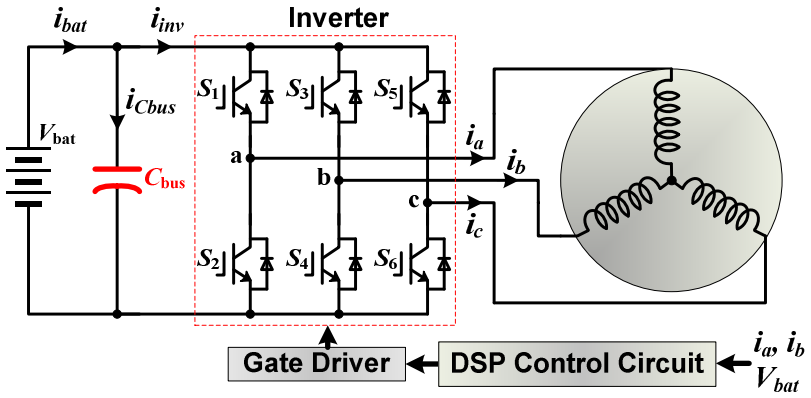


Fig. 1. Standard VSI based drive system in HEVs.

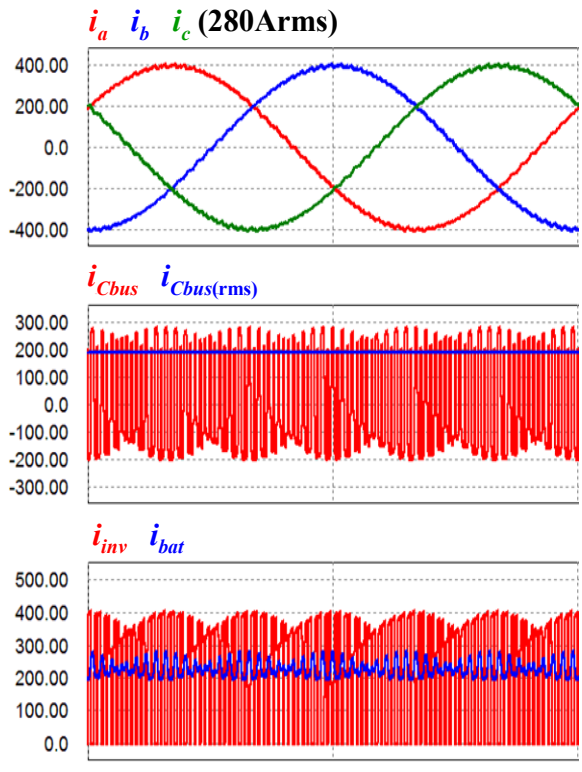


Figure 2. Simulated waveforms in the standard VSI based drive system.

Figure 2 shows simulated motor currents, i_a, i_b, and i_c; capacitor ripple current, i_{Cbus} and $i_{Cbus(rms)}$; inverter dc link current, i_{inv}; and battery current, i_{bat}, in a typical 55 kW HEV inverter. The capacitor ripple current reaches as large as 200 Arms, and thus, a bulky and costly dc bus capacitor of about 1,000 µF is required to prevent this large ripple current from flowing into the battery.

Concerns about the reliability of electrolytic capacitors have forced HEV makers to use film capacitors, and currently available film capacitors that can meet the demanding requirements are costly and bulky, taking up one-third of the inverter volume and making up one-fifth of the cost. The dc bus capacitor, therefore, presents significant barriers to meeting the requirements of the FreedomCAR goals for inverter volume, lifetime, and cost established by DOE and its industrial partners [1].

The large ripple currents become even more problematic for the film capacitors in high temperature environments because their ripple current handling capability decreases rapidly with rising temperatures, as indicated in Fig. 3, which maps this capability for a typical film capacitor. For example, as the ambient temperature rises from 85 to

105°C, the weight, volume, and cost of capacitors could increase by a factor of 5 due to the decrease of their ripple current capability from 50 to 11 A.

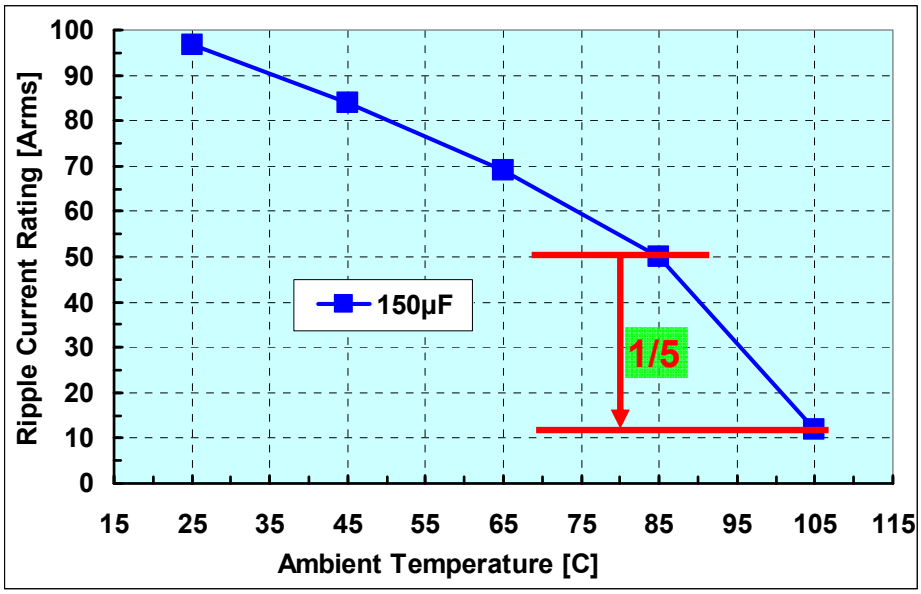


Fig. 3. Film capacitor ripple current capability vs ambient temperature (Electronic Concepts UL31 Series) [2].

To help achieve the FreedomCAR targets, there is thus an urgent need to minimize this bulky component by significantly reducing the ripple current. A much smaller dc bus capacitor would also enable inverters to operate at higher temperatures. The following factors, however, make this a difficult task: (1) increasing the switching frequency, which is one of the anticipated benefits with future wide bandgap based switches, has little impact on the bus capacitor ripple currents because the capacitor ripple currents depend on the motor peak current and (2) the major components of the capacitor ripple currents have frequencies of multiples of the switching frequency (nf_{sw}) or their side bands ($nf_{sw} \pm f_m$, $nf_{sw} \pm 2f_m$, …), as given by the equation below and illustrated in Fig. 4. The high frequency nature makes it impractical to actively filter out the ripple components because doing so requires the use of very high switching frequencies in the active filter.

$$i_{inv} = I_{dc} + \sum_{k=0}^{\infty}\sum_{n=1}^{\infty} I_{n,k} \sin[2\pi(nf_{sw} \pm kf_m)t + \alpha_{n,k}] \quad ,$$

where

f_{sw} = switching frequency
f_m = motor fundamental frequency.

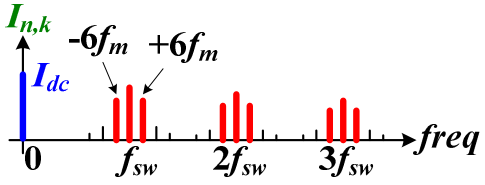


Fig. 4. Ripple components in the dc link current in the standard VSI based drive system.

Features of the Proposed Segmented Drive

A segmented drive system topology is being examined in this project to reduce the dc bus capacitor ripple current. Because the technology is under patent review, details of the topology will not be shown in this report. However, the segmented topology does not need additional switches or passive components but enables the use of optimized PWM schemes to significantly reduce the dc link ripple current generated by switching the inverter output currents.

The uniqueness of this technology is that, while being able to significantly reduce the capacitor ripple current, it *does not*

- need additional silicon or passive (L or C) components,
- need additional sensors, or
- add control complexity.

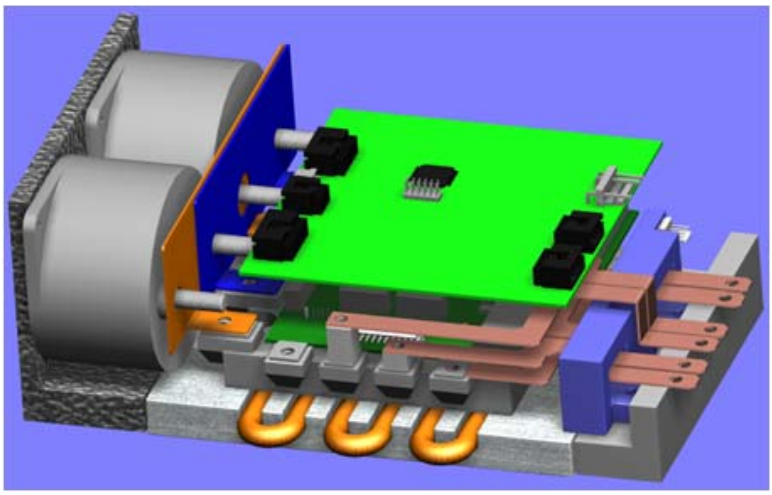
The following positive impacts are expected:

- substantially reduced bus capacitance (at least 60%) and thus reduced inverter volume and cost,
- reduced battery losses and improved battery operating conditions through elimination of battery ripple current, and
- significantly reduced motor torque ripples (up to 50%) or reduced switching losses (by 50%).

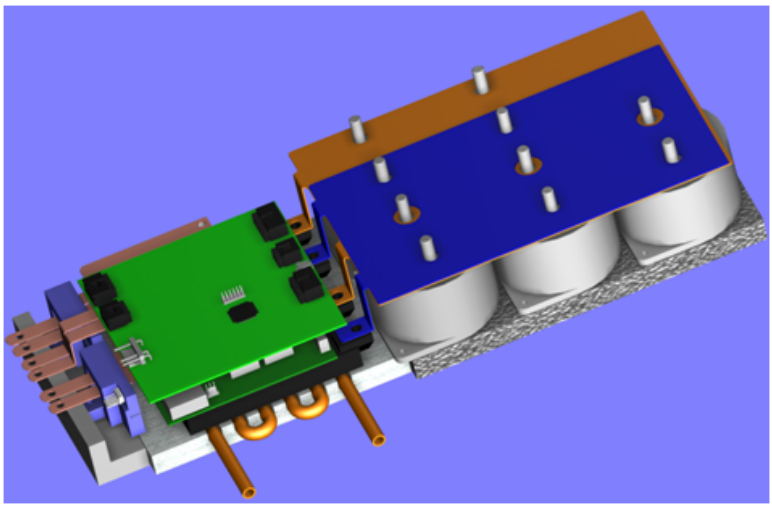
A simulation study using PSIM carried out in FY 2009 has validated the segmented drive concept and indicated that the bus capacitance can be reduced by 60% from that needed for a standard VSI. The simulation results also show that, compared to the standard inverter configuration, the segmented drive inverter can achieve (1) more than 65% reduction in capacitor ripple current, (2) 80% reduction in battery ripple current, (3) 70% reduction in dc bus ripple voltage, and (4) 50% reduction in motor ripple current.

Prototype Design and Test Results

Incorporating the simulation study, a 55 kW prototype was designed, built, and tested during FY 2010. Figure 5(a) is a three-dimensional drawing of the hardware design for the 55 kW prototype. A design for a 55 kW baseline standard VSI is also shown for comparison [Fig. 5(b)]. Both designs use the same IGBT modules, purchased from Powerex, and the same water-cooled cold plate, measuring 6 in. by 7 in., for cooling the IGBT modules. Capacitor requirements for the segmented inverter are 400 μF and are fulfilled with two film capacitors, each rated at 500 V/200 μF. In comparison, a total of 1,000 μF capacitance is needed for the baseline VSI design and is furnished by five film capacitors, each rated at 500 V/200 μF. The capacitors are mounted on an aluminum heat sink attached to the cold plate. Because of the capacitance requirement (more than twice that of the segmented inverter), the baseline design requires a significantly larger heat sink for mounting the capacitors. Table 1 gives a comparison of heat sink size and capacitor volume for the two designs. Figure 6 is a photo of the assembled 55 kW segmented inverter prototype. A Texas Instruments 32 bit fixed-point digital signal processor chip, TMS320F2812, is used to implement the motor control and PWM switching schemes.



(a)



(b)

Figure 5. Hardware designs for 55 kW prototypes: (a) segmented inverter and (b) baseline standard VSI.

Table 1. Comparison of Heat Sink Size and Capacitor Volume

	Baseline	Segmented
Heat sink footprint	**6" × 7"+ 6.6" × 9.6"**	**6" × 7"+ 6.6" × 2.2"**
Cap. volume	**1.39 L**	**0.56 L** → **a 60% reduction**

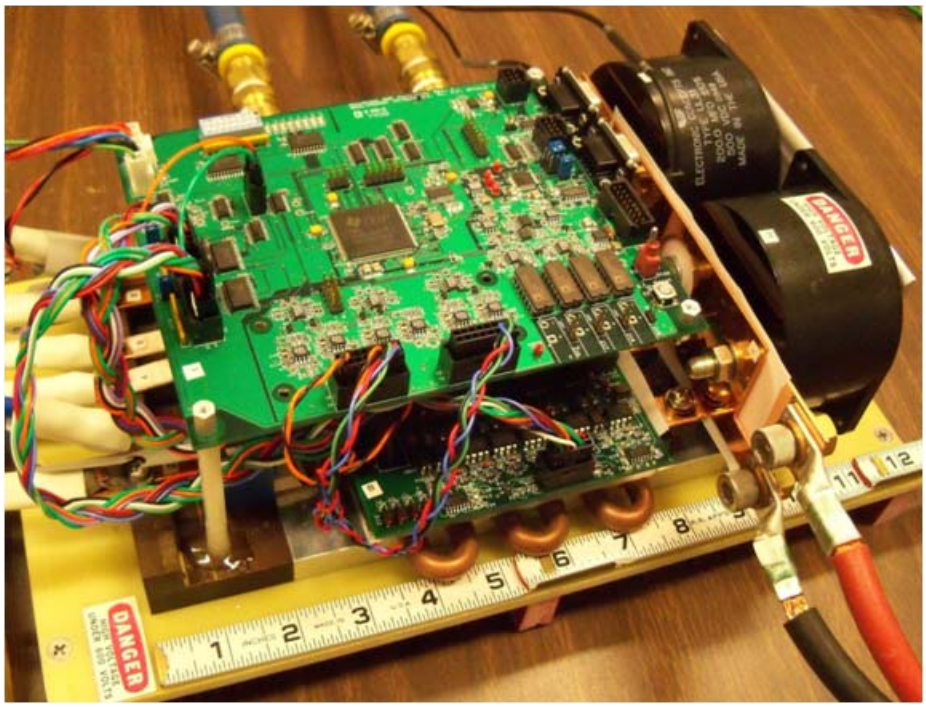
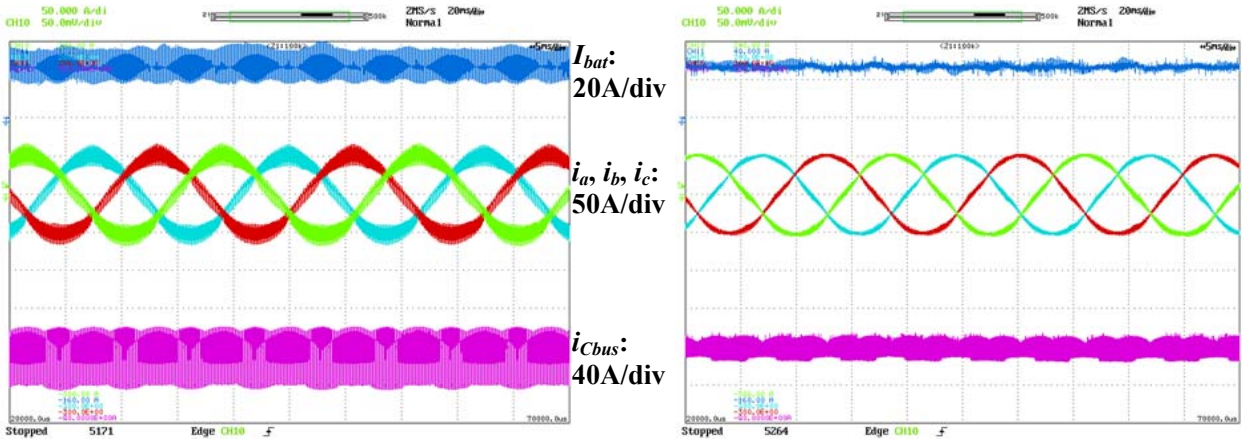


Fig. 6. A 55 kW segmented inverter prototype.

The prototype was tested first with an inductor-resistor (R-L) load bank with nominal circuit parameters of 0.45 mH and 1.6 Ω. A dc power supply was used to simulate a 300 V battery. For comparison, the prototype was reconfigured as the baseline VSI, but without the added capacitors, and tested at the same load conditions. Figure 7 shows battery current, I_{bat}; load currents, i_a, i_b, and i_c; and capacitor ripple current, i_{Cbus}, for a dc input power of 7 kW where (a) is for the baseline inverter and (b) for the segmented inverter. The measured capacitor ripple currents are 33.6 Arms for the baseline inverter and 9.2 Arms for the segmented inverter, and the measured peak-to-peak battery ripple currents are, respectively, 24 A and 8 A. These measurements give a reduction of 73% for capacitor ripple current and 67% for battery ripple current with the segmented inverter. Figures 8 and 9 show waveforms for the same currents at dc input power of 10.5 kW and 19 kW. Comparing the measured results reveals that the segmented inverter provides a reduction of 75% in capacitor ripple current and 73% in battery ripple current at the dc power of 10.5 kW. The reduction ratios are 62% and 78% for the case with dc input power of 19 kW. Moreover, while the three-phase load current waveforms in the baseline inverter have substantial harmonic components due to the relatively low load inductance, these harmonic components disappeared almost entirely from the current waveforms in the segmented inverter. This is another benefit with the segmented inverter and is important to permanent magnet (PM) motors, which have low inductance. It means a lower switching frequency can be used to increase the inverter efficiency.

Figure 10 plots the capacitor ripple currents at various levels of input dc power for both the baseline and segmented inverters. The segmented inverter offers a significant reduction of capacitor ripple current (in the range of 55%~75%).

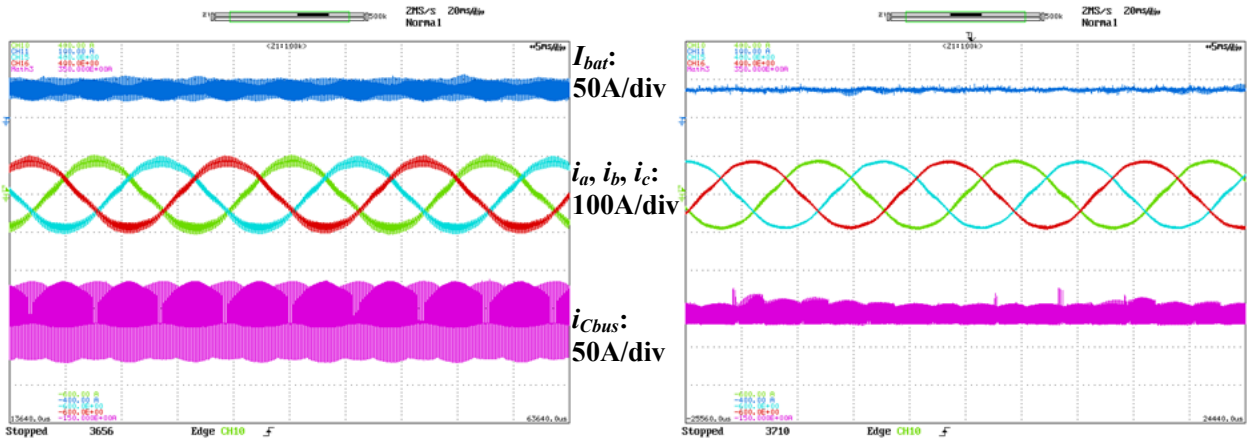
Figure 11 plots the battery ripple currents at various levels of input dc power for both the baseline and segmented inverters. Again, the segmented inverter offers a significant reduction of battery ripple current (in the range of 70%~80%).



Baseline inverter
$i_{Cbus(rms)}$: 33.6 Arms, $I_{bat,\ p\text{-}p\ ripple}$: 24 A

Segmented inverter
$i_{Cbus(rms)}$: 9.2 Arms, $I_{bat,\ p\text{-}p\ ripple}$: 8A

Fig. 7. Waveforms with an R-L load at dc input power of 7 kW, showing a reduction of 73% for capacitor ripple current and 67% for battery ripple current with the segmented inverter.



Baseline inverter
$i_{Cbus(rms)}$: 54.6 Arms, $I_{bat,\ p\text{-}p\ ripple}$: 37 A

Segmented inverter
$i_{Cbus(rms)}$: 13.4 Arms, $I_{bat,\ p\text{-}p\ ripple}$: 10A

Fig. 8. Waveforms with an R-L load at dc input power of 10.5 kW, showing a reduction of 75% for capacitor ripple current, 73% for battery ripple current with the segmented inverter.

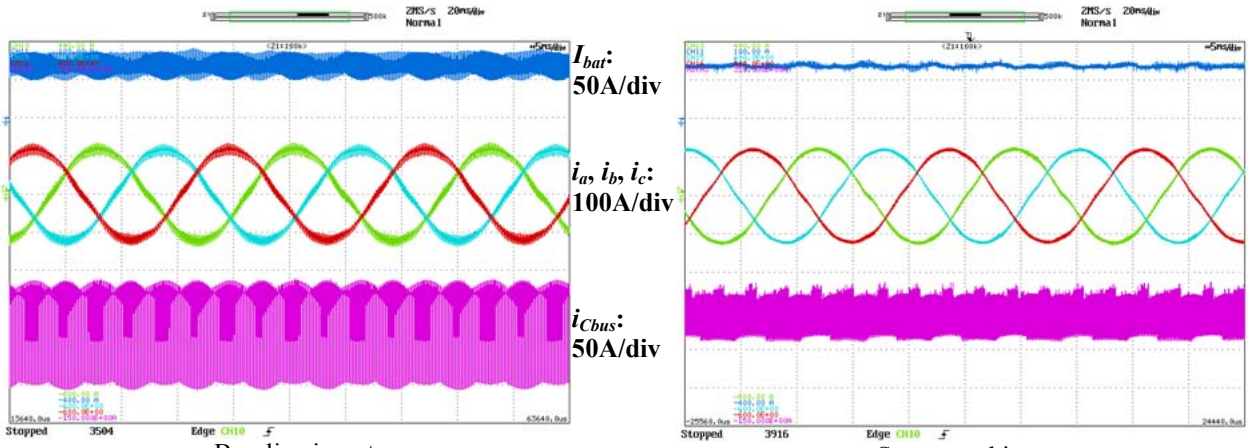


Fig. 9. Waveforms with an R-L load at dc input power of 19 kW, showing a reduction of 62% for capacitor ripple current, 78% for battery ripple current with the segmented inverter.

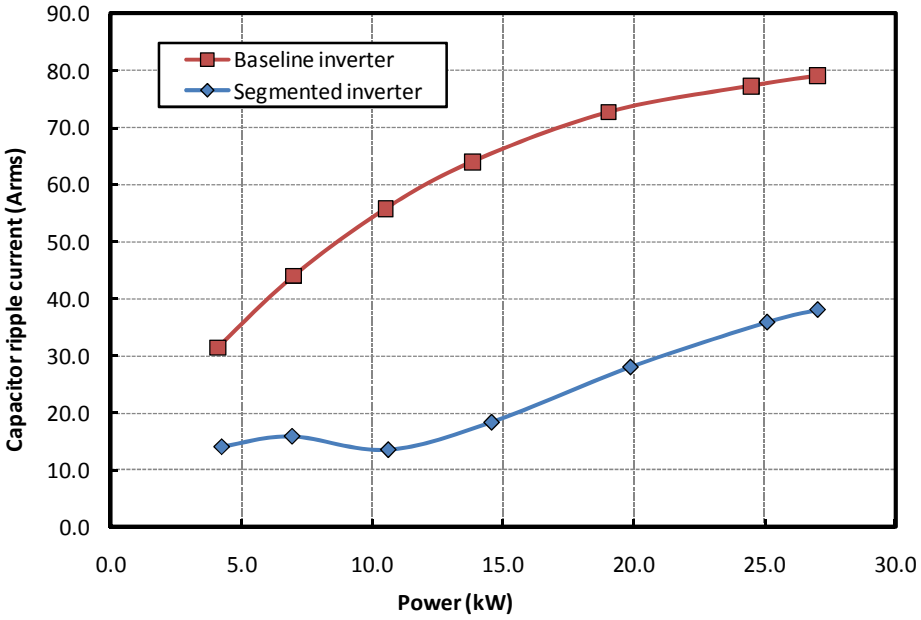


Fig. 10. Comparison of capacitor ripple current vs dc input power for an R-L load.

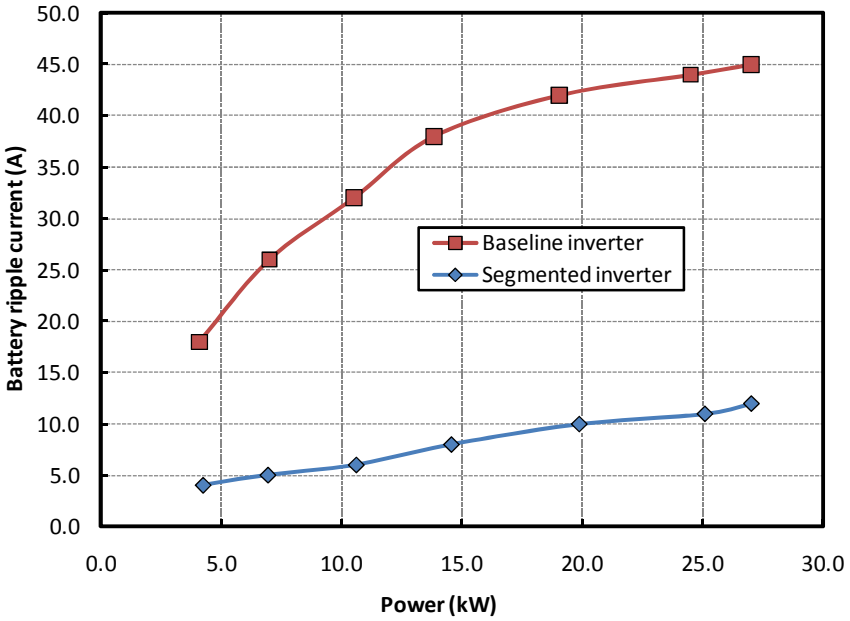


Fig. 11. Comparison of battery ripple current vs dc input power for an R-L load.

The prototype was then tested with a commercial, off-the-shelf, induction motor rated at 15 HP, 230 Vrms, 37.5 Arms, and 1,175 rpm. The motor is in delta connection and has six pole pairs. Tests were conducted at speed and load torque levels of 100%, 75%, and 50% of the rated value of 91 Nm. Due to the limitation of the maximum dc power supply voltage of 300 V, tests could not be done at the rated speed region. Figure 12 shows battery current, I_{bat}; motor currents, i_a, i_b, and i_c; capacitor ripple current, i_{Cbus}, at 565 rpm; and rated torque of 91 Nm where (a) is for the baseline inverter and (b) for the segmented inverter. The measured capacitor ripple currents are 37.1 Arms for the baseline inverter and 10.0 Arms for the segmented inverter, and the measured peak-to-peak battery ripple currents are 45 A and 5 A, respectively. These measurements show a reduction of 73% for capacitor ripple current and 89% for battery ripple current with the segmented inverter.

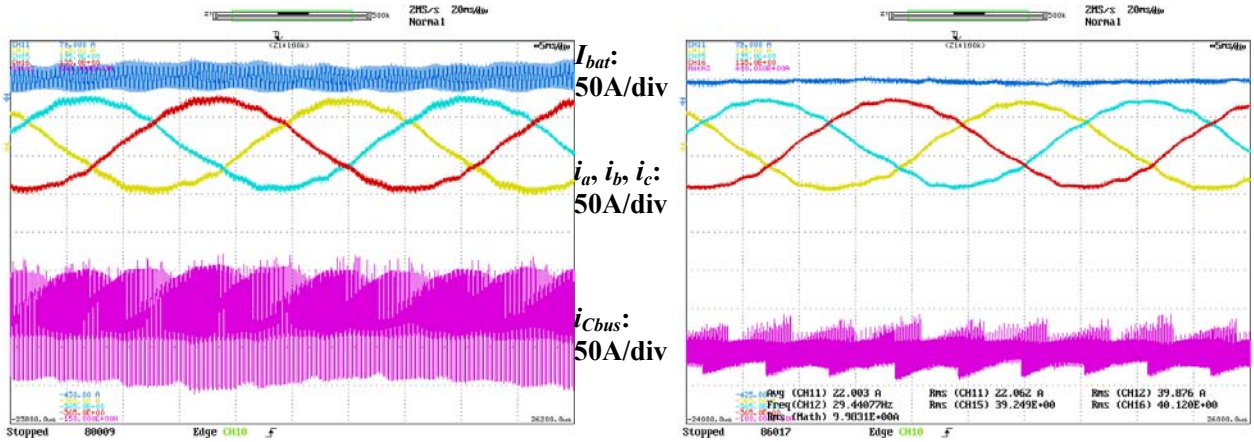


Fig. 12. Waveforms with an induction motor at 565 rpm and rated torque of 91 Nm, showing a reduction of 73% for capacitor ripple current and 89% for battery ripple current with the segmented inverter.

Figure 13 plots the capacitor ripple currents at various levels of load torque vs motor speed for both the baseline and segmented inverters. The segmented inverter offers a significant reduction of capacitor ripple current, in the range of 55%~75%, at the rated torque; 50%~70% at 75 % of rated torque; and 50%~60% at 50% of rated torque. It is also worth noting that the maximum ripple current with the baseline VSI approaches the rated motor current of 37.5 Arms.

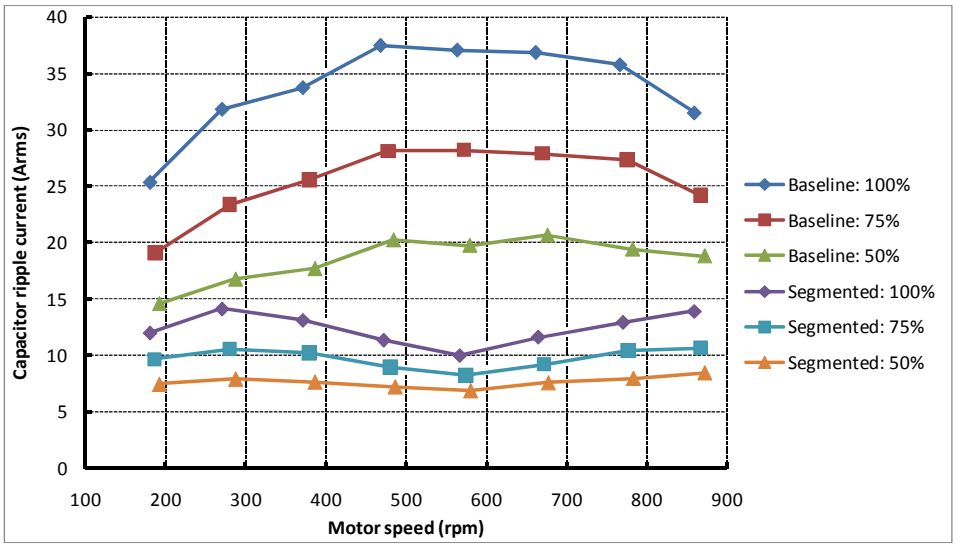


Fig. 13. Comparison of capacitor ripple current vs motor speed at load torque of 100%, 75%, and 50% of rated torque of 91 Nm.

Conclusion

A 55 kW segmented inverter prototype with a 60% reduction of dc bus capacitor was designed, built, and successfully tested with both R-L load and an induction motor. Test results show a significant reduction of 55%~75% in capacitor ripple current and 70%~90% in battery ripple current. Moreover, a lower switching frequency can be used with the segmented inverter to increase the inverter efficiency while still maintaining a low level of harmonic components in motor currents even for low inductance motors such as PM motors.

Table 2 shows estimated performance improvements when the technology is applied to the Toyota Camry motor inverter: 40% and 35% increases in specific power and power density, respectively, and 11% decrease in cost per kilowatt. It also indicates that the segmented inverter would exceed the DOE 2015 target for specific power and the 2020 target for power density.

Table 2. Estimated Performance Improvements

	Camry inverter[a]			**Segmented inverter[b]**		
	Weight (kg)	Volume (L)	Cost ($)	Weight (kg)	Volume (L)	Cost ($)
Bus Capacitor	3.57	2.6	182	1.43	1.04	73
Others	3.99	3.36	728	3.99	3.36	737
Subtotal	7.56	5.96	910	5.42	4.4	810
Metrics	**kW/kg**	**kW/L**	**$/kW**	**kW/kg**	**kW/L**	**$/kW**
	9.3	11.7	13	**12.9**	**15.9**	**11.6**
DOE targets	12	12	5	14.1	13.4	3.3
		2015			2020	

[a]Assumptions: Capacitor costs 20%.
[b]Assumptions: A reduction of 60% in bus capacitor requirement.

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1. U.S. Department of Energy, "FreedomCAR and Fuel Technical Partnership Technical Goals," http://www1.eere.energy.gov/vehiclesandfuels/about/partnerships/freedomcar/fc_goals.html.
2. Electronic Concepts Datasheet, http://www.eci-capacitors.com/product_details.asp?productid=29.

Patents

1. Gui-Jia Su, "Electrical Motor/Generator Drive Apparatus and Method," U.S. Patent App. 12/887,110, filed September 25, 2009.

2.6 Novel Packaging to Reduce Stray Inductance in Power Electronics

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Objectives

- Package devices in large power modules such that stray inductance is reduced.
- Reduce the stress on the insulated gate bipolar transistors (IGBTs) in hybrid electric vehicle (HEV) traction drives and dc-dc converters. Therefore, the IGBT can work at higher power rating and/or have better reliability and longer lifetime.
- Less distortion in output voltage and more reliable converter operation.

Approach

- Layout design of phase leg module using P-cell and N-cell technique, which is the series connection of IGBT and diode, instead of antiparallel connection of IGBT and diode.
- Perform electromagnetic-field simulation of the package to extract the parasitics using Ansoft Q3D Extractor.
- Perform circuit simulations for obtaining switching characterization with package parasitics.
- Use impedance analyzer to measure the parasitics in a prototype phase leg module.
- Use double pulse test (DPT) to experimentally test the switching behavior of the phase leg module.

Major Accomplishments

- Modeled package for phase leg module using Ansoft Q3D Extractor and obtained the parasitics in the module.
- Conducted double pulse testing using Saber simulator.
- Observed "turn-on" and "turn-off" switching behavior and analyzed the effect of the parasitics during switching.
- Fabricated the prototype of the power modules, obtained the steady state characteristics, and measured the parasitics (stray inductance and resistance).

Future Direction

- Build a DPT circuit to test and compare the conventional and proposed modules in terms of switching behavior, voltage (or current) stress, and ringing.
- Design single phase leg module with paralleling devices by using novel switching cell and conventional cells.
    - First, devices with positive coefficient will be selected.
    - Second, layout design and parasitics extraction will be performed using Q3D.

  - Third, electrical behavior will be investigated by Saber simulation.
  - Finally, two power modules with paralleling devices (one with conventional approach and one with new proposed approach) will be fabricated and experimentally compared.
- Extend the packaging design approach to three phase power module.
- Summarize and generalize the packaging design approach for P-cell and N-cell based power module.

Technical Discussion

Parasitics are a major concern in design and layout of IGBT packages and power stages with both high switching speed and high power handling requirements. In HEVs, this problem is especially important because of the high power rating and harsh working environment. The goal of this project is to reduce the stray inductance in a power module, improve the switching behavior of the power module, and improve the reliability and performance of the converter. To address the goal, we use the concept of the basic switching cells to package a phase leg module instead of the conventional antiparallel cell. The rearrangement of the layout of the phase leg module reduces the physical distance of a commutation loop so that the stray inductance is reduced.

Packaging Electrical Layout Considerations

Power electronics packaging technology has been developed for several generations, involving material upgrading, structure improvement, and inter-connection technique innovation. Several packaging technologies exist, and each has its own merits. However, currently, wire bonding technology is still the dominant method for commercial power modules, because of its maturity and reliability.

Figure 1 is a diagram showing the layers in an IGBT power module. The base layer, called the baseplate, is a thick layer of metal used for mechanical fixation. Direct bonded copper (DBC) is soldered to it. Power semiconductor dice and terminals are then soldered on top of the DBC. Aluminum wires are used for interconnection of dice and terminals. The module is then put in a plastic case. The case is infused with silicone gel for protection and insulation.

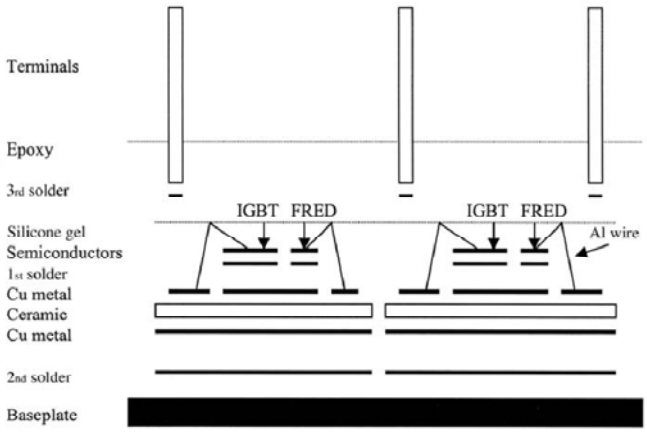


Fig. 1. Structure of an IGBT module. {*Source:* [1].}

In a wire bonding power module, terminal leads, bonding wires and DBC substrate all introduce stray inductance. For example, in a 300 A, 1,200 V, commercial power module, the terminal leads have inductance at the level of 30–40 nH, bonding wires have 10–15 nH, and substrate traces have 4–7 nH [2]. The parasitic inductance stores energy whenever the current flows through the interconnections inside the module when the IGBT is on. When it is turned off, the energy is released directly as a voltage spike and oscillation.

A scenario that is commonly used to explain the IGBT failure during thermal cycling is the coefficient of thermal expansion mismatch between the semiconductor dice and the DBC substrate. Actually, failures can be caused by the parasitic effects, and the performance of the device is limited by the parasitics. One of the examples is the IGBT or diode turn-off *dv/dt* spike, which is a function of total dc loop inductance. It can be controlled by the gate resistance of the IGBT, but slowing down the switching causes high turn-

on loss. After the IGBT fails, it is commonly found that one or two bonding wires were opened or the chip surface at the bonding joints is cracked.

High reliability and long term stability are essential in high power applications; therefore, reducing package stray inductance is an important issue. Several considerations and improvements in the structure of the package can reduce the parasitics of the module. They are discussed in the following paragraphs.

1. Terminal arrangement
As discussed above, in a power module the dominant stray inductance is the terminal. A laminated structure has smaller self-inductance, and also, when paralleling the positive and negative terminals, it enables the coupling of the two inductors to the greatest extent. The equivalent loop inductance equals the two self-inductances minus the mutual inductance. A larger mutual inductance will give smaller total equivalent loop inductance. When designing the terminals, the best way is put two parallel laminated bus bars as close as possible.

2. Bond wires consideration
The interconnection bond wires should be as short as possible. The direction of substrate current, which flows under the emitter bonding wires, is designed to be opposite to the direction of current flow in bonding wires. This wiring construction on the substrate is also achievable by using multilayered DBC technology. Consequently, the effect of the bonding wires on the module internal inductance can become practically negligible.

3. Use the substrate area
Although the substrate has the smallest inductance, a large substrate area can make the inductance considerably larger. This is especially true for high power modules because the paralleling of the power devices enlarges the substrate area. To accommodate the bonding wire connection, the substrate area has to be larger than the footprint of the semiconductor dice. When designing the substrate layout, maximum use should be made of the full substrate area.

4. The "U-package" technology [3]
In 1996 Mitsubishi made a major improvement on the bus bar structure that reduced stray inductance. The bus bars are molded into the sides of the case, aluminum wires are used to connect the substrate or die to the terminal. This relieves "S" bends that were needed in the electrodes of conventional modules. Elimination of these "S" bends helped to further reduce the electrode inductance. Overall, as a result of these inductance reducing features, the new package has about one third the inductance of conventional modules.

People are making every effort to reduce the stray inductance inside IGBT modules; however, one important issue has been neglected: the effective stray inductance while the module is operating. Stray inductance is everywhere in a module; the focus should be on stray inductance in the conduction path during switching on and switching off. The following sections introduce concepts of two basic switching cells in power converters, reveal the mechanism of how the switching cell works as a functional unit, and show how it can affect power module packaging. The concept and analysis have been verified by simulation.

Concept of Basic Switching Cells
As the basic circuit elements, switching devices [mainly metal-oxide semiconductor field-effect transistor (MOSFET) and IGBT], diodes, and inductors and capacitors are used in power electronic circuits to perform ac-dc, dc-dc, dc-ac, and ac-ac power conversion. On examining the basic building blocks of these power electronics converters, two basic switching cells were proposed in [4,5], as shown in Fig. 2. Each cell consists of one switching device (a MOSFET or IGBT) and one diode connected to three terminals:

(+), (–), and (→) or (←). Each cell has a common terminal which has a current direction shown as (→) or (←) on the schematic. For the P-cell, this common terminal is connected to the positive terminal of a current source or an inductor. For an N-cell, this common terminal is connected to the negative of a current-source or an inductor. The active switching device in a P-cell is connected between the (+) and common terminal, whereas in an N-cell, the switching device is connected between the (–) terminal and the common terminal. Although the switching cells have only two components, they can be connected in different combinations to construct various power electronic circuits.

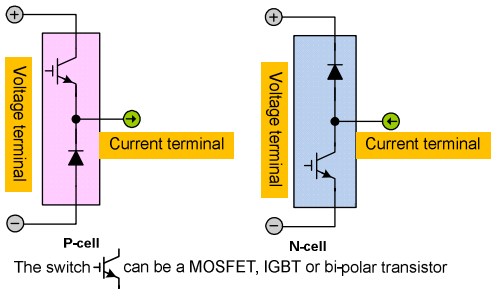


Fig. 2. Two basic switching cells: P-cell and N-cell.

Existing dc-dc converters can easily be represented and configured from the basic switching cells. Also, some new conversion circuits can be derived based on the mirror structure of the two switching cells. Figure 3 summarizes the four classical converters and their cell structures. The leftmost column [Fig. 3(a)] shows the four major classical converters. All of the conventional converters (except the boost converter) have an inherent P-cell structure where the active switching element is connected to the positive power supply terminal [Fig. 3(b)]. The conventional boost converter is inherently an N-cell boost converter.

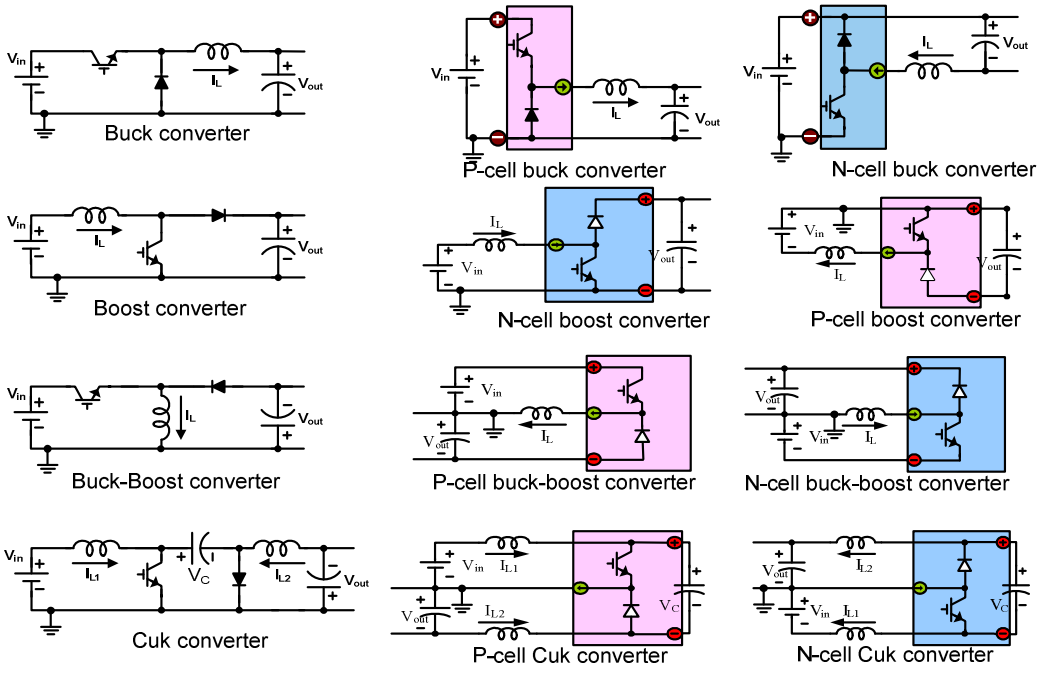
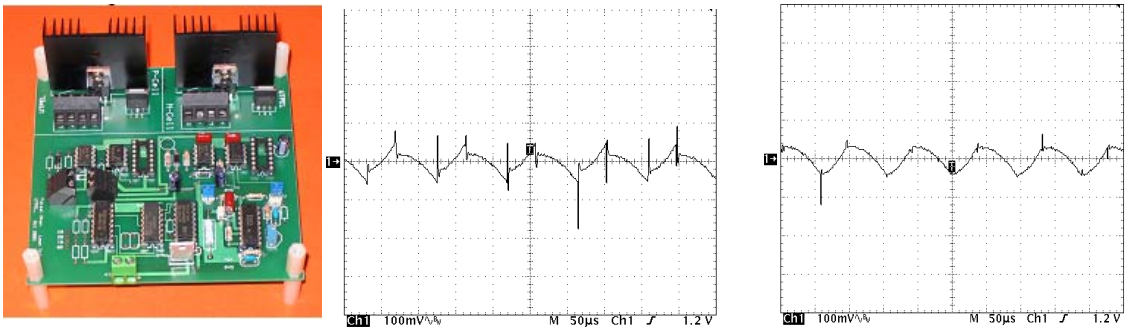


Fig. 3. The four classical converters and their cell structures:
(a) classical dc-dc converters, (b) structure of the basic cells, and (c) basic cell mirror circuits.

All of these classical converters also have a mirror circuit representation [Fig. 3(c)]. When the P-cell in a buck converter is replaced with an N-cell, the circuit takes a different configuration. In the same way, the

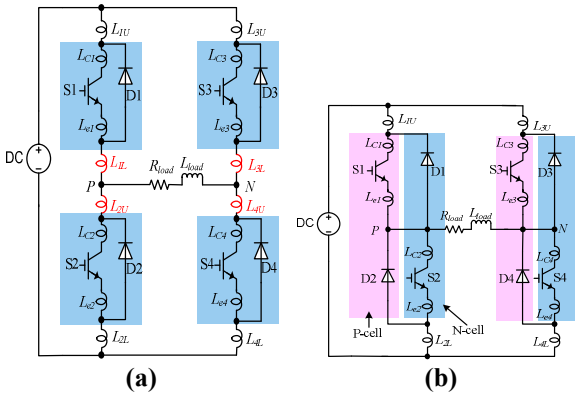
classical boost, buck-boost, and Ćuk converters can be reconstructed using their corresponding mirror cells. The reconstruction of the dc-dc converters using the mirror circuit can introduce advantages in gate drives. For example, in an N-cell buck converter, the gate drive signal is ground referenced so that the converter circuit is more tolerant to supply noise and ripple voltage. The experimental setup for P-cell and N-cell buck converters is shown in Fig. 4(a). As shown in Figs. 4(b) and 4(c), the output voltage is smoother in an N-cell buck than that in a P-cell buck because of the simplification of the gate drive circuit.



(a) **(b)** **(c)**

Fig. 4. Experimental setup for P-cell and N-cell buck converters: (a) experimental prototype of the P-cell and N-cell, (b) output voltage ripple (100 mV/div) of P-cell buck converter, and (c) output voltage ripple (100 mV/div) of N-cell buck converter.

In a traditional phase leg, the basic unit is the antiparalleled switch and diode as shown in Fig. 5(a). However, under induction load condition, current commutation is between S1 and D2 when current direction is from load terminal P to N or between S2 and D1 when current is from N to P. Therefore, in terms of natural current commutation pass, it is more reasonable to construct a phase leg by P-cell and N-cell, as shown in Fig. 5(b). Load current flows into the phase leg through an N-cell and goes out of the phase leg through a P-cell. Figure 5(a) also shows the stray inductance within each phase leg module. This stray inductance model is referred from [6]. L_{1U} and L_{2L} are introduced by terminal leads; L_{1L} and L_{2U} are the stray inductance of the internal bus connecting the upper and lower unit; and the values of these four inductors are relatively large. L_{C1}, L_{e1}, L_{C2}, and L_{e2} are associated with the die and wire bond, which are relatively small.



(a) **(b)**

Fig. 5. (a) Conventional full bridge inverter; (b) phase leg constructed by P-cell and N-cell.

Reorganization of the phase leg can reduce the stray inductance between the two commutation devices. Comparing Figs. 5(a) and 5(b) for the left phase leg, inductances L_{1L} and L_{2U}, introduced by the internal bus, are reduced in the cell structure.

These basic switching cells function as the basic building blocks in power electronic circuits, which cannot be further broken down or apart. They can be used as the basis for manufacturing/layout of single, dual, and six-pack modules that semiconductor manufacturers produce and should be integrated and manufactured as a module, which will have promising application in dc-dc converters and inverters. They not only bring convenience to building dc-dc converters but also reduce the stray inductance between the two devices. Separately packaged devices have stray inductance in both ends due to the package lead, wire bond connection, and external soldering. During current commutation from active switch to diode,

these inductances will cause voltage spikes and oscillations, which are the sources of electromagnetic interference and may even cause damage to the devices under high *di*/*dt* condition. Modularization of P-cells and N-cells can to a large extent reduce stray inductance.

IGBT Module Package Modeling and Parasitics Extraction

To build power modules and verify the concept proposed in the last section is expensive and time consuming. However, this process can be simplified by the aid of the software tool Ansoft Q3D Extractor. The software uses method of moments (integral equations) and finite element methods to compute capacitive, conductance, inductance, and resistance matrices. Providing the correct dimensions, material properties (resistivity of conductors and permittivity of insulators), and boundary conditions (the conductors and current paths), the software can extract the structural impedances of any arbitrary geometry. Thus, the module parasitics can be understood thoroughly before it is manufactured.

The conceptual phase leg modules (Fig. 6) are built using Ansoft Q3D Extractor. For comparison purposes, the two modules are similar in terms of substrate size and lead frame position. (Physical size characteristics are given in Table 1.)

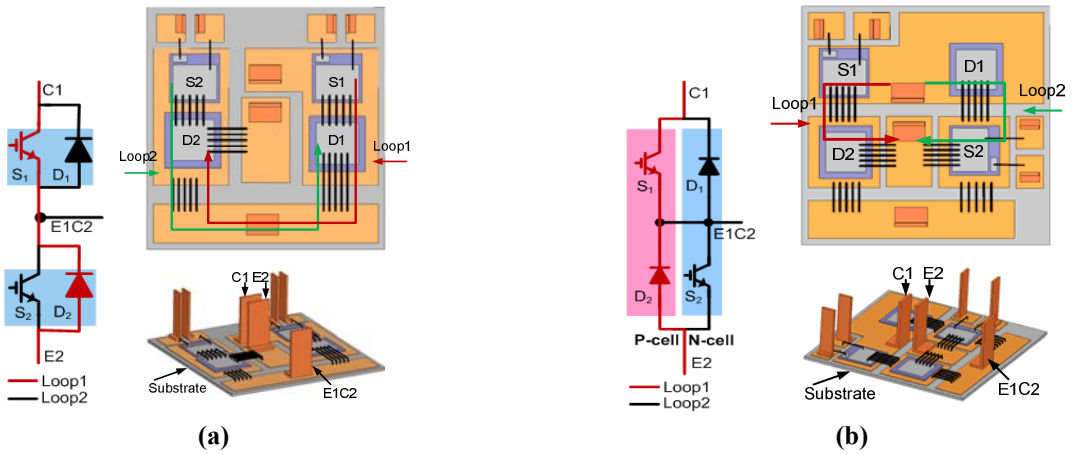


Fig. 6. Phase leg module layout: (a) conventional module layout; (b) proposed module layout.

Table 1. Physical Size of the Two Modules Shown in Figure 6

Component	Conventional module	Proposed module
DBC size (mm)	37.0 × 38.0	37.5 × 38.5
DBC thickness (mil)	8(Cu), 25(alumina)	8(Cu), 25(alumina)
IGBT (mm)	5 × 5	5 × 5
Diode (mm)	5.85 × 5.85	5.85 × 5.85
Bond wires	8 mil × 5	8 mil × 5

Figure 6(a) shows the connection and physical layout of a conventional module, while Fig. 6(b) shows the proposed P-cell and N-cell structure module. The marked Loop1 and Loop2 are two current commutation loops in a phase leg, specifically, from upper IGBT to lower diode and from lower IGBT to upper diode. In a conventional module, the upper leg devices S_1 and D_1 are seated at one side, while the lower leg, S_2 and D_2, are seated at the other side. The physical distance for Loop1 is shown as the red trace. It starts from lead C1, passes through S_1 and two groups of bond wires and output bus E1C2 and then another group of wires to D_2. The length for Loop2 is similar to Loop1. In the proposed P-cell and N-cell modules, the two devices in the commutation loop are seated at the same side; thus, the physical length of the commutation loop is reduced. For example, Loop1 (shown as the red trace) also starts from C1, goes

through only one group of wires, then reaches D_2. This is much shorter than the same loop in a conventional module.

After the geometries of the modules are built in Q3D Extractor, electromagnetic simulation is conducted. A dc excitation source is used in simulation; therefore, skin effect is neglected and the modeled parasitic resistance is smaller than the true value. The simulation results are shown in Table 2. It can be seen that Loop1 and Loop2 inductance are both more than 50 nH in the conventional module, while in the proposed module, the loop inductances are 39.91 nH and 35.18 nH, respectively. As expected, the main reduction is from S_1 emitter to D_2 cathode in Loop1 and from S_2 collector to D_1 anode in Loop2.

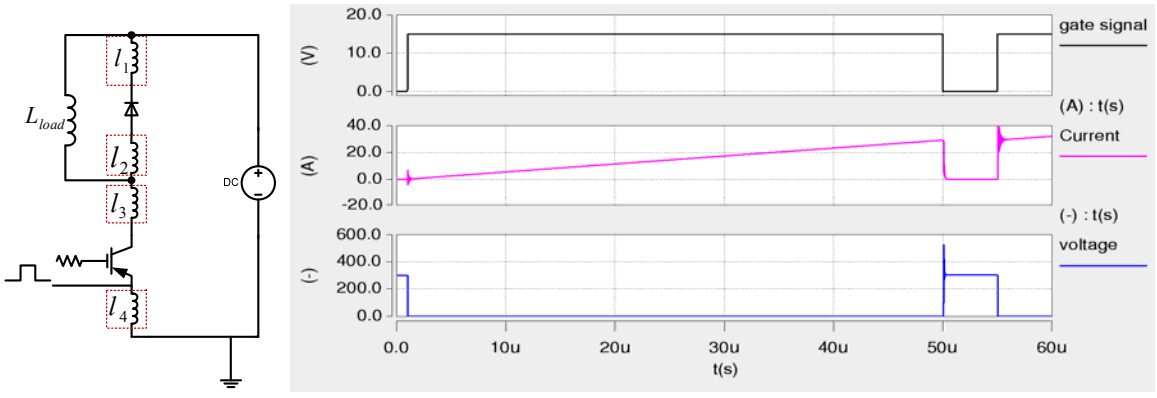
Table 2. Parasitic Resistance and Inductance Extracted from the Power Modules

Circuit	Conventional module	Proposed module
Loop1	8.36 mΩ, 53.06 nH	6.44 mΩ, 39.91 nH
Loop2	7.81 mΩ, 50.67 nH	5.62 mΩ, 35.18 nH
S_1 emitter to D_2 cathode	3.18 mΩ, 20.19 nH	1.26 mΩ, 4.23 nH
S_2 collector to D_1 anode	3.24 mΩ, 20.36 nH	4.04 mΩ, 5.14 nH

Simulation of Switching Characteristics Under Circuit Parasitics

The parasitics in a power electronics module affect the turn-on and turn-off transients and not the steady state performance. After extraction of the module parasitics, mainly the stray inductance, a study was performed to characterize the switching behavior for the two different power module layout cases.

A double pulse tester, shown in Fig. 7(a), was used to obtain the switching behavior under the influence of the module parasitics. It is essentially a step-down converter. The major components include one IGBT and one diode inside the module, an inductive load, L_{load}, the stray inductances extracted earlier (l_1, l_2, l_3, and l_4), and a dc voltage source. Only two pulses are applied to each IGBT; the first pulse is used to obtain the desired current. The switch turns off at the desired current, current commutates to the diode, and turn-off behavior can be observed accordingly. After a short while, the switch is turned on at the second pulse. Because of the large inductive load, the current does not change much, and turn-on behavior under the desired current can be observed. Some typical waveforms are shown in Fig. 7(b) for a DPT implemented in Synopsys Saber.



(a) **(b)**

Fig. 7. Double pulse tester: (a) circuit and (b) typical waveforms.

Table 3. Stray Inductance Used in Double Pulse Tester

	Conventional module	Proposed module
l_{p1}	15.3 nH	15 nH
l_{p2}	10.4 nH	2.07 nH
l_{p3}	10.4 nH	2.07 nH
l_{p4}	20.3 nH	20 nH

The parameters used in the double pulse tester are shown in Table 4. The point-to-point inductances are l_1, l_2, l_3, and l_4 (the loop inductance in Table 2 is the sum of these four inductances). The IGBT and diode are practical models from the Saber library: a Fairchild IGBT rated at 600 V, 40 A, and an IR diode rated at 600 V, 45 A. The simulation is conducted under 300 V, 30 A.

Table 4. Parameters Used in Double Pulse Tester

Parameters	Values
L_{load}	500 µH
IGBT	HGTG40N60B3
Diode	HFA45HC60C
dc source voltage	300 V
l_1, l_2, l_3, l_4 in proposed module	15.0 nH, 2.7 nH, 2.7 nH, 15.0 nH
l_1, l_2, l_3, l_4 in conventional module	15.3 nH, 10.4 nH, 10.4 nH, 15.3nH

Simulation results from the double pulse tester show the advantages of the proposed module compared with the conventional one. The voltage across the IGBT during turn off is shown in Fig. 8. After the voltage rises to the dc link voltage, there is an abrupt drop of the IGBT current and high *di*/*dt* causes a voltage drop across the stray inductance, which causes the voltage overshoot and oscillation as shown in Fig. 8. In the conventional module, the voltage overshoot is 246 V, while the overshoot voltage is 200 V in the proposed module. The overshoot is smaller in the proposed module because the stray inductance is smaller.

During turn on, after the IGBT current reaches the load current, the diode reverse recovery begins, and the IGBT turn-on current has an overshoot. After that, this current rings between the parasitic inductance and the diode parasitic capacitance. This phenomenon is shown in Fig. 9. The overshoot amplitude of the two cases is similar; however, the ringing damps faster in the proposed module as a result of the reduced inductance.

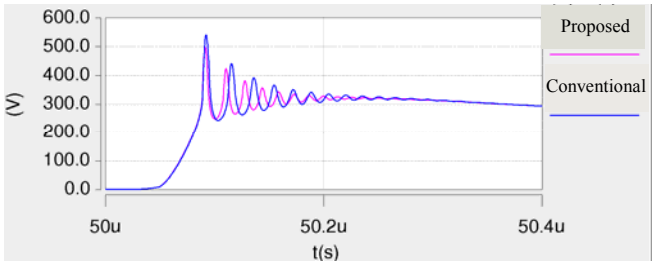


Fig. 8. Voltage waveform across IGBT at turn off.

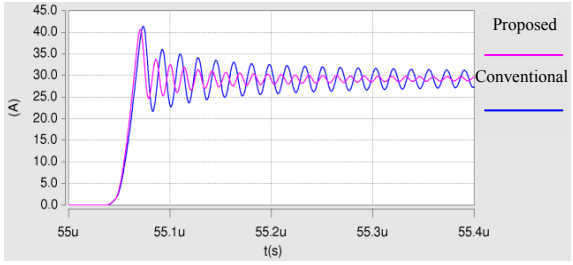


Fig. 9. IGBT current waveform at turn on.

Analysis of Resonance Caused by Parasitics

Oscillation during the turn-on and turn-off processes is triggered by not only the stray inductance but also the device capacitance in the IGBT and diode. The stray inductance introduced by the package and the capacitance of the device compose a resonant circuit that causes the voltage and current oscillation at switching. This section looks into the different current paths during turn on and turn off.

1. Identification of turn-off resonance circuit

The turn-off resonance sets up after the IGBT voltage reaches the dc source voltage; at this time the diode conducts current. The diode body capacitor C_J is bypassed. Resonance occurs between stray inductances, l_{diode} and l_{IGBT}, and the IGBT output capacitor, C_{OES}, as shown in Fig. 10(a). Stray inductance l_{diode} is the sum of the stray inductance connected to the cathode and anode of the diode, and l_{IGBT} is the sum of stray inductance connected to the collector and emitter of the IGBT.

2. Identification of turn-on resonance circuit

The turn-on oscillation occurs after the IGBT current reaches the load current. The voltage across the IGBT starts to drop, while the diode voltage increases. There is discharge current from capacitor C_{OES}; however, because the IGBT is already turned on, this current goes through the IGBT and does not resonate with the stray inductance. The diode capacitor C_J is also discharged; therefore, the resonance is between the stray inductance and C_J, as shown in Fig. 10(b).

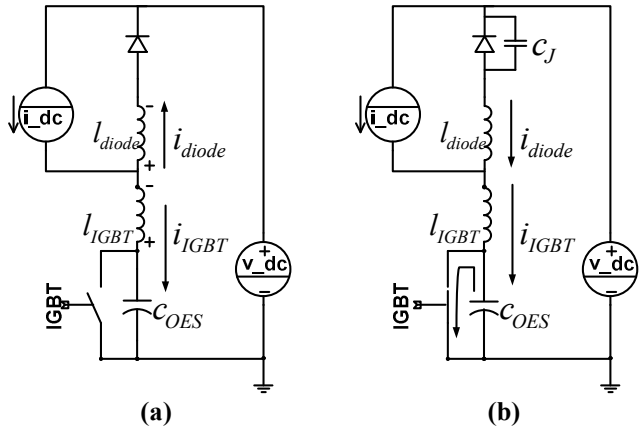


Fig. 10. Turn-off (a) and turn-on (b) equivalent resonant circuits.

Conclusion

As a result of investigating power electronics converters in terms of their topological characteristics and basic building blocks, a new packaging method based on the P-cell and N-cell has been proposed. The modularization of a single P-cell or N-cell increases the convenience of building dc-dc and dc-ac converters. More importantly, the proposed package reduces the parasitic inductance in the commutation loop and suppresses the LCR resonance, consisting of the parasitic inductance in the module and the capacitance in the power devices, during switch turn on and turn off.

Publications

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2.7 Air-Cooled Traction Drive Inverter

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Objectives

- Enable cooling the power electronics with air thereby eliminating the existing liquid-cooled thermal management system.
- Demonstrate the feasibility of air cooling for power electronics through studying component boundary conditions while achieving DOE Vehicle Technologies Program (VTP) 2020 inverter targets for a 55 kW peak/30 kw continuous power rated inverter.
- Reduce the cost for cooling power electronics by eliminating the liquid cooling system.

Approach

- Refine the air-cooled inverter models developed in FY 2009.
  - Perform thermal and fluid simulations on selected inverter architectures to predict the performance of the heat removal system.
  - Improve the geometric and airflow configuration developed during FY 2009 under the Wide Bandgap (WBG) project to improve the performance of the air-cooled inverter.
- Develop knowledge base to define requirements of the components in the inverter to meet VTP 2020 inverter targets (volume, weight, cost) using a baseline inverter design. The project will focus on studying the boundary conditions (such as ambient and inlet air temperatures, air flow rate, etc.) required for a 55 kW peak/30 kW continuous power rated inverter with air cooling.
- Prepare a summary report: A summary of feasibility study results of the air-cooled inverter will be incorporated into the VTP annual report.

Major Accomplishments

- Completed the parametric study of the air-cooled traction drive inverter with two different designs.
- Studied the parameters of the inverter designs for steady state conditions and drive cycle conditions to show the difference in the parameters affecting the air-cooled inverter design.
- Completed the study to determine the feasibility and boundary conditions required for a 55 kW peak/30 kW continuous power rated inverter with air cooling.

Future Direction

- ORNL will wait for the results of balance of plant thermal modeling from the National Renewable Energy Laboratory to determine whether this project should be continued in the future.

Technical Discussion

Parametric studies of two 55 kW peak/30 kW continuous power rated air-cooled inverter designs were conducted to determine their thermal performance and the boundary conditions of the components. The inverters were simulated over a range of parameters such as ambient conditions, inverter voltage, switching frequencies, etc. The two inverter designs are very different in configuration, and the designs will be referred to as design A and design B.

For evaluating their relative performance, both designs use the same number of identical devices, the same power generations curves, and the same materials and material properties. The parameters of the inverter designs were studied for steady state conditions and drive cycle conditions to show the difference in the parameters affecting the air-cooled inverter design. A total of 8 cases of steady state for design A and 24 cases for design B were computed.

A total of 16 combinations of transient performance results were computed using the US06 Supplemental Federal Test Procedure (hereafter US06 drive cycle) current distribution. The details of the technical approach to the design and the results of the simulations are presented below, starting with an overview of the design methodology followed by discussions of design A and design B.

1. Overview of the Design Methodology

The thermal performance of an inverter is based on the heat generated by the losses in devices. The loss models that are used in the inverter design are very critical and significantly impact the design process. In FY 2009, the inverter models used steady power dissipation in the power electronic devices based on the highest estimated losses of a 55 kW inverter obtained from test data. In FY 2010, device power loss equations which are dependent on voltage, current, switching frequency (f_{sw}), and temperature were used in the thermal-fluid simulations of the FY 2010 inverter geometries. These equations were generated from data taken at NTRC from testing the 1,200 V, 100 A, silicon carbide (SiC) metal-oxide semiconductor field-effect transistors and diodes performed under the WBG project. The data can be found in Sect. 4.1 of the annual report. These equations were used in an iterative process, with the junction temperature as the iterated quantity, to determine the steady state temperatures of both inverter geometries. The design methodology of this process is shown as a flowchart in Fig. 1.

Using the power dissipation equations of the SiC devices, the power loss values were significantly higher than FY 2009 models for constant current and voltage under steady state conditions. Having made the models more realistic with junction-temperature-based power losses, a parametric study of differing global inlet temperatures and flow rates was performed to obtain the thermal performance information of a single power module of the inverter. The parametric study was carried out on single power module and not the entire inverter. All the devices in the power module were modeled with their own power dissipation equations and feedback temperature loops to simulate the differing junction temperatures based on device position in the flow field and positioning relative to other thermal generating devices. This type of simulation provided useful information regarding gate driver connection temperatures, capacitor temperature, and phase connection temperatures.

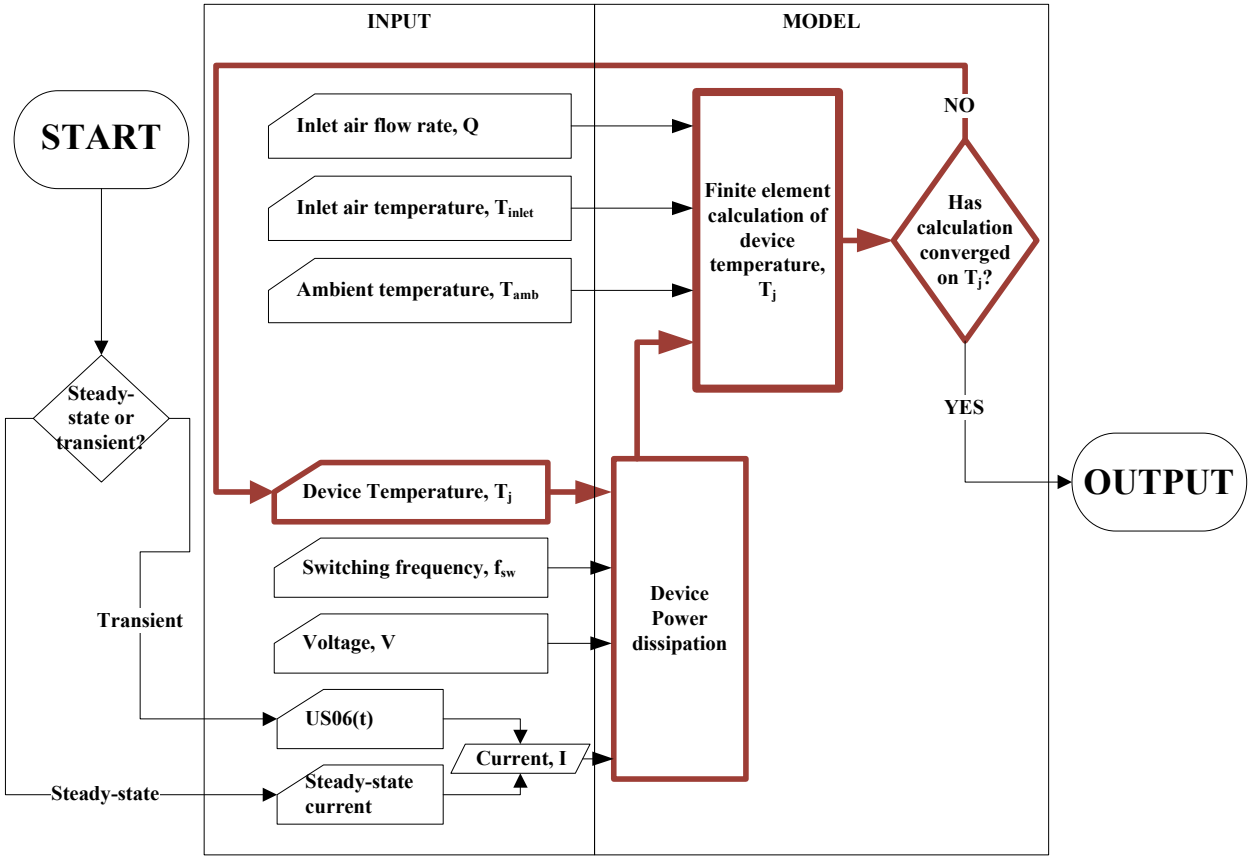

Fig. 1. Flowchart outlining junction temperature iterative procedure.

2. Design and Performance Evaluation: Design A

The overall air-cooled inverter concept was first evaluated in a feasibility study (FY 2009) of a radial-inflow inverter design concept from which the axial inflow inverter design process started. The first objective was to quantify this difference directly. Pressure drop was reduced 13% by simply changing the inlet air flow configuration from radial inflow to a more desirable and natural axial inflow. The design process underwent a series of revisions which were largely governed by the steady state temperature solutions.

2.1 Achieving Low Blower Power Requirements

Because the FY 2009 design had unacceptably high pressure drop and blower power requirements, the present study was focused on reducing them. The main reason for the high pressure drop in the radial inflow configuration is the unusually large area reduction of 90% (i.e., A_{out}/A_{in} = 10%).

Simply changing the inlet air flow orientation from radial in to axial, without reducing the area, and eliminating one turn of the flow reduced pressure drop (ΔP) across the device to 11.8 in. H_2O, which is an improvement of 11%. The results for the final configuration used in FY 2010 are shown in Fig. 2.

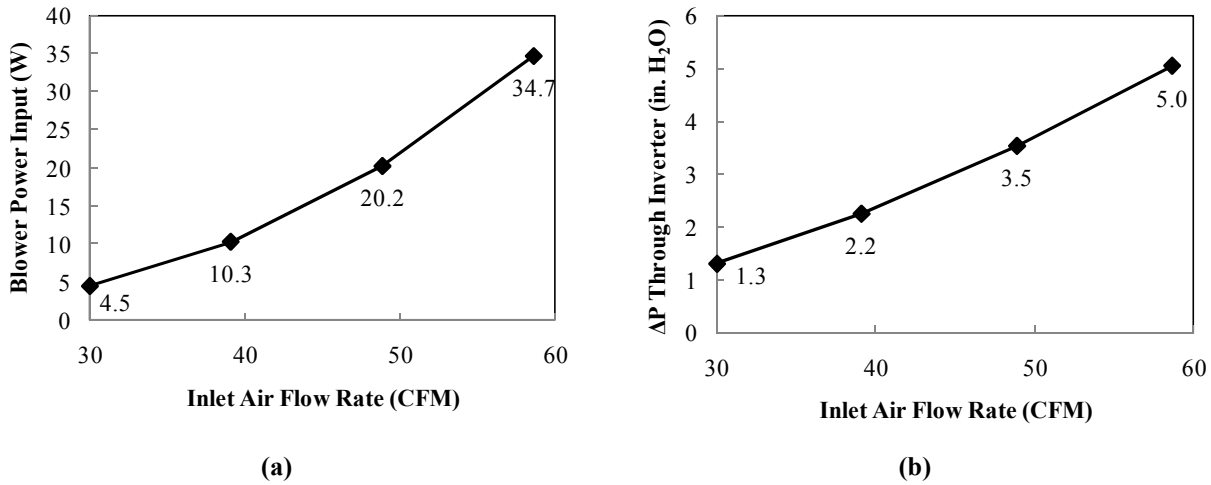

Fig. 2. Ideal blower power input (a) and ΔP across the inverter as a function of inlet air flow rate (b).

2.2 Steady State Thermal Modeling Results

For the results presented, power dissipated (E_{gen}) from the SiC power switches and SiC diodes is evaluated within the model as a function of current, voltage, f_{sw}, and device temperature. Steady state results for the final configuration are shown in Table 1.

Table 1. Steady State Temperature Results for Design A for Q = 50 and 60 CFM; V = 650V, I = 240 A, and T_{in} = 50–80°C

Q = 50 CFM				
Inlet temperature (°C)	50	60	70	80
Junction temperature (°C)	274	304	340	387
E_{gen}*(W)*	719	778	852	956
Q = 60 CFM				
Inlet temperature (°C)	50	60	70	80
Junction temperature (°C)	226	248	271	296
E_{gen}*(W)*	635	671	713	761

2.3 Transient Results of Finite Element Method Simulations of the Final Design Module

The transient response of the system is modeled with current as a function of time as provided by the US06 drive cycle. The transient response to the US06 drive cycle was obtained for two air flow rates of 30 and 60 cubic feet per minute (CFM), where 30 CFM represents the lowest cooling capability and 60 CFM the highest cooling of all the flow rates considered.

The parametric results are presented in Figs. 3 and 4. The junction temperature results for the transient models are tabulated in Table 2 for the 16 combinations of input frequency, voltage, ambient temperature (T_{amb}), and air flow rate. For all cases with inlet temperature (T_{inlet}) =50°C and T_{amb} = 120°C, the junction temperature (Tj) at the end of the cycle is always lower than that at the beginning, which is important when considering how the system would respond to multiple cycles. Essentially, the maximum temperature at the end of a cycle will not exceed 164°C for any number of cycles. For the input parameters described, the power density is calculated to be 12.4 kW/L (excluding the capacitor volume) based on 650 V bus voltage and 240 Arms output current.

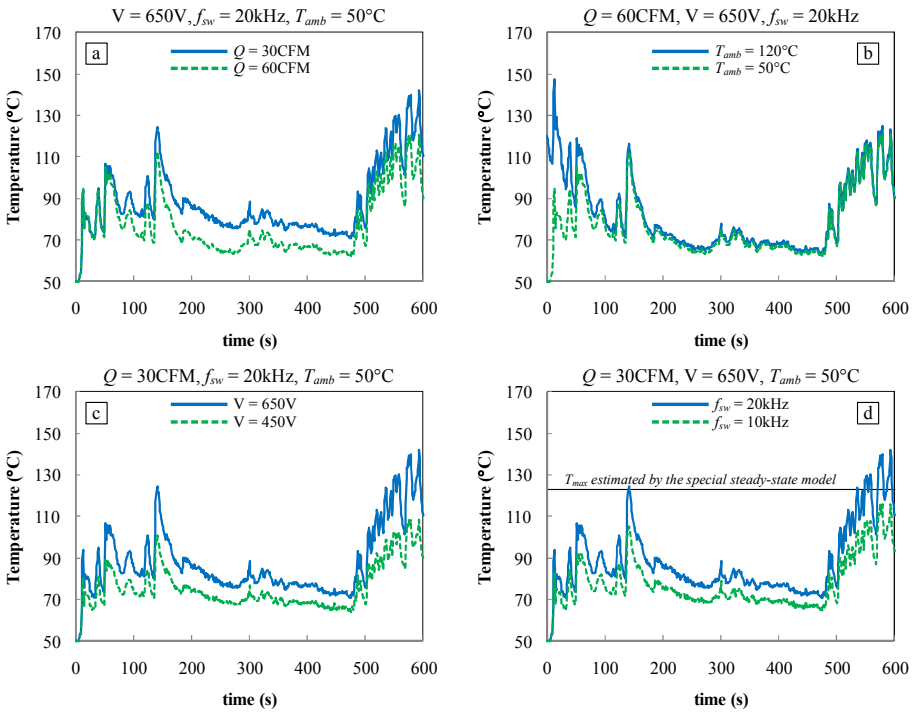

Fig. 3. Transient results for design A showing the effect of changing *Q*, T_{amb}, V, and f_{sw}.

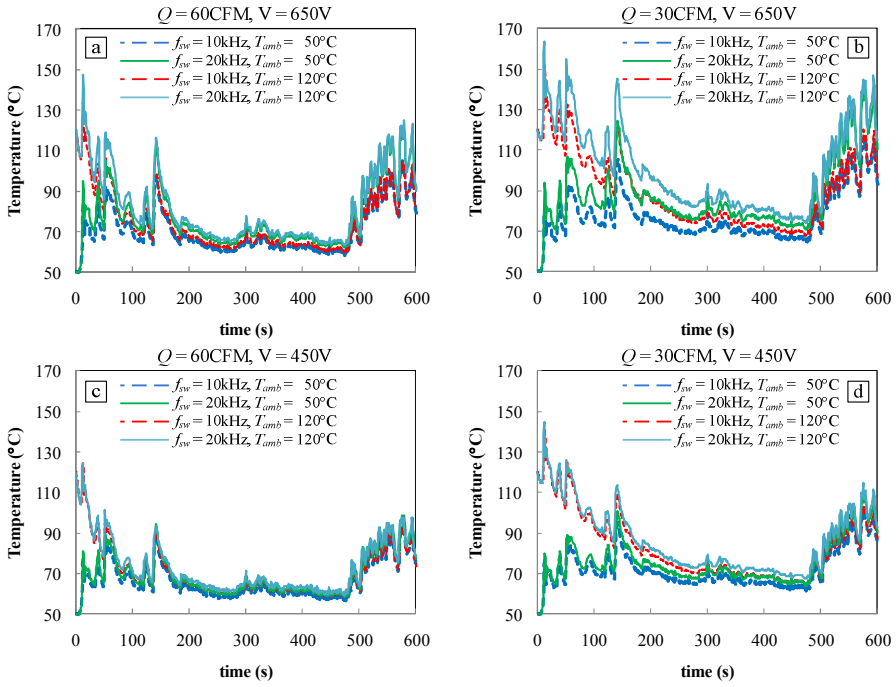

Fig. 4. Results of all 16 transient simulations of the US06 drive cycles for design A.

Table 2. Tabulated Results for all 16 Transient Cases of Design A

	Input parameters				Results
Case number	***Q*** **CFM**	T_{amb} **°C**	**V** **V**	***f*** **kHz**	***Max*** T_j **°C**
1	30	50	450	10	103
2				20	108
3			650	10	116
4				20	142
5		120	450	10	142
6				20	145
7			650	10	152
8				20	164
9	60	50	450	10	92
10				20	99
11			650	10	105
12				20	121
13		120	450	10	124
14				20	125
15			650	10	133
16				20	147

3. Design and Performance Evaluation of the Inverter: Design B

Design B is a new inverter design with a geometry that is different from design A. It was developed as an alternate solution to lower the blower power requirements below that of design A. However, for evaluating the relative performance of both designs, the same number of identical devices, power generations curves, materials and material properties are used in both designs.

3.1. Steady State Results of the Finite Element Simulations of the Final Module Design

The results for the finite element simulations of the three-dimensional (3-D) fully turbulent flow domain through the module are presented in Table 3. From Bernoulli's equation, we know that $\Delta P \sim \Delta Q^2$. The results from the simulations are consistent with this theory. A curve fit of the data with a quadratic polynomial yielded a coefficient of determination of 0.9991. The temperature results of the parametric study are presented in Table 4.

Table 3. Results for the Ideal Blower Power Requirements to Drive the Flow Field

Q per Module (CFM)	30	40	50	60	70	80
Q for Entire Inverter (CFM)	270	360	450	540	630	720
Inlet Velocity (m/s)	3.38	4.51	5.63	6.76	7.89	9.02
ΔP Across the Entire Inverter (Pa)	109	187	292	411	550	708
Ideal Blower Power for the Entire Inverter (W)	13.9	31.8	62	104.7	163.5	240.6

Table 4. Steady State Temperature Results for V = 650 V, I = 240 A, and T_{inlet} = 50 to 85°C

Q = 40 (CFM)								
T_{inlet} (°C)	50	55	60	65	70	75	80	85
Tj (°C)	252	264	276	288	302	315	330	346
E□$_{gen}$ (W)	730	753	777	804	831	862	892	932
Phase connection (°C)	159	168	177	185	195	204	214	225
Gate connection (°C)	165	173	183	191	201	211	221	232
dc connection (°C)	131	138	145	153	161	169	177	187
Capacitor (°C)	127	134	142	149	157	165	173	182
Q = 50 (CFM)								
T_{inlet} (°C)	50	55	60	65	70	75	80	85
Tj (°C)	206	215	224	234	243	253	263	274
E□$_{gen}$ (W)	646	662	679	696	713	732	752	773
Phase connection (°C)	126	133	140	147	154	161	169	176
Gate connection (°C)	134	141	148	155	162	170	178	185
dc connection (°C)	105	111	118	123	129	136	143	149
Capacitor (°C)	102	108	115	120	126	133	140	146
Q = 60 (CFM)								
T_{inlet} (°C)	50	55	60	65	70	75	80	85
Tj (°C)	184	193	201	209	218	227	235	244
E□$_{gen}$ (W)	610	624	638	652	667	683	699	716
Phase connection (°C)	111	117	124	130	137	143	150	157
Gate connection (°C)	119	126	133	139	146	153	160	167
dc connection (°C)	93	99	105	110	116	122	129	135
Capacitor (°C)	91	96	102	108	114	120	126	132

3.2. Transient Results of Finite Element Method Simulations of Final Module

A total of 16 different transient cases were simulated, comprising all possible combinations from two selected values for each of four parameters of interest. They are the volumetric flow rates of air at 30 and 60 CFM, voltages of 450 and 650 V, f_{sw}s of 10 and 20 kHz, and T_{amb}s of 50°C and 120°C. In all cases studied, the maximum Tjs reported in Table 5 are for the single device temperature, which was the maximum. The results of these simulations can also be seen in Figs. 5 and 6. All of these results are for T_{inlet} = 50 °C.

Note that the effect of changing T_{amb} has no significant effect on Tj at the end of the cycle, as can be seen in Fig. 5(b). This is a very significant result. Furthermore, the maximum temperature for all cases with $T_{amb} = T_{initial}$ = 120 °C occurs near the beginning of the cycle, as it was thermally soaked at this temperature. However, because T_{inlet} = 50°C (122°F) is lower than $T_{initial}$, the air flow cools the system and temperatures decrease beyond the initial peak values while the current levels are decreasing. Toward the end of the cycle when the current increases, the temperature begins to increase again. However, Tj at the end of the cycle is far below the peak value at the beginning of the cycle. The end-of-cycle Tj values are much closer to end-of-cycle Tj values for the $T_{amb} = T_{initial}$ = 50°C cases. In contrast, for the $T_{amb} = T_{initial}$ =

50°C cases, the maximum temperatures occur toward the end of the cycle in response to the increasing current.

Table 5. Transient Simulation Results of Design B for Operation Under US06 Drive Cycle

Case Number	Q (CFM)	Voltage (V)	Tamb (°C)	f_{sw} (kHz)	Tj (°C)
1	30	650	50	10	94
2				20	111
3			120	10	136
4				20	146
5		450	50	10	86
6				20	91
7			120	10	130
8				20	132
9	60	650	50	10	89
10				20	98
11			120	10	128
12				20	138
13		450	50	10	80
14				20	83
15			120	10	122
16				20	125

The maximum temperatures reported in Table 5 are valid for the simulations of the US06 drive cycle, but only for the first cycle. If these simulations are repeated sequentially, for more than one cycle, the maximum temperature results of all successive cycles after the first cycle (a) would be independent of T_{amb}, (b) would occur at the end of the cycle as in the T_{amb} = 50°C case, and (c) would be nearly equal to the value of the T_{amb} = 50°C case.

Increasing the voltage or f_{sw} increases the device temperatures as shown in Figs. 5(c) and 5(d). The shapes of the profiles are nearly identical. Figure 6 shows the results for all 16 transient simulations of the US06 drive cycle. The maximum temperature in these simulations was found to be 146°C.

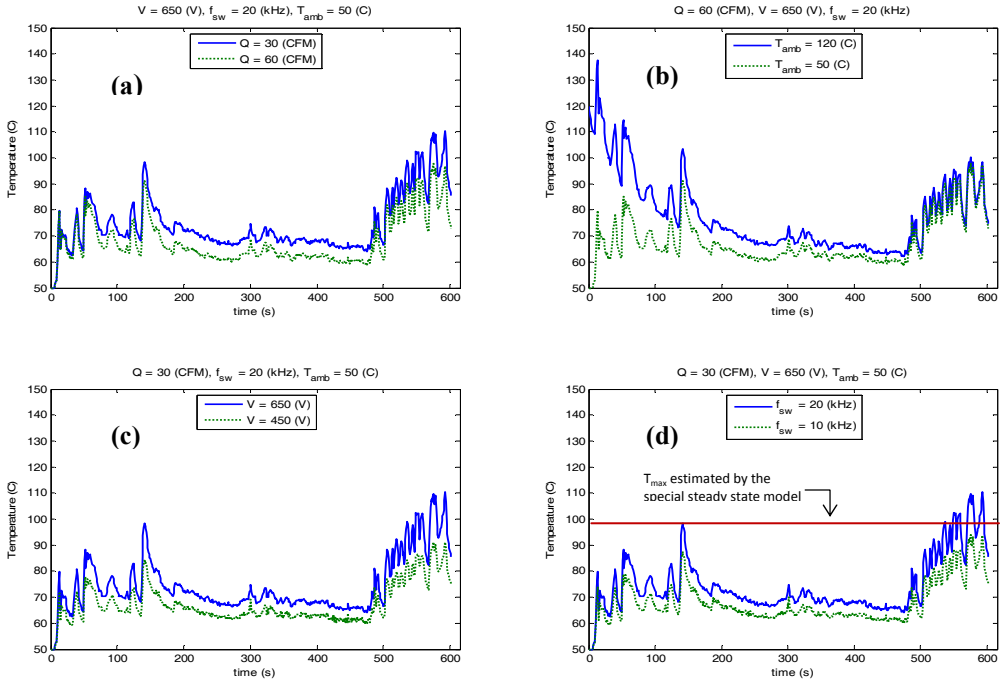

Fig. 5. Transient results showing the effect of changing Q, T_{amb}, V, and f_{sw}.

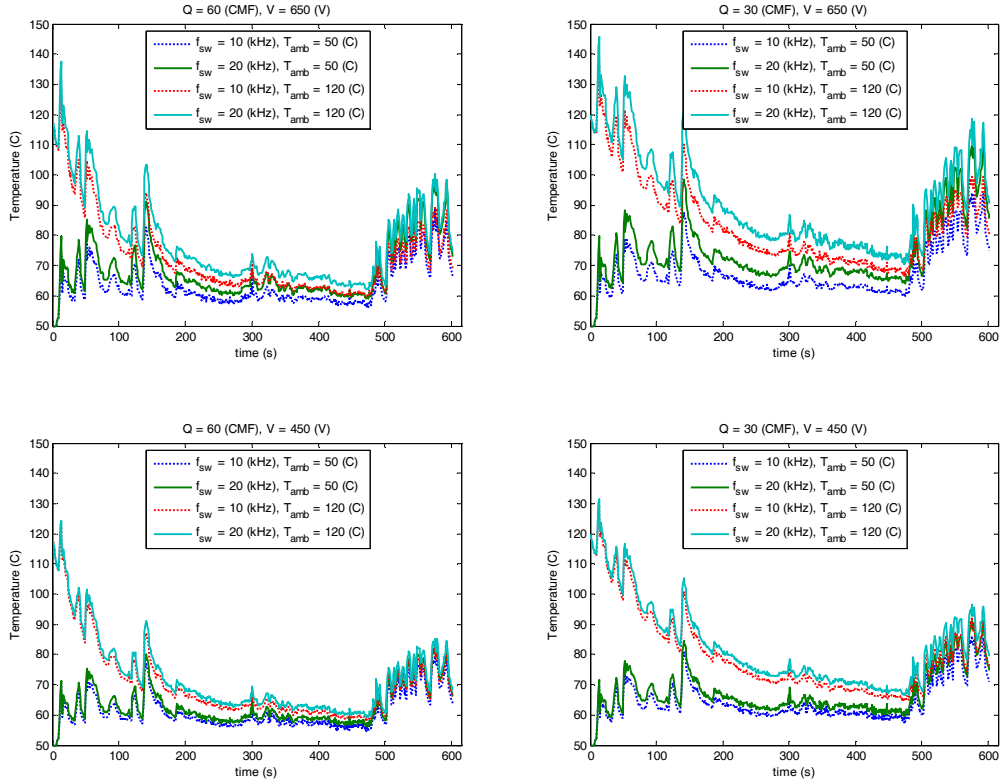

Fig. 6. Plot of all 16 transient simulations of the US06 drive cycle for design B.

From Table 6, which compares the performance of the two inverter designs, we note that (1) the power density ratios for these air-cooled inverters are comparable to those of liquid-cooled systems, (2) both the

pressure drop and the blower power requirements are lower for the lower flow rate and they increase as the square of the flow rate, and (3) the pressure drop and blower power values for design A are about 3 times those for design B.

Table 6. Comparison of the Performance of the Two Inverter Design Packages

Characteristic	Design A	Design B
Power density (kW/L)	12.4	12.01
Pressure drop (in. H_2O) at 30 CFM	1.3	0.436
Pressure drop (in. H_2O) at 60 CFM	5.0	1.64
Ideal blower power (W) at 30 CFM	40.3	13.9
Ideal blower power (W) at 60 CFM	312	104.5

4. Special Steady State Model to Verify Transient Results

Because the overall energy balances for the transient simulations could not be directly evaluated, a check case for the transient simulation results was conceived and implemented. The check case is a special steady state simulation for estimating Tj of all the devices. For this model, the current distribution of the US06 drive cycle, shown in Fig. 7, may be taken to have three distinct patterns: (1) a relatively higher level of current in the beginning up to about 192 s, (2) a lower level of current from 192 s up to a time of 482 s, and, finally, (3) a third higher level of current. An integrated average value of current is computed for the three time intervals, and the results are shown in Table 7 and by the red lines in Fig. 7. The highest of the three currents, 82.45 A, is used in the special steady state model under the most severe of the operational parameters, keeping Tinlet = Tamb = 50°C. The resulting junction temperatures are determined for both designs and compared to those resulting from the full cycle transient simulation (Table 8). As indicated in Table 8, the total power dissipated in this special model is higher than that dissipated over the entire US06 drive cycle.

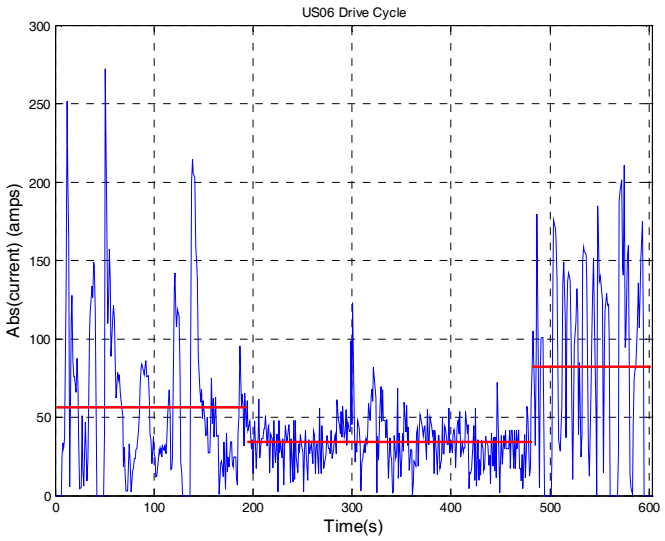

Fig. 7. Current distribution from the US06 drive cycle.

Each of the red lines (Fig. 7) represents the integrated average value over the time interval as shown. Each red level represents the effective steady state current that matches the power dissipation of the time dependent current in the particular time interval.

Table 7. Time-Averaged Values of Current for the Three Time Intervals of the US06 Drive Cycle

	Time Interval in the US06 Drive Cycle		
	1–194 s	194–482 s	482–602 s
Integrated average current (A) through inverter	56.31	34.19	82.45

Table 8. Comparison of Junction Temperature for Three Models[a]

Inverter	Ambient Temperature (°C)	Steady state		US06 drive cycle simple steady state model		Full transient US06 drive cycle
		Current (A)	Tj (°C)	Current (A)	Tj (°C)	Tj (°C)
Design A	50	240	> 274[b]	82.45	123.5	142
Design B	50	240	> 252[c]	82.45	97.8	111

[a]The three models compared in this table are (1) steady state simulation; (2) special steady state simulation; and (3) full transient simulation of the two inverter designs for the most demanding of the parametric cases with V = 650 V, f_{sw} = 20 kHz, Q = 30 CFM, and T_{inlet} = 50°C.

[b]The value for Q = 50 CFM. At Q = 30 CFM, expect Tj > 274°C.

[c]The value for Q = 40 CFM. At Q = 30 CFM, expect Tj > 252°C.

With a current of 240 A, the steady state simulations result in very high Tjs for all cases considered in this study (Tables 1 and 4). However, those temperatures are useful in establishing the upper limit on Tj that the device can reach. In reality, however, the current level will not be constant at 240 A but will be a time dependent function like the US06 drive cycle shown in Fig. 7. For this case the results are compared in Figs. 3(d) and 5(d) for both the inverter designs, design A and design B respectively. The Tj values from the transient simulations are lower than that predicted by the special steady state simulation for the first 550 s of cycle and exceed the predicted value during the final 50 s of the cycle, so the transient results can be considered to be realistic.

Conclusion

In this study two different inverter thermal packages, incorporating new concepts of thermal packaging, were designed, and their thermal performance was evaluated. Full 3-D turbulent-thermal-fluid models were developed. Further, device power dissipation at the individual chip level as a function of Tj, voltage, and current and f_{sw} is included in the models. These effects are included for both the steady state and transient models of the final designs. From the results presented and discussed, the following conclusions may be drawn.

1. For the steady state models with a current of 240 A, Tjs are very high.

2. For the transient models with US06 drive cycle,
   a. Tjs, compared to corresponding steady state models, are lower by about 100°C,
   b. for T_{amb} = 50°C, the highest Tjs occur toward the end of the cycle, and
   c. for T_{amb} = 120°C and T_{inlet} = 50°C, the highest Tjs occur early in the cycle and decrease significantly with decreasing current as a function of time. In the final 50 s of the cycle, Tjs increase to a level below the highest values. The end-of-cycle values of Tj are comparable to those of the case in 2b (above).
3. A special steady state model was developed to validate and provide a means to estimate the expected Tjs from the transient simulations. The results of this simplified model confirmed that the transient model predictions of Tjs are reasonable. As transient simulations require significantly higher computational resources and computational time, this simplified model may be used to estimate Tjs for other drive cycles.

2.8. Power Device Packaging

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Objectives

- Identify the limitations and shortcomings with existing device packaging approaches.
- Develop new packaging concepts to overcome the issues for improved power density, thermal management, cost, and reliability.
- Complement other packaging and thermal management research efforts within the Vehicle Technologies Program (VTP).

Approach

1. Benchmark through analysis and simulation selected state-of-the-art (SOA) commercial device packages. This involves
    1. selecting the SOA commercial packages, such as Toyota's and Semikron's, and
    2. analyzing the selected packages, including module packaging and cooling.
2. Identify underpinning issues with existing packaging.
3. Based on the results of benchmarking, determine why the available technologies are not sufficient to achieve the desired target. (This task focuses on key contributor identification.)
4. Develop and benchmark promising new packaging concepts and technologies through survey, analysis, and simulation.
5. Select and develop candidate technologies.
6. Prepare a summary report that includes evaluation results (incorporate into the annual VTP report).

Major Accomplishments

- Analyzed and summarized the advantages and disadvantages of SOA automotive power modules.
- Benchmarked existing packages by sectioning and constituent characterization of automotive inverter insulated gate bipolar transistor (IGBT) modules.
- Developed a new package concept and performed electrical properties and thermal performance simulations.
- Performed evaluation and down selection of packaging technologies (materials and processes), including die attach, substrate, insulation, and mechanical support.
- Extended the critical in-house packaging capability through integration of on-site packaging facilities.

Future Direction

Develop advanced power module packaging technologies aiming at the following.

- improved electrical performance;

- reliable high temperature operation;
- efficient thermal management (and cooling capability); and
- economic manufacturability;

by

  - packaging structure optimization,
  - material exploration, and
  - processing techniques innovation.

Technical Discussion

1. Introduction

Power semiconductor devices, IGBTs, metal-oxide semiconductor field-effect transistors, and diodes fulfill the role of switching electric power through their fast turn-on and turn-off in tens of kilohertzes in power electronic conversion systems such as motor drives. The core element of these power switches is a small semiconductor die with a dimension of, for example, 10 mm × 10 mm × 0.3mm with rated current/voltage at hundreds of amperes (A) and hundreds of volts (V) for silicon (Si) IGBTs. To facilitate high power conversion configurations such as half or full bridge, three phase, matrix, etc., power modules are constructed by electrically interconnecting multiple dies and then encapsulating to form the building blocks for power conversion systems (converters and inverters). The process from multiple bare semiconductor dies to a module has been called power device/module packaging, as illustrated in Fig. 1(a).

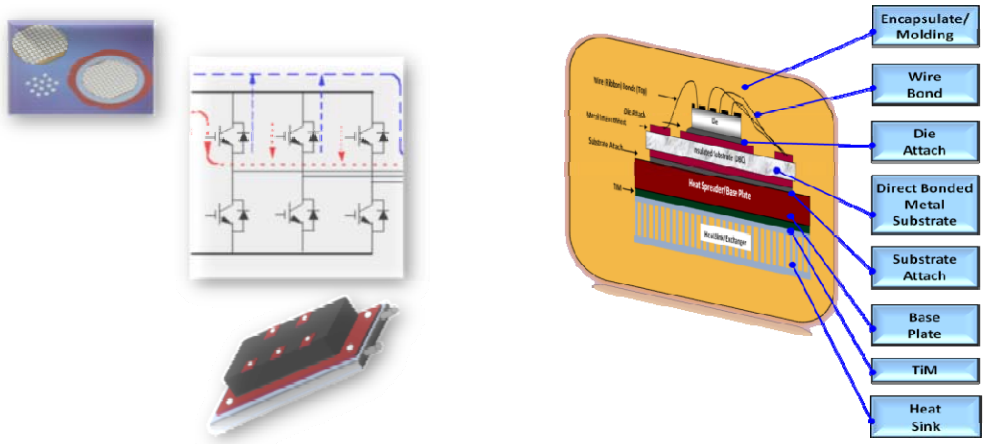


Fig. 1. Power module packaging: (a) from multiple semiconductor chips (dies) to a power electronics building block (not in scale); (b) typical power module packaging structure (inside).

During operation, the dies generate relatively large amounts of heat (on the order of hundreds of watts per die), leading to temperature increases. Semiconductor devices and the associated packaging materials ultimately dictate the inherent temperature limitations. For example, the maximum operation temperature of Si devices is 150°C to 200°C [1], depending on the voltage rating. So refined cooling measures must be taken to control the die's temperature, which leads to strict requirements for a module's thermal performance. In addition, another main function of the module structure is to supply mechanical support for operation under heavy vibration conditions and in harsh environments.

The characterization of power modules' packaging includes specific parameters; for example, thermal resistance, electrically parasitic inductance/resistance, power density, and thermal/power cycling number

to failure. All these performance parameters are related mainly to the physical structure and material properties of the power module assembly. These factors, plus associated packaging process technologies, determine the overall cost of the power modules and systems.

To meet these requirements, hybrid packaging technology has been used with diverse materials and process techniques. Figure 1(b) illustrates a conventional wire-bond packaging structure. The bonding wire and solder are used to connect the electrodes on the top and bottom of the die onto the etched circuit of the direct bonded copper (DBC) substrate, which comprises of copper (Cu) bonded with an electrically insulative ceramic plate sandwiched between double side Cu layers. The power and signal input/output are accomplished through soldered Cu terminals on the DBC substrate. This assembly is then soldered onto a flat Cu baseplate and encapsulated in a plastic housing with an electrically insulative polymer (silicone gel) to provide mechanical support, electrical isolation, and protection. This module will then be bolted onto a heat sink or cooler with thermal paste (thermal interface material or TIM) in between to reduce the contact thermal resistance. The module may also be bolted onto a bus bar for a higher level electrical connection.

2. Benchmarking Automotive Power Modules

Advances in power module packaging have been a direct result of modifications to this basic structure. Table 1 gives a few examples of SOA automotive power modules with the results of our analyses. It can be seen that many concepts have been pursued in the quest for improvements in packaging structure, materials, and techniques.

The module in the Toyota LS 600 [2] consists of many packaged switch units based on paralleled IGBT and diode die. These dies are interconnected by direct soldering onto planar electrodes. The dies have solderable front surface metallization (FSM) supplied by Fuji Semiconductor [3]. These switch units are sandwiched between minicoolers with bare silicon nitride, electrically insulative ceramic slices between cooler and electrodes to exploit the thermal advantages of double sided-cooling. However, the double sided thermal grease layers with each ceramic insulator add thermal resistance to each thermal path, negating the positive effects of double sided cooling. In addition, a pressure mechanism must be continually applied to ensure the press contact of all package units and minicoolers. A complicated bus bar is needed for electrical connection of these units. This complex assembly is costly.

In the Prius III (2010), Toyota uses an integrated cooler structure [4] in which the DBA (direct bonded aluminum) substrates are directly bonded (by brazing) onto a specially fabricated cold plate. Compared to the standard module structure, it eliminates the need for a baseplate and TIM layer. It is estimated this construction achieves a 30% improvement in thermal performance. However, to release the stresses between the cooler and DBA due to the coefficient of thermal expansion (CTE) mismatch, a buffer plate with punched holes was inserted. This addition results in processing complexity and worsens the thermal conduction.

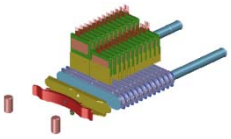
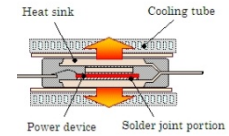
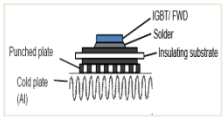
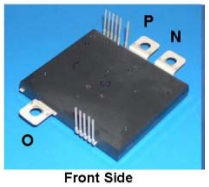
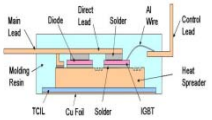
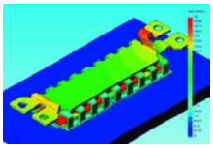
Infineon, a leading power semiconductor manufacturer, has developed power modules for automotive applications [5]. Their Hybidpack2 features a direct-cooled Cu baseplate with pin fins, eliminating the TIM layer and reducing the thermal resistance. In this structure the Cu pin fins baseplate is difficult to manufacture. The O-ring sealing between baseplate and coolant channel is an issue.

Mitsubishi, another major power semiconductor manufacturer, supplied a TPM (transfer-molded power module) [6] for the Honda Insight and other hybrid vehicles. It is a phase leg package and needs further assembly to form inverter modules. It eliminates the DBC substrate and instead uses a thermal conductive insulation layer (TCIL) sandwiched in between two Cu plates as an insulator and bonder. Double sided planar interconnection has been used by soldering Cu leads on the IGBT/diode dies. Again the dies have

solderable FSM. It reduces parasitic electrical resistance (compared to wire bond top interconnection). The disadvantage of this packaging includes poor thermal conductivity of the TCIL layer, and assembly from phase leg package to module requires double layers of TIM. This will worsen the thermal performance.

Semikron, a power module packaging developer, produced their SKiM modules [7], in which the baseplates are eliminated. Press contacts provide both the terminal electrical connection to pads on the DBC and the DBC to heat sink. More remarkably, sintered silver (Ag) has been used for the die attach bonding material, replacing widely used solders. This significantly increases the reliability of the power module thermal cycling; however, the mechanical integrity of the assembly and TIM layer uniformity remain concerns.

Table 1. Features of State-of-the-Art Automotive Power Modules

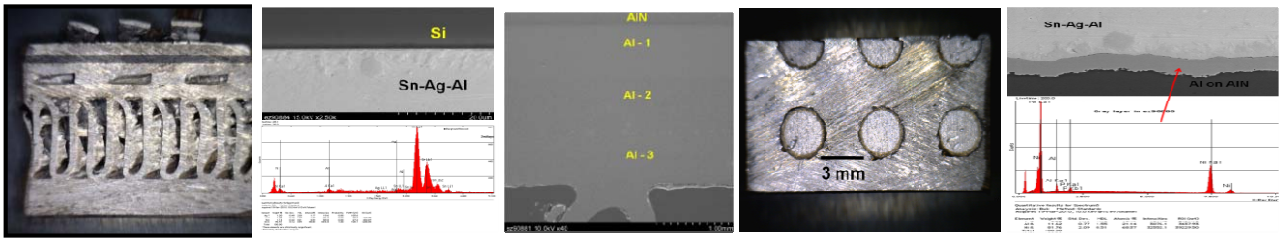
	Toyota LS600 [2]	Toyota Prius III [4]	Infineon Hybridpack2 [5]	Mitsubishi TPM [6]	Semikron SKiM [7]
Module	 	 		 Front Side 	 
Advantage	• Double sided planar interconnection; • No baseplate; • Double sided cooling	• Direct bond cooler • No baseplate • No TIM layer • Al Ribbon bond	• Direct cooled baseplate • No TIM layer • Integrated cooler	• No DBC substrate • Phase leg unit • Direct planar lead bond	• No baseplate • Press contact • Ag sintered die attach
Disadvantage	• Complex inverter (electrical and thermal) assembly • Ceramic slice insulation and double TIM layers	• Stress relax buffer layer worsens thermal conductivity • Large electrical parasitic parameters	• Difficulty in pin fin manufacture • Large electrical parasitic parameters • Difficult integration of cooler	• Double TIM layers • Poor thermal of TCIL • Module level assembly needed	• Mechanical integrity concern • Large electrical parasitic parameters • Poor TIM layer uniformity

To further understand the details of these modules, advanced microstructure chemical analyses (energy dispersive spectroscopy, elemental mapping, etc.) and scanning electron microscopy technologies have been used. Figures 2–5 present some examples of the microstructural and chemical analysis results. Figure 2(a) shows the package in the Toyota LS 600 module, and Fig. 2(b) is a cross-sectional view of a double sided planar interconnection and paralleled IGBT and diode die. Figure 2(c) shows the die attach structure at a high magnification, where a Cu shim and dimples (for stress release) can be seen. Figure 3 shows the Toyota Prius III module's microstructure. The cross section is shown in Fig. 3(a). It is a complete integrated stack from semiconductor die to cooler configuration. Figure 3(b) presents the chemical constituents of the die attach solder layer, which is clearly lead free. Figure 3(c) features a highly magnified portion of the multilayer aluminum (Al) construction, including the directly bonded

interface between the DBA and laminated cooler. Al-2 is a machined Al slice with punched holes, as shown in Fig. 3(d), which is designed to promote passive stress relaxation within the structure. Figure 3(e) shows the chemical composition of finishing metallization on the DBA substrate, which must be metallurgically compatible to solder. Figure 4 shows the Mitsubishi TPM module's microstructure. The IGBT and diode dies are directly attached onto a thick (3 mm) Cu plate with multiple dimples for stress release, as shown in Fig. 4(a). Figure 4(b) presents the cross-sectional view of the die attach solder layer, where voids can be clearly observed. Figures 4(c) and 4(d) are the microscopic view of the molding compound and TCIL, respectively. The TCIL's measured thermal expansion property is illustrated in Fig. 4(e), where the nonlinear behavior can be observed. Figure 5 shows the metallurgical details of die attach in the Semikron SKiM module. The sintered Ag layer for bonding includes Al, Mg, Si, and oxygen additives. After sintering, there is a transition zone from die bottom metallization to the Ag layer in which the constitution elements, including titanium, nickel, Al and Ag, are gradually changed. The same analysis has also been performed on the Ag to substrate interface.

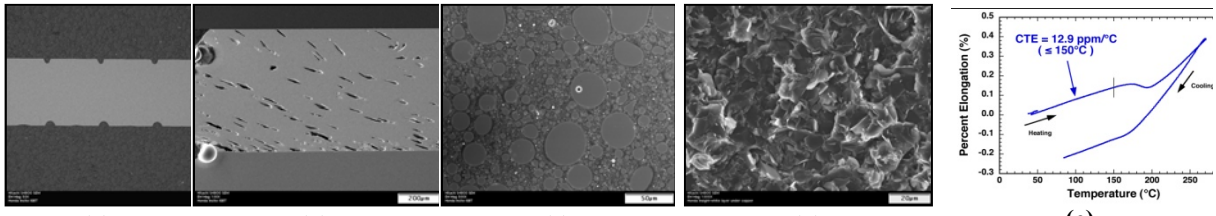
(a) (b) (c)

Fig. 2. Toyota LS600 module planar inteerconnection structure: (a) unit package, (b) cross-sectional view, and (c) shim and dimples.



(a) (b) (c) (d) (e)

Fig. 3. Toyota Prius III module microstructure: (a) cross section, (b) solder elements, (c)multiple Al plate stack, (d) stress release holes, and (e) metallization finish on DBA substrate.



(a) (b) (c) (d) (e)

Fig. 4. Honda Insight (Mitsubishi TPM) microstructure: (a) dimple in heat spreader, (b) voids in solder layer, (c) molding component, (d) TCIL, and (e) thermal expansion of molding

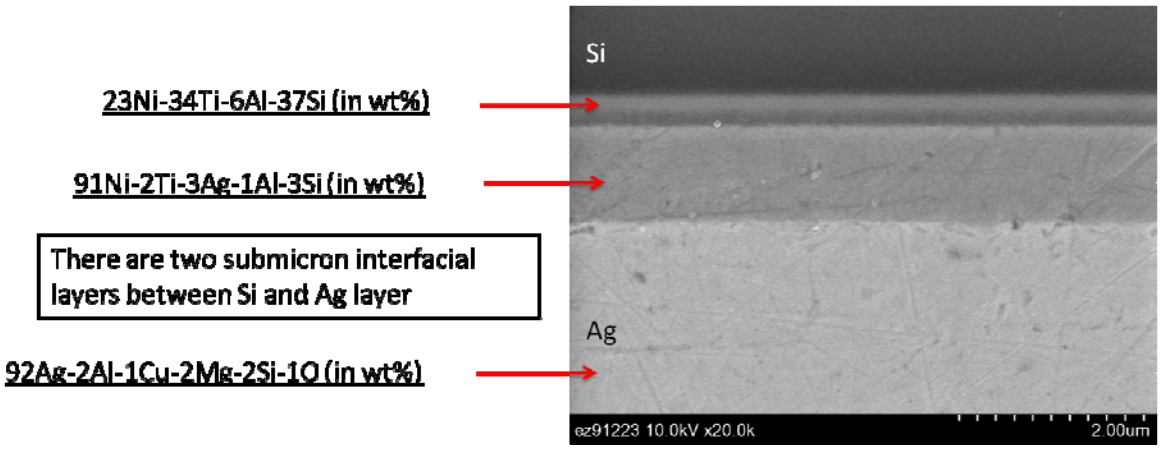


Fig. 5. Semikron SKiM die attach metallurgical scheme.

The parasitic electric parameters (inductance and resistance) with specific packaging electrical interconnection configurations are important characteristics of a module's packaging. They can be obtained by electromagnetic simulation of the packaging structure. Figure 6 shows the simulation results for the module in the 2007 Toyota Camry Hybrid. The electrical interconnection consists of bond wires and Cu traces on the DBC substrate, as illustrated in Fig. 6(a). The extracted electric circuit parameters are depicted in Fig. 6(b). The larger these parameters are, the greater the negative impact on system operations.

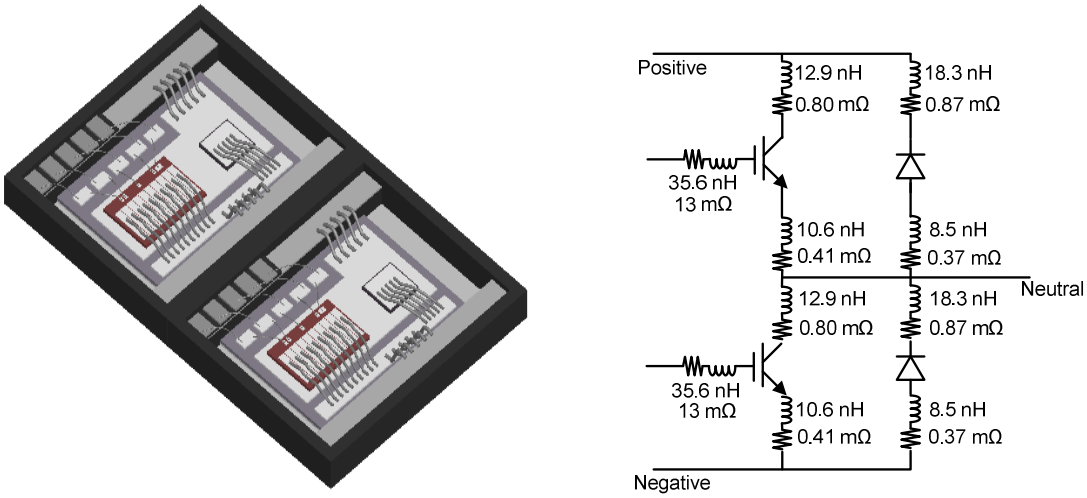


Fig. 6. The electrical parasitic parameters extraction of the 2007 Toyota Camry module: (a) electrical interconnections and (b) parasitic parameters in the converter circuit.

3. New Power Module Packaging Concept

As indicated in the previous section, the automotive power electronics module has undergone intensive development. Each one of these diverse products offers incremental improvements to the baseline, conventional automotive electronics module through different packaging technologies. However, none of them offers comprehensive features that are optimized for all aspects of performance, reliability, and cost effectiveness. To meet targets for advanced automotive power electronics, a more integrated design scheme should be pursued. In FY 2010, we developed a module concept that features (1) easy inverter/converter integration, (2) ultralow thermal resistance, (3) ultralow electrically parasitic parameters, and (4) low manufacturing costs.

The following are the electrical parameters associated with the major commute loops of the ORNL concept packaging module in comparison to the module in the 2007 Toyota Camry Hybrid.

- Parasitic inductance for the ORNL module is 12.8 nH vs 50.3 nH for the Camry module.
- Parasitic resistance is 0.22 mΩ (ORNL) vs 2.35 mΩ (Toyota).

There is a much greater reduction in parasitic inductance and resistance compared to Toyota's wire bonded module because of the special interconnection used in the ORNL design. The smaller electrical parasitic parameters will not just improve the conversion efficiency of the system, but also can reduce use of the semiconductor die, the most costly part in the module, through reduction in both voltage and current rate.

The semiconductor cost can be further reduced through decreasing the thermal resistance of the packaging stack while maintaining the use of the same cooling capability. We have designed two different integration schemes between substrate and cooler. The finite element analysis thermal simulation results demonstrate that 60% improvement of thermal performance can be achieved.

Increasing the operational temperature of semiconductor dies in modules is a promising approach to reduce the power electronics system cost further. Currently, the IGBT and diode are rated for continuous operation at 125°C. Recently this temperature has been increased to 170–200°C for Si switches. Wide

bandgap semiconductor [e.g., silicon carbide (SiC), and gallium nitride (GaN)] switches offer higher temperature capability (>300°C). This advance has thus transferred the challenge to the power device/module packaging because the ambient temperature and temperature excursions are two major sources of module failure. It is well known that different thermal expansion rates of adjacently bonded parts cause fatigue and cracking into the bonding layer because of material CTE mismatches. A successful power module packaging design must consider matching (or minimizing the differences) of all material CTEs. Figure 7 illustrates the thermal properties (thermal conductivity and CTE) of conventional power module packaging materials.

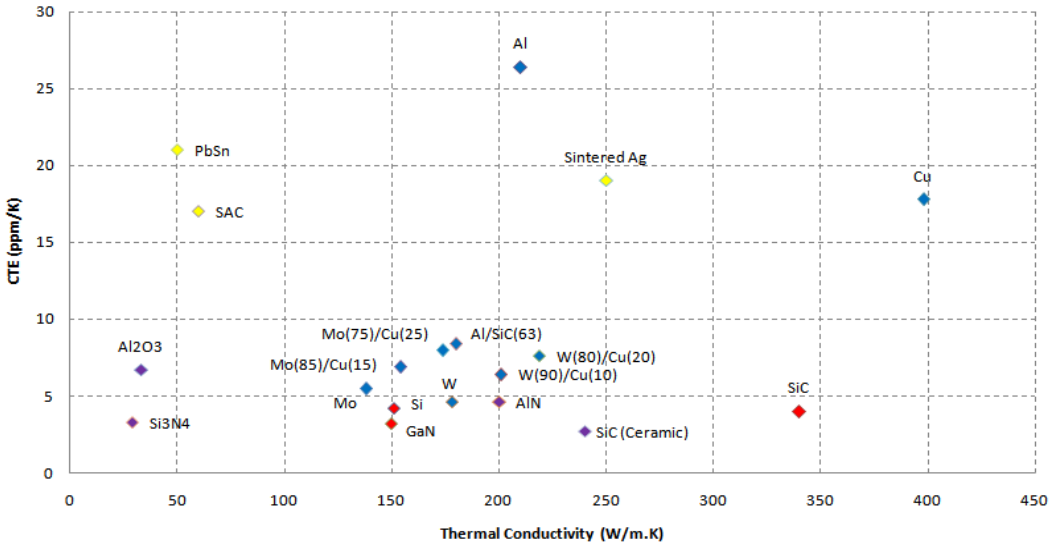


Fig. 7. Thermal properties of power module packaging materials.

The CTE values of Si, SiC, and GaN are in the range of 3.2–4.2 × 10^{-6}/K (or ppm/K). Ceramic materials such as alumina (Al_2O_3), aluminum nitride (AlN), and silicon nitride (Si_3N_4) are used as insulation substrates where the substrate's apparent CTE ranges from 3.3 to 6.7 ppm/K, values close to those of the candidate semiconductors. However, most metals used as electric conductors and/or bonding media possess much higher CTEs; for example, Cu (17.8 ppm/K), Al (26.4 ppm/K), and solder (17–21 ppm/K). There are two ways to deal with CTE mismatch problems. One is to optimize the structure to release or minimize the thermal stress, such as in the Prius III, TPM, etc. Another is to use advanced materials with CTEs closer to the die's such as aluminum silicon carbide, AlSiC, (8.4 ppm/K); MoCu (6.9 ppm/K); and MoW (7.0 ppm/K), especially for high temperature modules.

4. Development of the Silver Sintering Die Attach Technique

Solder and soldering have been widely used for die attach and substrate attach. For automotive applications, the formed joint must withstand large stresses and strains under high power/thermal cycling operating conditions. To meet this high reliability requirement, the Ag sintering joining technique is undergoing scrutiny in-house. Figure 8 shows the experiment equipment and initial samples we have made. A small-scale model sintering facility with local heater and pressure control has been fabricated [Fig. 8(a)]. The heater and piston for pressure application and a sintered bulk Ag disk produced in the facility are shown in Fig. 8(b). The disk is ready for material property examination including modulus of elasticity, CTE, and thermal conductivity as a function of porosity and temperature. These parameters are related to the processing temperature profile and pressure applied; a typical example is shown in Fig. 8(c). Based on the bonding mechanism of Ag sintering, the surface finish metallization plays an important role. Various metallurgical schemes have been studied. The silver pastes from different vendors have been

examined. Figure 8(d) shows a furnace acquired for future module level Ag sintering processing, which will be located in the ORNL Power Electronics Packaging Laboratory.

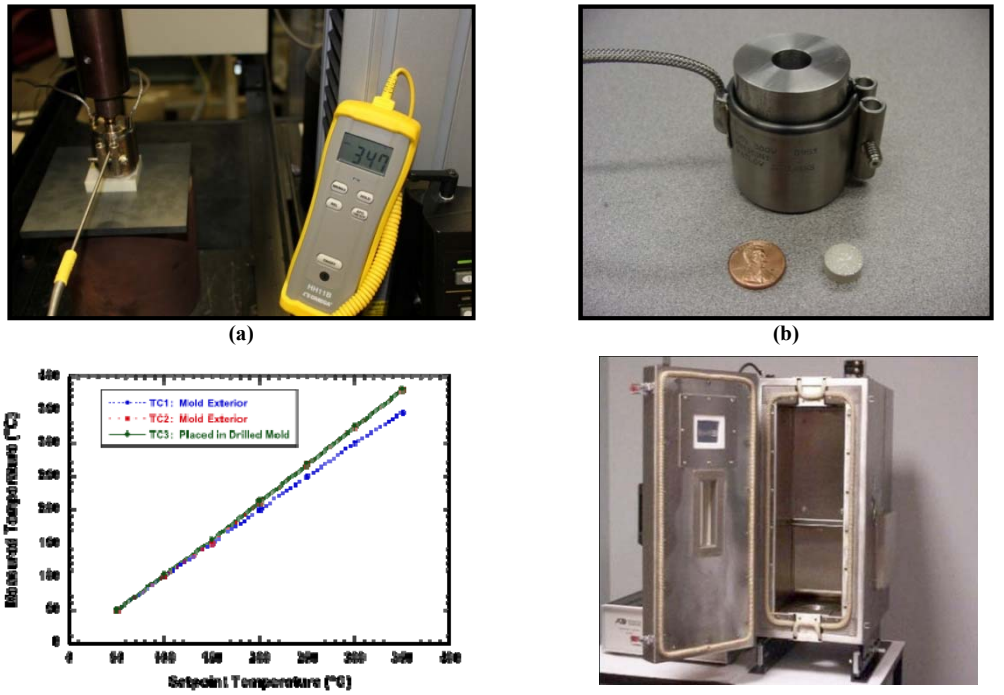


Fig. 8. Silver sintering technology development for die and substrate attach: (a) ORNL model sintering facility, (b) fixture and sintered silver disk, (c) temperature validation, and (d) furnace for module-level fabrication.

5. Integration of Power Electronics Packaging Laboratory

Power module packaging manufacturing is a combination of several hybrid processes, as indicated in Fig.1. To extend ORNL's research capabilities in power modules and power electronics systems, we designed and acquired a suite of equipment for different packaging processes: clean storage/operation station (N_2 purged desiccators cabinet, laminar flow ESD clean bench), chemical processing station (fume hood, etching bath, ultrasonic cleaning, electro-, electro-less plating machine), pattern and selective deposit (spin coating machine, ultraviolet exposure, paste screen/stencil printer), die/substrate attach (vacuum reflow furnace, dual heating reflow oven, pressure-assisted sintering oven), wire bond (thick wire/ribbon bonder), encapsulation (dispensing machine, de-air pump, curing oven), process qualification (microscopic observation, probe station, and curve tracer), and environment chamber (thermal shock and thermal cycling ovens). A dedicated laboratory has been built to facilitate module packaging processing. Figure 9 illustrates the layout in this laboratory with pictures of the major equipment.

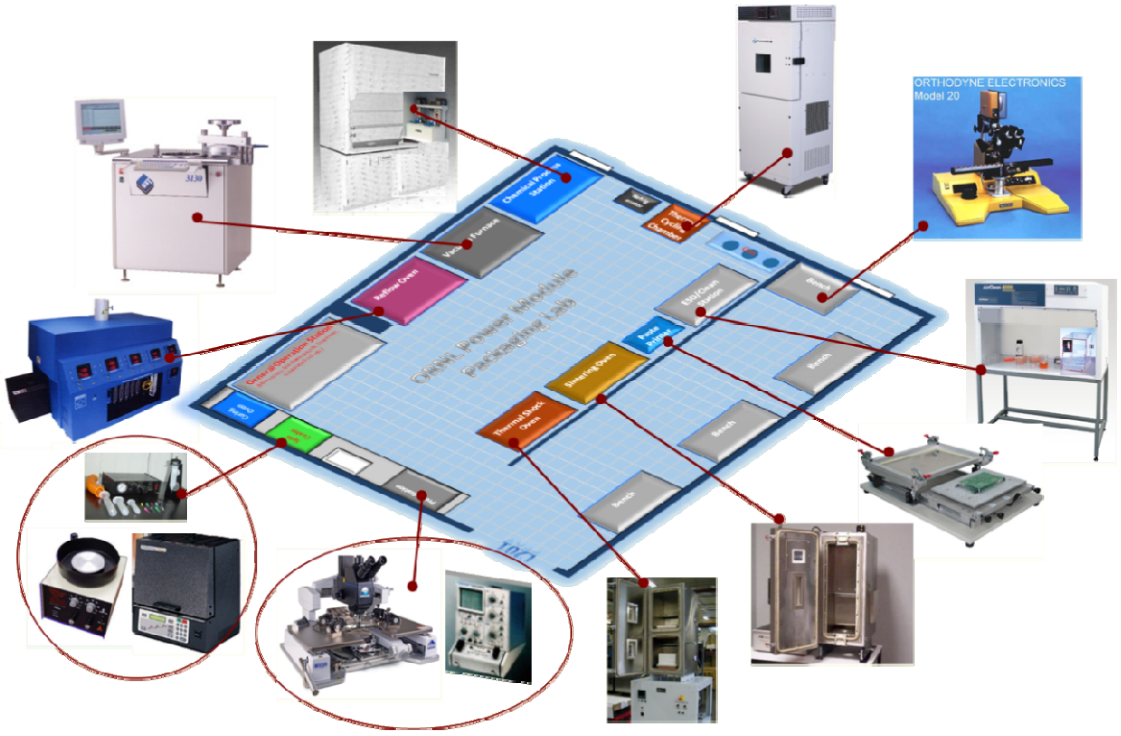


Fig. 9. Power module packaging process facilities and layout in a specially built laboratory.

Conclusion

In FY 2010 we launched the power device/module packaging project. Typical existing advanced automotive power modules and their packaging technologies have been examined. The packaging structures, materials, and technologies and their effects on power module performance, reliability, and cost have been analyzed. Based upon these benchmarked results and interpretations, we proposed an innovative power module structure with high power conversion efficiency and cost effectiveness. To realize successful high operational temperatures, some new processing technologies have been explored in-house. In addition, a complete Power Electronics Packaging Laboratory has been designed and constructed. It will become a prestigious platform to enhance the projects within the VTP program. All these accomplishments provide a solid foundation for next year's objectives.

Publications

1. Zhenxian Liang, *ORNL Advanced Power Electronics Packaging Laboratory*, presentation at DOE FreedomCar EETT conference, Aug. 26, 2010.
2. Andy Wereszczak, *Packaging Characterization: Power Module Tear-Down*, presentation at DOE FreedomCar EETT conference, May 27, 2010.

References

1. Cyril Buttay, et al., "State of the art of high temperature power electronics," *Microtherm,* hal-00413349, version 1–3, September 2009.
2. Yasuyuki Sakai, Hiroshi Ishiyama, and Takaji Kikuchi, "Power Control Unit for High Power Hybrid System," in *Proceedings of the 2007 SAE International Conference,* p. 2007-01-0271.

3. Seiji Momota, et al., "Plated chip for hybrid vehicles," *Fuji Electric Review,* Vol. 54, No. 2, 2008, p. 49.
4. Natsuki Nozawa, et al., "Development of Power Control Unit for Compact-Class Vehicle," in *Proceedings of the 2009 SAE International Conference,* p. 2009-01-1310.
5. Sayeed Ahmed, "Putting the electrical power in hybrid powertrains," *Auto Electronics,* May/June 2007, p. 22.
6. T. Ueda, et al.; "Simple, compact, robust and high-performance power module T-PM (transfer-molded power module)," The 22nd IEEE International Symposium on Power Semiconductor Devices & ICs (ISPSD), 2010, pp. 47–50;
7. Arendt Wintrich, "Power modules for electric and hybrid vehicles," *Bodo´s Power Systems,* February 2009, p. 24.

Patents

1. Invention Disclosure: Zhenxian Liang, Laura Marlino, Fred Wang, and Puqi Ning, *Power Module Packaging with Double Sided Planar Interconnection and H/E*, ID NUMBER: 201002429 DOE-S Number: S-115,481.

2.9 Development, Test and Demonstration of a Cost- Effective, Compact, Light-Weight, and Scalable High Temperature Inverter for HEVs, PHEVs, and FCVs

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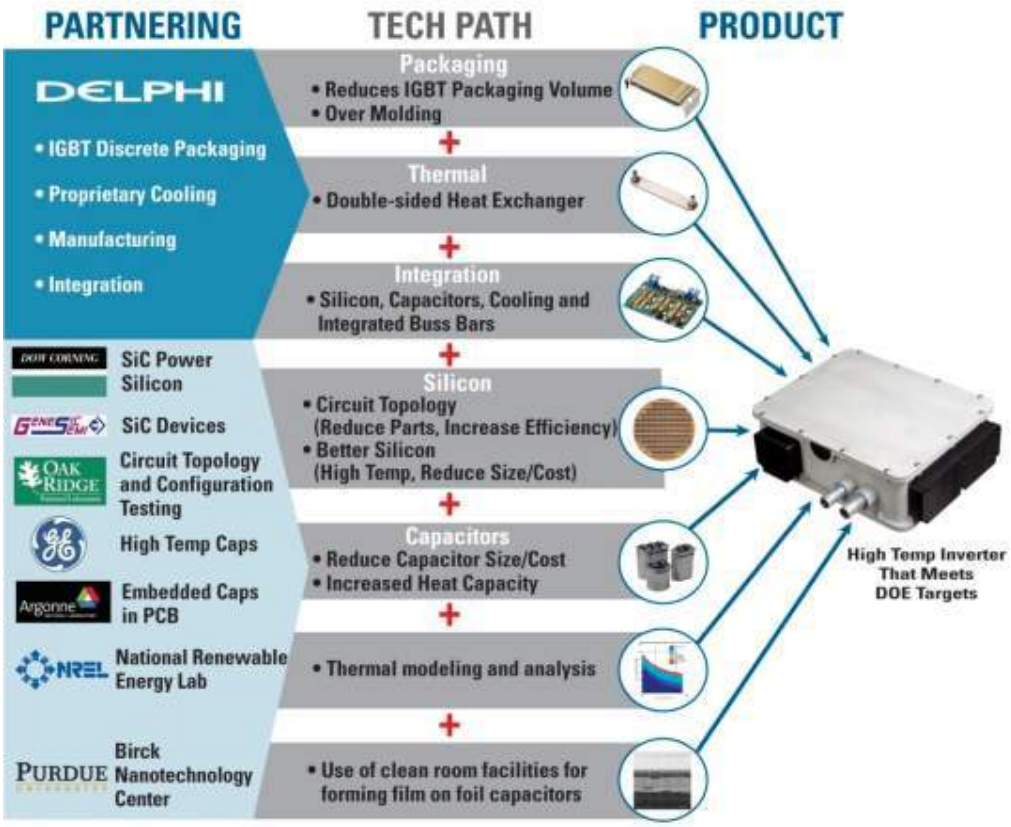
Objectives

- Design Build and Test Selected Concepts
  - Design, procure, build and test selected concepts for discrete power switches, DC buss capacitors, heavy copper laminate PCB, high efficiency cooling subsystem, and mechanical packaging. Hold internal review of bench-level testing results with technical team and Delphi management to evaluate compliance to DOE requirements. Incorporate lessons learned and include in improvements in Task 6.

Approach

- Work with our partners to develop the technologies required for DC bus capacitors, power silicon, packaging, thermal management, and integration.



Major Accomplishments: Film Capacitors (GE)

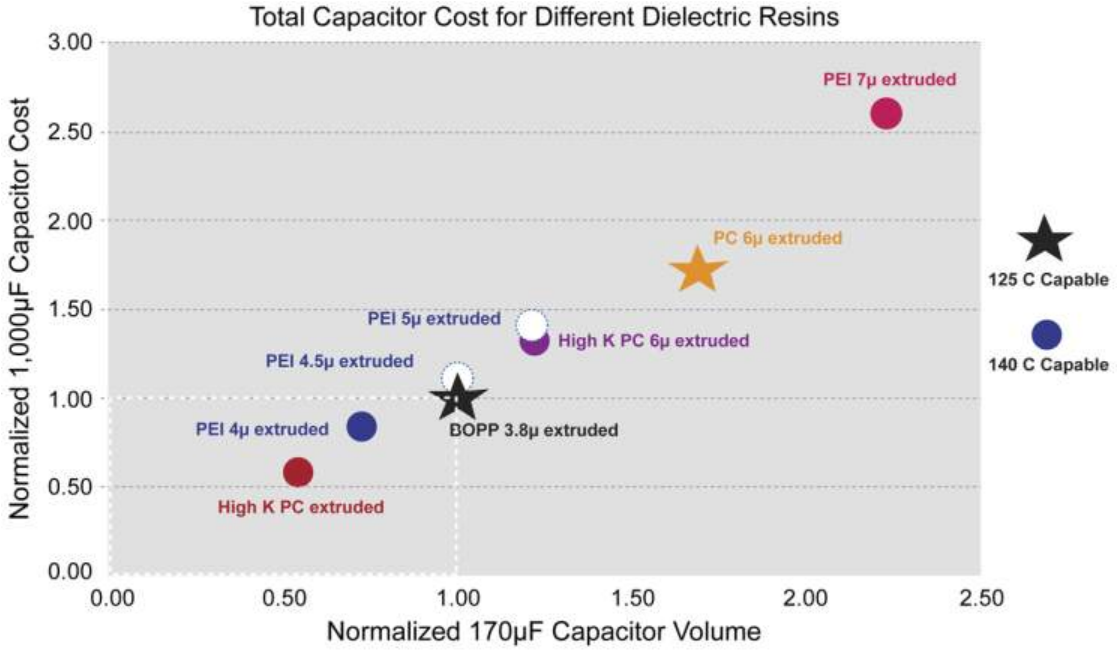
- Various resins (PEI, PPS, PC) were identified as high temperature dielectrics for capacitors.
- Extrudable PEI and high-Dk PC showed the most promise:
  - PEI film: Tg = 217°C, D_k = 3.2, Df = 0.1%, 550-600V/m,
  - Experimental PC Tg = 172°C; D_k at RT, 1kHz = 4.0; Df < 0.3%; BDS = 663 V/μm
  - A cost vs. volume model was derived to compare the different film technologies.
  - Team proposes use of 5 μm thick extruded PEI film to build the 1,000 μF prototype capacitors for inverters.
  - A batch of 5 μm thick extruded PEI film was qualified and metallized, and has been turned into 1 μF and 25 μF POC capacitors.
    - 25 μF caps are being considered as the individual modules that could be used to build the 1,000 μF prototype caps.
    - The 1 μF and 25 μF 5 μm thick extruded PEI caps are currently being tested by Delphi; initial results have been shared with GE
  - The high-Dk PC extruded film, while promising, requires more time to develop and will not be available in time for building the prototype capacitors required this program.
    - Sample 1 μF caps have made with 5 μm thick film created by a solvent cast process and are currently being tested

Future Direction

- For FY11, we are planning on using an array of 5 μm thick extruded PEI film capacitors to form the bulk capacitor for the inverter deliverable. It should be noted that the 5 μm thick extruded PEI film will be larger than baseline equivalent polypropylene capacitor; however, the 5 μm thick extruded PEI film will be higher temperature capable and will validate the model, when comparing size and cost to the baseline equivalent polypropylene capacitor.

Technical Discussion

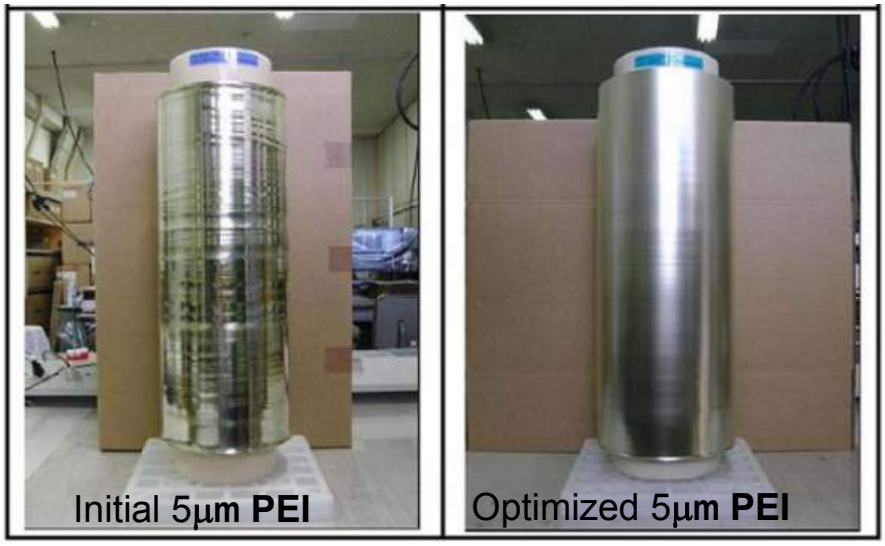
- The graph below summarizes the potential capability of different dielectric resins compared to today's baseline biaxially-oriented polypropylene (BOPP) film capacitors.



- For this graphical comparison, the ***processing cost per unit volume of capacitor module was kept constant***, the same as that for the BOPP, although it may be different for resins other than BOPP, especially in those cases in which the raw material cost or the processing cost to make the film by extrusion, or both, are substantially higher than the values assumed for BOPP.

- Also, the ***cost to make the High Dk 4 μm extruded polycarbonate polymer commercially was estimated based on the information presently available***, and it will strongly depend on the cost to make the monomer required to build the polycarbonate molecule and the final volume of resin produced, which are both unknown at this point in time.

The pictures below illustrate the progress made in the extrusion process for the 5 μm PEI film.



Major Accomplishments: Film-on-Foil Capacitors (Argonne National Laboratory)

- Transferred process as it exists today to a clean room facility at the Birck Nanotechnology Center (BNC)/Purdue University
- Less variation in dielectric properties observed on samples made in clean room
- Added process controls (inspection of substrate before & after each process step)
- Moved away from polished nickel substrate to metalized silicon wafers and demonstrated good breakdown fields
- Fabricated physically larger size capacitors
- Capacitors that are being fabricated today are larger and better quality than earlier versions.
- By altering the process for forming the capacitors defect free films can be made
  - This process is not yet optimized, but shows potential for forming larger area thin films
- Still have a long way to go

Future Direction

- For FY11, continue working at BNC/Purdue to develop a better understanding of the viability of this technology, particularly to reduce capacitor cost and volume.

Technical Discussion

Cap Size	Room 0V Bias	+140 C 0V Bias	- 40 C 0V Bias	DK Room 0V Bias	DK +140 C 0V Bias	DK -40C 0V Bias	Room 18V Bias	+140 C 18V Bias	- 40 C 18V Bias	DK Room 18V Bias	DK +140 C 18V Bias	DK -40C 18V Bias
	nF	nF	nF				nF	nF	nF			
5mm	572	698	526	1975	2410	1816	220	218	208	759	753	718

Table 1. Film-on-Foil measured results on sample made at BNC/Purdue

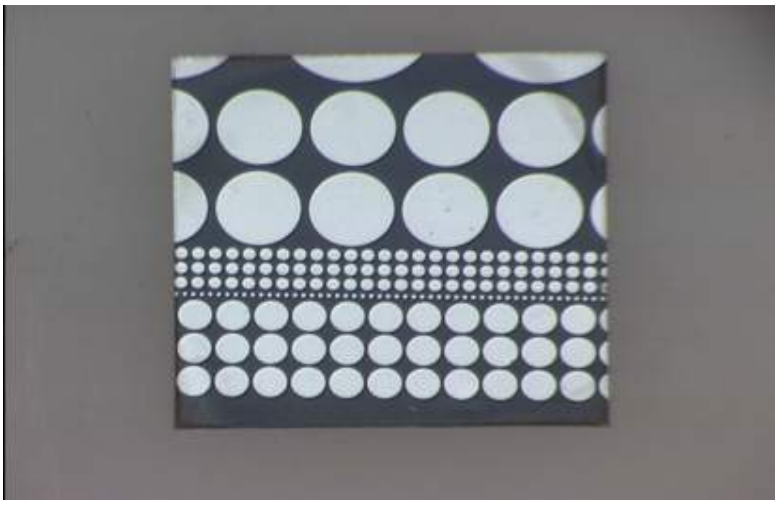


Fig. 1. Capacitors made at Purdue on metalized Si substrate

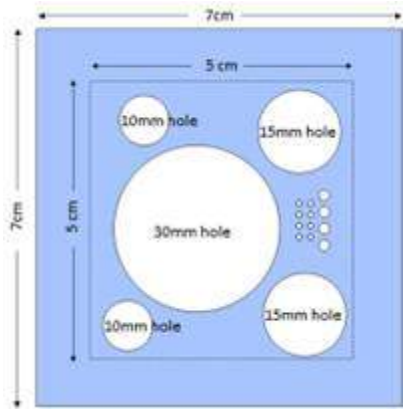


Fig. 2. Mask set to allow larger for area capacitors

Major Accomplishments: 3C-SiC/Si (Dow Corning)

- Objective
  - Demonstrate functional 3C-SiC on Silicon diodes and MOSFETs
  - Show materials process and device process cost reduction routes to achieve DOE cost targets for inverter chip set
- Cost model complete
- Epitaxy thickness uniformity good and bow/warp in line with targets
- Demonstrated good crystal quality in CVD processes
- Mechanical samples performed well in package integrity tests using Delphi packaging technology
- Delivered SiC-on-Si wafers to GeneSiC for development of unit process steps
  - Etching development and oxide growth unit processes completed at GeneSiC

Future Direction

- First fully fabricated diode lots scheduled to be delivered to Delphi by end of Mar/2011

Technical Discussion

- Current film doping is too high and does not currently meet Delphi's final deliverables needs.
- Dow Corning is experiencing difficulty in making wafers with correct doping, due to undetermined source of N2 in CVD system
  - Working with vendor, Dow devised way to run a leak rate test on CVD system at high temp
  - At 25C (room temp), leak rate is 5 mT/min (good), but at 1000C, leak rate is >50 mT/min (poor)
  - This finding provides the first clear signal for identifying the leak source

Major Accomplishments: Modeling and Test ORNL

- Advanced silicon parts, Si IGBT and Si diode, were received from Delphi
- Static characteristics of the Si IGBT were obtained over the temperature range 25°C to 150°C
- New gate driver board for the power package was designed and tested
- Dynamic characteristics of Si IBGT were obtained at 360V, for 10A up to 300A, at room temperature
- Results of static and dynamic testing were sent to Delphi for verification of the device behavior
- Obtained device losses at 10A-50A for inverter loss model at low power over simulated drive cycle
- Completed a draft plan for the inverter testing

Future Direction

- Provide test plan to Delphi for review
- Verify inverter performance with Delphi using motor supplied by Delphi at Delphi Kokomo.

Technical Discussion

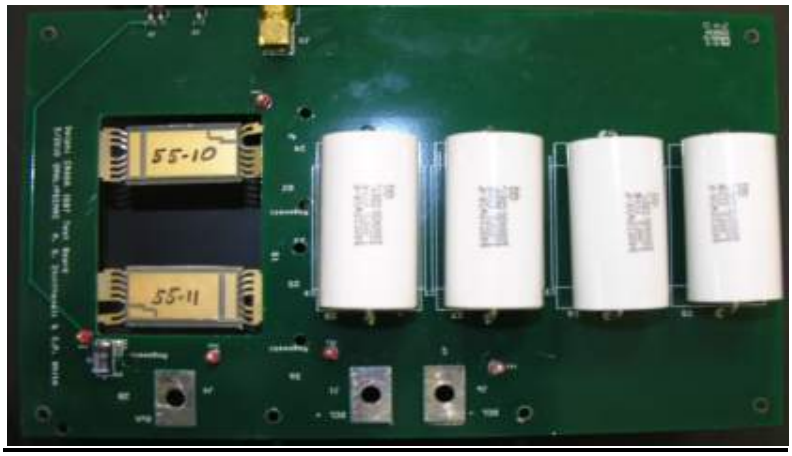


Fig. 3. Power Board used for Testing

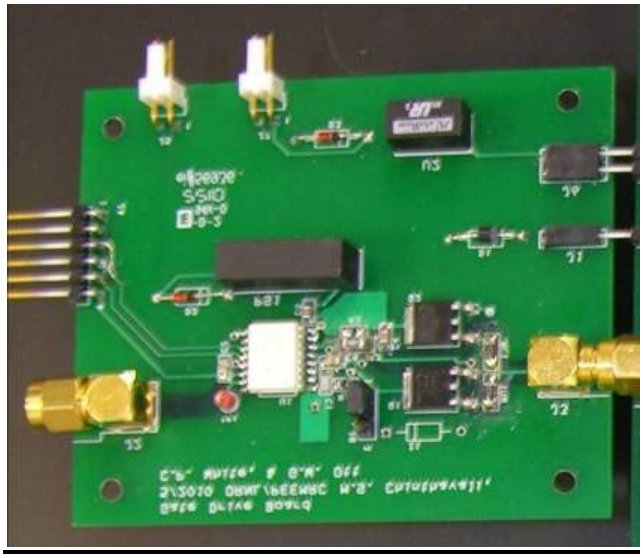


Fig. 4. Gate Drive Board used for Testing

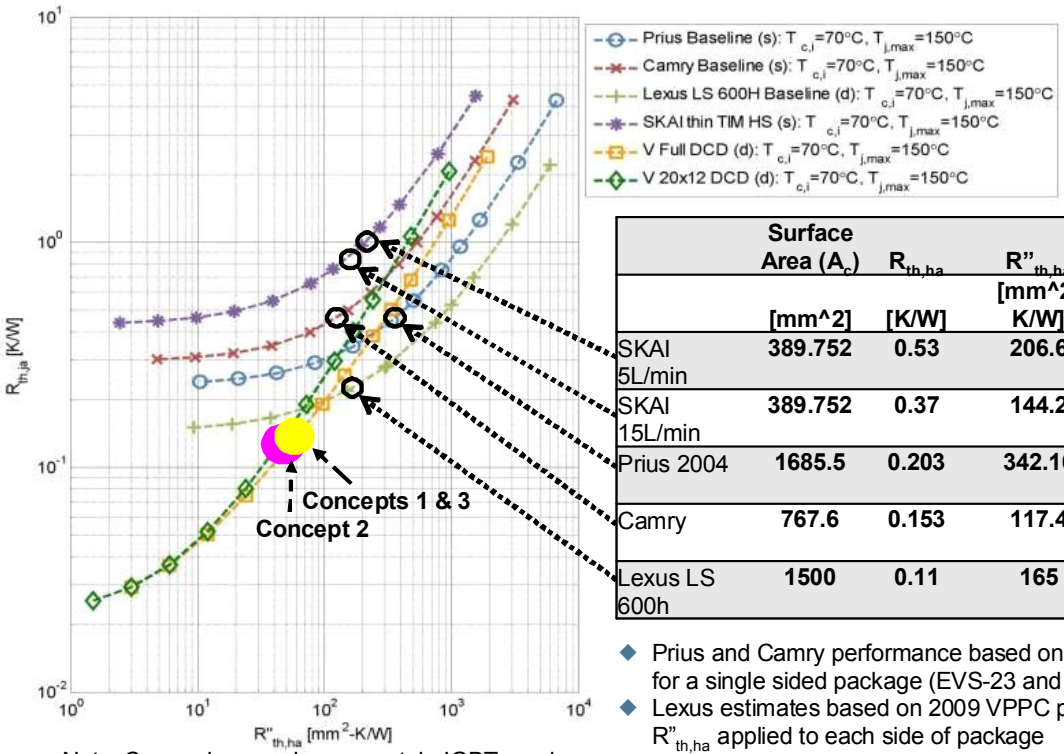
Major Accomplishments: Thermal Modeling of Package (NREL)

- Working with Delphi, NREL has performed analysis of various cooling strategies proposed by Delphi
  - Package comparisons completed for R"th,ha vs. Rth,ja
  - In some cases, NREL verified Delphi's results
- Results of these analysis were compared to commercial systems currently in the marketplace
  - Comparisons showed Delphi's power device packaging provides at least 30% improvement in thermal resistance junction to coolant, compared to "best" commercially available product today (see Figure 5 below).

Future Direction

- Continue to evaluate and develop high performance thermal interface materials in conjunction with suppliers and customers.
- Continue to evaluate novel thermal stacks with lower thermal resistance junction to water, than is currently being demonstrated today.

Technical Discussion



	Surface Area (A_c) [mm^2]	$R_{th,ha}$ [K/W]	$R"_{th,ha}$ [mm^2-K/W]	$R_{th,ja}$ [K/W]
SKAI 5L/min	**389.752**	**0.53**	**206.6**	1
SKAI 15L/min	**389.752**	**0.37**	**144.2**	0.84
Prius 2004	**1685.5**	**0.203**	**342.16**	0.452
Camry	**767.6**	**0.153**	**117.4**	0.452
Lexus LS 600h	**1500**	**0.11**	**165**	0.22

- Prius and Camry performance based on $R_{th,ja}$ of 0.452 °K/W for a single sided package (EVS-23 and SAE Paper)
- Lexus estimates based on 2009 VPPC paper with same $R"_{th,ha}$ applied to each side of package
- Semikron SKAI estimates based on data from spec sheet

Note: Comparison packages contain IGBTs and diodes of different die areas.

Fig. 5. Comparisons of Delphi's thermal performance concepts 1,2 and 3 vs. commercially available products

Major Accomplishments: Packaging Thermal and Integration (Delphi)

- Three concepts were presented for the deliverable
  - Micro-channel cooled power package
  - New interconnect technology
  - Advanced silicon with improved heat sink
  - All concepts allow for cooling of the top as well as the bottom of the substart
    - No wirebonds

- Micro-channel Cooled Power Package
  - Measurements of thermal resistance (junction-to-coolant) were performed by NREL and indicated lower performance than originally measured by Delphi.
  - Delphi repeated the measurements and also found lower performance.
  - Further analysis of the micro-channel package indicated corrosion of micro-channels (aluminum) had occurred over a period of several months.
  - Deionized water was used as coolant; we should have used engine coolant (anti-freeze) which contains corrosion inhibitors.
  - New packages are being assembled for further testing.
  - Testing of materials compatibility (package plastic, sealant, Viper DBA/DBC) with engine coolant is in progress (long term, high pressure soak at 105°C).
    - Co-development of materials with suppliers focused on achieving thermal resistance of 0.05 cm2 °C/W and no more than 15% decrease in thermal resistance over time
  - Due to the potential to reduce silicon requirements, future work will address:
  - Package design for manufacturability
  - Materials compatibility
  - Long-term reliability

- New Interconnect Concept
  - Encapsulation trials are complete and a process was developed to fully encapsulate IGBT, diode, substrates and leads.
  - A total of 45 parts were built and tested to date.
  - High voltage testing was completed and 14 parts passed all testing.
  - Based on evidence from root cause assessment of failed groups of flex packages, it was determined the build can be improved in future by eliminating pre-forms. .

- Advanced Silicon with Improved Heat Sink
  - Utilizes advanced Si with improved heat sink
  - Characterized static and dynamic performance of advanced silicon devices over temperature (25°C and 150°C)
    - Conduction losses show substantial reduction vs. baseline and target
    - Switching losses can be optimized to minimize total losses for a given drive cycle
  - Meets DOE performance requirements
  - Scalable and capable of operating over a wide range of applications
    - Capable of 80A to >300A/ rms phase output
    - Parts delete and part substitution
  - Utilizes 105°C engine coolant
    - Double-sided cooled power package (discrete power switch)
    - Using light weight, high performance heat rails
    - Thermal performance characterized with 105°C coolant
  - Utilizes high performance phase-change thermal interface material
    - Thermal resistance of 0.08 cm2 °C/W

- Utilizes scalable, high current connection system
- Utilizes PP or extrudable PEI capacitor
  - PEI capacitor will meet 140°C temperature requirement

Future Direction

- While all three concepts show promise for reducing inverter size and cost in the future, Delphi has chosen the advanced silicon with improved heat sink concept for the inverter build.

Technical Discussion

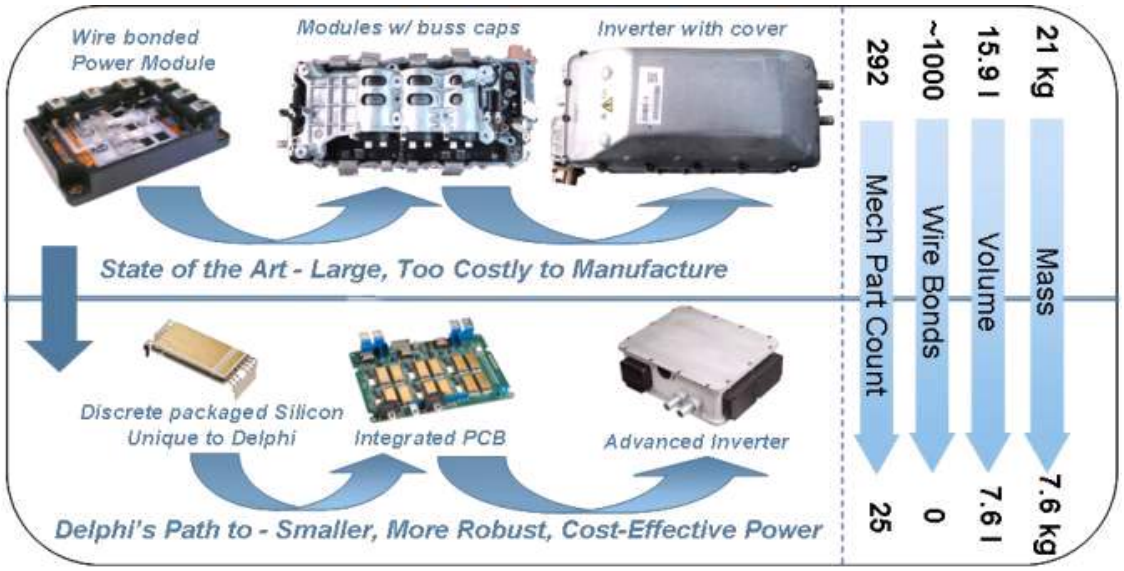


Fig. 6. Delphi's Power Technology Path to Smaller, Lighter, Manufacturable and Lower Cost Power Electronics

Conclusion

- Power device packaging provides at least 30% improvement in thermal resistance junction to coolant, compared to the "best" commercially available product today
- Advanced Si devices provide conduction losses ~17% lower than target
- Developing a technical path to smaller, lower cost, high temperature bulk capacitors
- Lower thermal resistance packaging with lower device losses allows for use of less silicon
- Less silicon implies less silicon packaging
- Less silicon, silicon packaging and smaller bulk capacitor implies smaller package size
- Results in smaller Inverter with Reduced Volume and Weight – Easier to Manufacture – Lower Cost

2.10 High Dielectric Constant Capacitors for Power Electronic Systems

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Objectives

- Develop ceramic dielectric films that have potential to reduce size, weight, and cost, concomitant with increased capacitance density and high temperature operation, for capacitors in electric drive vehicle inverters.
- Current DC bus capacitors occupy a significant fraction of volume (≈35%) and weight (≈25%) of the inverter module, cannot tolerate temperatures >120°C, and suffer from poor packaging, and inadequate reliability.
- Traditional capacitor architectures with conventional dielectrics cannot adequately meet all of the performance goals for capacitance density, weight, volume, and cost.
- Meeting these goals requires a dielectric with high permittivity and breakdown field that tolerates operating at high temperature, is packaged in architecture with high volumetric efficiency, and exhibits benign failure features.

Approach

- Develop high-dielectric constant, high-temperature, low-cost ferroelectric $(Pb,La)(Zr,Ti)O_3$ (abbreviated as PLZT) dielectric films on base-metal foils ("film-on-foil") that are either stacked on or embedded directly into the printed wire board (PWB).
- Stack high performance film-on-foils, produce prototype capacitor with termination, and characterize its properties.
- Use of base-metals and solution-based deposition techniques reduce the cost.
- Ferroelectrics possess high dielectric constants, breakdown fields, and insulation resistance. With their ability to withstand high temperatures, they can tolerate high ripple currents at under-the-hood conditions.
- Stacked and/or embedded capacitors significantly reduce component footprint, improve device performance, provide greater design flexibility, achieve high degree of volumetric efficiency with less weight, and offer an economic advantage.
- R&D efforts focus on examining the issues that underpin the performance of film-on-foil capacitors, establishing fabrication protocols that are commercially robust and economically viable.

Major Accomplishments

- Built a ≈5 μF prototype capacitor with termination by stacking three 1" x 1" film-on-foils.
- Demonstrated film-on-foil PLZT dielectrics with dielectric constant, k >1300, breakdown field >2.6 MV/cm, and leakage current $<10^{-8}$ A/cm^2 at room temperature.

- Measured k ≈120, loss factor ≈0.008 at 300 V bias, and energy density ≈85 J/cm^3 on a ≈3.0 μm-thick PLZT film-on-foil at room temperature (for comparison, k of polymer films are ≈6).
- Fabricated and measured a 20-mm diameter film-on-foil (≈0.7 μm-thick PLZT) with capacitance of ≈6 μF at zero bias.
- Fabricated and characterized PLZT dielectrics on nickel metal foils with self-clearing electrodes. The key to large-area yield is to electrically isolate the defect spots that compromise the integrity of the dielectric layer.
- PLZT film-on-foil capacitors were thermally cycled ≈1000 times between -50°C and 150°C with no measurable degradation in k.
- Highly accelerated lifetime tests (HALT) were performed at elevated temperature and high field stress to predict the lifetime of film-on-foils.
- Presented program status and future direction to DOE APEEM projects kickoff, EE Tech Team, and Annual Merit Review meetings.
- Published five papers in peer reviewed international journals and three papers in conference proceedings.
- Filed two patent applications and submitted one new invention report.
- Presented the results at seven scientific conferences.

Future Direction

- The primary emphasis of FY 2011's effort is toward advancing the proven laboratory scale film-on-foil technology and fabricating a ≈10 μF, high-voltage capable capacitor with termination. The effort will be focused on optimizing processing conditions investigated in FY10 to produce high-voltage capable film-on-foils. Using small area top electrodes, the R&D effort in FY10 has demonstrated that the properties of PLZT film-on-foils are suitable for power electronics operating at under-the-hood temperatures. Important processing issues such as substrate polishing, humidity control, organic removal, clean room processing, and rapid thermal annealing have been identified to make large area capacitors with the desired dielectric properties.
- Stack high-voltage capable film-on-foils and produce a ≈10 μF capacitor with termination.
- In collaboration with Pennsylvania State University, characterize the dielectric properties of film-on-foils and the stacked, multilayer capacitor.
- Provide a prototype multilayer capacitor to ORNL to test the device's performance and benchmark it against APEEM goals.
- Investigate electrode material and architecture to achieve benign failure in multilayers.
- Develop new fabrication methodology (sol-gel with nano-particle seeds and aerosol deposition) to reduce the capacitor cost.
- Identify industrial partner to manufacture multilayer capacitors.

Technical Discussion

The overall project objective is to develop dielectric films that have potential to reduce size, weight, and cost, concomitant with increased capacitance density and high temperature operation, for capacitors in electric drive vehicle inverters. The purpose of this project is to build and test a prototype capacitor capable of meeting APEEM requirements. The performance of presently available capacitors degrade rapidly with increasing temperature and they occupy significant fraction of the inverter volume (≈35%), weight (≈25%), and cost (≈23%). The ceramic dielectric capacitor R&D program at Argonne National Laboratory (Argonne) addresses the technology gap in an innovative manner. We are developing high performance, low cost capacitors that are either stacked on or embedded directly into the PWB. In these

"film-on-foil" capacitors, a base-metal foil (nickel or copper) is coated with a high permittivity ferroelectric material, PLZT, via chemical solution deposition (CSD) technique. Ferroelectrics possess high permittivity, breakdown electric fields, and insulation resistance. They can withstand high temperatures such that high ripple currents can be tolerated at under-the-hood temperatures. Use of base-metals and solution-based deposition techniques reduce the cost. The stacked and embedded capacitors approaches significantly reduces component footprint, improves device performance, provides greater design flexibility, and offers an economic advantage for commercialization. This technology will achieve the high degree of packaging volumetric efficiency with less weight. Device reliability is improved because the number and size of interconnections are reduced. While this technology has primarily received attention for low voltage, high frequency decoupling capacitors, it can potentially be extended to the higher voltages of electric drive vehicle systems. The vision of embedded DC bus capacitors is compelling and offers US automotive companies a substantial technological advantage over their foreign counterparts. The bulky coke-can-like banks of capacitors can be replaced by lengths of capacitors tucked flat and neatly underneath the active components and bus structure. While embedding the film-on-foil capacitors into the PWB is the ultimate goal, the short-term practical approach is to target high voltage, high temperature, stacked capacitors for the inverter applications using film-on-foil dielectric layers. The short-term target will address the important issues, namely, weight, volume, and cost advantages of the film-on-foils compared to the conventional, bulky, wound polymer capacitors. Our R&D efforts focus on examining the issues that underpin the performance of film-on-foil capacitors, establishing fabrication protocols that are commercially robust and economically viable.

We have developed a core technology for fabricating CSD PLZT on Ni foils with $LaNiO_3$ (LNO) buffer layers. CSD solutions were synthesized at Argonne, and films were deposited by spin coating. Nickel substrates (25 mm × 25 mm, 0.5 mm thickness, 99.8% pure, ESPI Metals) were polished to 1-μm finish (≈0.4 mm final thickness) and ultrasonically cleaned in acetone and methanol prior to coating. Stock solutions of 0.3M $LaNiO_3$ (LNO) and 0.5M $Pb_{0.92}La_{0.08}Zr_{0.52}Ti_{0.48}O_3$ (PLZT) were prepared by modified sol-gel synthesis using 2-methoxyethanol as the solvent. The detailed procedure is reported elsewhere [1-5]. The LNO solution was spin-coated onto the substrate at 3000 rpm for 30 sec, pyrolyzed at ≈450°C for 5-10 min, and crystallized at ≈650°C for 2-5 min. This process was repeated five times to build the desired thickness with a final annealing at ≈650°C for 20 min. The PLZT stock solution was spin-coated onto the LNO-buffered substrate at 3000 rpm for 30 sec. Films were then pyrolyzed at ≈450°C for 10 min and crystallized at ≈650°C for 2-5 min, followed by a final annealing at ≈650°C for 20 min after repeating the coating steps to build up layers of sufficient thickness. By this process, we have fabricated PLZT films with thicknesses up to ≈3 μm. Platinum top electrodes were then deposited by electron beam evaporation using a shadow mask. These electrodes had diameters of 250 μm, 750 μm, and 20 mm and thickness of ≈100 nm. Films with top electrodes were annealed at ≈450 °C in air for 2 min for electrode conditioning. A Signatone QuieTemp® probe system with heatable vacuum chuck (Lucas Signatone Corp., Gilroy, CA) was used for electrical characterization. For the electrical measurements, the Pt/PLZT/LNO/Ni heterostructure was contacted by a Pt top electrode pad with one probe and the substrate (bottom electrode) with the other. A positive applied voltage corresponds to the configuration where the top electrode is at a higher potential than the bottom electrode. An Agilent E4980A Precision LCR Meter measured the capacitance and dissipation factor under applied bias field. A Radiant Technologies' Precision Premier II tester measured the hysteresis loops. The capacitor samples were immersed in Fluka silicone oil (Sigma-Aldrich) during high-field hysteresis loops and dielectric breakdown measurements. A Keithley 237 high-voltage source meter measured the current-voltage characteristics. The leakage current density was determined by fitting the current density relaxation data to the Curie-von Schweidler equation [6].

The PLZT films grown on LNO-buffered Ni foils were phase pure with no preferred crystallographic orientation as shown by X-ray diffraction, and no crack or delamination was observed from SEM [1]. Average grain size of ≈60 nm was determined from SEM and confirmed by AFM [4]. The use of LNO

buffer allows the film-on-foils to be processed in air without the formation of a parasitic interfacial nickel oxide layer. The LNO also compensates for the roughness of the Ni foil and provides a smooth interface for the PLZT films, resulting in higher breakdown strengths. In addition, the LNO buffer helps to reduce the compressive strain in the PLZT films deposited on nickel substrates due to the thermal expansion coefficient mismatch between PLZT and metal foils [7].

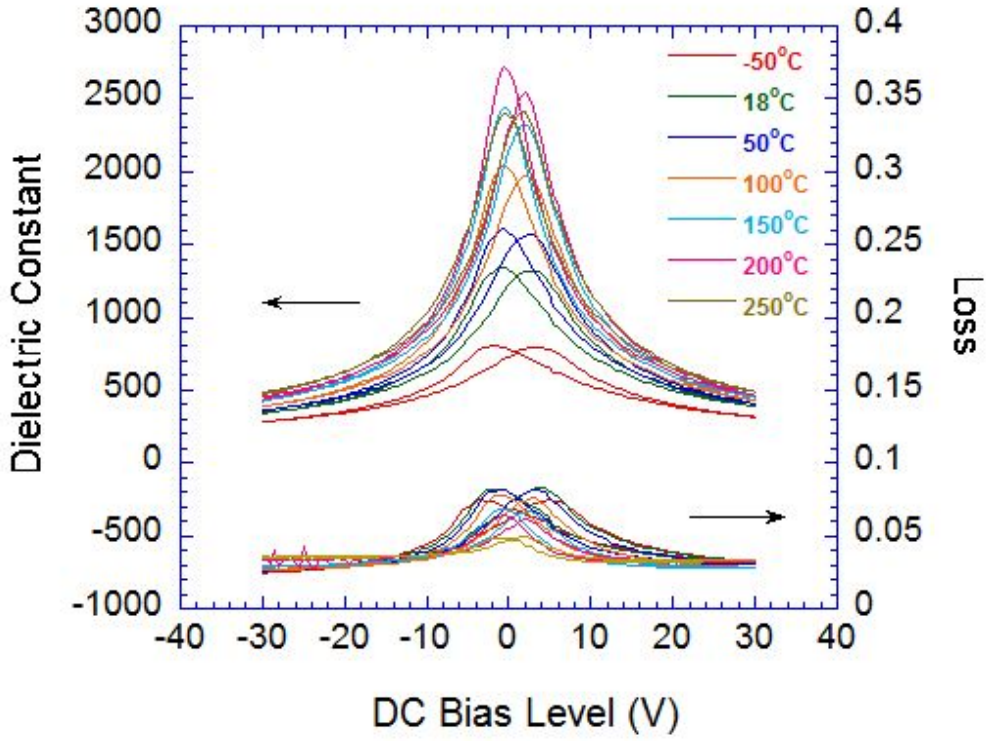

Fig. 1. Dielectric properties of a ≈1.15-µm-thick PLZT/LNO/Ni film-on-foil measured as a function of applied bias voltage at various temperatures.

Figure 1 shows the dielectric constant and loss measured as a function of bias voltage at different temperatures on a ≈1.15-µm-thick PLZT deposited on a 0.4-µm-thick LNO buffered Ni substrate coated with Pt top electrodes. Typical ferroelectric behavior, butterfly shaped curves, were observed at all temperatures from -50°C to 250°C. The double-peak separation decreases with increasing temperature. We measured dielectric constant of 1300 and dielectric loss of ≈0.07 at room temperature and dielectric constant of 2200 and dielectric loss of ≈0.06 at 150°C, respectively. The dielectric constant and dielectric loss decreases with increase in bias field.

Figure 2 shows the dielectric constant and dielectric loss measured under various applied bias voltages as a function of temperature from -50°C to 250°C. The sample is a ≈1.15-µm-thick PLZT deposited on a 0.4-µm-thick LNO buffered Ni substrate coated with Pt top electrode. Dielectric constant (hence the capacitance) increases and dielectric loss decreases with increase in temperature up to 200°C. Increase in capacitance lowers the ESR and the ripple current capability of the capacitor improves with increase in temperature. This improvement in performance is desired for DC bus capacitors in high temperature inverters for electric drive vehicles.

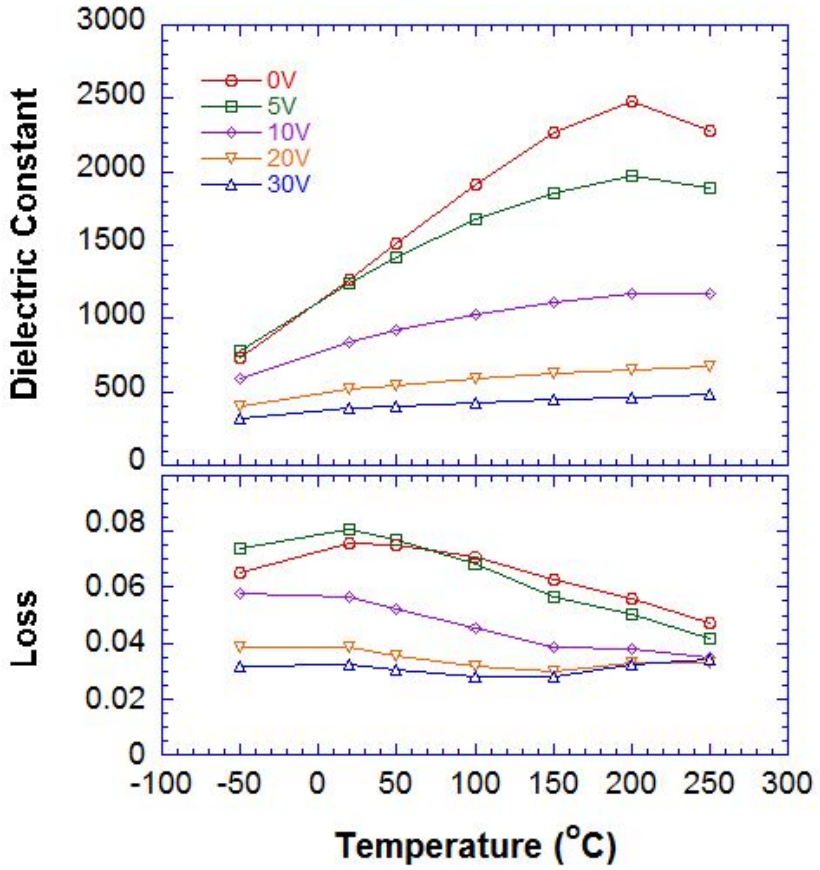

Fig. 2. Dielectric constant and loss as a function of temperature measured under applied bias voltages.

Figure 3 shows the time relaxation for the current density measured on ≈1.15-µm-thick PLZT/LNO/Ni sample at 25°C, 75°C, and 150°C with a constant bias potential of 10 V (corresponding to an applied electrical field ≈8.7×10^4 V/cm) across the top and bottom electrodes. The measurements were conducted by keeping the top Pt electrode positive and the bottom Ni electrode grounded. Both curves show strong initial time dependence, indicating depolarization process. The current density measured at 150°C is roughly a factor of two higher than that measured at 25°C. The decay in dielectric relaxation current obeys the Curie-von Schweidler law [6],

$$J = J_s + J_0 \cdot t^{-n} \qquad (1)$$

where J_s is the steady-state current density, J_0 is a fitting constant, t is the relaxation time in seconds, and n is the slope of the log-log plot. Fitting the data to Eq. 1, we found n values of 0.97, 0.77, and 0.65 and leakage current densities of 4.6×10^{-9} A/cm^2, 8.8×10^{-8} A/cm^2, and 1.6×10^{-7} A/cm^2 for the measurements at room temperature, 75°C, and 150°C, respectively.

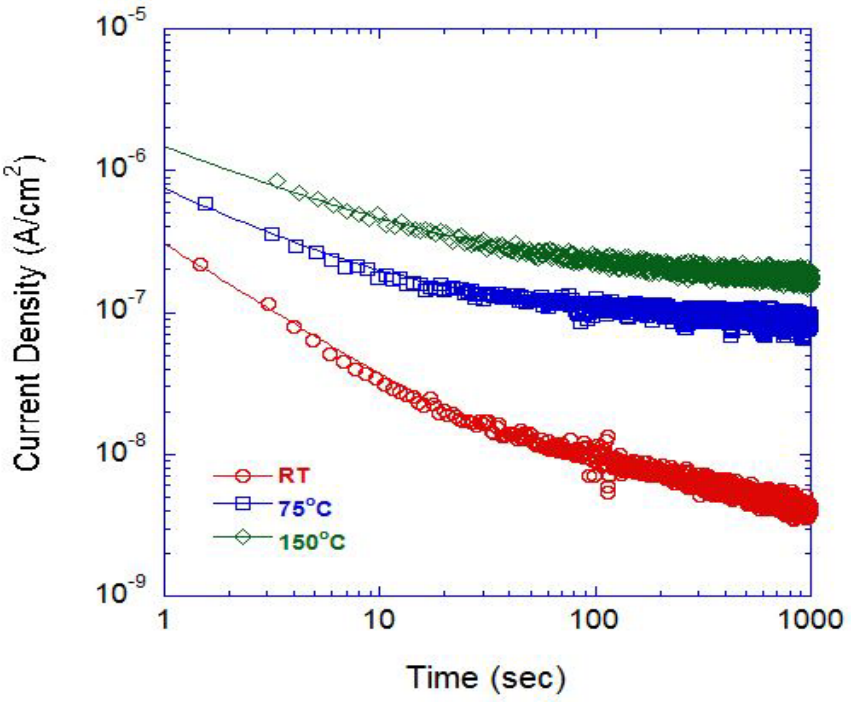

Fig. 3. Time-relaxation current density measured on a PLZT/LNO/Ni sample under 8.7 × 10^4 V/cm electric field at room temperature, 75°C, and 150°C.

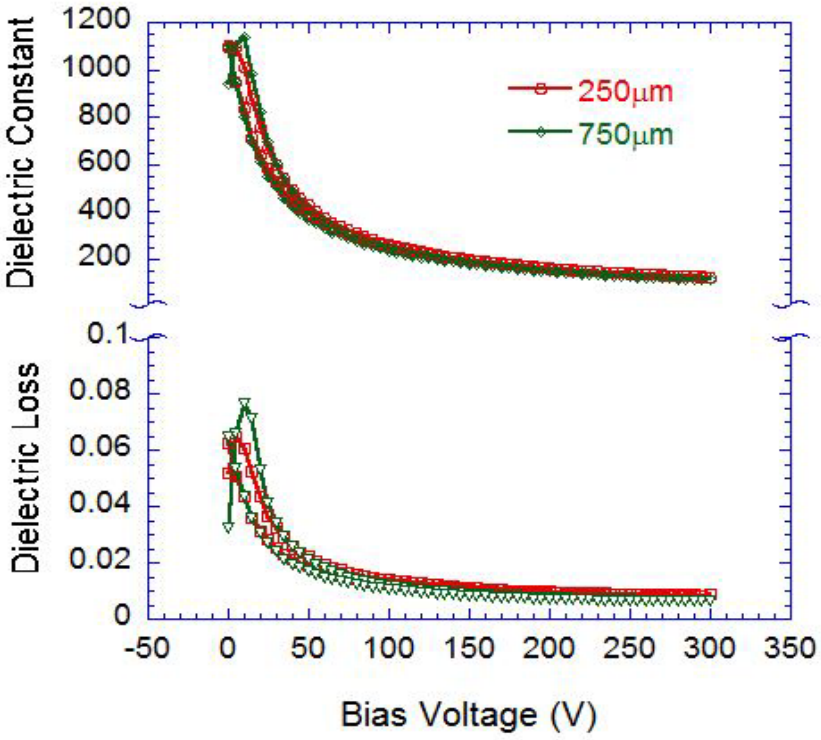

Fig. 4. Dielectric properties as a function of bias voltage measured on a ≈3-μm-thick PLZT/LNO/Ni film-on-foil at room temperature.

Figure 4 shows the dielectric constant and dielectric loss measured as a function of bias voltage up to 300 V. The measurements were performed at room temperature on a ≈3-µm-thick PLZT/LNO/Ni film-on-foil coated with Pt top electrodes. Both dielectric constant and dielectric loss decrease with increasing bias field. At room temperature and 300 V bias (corresponding to a bias field of ≈1 MV/cm), dielectric constant of ≈120 and dielectric loss ≈0.008 were measured. Our experimental results show that the PLZT ceramic dielectric films exhibit superior dielectric properties (higher dielectric constant) compared to the presently used polymer film capacitor which has a dielectric constant ≈6. Therefore, the PLZT based film-on-foils have great potential in realizing high degree of volumetric and gravimetric efficienices for the electric drive vehicle inverters.

Figure 5 shows capacitance and dielectric loss as a function of bias field measure at room temperature on a ≈0.7-µm-thick PLZT deposited on Platinum-coated silicon (Pt/Si) substrate. A 200-nm-thick and 20-mm-diameter Pt top electrode was coated by electron-beam evaporation. Sample was annealed at ≈450°C for 2 minutes for electrode conditioning before the dielectric properties were measured. We measured a capacitance of ≈6 µF on this large area film-on-foil at room temperature under zero-bias field.

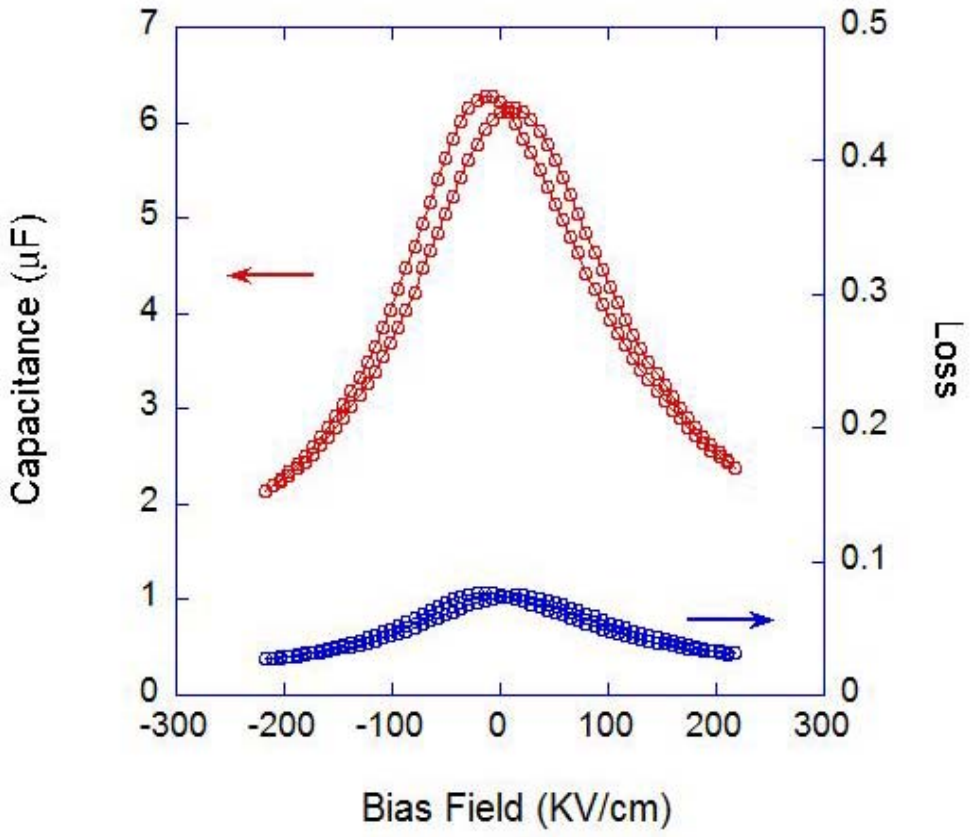

Fig. 5. Dielectric properties of a ≈0.7-µm-thick PLZT on Pt/Si substrate measured at room temperature on a ≈20-mm-diameter top electrode.

Figure 6 shows dielectric constant and dielectric loss of a large area (20-mm-diameter), ≈3-µm-thick PLZT on Ni foil measured as a function of bias field. The ≈200-nm-thick and 20-mm-diameter Pt top electrode was deposited on PLZT/LNO/Ni by electron-beam evaporation. Sample was annealed at ≈450°C for 2 minutes for electrode conditioning before the dielectric property measurement. At room temperature, we measured dielectric constant ≈1300 (capacitance ≈1.2 µF) and dielectric loss ≈0.08 under

zero-bias field and dielectric constant ≈500 (capacitance ≈0.45 μF) and dielectric loss ≈0.025 under ≈100 KV/cm bias field, respectively, on this large area film-on-foil. We fabricated a ≈5 μF capacitor with termination by stacking three film-on-foils that were previously tested using small size top electrodes.

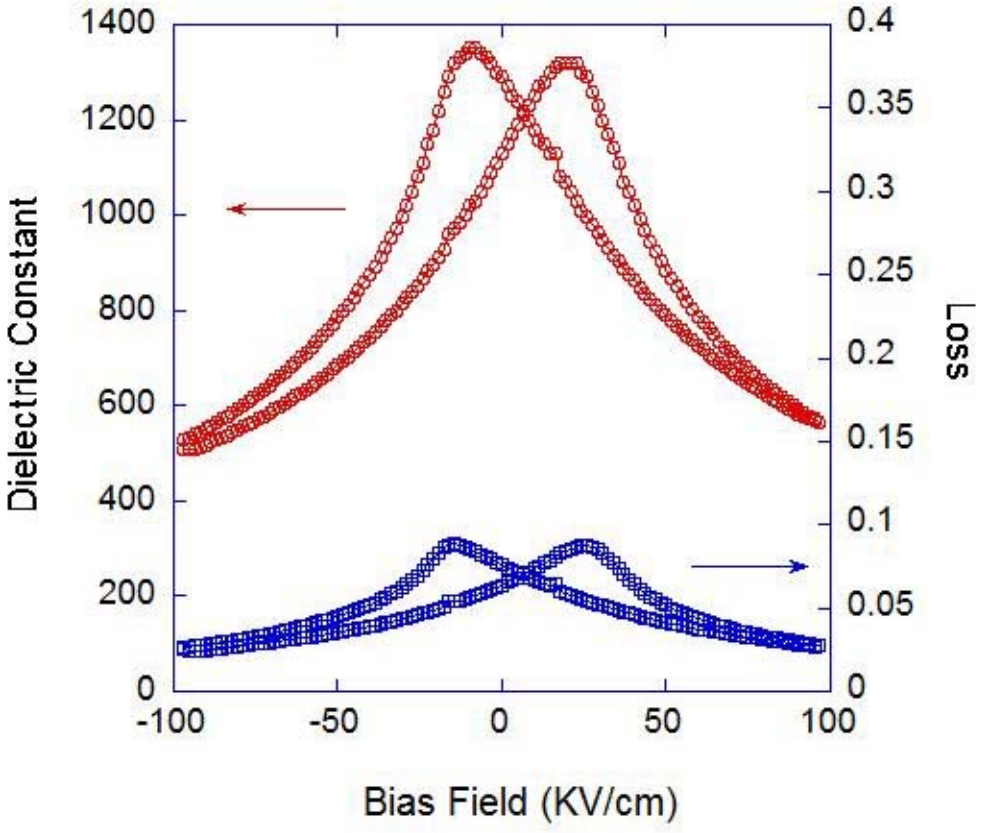

Fig. 6. Dielectric properties of a 20-mm-diameter, ≈3-μm-thick PLZT/LNO/Ni film-on-foil measured at room as a function of bias field.

Figure 7a shows hysteresis loop measured on a ≈3-μm-thick PLZT film deposited on LNO buffered nickel substrate with a 5-mm diameter top electrode at room temperature. An external electric field of 250 V was applied across the ≈3-μm-thick film, which correspods to an electric field ≈800 kV/cm. We observed a slim loop, indicative of low energy loss. Low energy loss is desirable for energy storage/conversion applications.

Figure 7b shows the polarization-field loop measured with maximum applied voltage of 1400 V on a second ≈3-μm-thick PLZT film using ≈250-μm diameter top electrode. By fitting and integration of the discharging portion of the P-E hysteresis loop curve, we measured an energy density of ≈85 J/cm^3 (at 1400 V) as indicated by the shaded area shown in Fig. 7b. Estimated energy density at 600 V is ≈15 J/cm^3. From the P-E loop measurement, we calculated the dielectric constant of this film to be ≈200 at 300 V and ≈120 at 600V. These unique properties (high dielectric constant, outstanding breakdown strength, and high energy density) demonstrate that these film-on-foils have potential for use in high-voltage power electronic systems in electric drive vehicles.

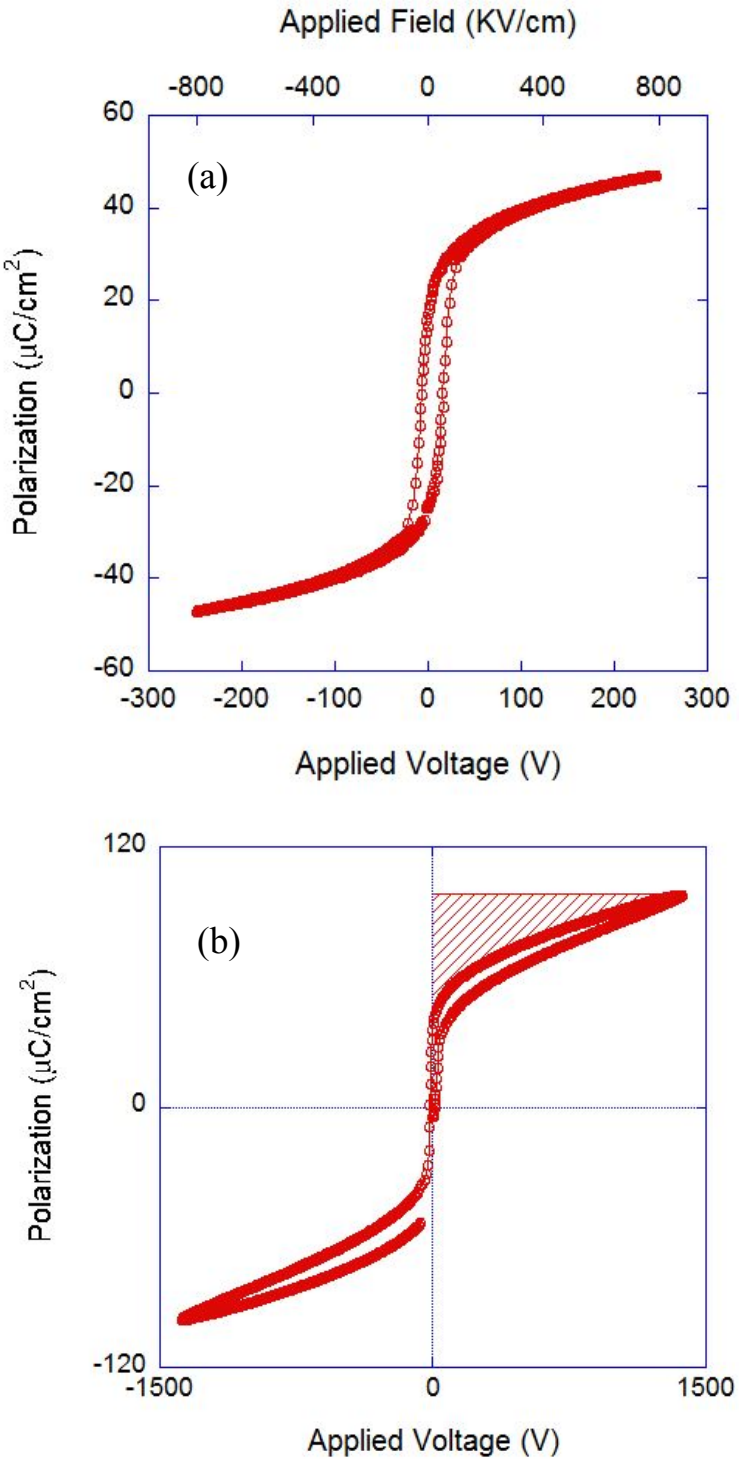

Fig. 7. Hysteresis loop of a ≈3-μm-thick PLZT/LNO/Ni film-on-foil measured at room temperature with applied field of (a) 250 V and (b) 1400 V.

For rapid assessment of the reliability of film-on-foil capacitors under stresses of applied voltage and temperature, we used the following empirical relationship among the mean time to failure (MTTF) [also known as mean time before failure (MTBF)] t, applied voltage V, and testing temperature T [8,9]:

$$t = C \cdot V^N \exp\left(\frac{E_a}{k_B \cdot T}\right) \qquad (2)$$

where C is a constant, E_a is a pseudo-activation energy, N is the voltage acceleration factor, k_B is the Boltzmann constant, and T is the absolute temperature measured in K.

Figure 8 shows the Weibull plot of time to breakdown data measured on ≈1.15-µm-thick PLZT/LNO/Ni film-on-foils at three temperatures (20°C, 75°C, and 125°C) with an applied voltage of 120 V (corresponds to ≈1.05 x 10^6 V/cm). The straight lines are least square fittings of experimental data to the 2-parameter Weibull function.

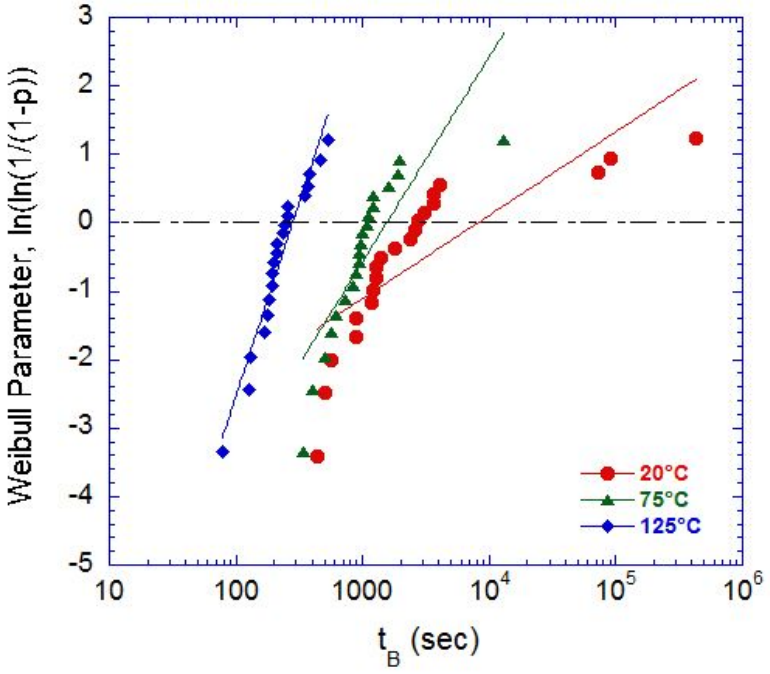

Fig. 8. Weibull plot of time to breakdown for ≈1.15-µm PLZT/LNO/Ni film-on-foils measured at 20°C, 75°C, and 125°C with 120 V applied voltage.

Figure 9 shows the MTTF vs. temperature for ≈1.15-µm-thick PLZT films at an applied bias voltage of 120 V. The symbols correspond to the measurement conditions used for collecting the data shown in Figure 8. The pseudo-activation energy calculated under the high field condition is ≈0.35 eV. This value is smaller than the 0.78 eV reported by Polcawich *et al.* for PZT grown on platinized silicon substrates [9]. Please note that we applied an electric field that is four times higher than that used in the Polcawich *et al.* work. Because of the good quality of our samples, measurements at low applied electric filed take much longer time.

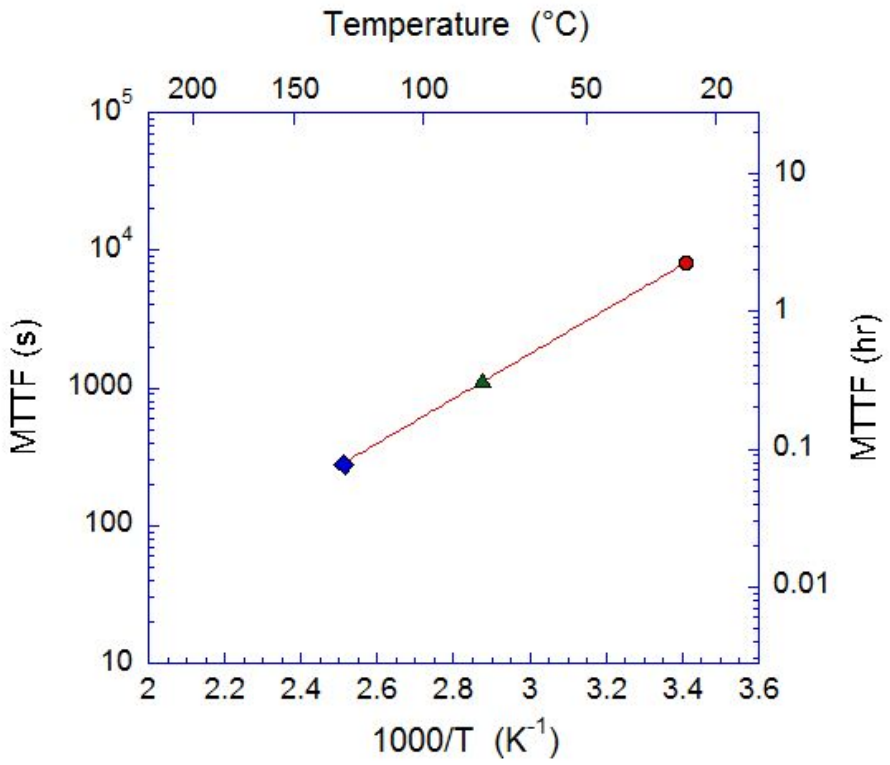

Fig. 9. Mean time to failure as a function of temperature for ≈1.15-µm-thick PLZT/LNO/Ni film-on-foils measured with 120 V applied voltage.

Conclusion

We have developed a core technology for fabricating high capacitance density PLZT dielectric films on base metal foils. PLZT film-on-foils have been fabricated with LNO buffer layers atop Ni foils, allowing the capacitors to be processed in air. We measured dielectric constant ≈1300 and dielectric loss ≈0.07 at room temperature and dielectric constant ≈2200 and dielectric loss ≈0.06 at 150°C, respectively (all values under zero bias fields). Leakage current densities of 4.6×10^{-9} A/cm^2, 8.8×10^{-8} A/cm^2, and 1.6×10^{-7} A/cm^2 were measured at room temperature, 75°C, and 150°C, respectively. Significant improvements have been made in increasing the area of the dielectric films compared to previous years. We have fabricated a 20-mm diameter film-on-foil (≈0.7-µm-thick PLZT) with capacitance of ≈6 µF measured at room temperature under zero bias field. Thicker films (≈3 µm-thick PLZT) to withstand high voltage (operating voltage of 450 V) have been fabricated and their P-E loop measurements were made with applied voltage as high as 1400 V. Dielectric constant ≈120 and dielectric loss ≈0.008 were measured with 300 V bias voltage applied on a ≈3 µm-thick PLZT film-on-foil. By stacking three 1" x 1" film-on-foils we fabricated a ≈5 µF capacitor with termination. Highly accelerated lifetime tests were conducted at different temperatures under bias field of 120 V to determine the lifetime of the film-on-foil dielectrics. The properties measured show that these film-on-foils have potential to meet the APEEM goals. Our results and the research plans were presented at the OVT-APEEM project kickoff, Annual Merit and Peer Review, and EE Tech Team meetings. The primary emphasis of FY11's effort is toward advancing the proven laboratory scale film-on-foil technology towards fabricating a ≈10 µF, high voltage capable capacitor with termination.

Publications

We have over 45 publications and presentations, and few selected publications are listed below.

1. B. Ma, M. Narayanan, S. Tong, U. Balachandran, *Fabrication and Characterization of Ferroelectric PLZT Film Capacitors on Metallic Substrates,* J. Mater. Sci., 45, 152, 2010.
2. U. Balachandran, D. K. Kwon, M. Narayanan, B. Ma, *Development of PLZT Dielectrics on Base-Metal Foils for Embedded Capacitors*, J. European Cer. Soc., 30, 365, 2010.
3. M. Narayanan, B. Ma, and U. Balachandran, *Improved Dielectric Properties of Lead Lanthanum Zirconate Titanate Thin Films on Copper Substrates,* Mater. Lett., 64, 22, 2010.
4. M. Narayanan, B. Ma, U. Balachandran, and W. Li, *Dielectric Spectroscopy of $Pb_{0.92}La_{0.08}Zr_{0.52}Ti_{0.48}O_3$ Films on Hastelloy Substrates with and without $LaNiO_3$ Buffer Layers,* J. Appl. Phys. Lett., 107, 024103, 2010.
5. B. Ma, D. K. Kwon, M. Narayanan, U. Balachandran, *Dielectric Properties and Energy Storage Capability of Antiferroelectric $Pb_{0.92}La_{0.08}Zr_{0.95}Ti_{0.05}O_3$ Film-on-Foil Capacitors,* J. Mater. Res., 24, 2993, 2009.
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12. B. Ma, D. K. Kwon, M. Narayanan, and U. Balachandran, *Leakage Current Characteristics and Dielectric Breakdown in Antiferroelectric $Pb_{0.92}La_{0.08}Zr_{0.95}Ti_{0.05}O_3$ Film Capacitors Grown on Metal Foils,* J. Phys D: Appl. Phys., 41, 205003, 2008.
13. B. Ma, D. K. Kwon, M. Narayanan, and U. Balachandran, *Dielectric Properties of PLZT Film-on-Foil Capacitors,* Mater. Lett., 62, 3573, 2008.
14. M. Narayanan, D. K. Kwon, B Ma, U. Balachandran, *Deposition of Sol-gel Derived PLZT Thin Films on Copper Substrate,* Appl. Phys. Lett., 92, 252905, 2008.

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2.11 High Temperature Thin Film Polymer Dielectric Based Capacitors for HEV Power Electronic Systems

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Objectives

DC bus capacitors are currently the largest and the lowest reliability component of fuel cell and electric hybrid vehicle inverters. Capacitors represent up to 23% of both inverter weight and inverter cost and up to 35-40% of the inverter volume. Furthermore, existing DC bus capacitors cannot tolerate temperatures greater than 120°C. Our project goal is to develop an inexpensive replacement high energy densisty, high temperature dielectric for DC bus capacitors that will find use in next generation hybrid electric vehicles (HEVs), plug in hybrid electric vehicles (pHEVs), and electric vehicles (EV). The improved capacitors will be based on novel high temperature polymer thin film dielectrics. Our technical goal is to enhance high temperature performance and volumetric efficiency compared to present dielectrics. Specific metrics include the development of polymer film dielectrics with dissipation factors of 0.02 or less at 150 ºC. Synthesis, fabrication, and high temperature (room temperature to 150 ºC) characterization of these dielectric materials is an integral part of the material development program. In addition, work will focus on transitioning the material to industry to produce rolls of the novel high temperature polymer dielectric film which will lead directly to the production of a prototype capacitor.

Approach

Sandia National Laboratory's (Sandia) capacitor R&D program addresses the technology gap in an innovative manner. We are developing high performance, high temperature, low cost capacitors that are based on novel Sandia developed polymer chemistry. Capacitors fabricated using this polymer technology will achieve the high degree of packaging volumetric efficiency with less weight while maintaining a cost of less than $0.03 per µF. In addition, our work focuses on high glass transition (T_g) temperature materials to increase the operational temperature range of the capacitor. Our R&D specific efforts focus on 1) producing polymer film at Electronic Concepts, Inc. (ECI) in an appropriate quantity to fabricate prototype capacitors and 2) using the optimum polymer film stoichiometry as a starting point to improve the dielectric breakdown.

Major Accomplishments

- Identified and addressed problems associated with thin film production at ECI due to reactivity of the olefinic functional groups within our polymer dielectric.
- Explored three methods including hydrogenation, thiol-ene reaction, and free radical inhibitor additives to remove the double bond or decrease the reactivity within the double bond.
- Fabricated and characterized two types of stacked capacitors in-house using the improved non-crosslinking polymer formulation based on hydrogenation. These capacitors were also sent on to ORNL for further evaluation.

Future Direction

The R&D effort has demonstrated the feasibility of using high temperature dielectrics for power electronics operating at high temperatures (150 ºC). Progress achieved thus far sets the stage to begin fabrication of prototype high temperature capacitors, which will require the development of polymer casting or polymer extrusion conditions that allow the production of large spools (>100 m length) of polymer dielectric films. The spools of polymer dielectric will then be slit, metalized and rolled into capacitors. We have worked with our industrial partner (ECI) to produce a desired amount of polymer dielectric film capable of prototype capacitor formation. Research in FY09 led to the identification of the side reaction that was occurring in solution leading to polymer gel formation which was inhibiting the large-scale film formation. Work in FY10 was focus on the removal of the crosslinkable double bonds in the backbone of the polymer to yield polymer film solutions with greatly enhanced shelf life. With an improved polymer formulation in-hand, we will continue to work with ECI to produce several prototype capacitors. At least six prototype capacitors with capacitances of 1.0 μF or greater will be evaluated and benchmark it against APEEM goals. In addition, we will produce at least six "stacked" capacitors at Sandia National Labs in the event that we are unable to produce six rolled prototype capacitors at ECI. These initial prototype capacitors (rolled or stacked) will be evaluated by ORNL as well as other research institutions. We will continue our effort in developing dielectric materials with improved performance focusing on the incorporation of nanoparticle fillers to increase the energy density further leading to smaller volume capacitors.

Technical Discussion

1.0. Polymer Film Production Leading to Capacitors

An industrial partner (ECI) was identified in January 2008 to begin the fabrication of large spools (>100 m length) of polymer dielectric films. A purchase order was placed to begin the production of polymer films and an initial amount of 1 kg of the identified polymer (**1**, Figure 1) was sent to ECI where several solvents and solvent combinations were evaluated in order to produce the required rolls of polymer film. The initial attempts to cast on a larger scale yielded only small amounts of polymer dielectric film. Work during FY09 continued to focus on development of the "pilot scale" process that would yield a spool with a large length of polymer dielectric film. Again, the work with ECI began with Sandia synthesizing 1 kg of polymer **1** which was sent to ECI for large scale casting experiments.

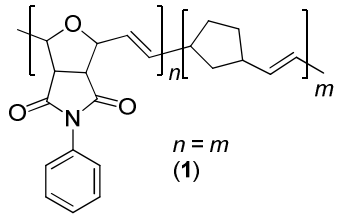

Fig. 1. Structure of the high temperature polymer dielectric polymer

A switch to dichloroethane resulted in the fabrication of a larger length of polymer film than had been cast the previous year (Figure 2), however, the polymer solutions were not stable for long periods of time.

Fig. 2. Spool of the high temperature polymer dielectric produced at ECI

A typical procedure to produce polymer film started with forming a solution of the polymer by dissolving the dielectric polymer in dichloroethane prior to casting the polymer. Unused polymer solution would be stored in air usually over a weekend. When the polymer solution was examined, Polymer was precipitating out of solution and did not go back into solution upon heating or stirring. These results are consistent with the crosslinking of the double bonds in the backbone of polymer **1** as shown in Figure 3.

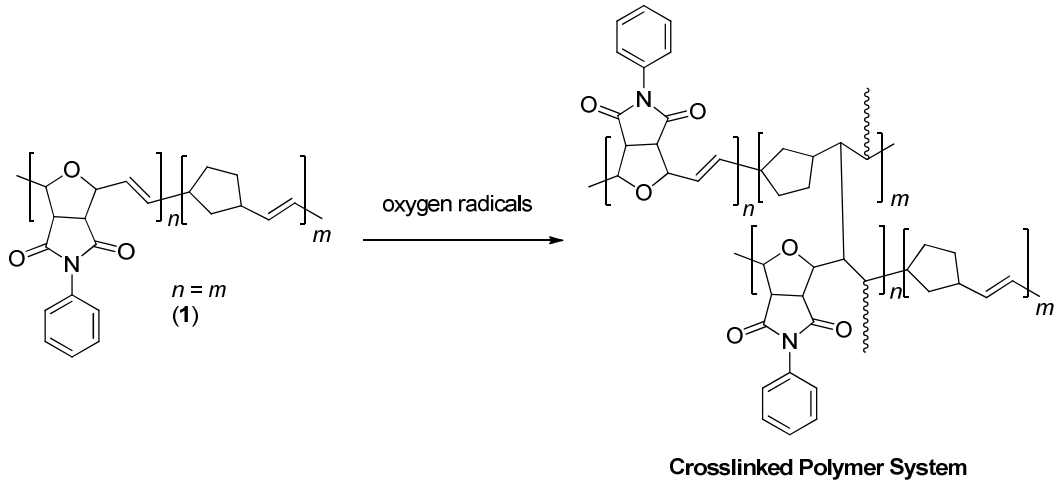

Fig. 3. Crosslinking reaction that results in polymer precipitation from casting solutions

Furthermore, several experiments were conducted where free radical inhibitors were added to the dielectric polymer solutions. In all cases, the polymer solution stability was greatly improved by the addition of free radical inhibitor to dielectric polymer solutions. These results further confirmed the suspicion that a free radical process was initiating a polymerization (or crosslinking) process that eventually leads to the polymer falling out of solution. Figure 4, shows two solutions of polymer both formed at concentrations of 7% (w/w). Solution A contained no free radical inhibitor, whereas, solution B contained the common free radical inhibitor 3,5-di-*t*-butyl-4-hydroxytoluene (BHT). Solution A became cloudy after 48 h, whereas the solution B was still transparent. Clearly, the solution that contained the free radical inhibitor was inhibiting the side reaction that was leading to crosslinking.

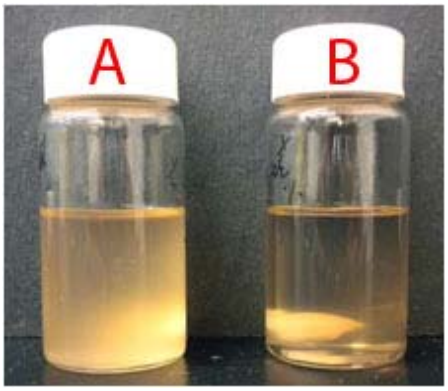

Fig. 4. A) Solution of polymer (7% (w/w)) dissolved in chloroform without removal of ambient atmosphere after 48 hours. B) Solution of polymer (7% (w/w)) containing (0.1 % (w/w)) 3,5-di-*t*-butyl-4-hydroxytoluene (BHT) dissolved in chloroform without removal of ambient atmosphere after 48 hours.

2.0. Polymer Hydrogenation

Polynorbornene based polymers are highly unsaturated polymers which are quite prone to oxidative degradation or crosslinking which limits solubility in organic solvents (as shown above). Removal of the reactive double bonds was evaluated as a potential method to enhance polymer solution lifetimes, improve processing, and film formation. Hydrogenation of the olefin containing polymers was accomplished using tosylhydrazide as the diimide hydrogenation precursor. The hydrazide undergoes decomposition at elevated temperatures to form diimide at high temperatures, which is the reactive species responsible for hydrogenation.[2, 3] In large-scale production, less expensive hydrogenation processes could be used such as hydrogen gas in combination with a heterogeneous or homogeneous catalyst.[4, 5] Hydrogenation of the polymer system **1** produced the desired hydrogenated polymer (**2**) which is shown in Figure 5.

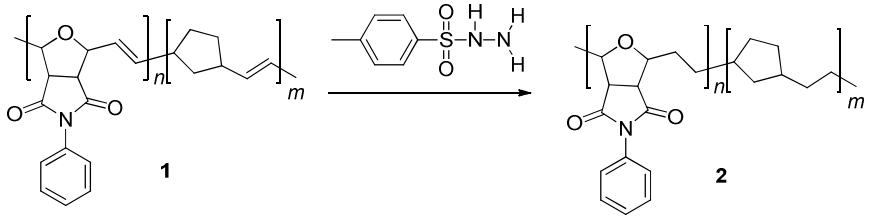

Fig. 5. Hydrogenation of a model polymer dielectric

Thermal characterization of polymer 2 where n = m produced a polymer with a relatively low glass transition temperature (T_g) 100 °C (data not shown) and capacitors produced using hydrogenated polymers with n = m failed at temperatures less than 150 °C. Thermal characterization of polymer 2

where m = 0, resulted in a polymer with a T_g of 250 °C (data not shown). Changing the copolymer stoichiometry to n = 3m, followed by hydrogenation resulted in a polymer with a T_g of 175 °C. Differential scanning calorimeter (DSC) data is shown in Figure 6.

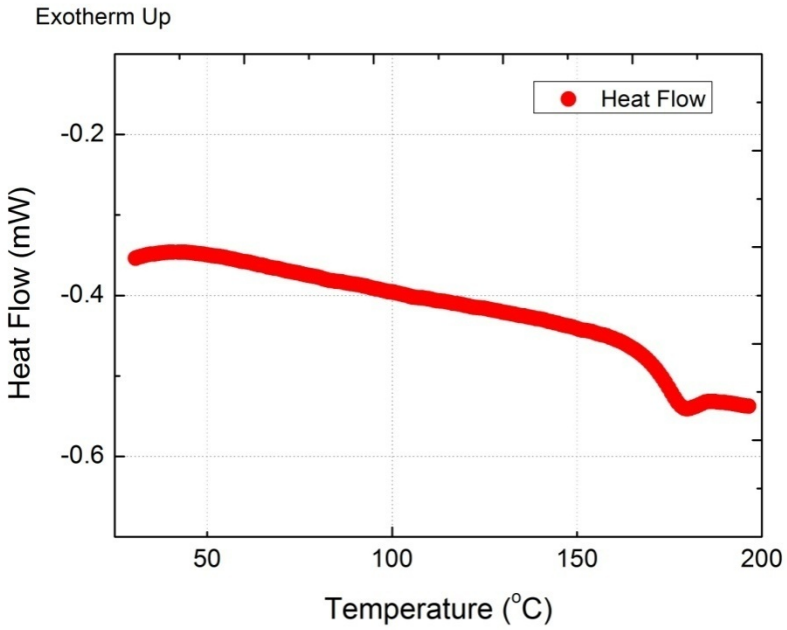

Fig. 6. DSC data on polymer 2 where n = 3m

Several small capacitors (50-70 pF) were prepared using copolymer 2 where n = 3m. Electrical characterization was performed as a function of frequency to determine what affect removal of the double bond would have on dissipation factor and the relative permittivity of the dielectric. Removal of the double bond decreased the relative permittivity of the polymer but had little effect on the dissipation factor as shown in Figure 7.

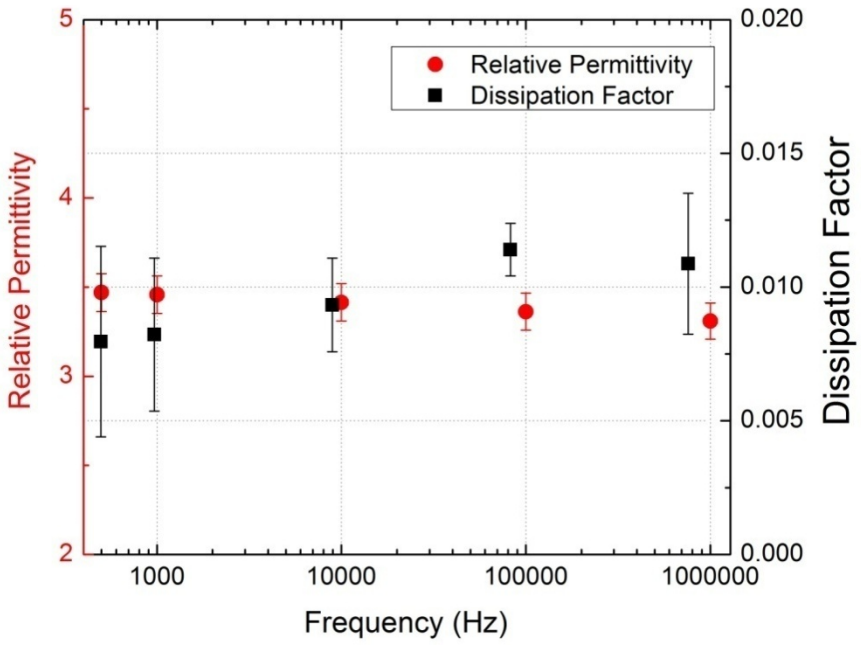

Fig. 7. Dielectric properties as a function of frequency

Twenty-four parallel plate capacitors were fabricated with top-side electrodes having diameters of 6.3 mm. The bottom electrodes were a continuous film. All electrodes were Au, deposited using a sputter coater at rate of 16 nm/min for a total Au thickness of 50 nm. The metalized dielectric film was placed on a Ni ground plate and the top electrodes were immersed in Fluorinert FC-40 (Aldrich) prior to electrical testing to prevent arcing and surface discharge. Weibull statistics were used to analyze the breakdown field, which was determined to be 2430 kV/cm (Figure 8), which results in a calculated energy density of 0.88 J/cm^3.[6-8]

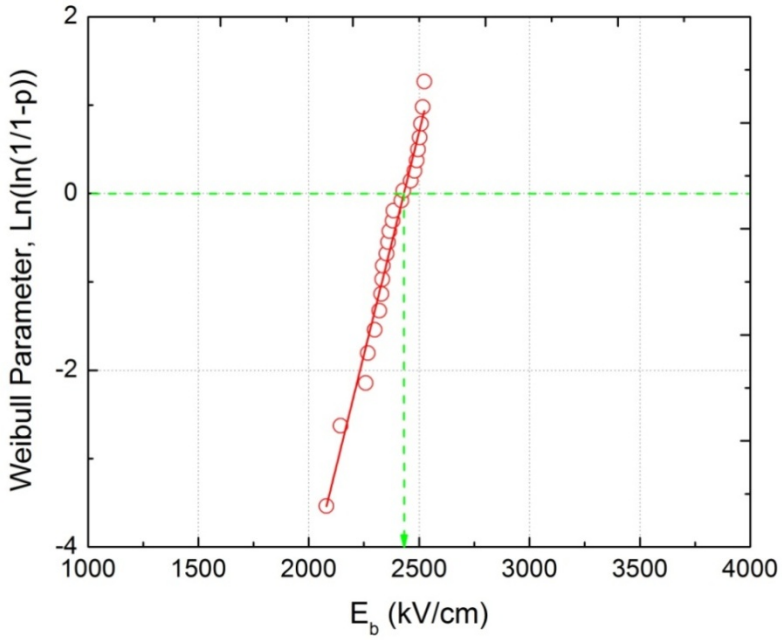

Fig. 8. Weibull distribution of capacitors formed using hydrogenated polymer with stoichiometry n = 3m

3.0. Stacked Capacitor Fabrication and Characterization

Multilayer stacked capacitors were fabricated using a hot press technique where the polymer dielectric (n = 3m, ~12 μm) was layered iteratively with discrete Al layers (5 μm thick). A schematic of the process is shown in Figure 9. Heat was applied to raise the temperature of the polymer dielectric above the polymer's T_g while applying a load of 500-1000 lbs. After pressing at temperature the dielectric/metal stack is cooled to room temperature prior to electrical characterization and evaluation. One dozen capacitors were fabricated using the discrete Al/polymer dielectric configuration. Capacitors fabricated using this technique had capacitances ranging from 2 to 16 nF depending upon the number of dielectric/Al layers.

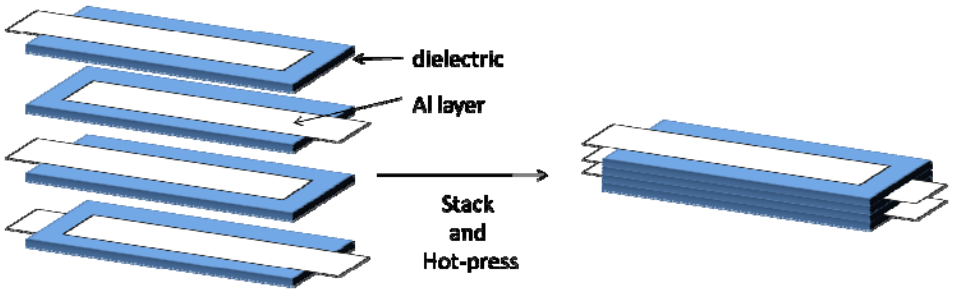

Fig. 9. Scheme for fabrication of larger value capacitors

An image of one of the many capacitors fabricated is shown in Figure 10. Device yield was only ~50% using the hot-press combined with discrete Al layers. These failures were mainly due to polymer/Al adhesion problems. Three working and electrically characterized devices were sent to ORNL for further characterization and evaluation.

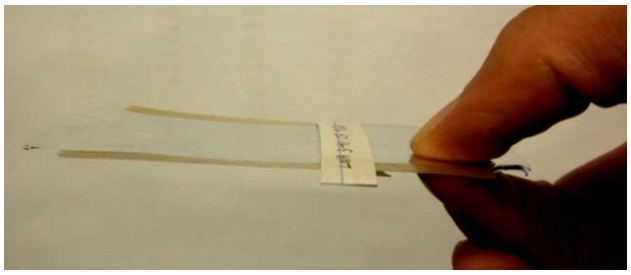

Fig. 10. Image of hot pressed stacked capacitor using discrete Al layers

Several stacked capacitors fabricated using discrete Al layers were characterized electrically at temperatures ranging from room temperature to 150 °C. None of the stacked capacitors failed when taken to a temperature of 150 °C. An example of the data collected for normalized capacitance and dissipation factor as a function of temperature are shown in Figure 11.

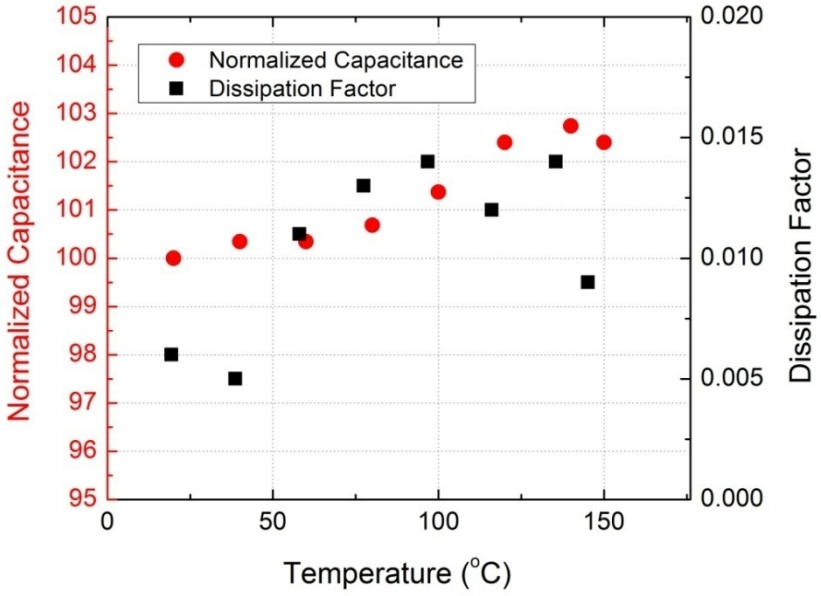

Fig. 11. Electrical Characterization of discrete Al based stacked capacitors.

Better yields for stacked capacitor fabrication were obtained when Au electrodes were sputter coated directly onto the polymer dielectric. Thin Au electrode films were deposited using a sputter coater at rate of 16 nm/min for a total Au thickness of 50 nm. Polymer films containing one Au electrode were stacked and then hot pressed with a force ranging from 500 to 1000 lbs. at a temperature above the T_g of the polymer dielectric. Silver filled epoxy was used to establish an electrical connection to half of the Au layers on one end of the stacked capacitor. The process was repeated on the other end of the capacitor to form a complete capacitor. Two capacitors were fabricated using this technique and each capacitor had a capacitance of between 5-6 nF. Fabrication of capacitors using the sputter coating technique resulted in a device yield of 100%. An image of capacitors fabricated using the sputter coating technique is shown in Figure 12.

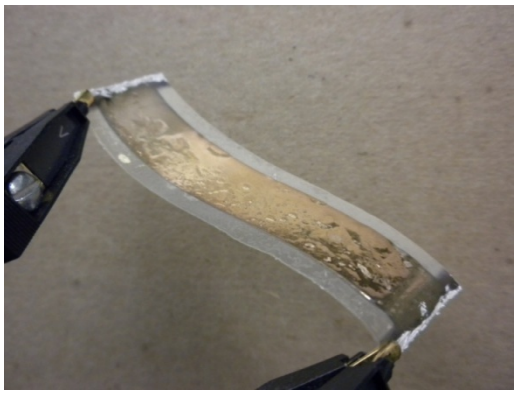

Fig. 12. Scheme for fabrication of larger value capacitors

4.0. Thiol-ene Coupling Reaction [9]

The thiol-ene reaction was also explored as a possible method to decrease the reactive olefin content completely in order to convert the material from a thermo-set resin to a thermoplastic. In order to achieve this conversion, 100% of the olefins needed to be converted to the desired thioether linkages. Initial experiments to remove the double bonds of polymer **1** resulted in only 15-25% of double bond functionalization (as shown in Figure 13). In all cases, polymers modified with the thiol-ene reaction were more soluble than the starting materials containing 100% olefin, however, we were unable to attain 100% thiol addition to the double bond due to the fact that the olefins were internal and the reactivity is decreased relative to terminal olefins. Olefin conversion up to 80% was accomplished.

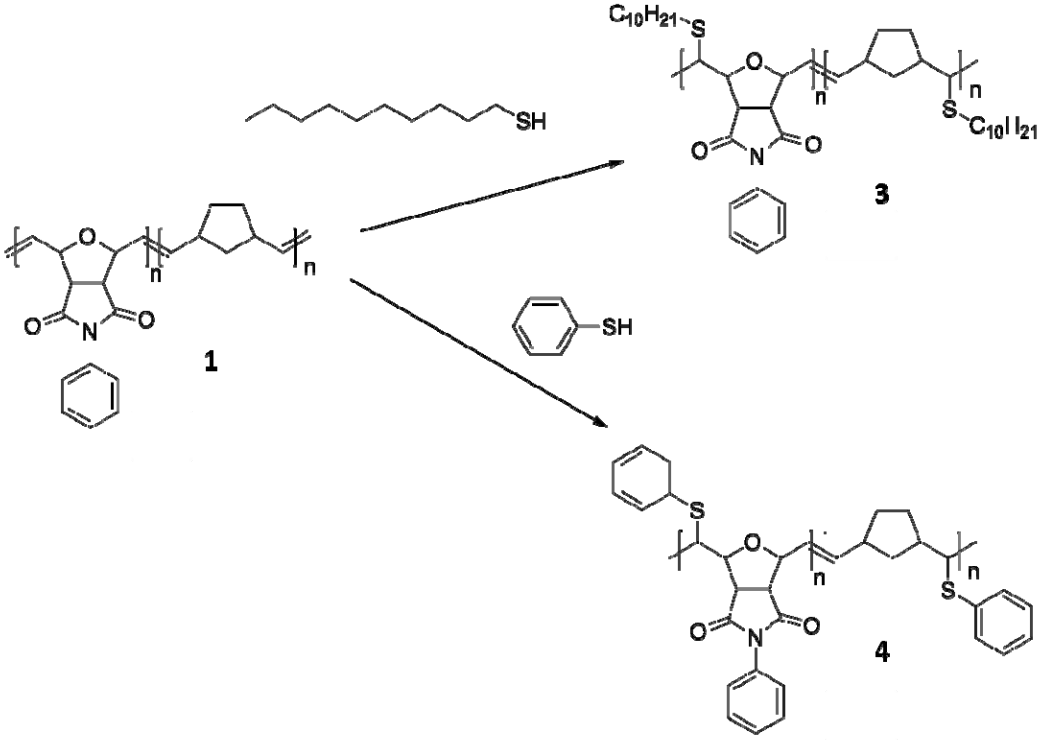

Fig. 13. Thiol-ene reactions in order to decrease reactive double bond content

Five small capacitors (50-70 pF) were fabricated using the procedure described above in Section 2. Electrical characterization of the capacitors fabricated using the thiol-ene modified polymers indicated that the decrease in olefin content decreased the relative permittivity and the dissipation factor while increasing the breakdown strength of the dielectric material.

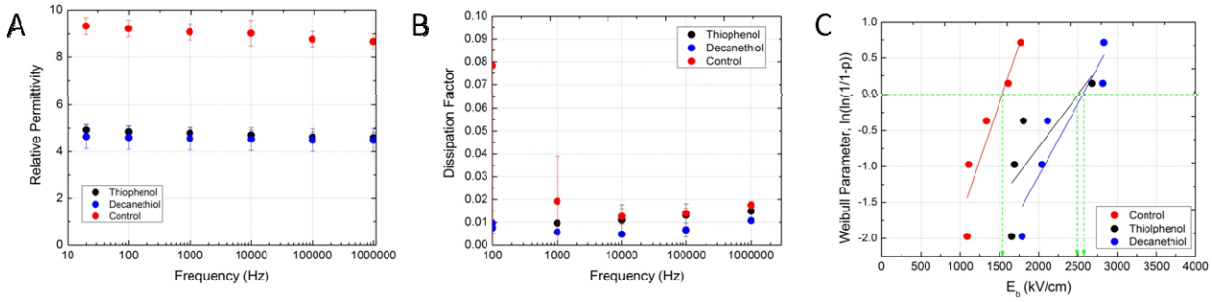

Fig. 14. Electrical characterization of polymer modified using the thiol-ene reaction A) Relative permittivity B) Dissipation factor and C) Dielectric breakdown

Conclusion

We have developed a novel polymeric material that has superior high temperature dielectric properties. We are working with and industrial partner (ECI) to fabricate large rolls (> 100 m length) of polymer dielectric film leading to prototype capacitor fabrication. Through this industrial interaction we have identified an oxidative free radical induced crosslinking/degradation reaction leading to decreased polymer solution lifetimes. We have explored the thiol-ene reaction as well as hydrogenation to remove the reactive double bonds within the backbone of the polymer. Hydrogenation was determined to be the preferred method to modify the dielectric polymer to improve processing and was accomplished using a diimide based hydrogenation reaction. Hydrogenated dielectric polymer with stoichiometry n (imide) = m (norbornene) had a T_g of 100 °C, which was too low for high temperature operations. Changing the polymer stoichiometry to n = 3m, followed by hydrogenation resulted in the formation of a polymer with a T_g of 175 °C. Several stacked capacitors were fabricated and the electrical performance was characterized as a function of temperature. Capacitors fabricated in this manner were also sent to ORNL for further characterization. Work for FY11 will focus on the scale-up of the hydrogenated polymer synthesis followed by and production of large lengths of polymer thin film. The thin dielectric film will be used for the fabrication and characterization of capacitors with capacitances >1 μF. In addition, further improvements in the relative permittivity and breakdown strength will be gained by the incorporation of dispersed nanoparticles. These high temperature, thin film, polymer dielectrics will be used to fabricate high temperature DC bus capacitors with significantly reduced size and weight, and improved performance and reliability.

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Patents

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2.12 Glass Ceramic Dielectrics for DC Bus Capacitors

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Objectives

Commercial capacitors for hybrid electric vehicles (HEVs) and plug-in hybrid electric vehicles (PHEVs) do not meet US automaker's specifications for high temperature operation, cost and reliability. The objectives of this project are to develop high temperature capacitors that go beyond what is commercially available and to minimize the need for costly coolant systems within the HEVs and PHEVs. Ceramic capacitors have excellent high temperature performance and meet a majority of HEV and PHEV specifications for power electronic converters; however, low reliability is a primary impediment to their use in hybrid vehicles. The goal of this project is to produce reliable glass capacitors without compromising the energy density (related to capacitor volumetric efficiency). Specific goals include:

- Characterize the thickness and temperature dependence of dielectric breakdown of commercial flat panel display glass that is manufactured by Corning, Schott, and Nippon Electric Glass.
- Collaborate with Argonne National Laboratory to understand coated conductor breakdown strength and reliability.
- Commercialize glass capacitor technology by collaborating with glass manufacturers and capacitor companies.

Approach

- Adapt low-cost production methods and materials, already developed for flat panel displays, to high temperature capacitors.
- Characterize glass materials at high temperature to project reliability.
- Develop benign failure modes in glass capacitors to avoid catastrophic failure.
- Manufacture prototype capacitors in collaboration with industrial partners.

Major Accomplishments

- Demonstrated that flat panel display glass can operate as a capacitor up to temperatures of 250 °C.
- Demonstrated thickness dependent dielectric breakdown and the statistics for making glass capacitors more reliable
- Demonstrated self-healing in a glass capacitor

Future Direction

- Scale-up glass capacitors to 10 µF 1,000 V levels - large-scale capacitors that are based on flat-panel display glass will require a multilayer construction. This project will develop robust terminations for multilayer glass capacitors.
- Penn State has been working with flat-panel display manufacturers to reduce the glass layer thickness. Currently 50 µm thick glass sheets are available and 10 µm thick sheets have been fabricated at the laboratory scale. The final design for a high-temperature DC link capacitor will require glass layer thicknesses between 5 and 10 µm.

Technical Discussion

There is general agreement within the automotive and power electronic communities that revolutionary approaches, drawing on diverse disciplines, will be necessary to develop the next generation of power systems for electric vehicles. New active and passive components need to be manufactured which can operate at high temperature for long periods of time. In addition, component miniaturization is important to reduce the total volume of the power electronic circuitry on board an electric vehicle. A summary of the results of this study is shown in Figure 1.

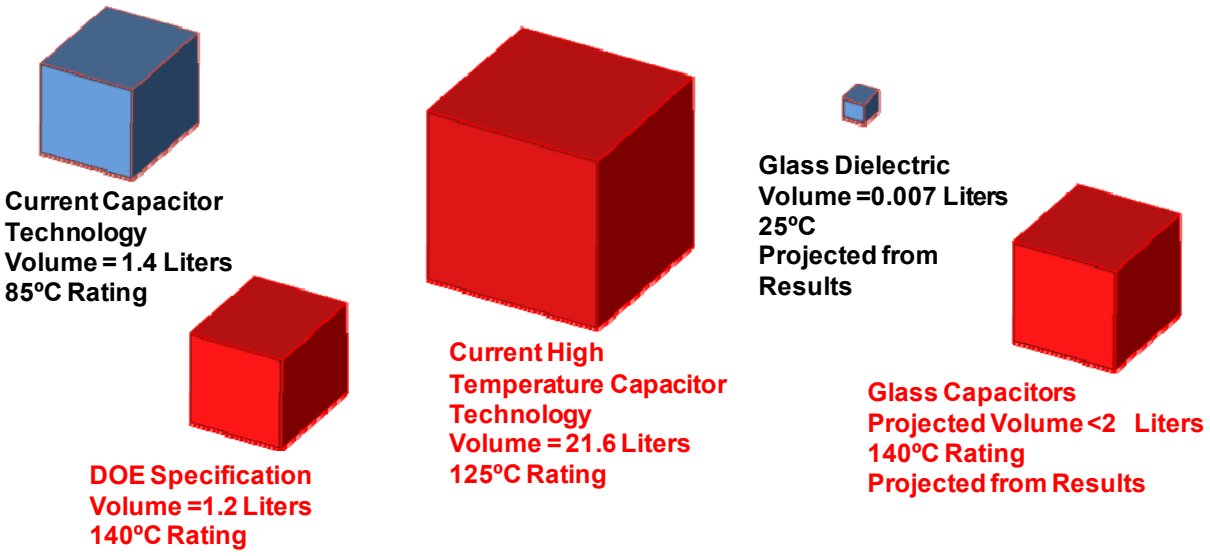

Fig. 1. Volumetric comparison between DOE capacitor specifications, commercial capacitors and the projected capacitor volumes from the research at Penn State. All volumes shown are for a 1000 µF 1000 V capacitor.

The DOE specifications (Figure 1 lower left corner) were derived from discussions with the EE tech team and component manufacturers. Presently, high-temperature film capacitors (middle of Figure 1) have 18 times the volume of the DOE specification. The glass dielectrics explored in this study have the potential to operate above 140ºC and the volume is much smaller than commercial high temperature capacitors (Figure 1 right side).

Thin glass sheet production has grown substantially because of strong demand from the flat panel display industry and a $30 billion investment in the development of new glass fabrication methods [1]. Glass manufacturers have been able to develop a continuous sheet casting process with sufficient control to make significant lengths of thin flexible sheet (Figure 2). Within the past 2 years, Penn State has utilized an etching technique to reduce the commercially available glass thicknesses from 50 μm to 5 μm (Figure 2). The thickness reduction is a key factor in increasing the dielectric breakdown strength and the mechanisms associated with this improvement are under investigation.

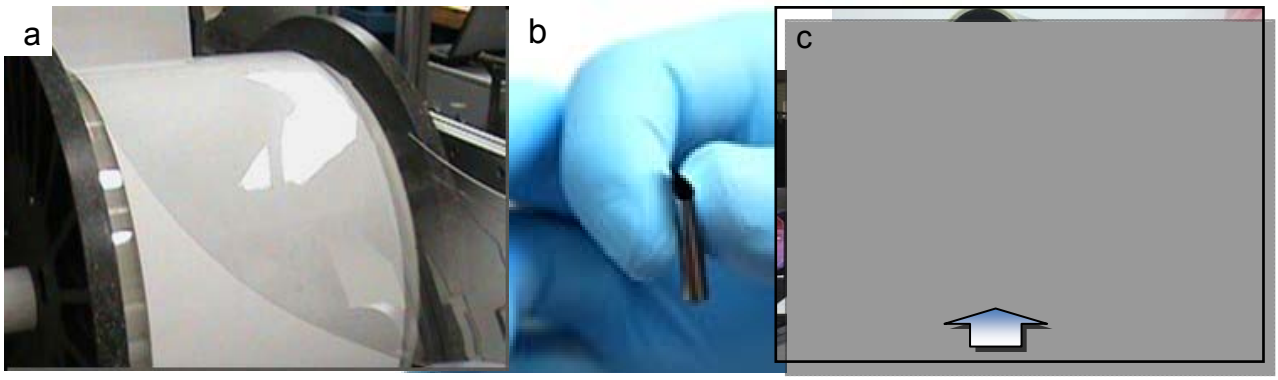

Fig. 2. (a) Corning announced that it has developed a flexible glass substrate that can be used for printed electronics applications [2]. The glass manufacturer says the product performs like glass and is as flexible as plastic. (b) Demonstrating the mechanical flexibility and strength of chemically etched 10-μm thick glass sheet. Glass was etched at PSU. (c) First glass rolls made by NEG Corporation. The glass sheet is 150 meters in length[courtesy of T. Murata].

The self-healing mechanism for the thin glass capacitor was explored in detail. Visual damage for 56 to 120 spots for each breakdown event was inspected and categorized as either self-healing (Figure 3a) or catastrophic (Figure 3b). Detrimental cracking of the glass layer and inadequate conductor clearing are observed after a shorting dielectric breakdown. We anticipate that many of the benefits that are common in polmer capacitors (enhanced large-scale manufacturing and ease of graceful failure) will be achievable in a glass capacitor.

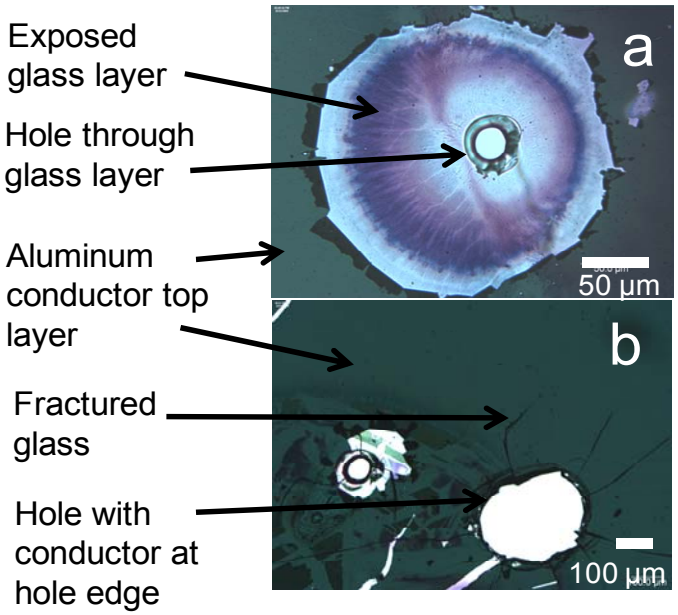

Fig. 3. (a) Self-healing and (b) catastrophic dielectric failure modes in a 15 μm thick glass layer with evaporated 10 nm thick aluminum electrodes. Figure 3a shows a classic self-healing mode with a significant clearing of the electrode away from the glass and very little damage to the glass. Note that the hole has a ring of glass that has melted during the breakdown event. Figure 3b illustrates extended fracture due to thermal shock and the electrodes cover the entire glass layer except for the hole created by breakdown. Note a significant cracking in the lower left hole for Figure 3b.

The percentage of self-healing spots plotted as a function of sample thickness is shown in Fig. 6. The percentage of self-healing spots increased with decreasing glass thickness and reached 58% for a glass thickness of 10 μm.

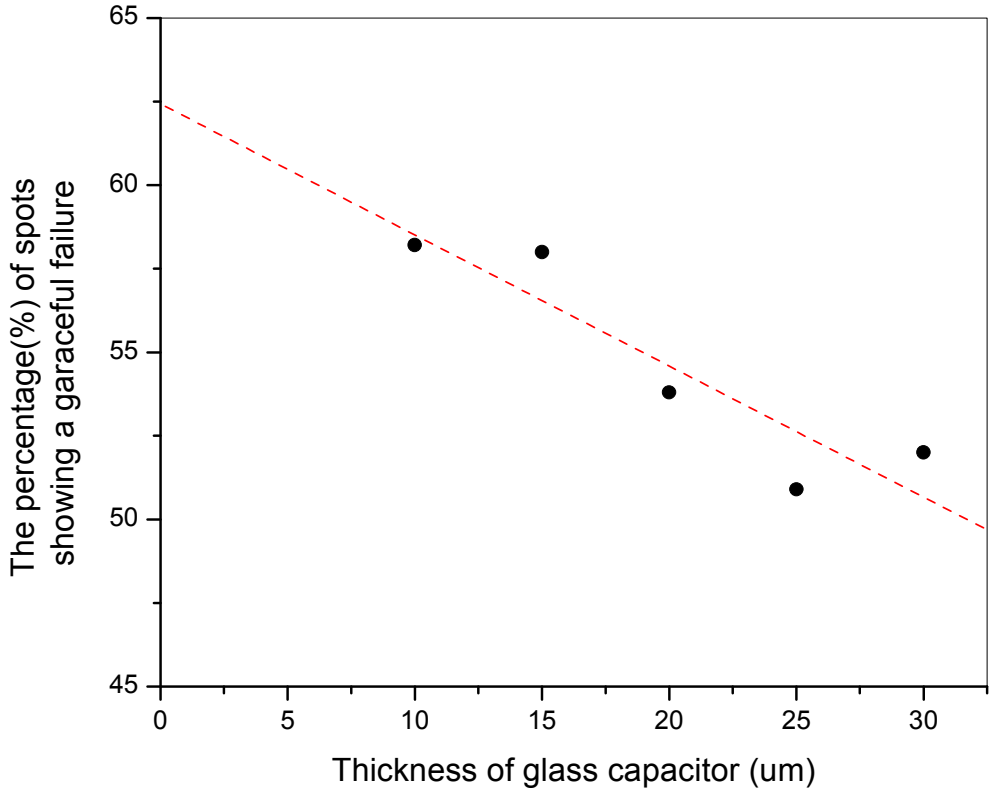

Fig. 4. Percentage (%) of spots showing graceful failure for thinned glass sheet

The condition for self-healing breakdown is is given by:

$$\frac{\varepsilon_0 \varepsilon \rho_m A_C \log(A_C / A_m)}{8\pi \rho_i h_m^2} F_B^2 \geq q_m \qquad (1)$$

where A_c and A_m are the capacitor area and metal hole area, respectively; h_m is the thickness of a metal electrode; ρ_m and ρ_i are the resistivity of metal and insulator channel, respectively, on breakdown; ε_0 and ε are the permittivity of free charge and the relative permittivity, respectively; and q_m is the latent heat of vaporization of the metal. The left side of the equation is the energy delivered to the self- healing process and the right side of the equation is the amount of energy required for electrode clearing.

The area of the hole evaporated (A_m) in the electrodes should be significantly larger than the cylindrical hole of area A_s in the insulator after discharging. Equation 1 shows that the likelihood of graceful failure is proportional to the square of breakdown field (F_B). The left term of equation (1) was calculated with experimental data as a function of glass thickness and is shown in Fig 7. In the calculation, the increase of dielectric constant according to temperature was not taken into account. The estimated resistivity of a

gold electrode (1×10^{-5} Ωcm) and glass (1×10^{2} Ωcm) at 1500 K were used as the resistivity of metal/insulator channel on breakdown. The values of the left term (condition for self-healing breakdown) increases with decreasing glass thickness which is primarily correlated with the electric field, F_B^2.

Equation 1 also supports the fact that self -healing is promoted for additional energy terms on the left side of the equation. For example, a favorable chemical reaction (e.g. redox reaction) will increase the magnitude of the left side of equation 1. Ablation processes will decrease the value of the right side of equation 1, effectively increasing the driving force for self- healing. The high dielectric breakdown strength in conjunction with a relatively high permittivity, results in energy densities of 38 J/cm^3.[1] The local energy released during breakdown heats the electrode and glass in the defect region. Therefore, the self-healing condition is determined by the breakdown strength of glass for a given electrode composition and thickness. Gold electrodes were used in this study and the electrostatic energy supplied during breakdown exceeds the latent heat of vaporization of gold (3.17×10^{10}J/m^3) for all cases. The latent heat of vaporization of quartz, which has a high melting temperature compared to the glass used in this work, is 1.57×10^{10} J/m^3.

A potential design of a self-clearing high energy glass capacitor is shown generally in Figure 5. The capacitor structure has a glass layer with a polymer layer attached to one side and another polymer layer attached to opposite side. Extending across the layers is a top electrode and a bottom electrode as illustrated in the figure. Regarding the interfacial bond layer, a range of polar molecules can be bonded to the glass layer. For example and for illustrative purposes only, highly polar 3-aminopropyl-triethoxysilane (APTES) or low polarity heptadecafluoro-1,1,2,2-tetrahydrodecyltrimethoxysilane (HTDF) can be attached to a hydroxylated glass surface. In addition, polymer layers can bond to the glass through an interfacial silane coupling agent and the electrical properties of the laminate can be controlled through the interfacial bond layer.

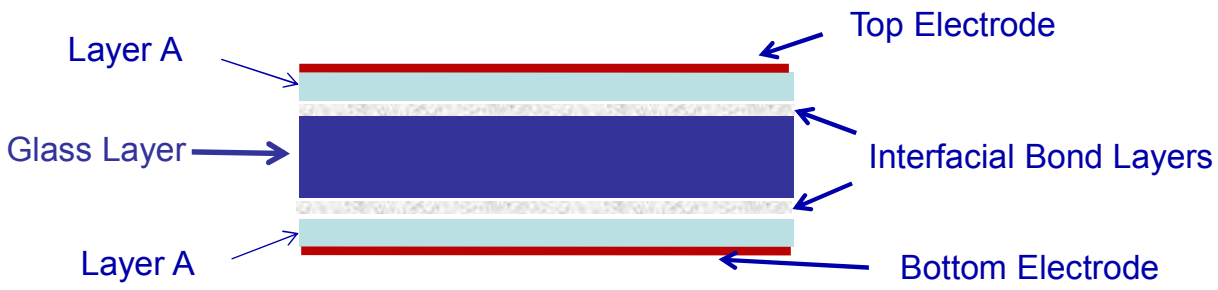

Fig. 5. Schematic of a capacitor cross section with a polymer (layer A), interfacial bond layers (surfactant) and glass.

Figure 6 illustrates clearing area (Sv) for a self-healing dielectric breakdown as a function of breakdown strength for plain etched glass, etched glass with an 3-mercapto-propyl-trimethoxy-silane (MPTMS) coating and etched glass with an APTES coating. As shown in this figure, the etched glass with an interfacial bond coating provides a higher clearing area than the uncoated glass, thereby showing the improvement of interfacial bond layer use.

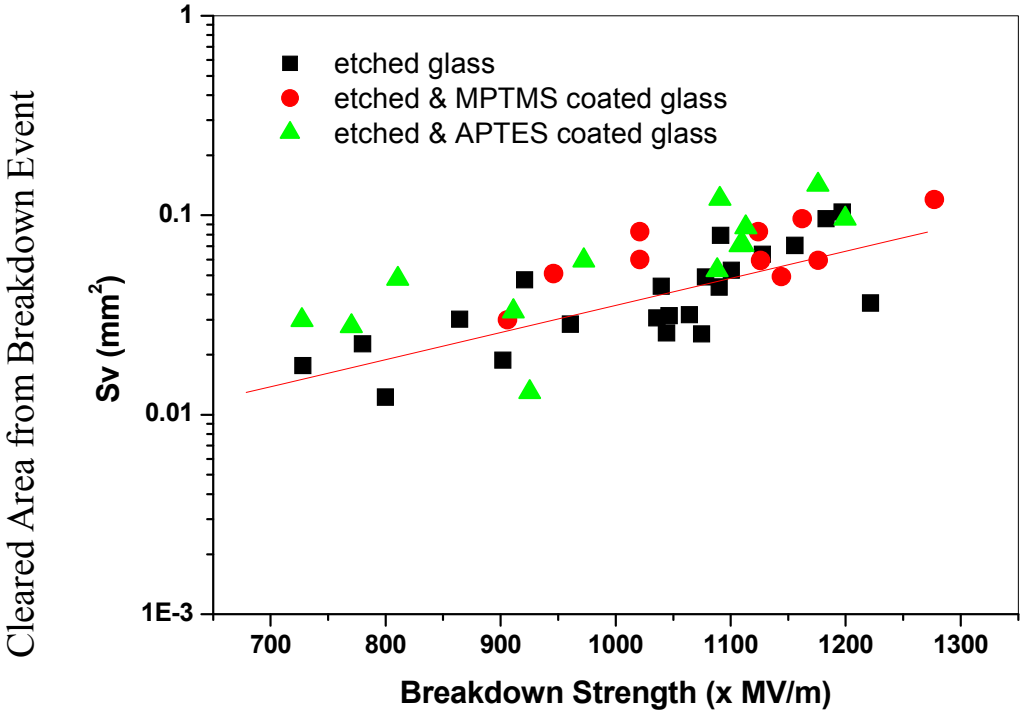

Fig. 6. Clearing area (see figure 3a for demonstration) for uncoated and polymer coated class samples. Note that the black squares are generally lower than the green triangles or red circles. Dielectric breakdown is a statistical process that has a range of dielectric breakdown strengths.

Conclusion

The outcome of this project is a cost effective manufacturing process for high temperature capacitors that will meet the US automaker specifications for HEV and PHEV applications. Penn State has collaborated with several industrial partners including large raw materials manufacturers (NEG, Corning Inc. and Schott Glass USA) and small capacitor manufacturers (Strategic Polymer Sciences Inc.) to investigate reliable prototype capacitors from glass-ceramic materials. Penn State has developed a polymer/glass composite laminate that promotes self-healing and this technology is currently being explore for large scale glass capacitors.

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2. B. Rangarajan, S.S.N. Bharadwaja, E. Furman, T. Shrout and M. Lanagan, "Impedance Spectroscopy Studies of Fresnoites in BaO-TiO2-SiO2 System," J. Amer. Ceram. Soc., 93(2):522-530, 2010.

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2.13 Development of SiC Large Tapered Crystal Growth

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Objectives

- **Demonstrate initial feasibility of totally new "Large Tapered Crystal" (LTC) approach for growing vastly improved large-diameter wide-band gap wafers.**
- Open a new technology path to large-diameter SiC and GaN wafers with 1000-fold defect density improvement at 2-4 fold lower cost. This would enable a leapfrog improvement in wide band gap power device capability and cost.

Approach

- Experimentally investigate and demonstrate the two key unproven LTC growth processes in SiC:
  - Laser-assisted growth of long SiC fiber seeds.
  - Radial epitaxial growth enlargement of seeds into large SiC boules.

Major Accomplishments

- **Completed major design and hardware modifications of two NASA Glenn crystal growth laboratories:**
- Major modifications to NASA Glenn SiC Growth Reactor #2 have been implemented (95% complete).
  - Modifications needed for experimental demonstrations of LTC radial growth enlargement of SiC fibers into boules.
  - Fundamental change in configuration from cold-wall with pancake coil RF heating to hot-wall with barrel coil RF heating.
  - First growth experiment carried out on SiC saw-cut pseudo-fiber October 2010.
- Design and build-up of laser-heated SiC fiber growth system has been implemented (95% complete)
  - Needed for experimental demonstration of LTC fiber growth process.
  - First attempt of Solvent-Laser Heated Float Zone fiber growth to be conducted November or December of 2010.

Future Direction

- Use newly constructed hardware to demonstrate, for the first time, that both fiber and radial SiC growth processes can be successfully carried out. This would experimentally establish feasibility of the two critical LTC processes. (FY11 – in current NASA/DOE Agreement).
- Launch joint development of full prototype LTC SiC growth system (simultaneous fiber growth + lateral growth to grow full prototype SiC boules) in collaboration with commercial and/or university development partners (FY12-13 - beyond current NASA/DOE agreement).
- Explore GaN LTC experiments. (FY13-14 - beyond current NASA/DOE agreement).

Technical Discussion

Technical Motivation

It is generally accepted that the use of silicon carbide (SiC) power electronics could enable power systems that are significantly more efficient, lighter, and smaller than systems based on silicon (Si) electronics. Although some SiC devices (e.g. Schottky diodes and field-effect transistors (FETs)) have been developed, the energy-saving performance and reliability of SiC power devices are significantly degraded, and device cost significantly increased, because of a high density of dislocation defects (> 1000 per cm^2) in all commercially-available SiC semiconductor wafers. Eliminating these defects economically (i.e., down to densities < 1 per cm^2 while greatly lowering SiC wafer cost) would unlock SiC's enormous (as yet unfulfilled) promise to revolutionize nearly all high-power electronic systems.

The reason for the high density of defects in commercial SiC wafers is that all current approaches for growing single-crystal SiC boules are fundamentally flawed. The problem with current SiC growth processes is that a high-density of screw dislocation defects (on the order of 10^2 to 10^4 per cm^2) is necessary in order to achieve commercially viable SiC wafer growth rates. Unfortunately, many researchers (including NASA) have now shown that these same dislocation defects harm the yield, performance, reliability, and commercialization of SiC high power devices. If SiC is to fulfill its huge theoretical power device promise, SiC wafer dislocation densities must be brought down 100-1000 fold via a totally new crystal growth approach, yet be able to mass-produce larger-area wafers (at least 6-inches in diameter) at significantly lower cost.

Technical Approach and Progress

A. Introduction to Large Tapered Crystal (LTC) Growth

A NASA Glenn Research Center (GRC) team (J. A. Powell, P. G. Neudeck, A. J. Trunek, D. J. Spry) recently patented (US Patent 7,449,065) a radically different, SiC crystal growth concept that can mass-produce large-diameter SiC wafers wherein each wafer ideally contains only a single screw dislocation (in the center of the wafer). This new growth concept utilizes a revolutionary seed crystal configuration and two simultaneous growth processes in connected chambers for rapidly growing large single-crystal SiC boules with only one centrally-located screw dislocation. Because this new process grows a large crystal with a tapered shape, we have named this the Large Tapered Crystal (LTC) growth process. The crystal growth initiates from a small-diameter fiber (with a single screw dislocation at its core) that is grown in a first chamber, from which it is withdrawn, as it elongates, into a second growth chamber where radial growth on the fiber produces a large tapered crystal. Each growth run produces a low-defect (ideally with a single screw dislocation) SiC crystal boule (100 mm diam.) at the top end of the LTC. A comprehensive technical description of the process and apparatus involved can be found in US Patent 7,449,065 that is now available online at the U.S. Patent Office website http://www.uspto.gov. This section presents a highly condensed summary of the contents of the patent.

Fig. 1 illustrates schematic cross-sections of SiC crystals during steps S1, S2, and S3 of the LTC growth process. Each LTC growth cycle starts with a large tapered crystal (LTC) as the seed crystal as shown in Fig. 1(a). The central axis of the LTC seed will be parallel to the crystallographic c-axis. During a growth step S1, the small end (the fiber portion in chamber 1), as shown in Fig. 1(b), will be grown in the c-direction and maintained at a diameter of less than 1 mm; the large end of the LTC will be maintained at some designated large diameter (e.g. 100 mm for commercial systems). Simultaneously with the axial growth of the small-diameter fiber in chamber 1, radial epitaxial growth enlargement of the large tapered section takes place in a growth chamber 2 during a growth step S2. Ideally, only a single screw dislocation (along the central axis) will be present in the entire crystal. This single screw dislocation provides the necessary crystal stacking sequence for a given SiC polytype. This stacking sequence also establishes the sequence of atomic steps that propagate radially during growth in chamber 2. It is

important to note that defects (i.e., screw dislocations) are not required for the radial growth in chamber 2. Indeed, the bulk of the crystal boule (except for the very small volume of the central fiber) is deposited by "step-flow growth" in chamber 2 (utilizing the crystal stacking sequence established by the small-diameter fiber).

Typically, the vertical growth rate parallel to the c-axis (on the small tip) will be much greater (e.g. the order of 1 mm/hour) than the radial epitaxial growth rate. Because of the large surface area of the tapered portion, moderate radial growth rates (e.g. about 0.1 mm/hour) will yield rapid bulk growth of the LTC in chamber 2. As growth proceeds in steps S1 and S2, the top of the tapered crystal enters an isothermal chamber 3 of inert gas atmosphere where no additional SiC is deposited. This enables a cylindrical (hexagonal cross-section) crystal boule to form as the large end continues to exit chamber 2 into the "no-growth" isothermal chamber 3. The top of the crystal is physically moved upward during growth steps S1 and S2 so that the bottom of the downward-growing small-diameter tip is maintained at the same position inside chamber 1.

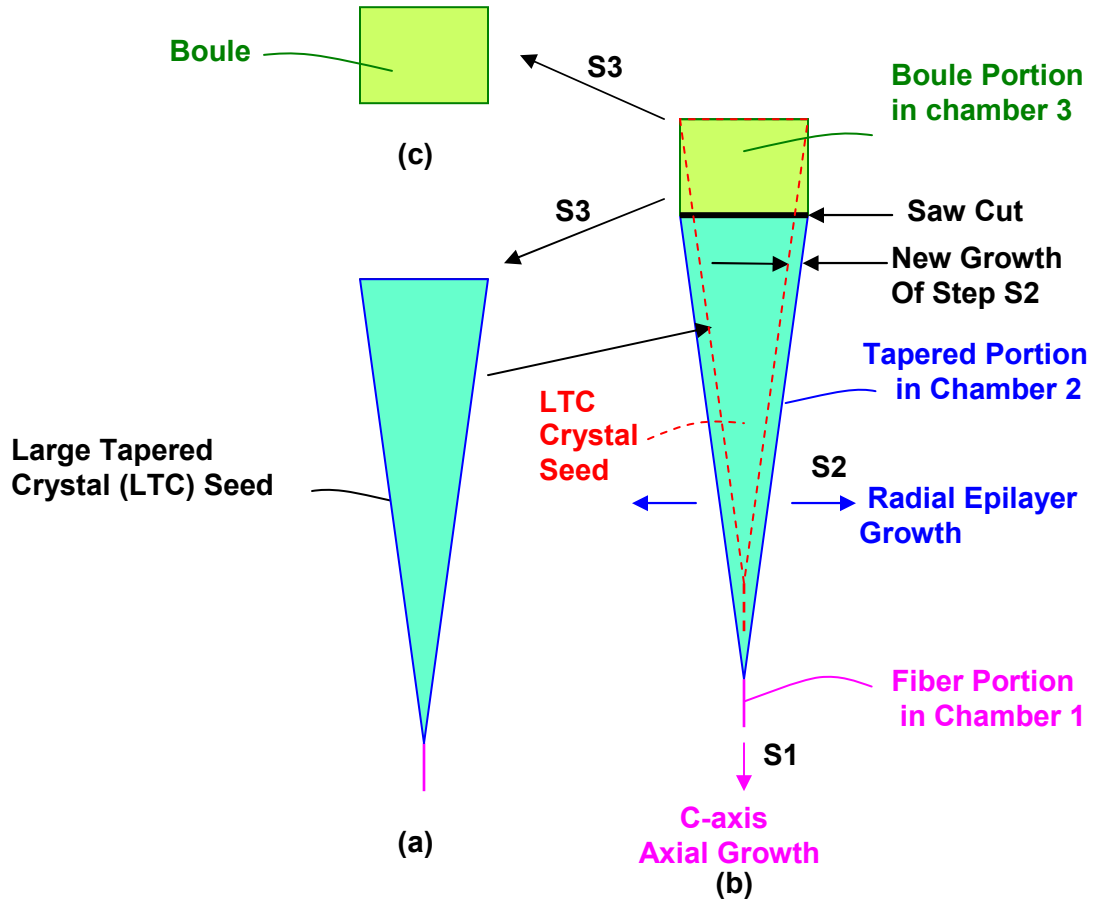

Fig. 1. LTC Growth Process

At the end of each growth cycle, the boule portion will be cut from the whole crystal in step S3 (Fig. 1c), and the remainder of the LTC will be used as a seed crystal in steps S1 and S2 of a subsequent growth cycle. Note that in a subsequent growth cycle, the large end (the boule end) of the LTC seed will immediately begin growing in the c-axis direction at the same growth rate as the rapid growth of the LTC

fiber end. Additional advantages of the LTC process are that boules can be grown at high growth rates and the process can easily be scaled up to larger diameter boules, resulting in increased wafer size and reduced wafer cost. Also, the process should be capable of boules of much greater length than is possible with current SiC growth techniques. Note that only the very first LTC seed crystal will need to be grown in a preliminary and separate process from the LTC process cycle depicted in Fig 1.

The LTC growth process as presented above relies on two separate high-quality SiC growth processes taking place on different surfaces/regions of the same crystal, namely (S1) c-axis fiber growth and (S2) radial epilayer growth. Neither of these processes has been experimentally attempted or demonstrated for SiC in the manner/configuration that is proposed above. Therefore, the immediate first objectives of this work is to separately demonstrate, for the first time, that both of these new SiC growth processes can be successfully carried out.

B. SiC Fiber Growth by Solvent-Laser Heated Float Zone Growth

A key (and most challenging) aspect of demonstrating the viability of the LTC process is the demonstration of rapid growth (on the order of 1 mm/hour in the crystal c-axis direction) of a single-crystal SiC small-diameter fiber containing a single screw dislocation (i.e., demonstrating growth S1 of Fig. 1). The basic feasibility goal of initial fiber growth work under this project is to demonstrate single crystal SiC fibers of at least 100 mm in length. To achieve this, a growth a method has been chosen which combines the advantages of two well know growth methods: Laser Heated Floating Zone (LHFZ – proven for oxide-based crystals) [1] and Traveling Solvent Method (TSM – demonstrated for SiC) [2] which we have named Solvent-Laser Heated Floating Zone (Solvent-LHFZ).

Solvent-LHFZ of SiC (depicted schematically in Fig. 2) uses a laser to melt a feed rod composed of source material and metal solvent for crystal growth. The use of a metal solvent to grow SiC has been successfully used as a way to work around the lack of ability to melt SiC as a source material, and solubility of C in Si [2]. Once melted, a SiC seed crystal is dipped into the melted source material (wetting to the seed crystal), and then pulled away. As the seed is pulled away, the liquid source material cools, solidifying on the crystal forming the fiber. As the source material is consumed, more source material is fed into the melt so that the growth proceeds continuously well beyond consumption of volume of the original melt. This technique has the advantage of relatively unlimited source material (feed rod) from which to grow, so that resulting SiC boules could be made orders of magnitude longer than manufactured today leading to significant manufacturing cost savings. The SiC seed crystal determines the orientation and structure of the grown crystal. SiC is known to grow along the <0001> "c-axis" crystallographic direction with the assistance of screw dislocations. Researchers at NASA Glenn Research Center (GRC) have learned how to isolate and grow a single screw dislocation into short mesa seed crystals, such as show in the inset to Fig. 2. These seed mesas will provide the crystallographic basis for a continuous fiber to be grown in the c-axis direction.

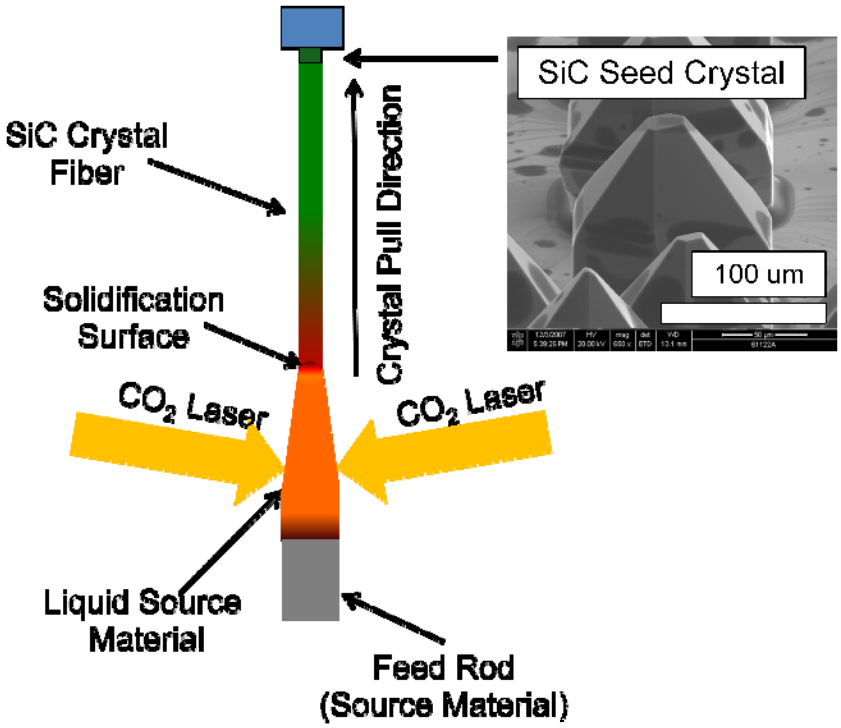

Fig. 2. Solvent Laser Heated Float Zone (Solvent-LHFZ) approach for growing single-crystal SiC fibers.

The system designed, purchased/fabricated and assembled to perform solvent-LHFZ is shown in Fig. 3. It can be broken down into three systems: vacuum/pressure management, optical, automation/data collection. The vacuum/pressure management system's main purpose is to eliminate reactants which are counterproductive to SiC growth, specifically H_2O andO_2. To this end, the growth chamber is designed to be evacuated (pressure less than 100 µTorr, and then flow an inert gas (argon) thru the chamber during growth. The optical system is designed to focus and bring the laser beam (CO_2 laser, wavelength = 10.6 µm) into the growth chamber in order to create a heated zone 1-2 mm high and 2-4 mm wide. Finally, the automation/data collection system will control the growth conditions (crystal pull rate, source material feed rate, chamber pressure and argon flow) while recording the growth (via a long range optical microscope), and chamber pressure and other growth parameters.

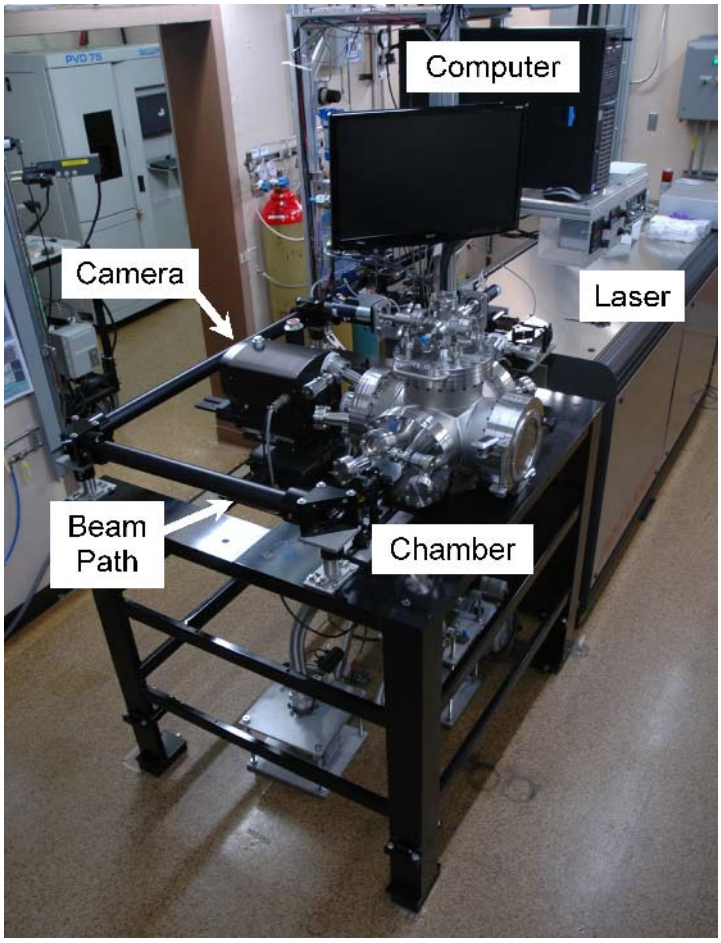

Fig. 3. Solvent-LHFZ system featuring growth chamber, high power CO_2 laser, beam path, long range optical microscope camera, and automation/data collection computer.

During FY10 the design, purchasing, fabricating and assembling of the Solvent-LHFZ system was completed. The buildup of this system used roughly $125,000 of new equipment (purchased once Dept. of Energy project funds became available), and $140,000 of repurposed NASA equipment. Also Si-C-solvent systems have been identified which lead to the development specific elemental feed rod compositions which will be used in the initial experiments. Currently under development is the automation/data collection software, specifics of the feed rod processing, and the seed crystal processing (building on significant amounts of expertise exist at NASA GRC). Following final pending approvals from NASA GRC Safety office, initiation of first Solvent-LHFZ SiC fiber growth experiments should occur in November or December of 2010.

C. SiC Radial Growth via CVD Epitaxy

The vast majority of the LTC boule will be deposited via epitaxial radial growth via CVD during step S2 (in chamber 2, Fig. 1b). Fig. 4 illustrates the 3-dimensional shape of the LTC boule that we expect to produce. The LTC boule is expected have a hexagonal cross-section whose outer surfaces will be "M-planes". The radial growth deposition enlarging the fiber into a boule as it is pulled through Chamber 2 is expected to produce "Off-M" crystal surfaces that are slightly tilted (the order of 6º) off of the 4H-SiC "M-planes" toward the C-axis. **Because epitaxial growth on large-area 4H-SiC surfaces with this particular orientation have never been investigated, it is vital in this initial project to demonstrate that excellent (essentially defect-free) epitaxy can be achieved at sufficiently high growth rates (on**

the order of 50 to 100 um/hour) on these surface orientations. In particular, the project is slated to grow small-diameter fibers (or simulated fibers cut from larger SiC crystals) into 5 mm diameter or larger demonstration boules.

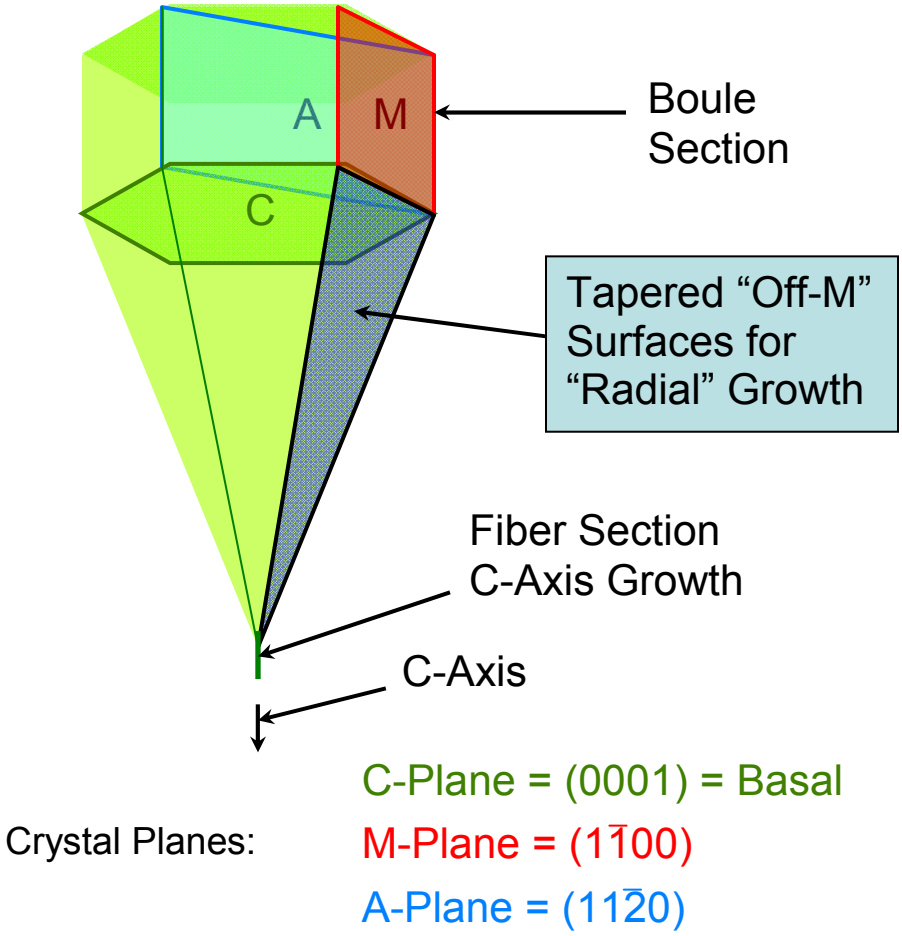

Figure 4. Boule shape and crystal planes pertinent to LTC radial growth process.

Until high quality SiC fiber crystals are grown, development of the radial growth process will proceed using simulated "pseudo-fiber" SiC crystals that simulate/mimic the growth surfaces illustrated in Figure 4. Towards this end "a-face", "m-face", and "off-m" face oriented 4H-SiC and 6H-SiC crystals cut and polished from prototype boules have been ordered from Aymont Technology. Some A-face and M-face crystals delivered to NASA have been cut into strips forming physically "flat toothpick" small crystal fibers. While these "pseudo-fibers" are not ideal in terms of their defect content and growth surface quality, we nevertheless hope to carry out radial enlargement growth experiments on these fibers. Such experiments will enable optimization of reactor growth conditions (flows, temperature, pressure, etc.) and hardware/procedures (sample loading, mounting, etc.) to achieve significant radial crystal enlargement at high growth rate.

One of the task milestones in the present NASA/DOE Agreement is demonstration of a 0.5 cm diameter SiC boule. Assuming a .4mm diameter SiC pseudo fiber as a starting seed crystal an additional 2.2mm or 2200 µm's of radial growth must to be accomplished to achieve a completed 0.5 cm diameter boule. At 100 µm's/hour growth rate, the total growth time may exceed 22 hours of growth. Recent advances in

obtaining growth rates of 100 μm's per hour have been reported [3-5]. These recent reports can be divided into two different approaches. The first approach uses halogenated compounds that are reported to suppress gas phase nucleation and increase adatom surface mobility along with carbon precursors (i.e., ethylene) that yield more growth contributing species to the gas phase [3,4]. The halogen compounds increase the amount of gas phase reactants available at the surface for incorporation into the growing crystal. The second approach is to use traditional silane and propane chemistry but at greatly reduced pressures (i.e. 40mb). The reduced pressure high growth rate epilayers have resulted in high quality films without the need for corrosive halogen containing compounds. Our immediate future is to focus on reduced pressure high growth rate techniques and avoid using HCl. Techniques and hardware for seed (fiber or pseudo-fiber) preparation, mounting, and loading will also be refined.

A vertical hot-wall growth reactor is presented as the preferred embodiment for LTC in US Patent 7,449,065. The hot-wall growth reactor configuration was selected in part because it provides more isothermal growth environment and higher growth temperature. The overall concept and use of hot wall reactors for SiC crystal growth is fairly common at universities and companies researching SiC. However, the existing NASA Glenn Research SiC epitaxial growth system (an Aixtron 1200HT chemical vapor deposition system) is configured as a cold-wall horizontal flow system. This Aixtron CVD system represents approximately $1M in original purchase price and $250K in upgrades along with approximately in $1M in previous NASA-funded laboratory infrastructure upgrades. After conducting initial tests/experiments, it became clear that the pre-existing horizontal cold wall reactor (Fig. 5 Left) with pancake RF coil heating was insufficient for conducting longer-duration and high deposition rate lateral growth experiments.

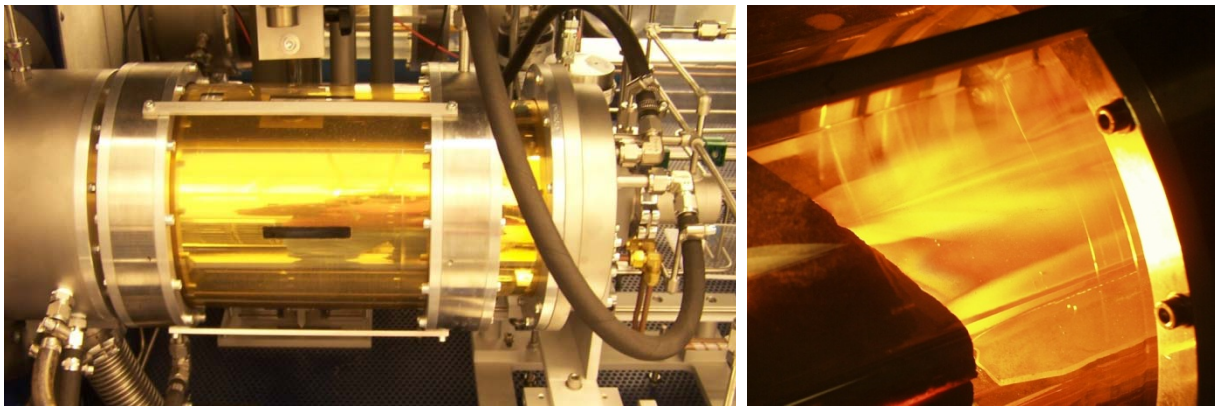

Fig. 5. (Left)NASA GRC horizontal cold-wall SiC growth reactor as installed by manufacturer. (Right) Operation of NASA GRC cold-wall SiC reactor in "pseudo-hot-wall" configuration.

A straightforward modification of one of NASA's existing cold wall reactors was attempted. This involved installation of graphite foam to form a surrounded cavity "pseudo-hot-wall" growth zone above the existing cold wall susceptor and pancake RF coil. This configuration did successfully achieve elevated growth temperatures over 1600° C (Fig. 5 Right), but due to the physical construction of the reactor it was impossible to construct a closed gas flow path. The majority of growth precursors flowed around (instead of through) the hot growth zone preventing successful growth from being achieved.
The initial test results led to a decision to much more extensively modify the reactor to a full hot-wall configuration in order achieve the feasibility demonstration goals of this project. The new horizontal hot wall reactor was designed (Fig. 6 Left) such that it would physically fit into the existing reactor space and could be integrated with the rest of the NASA SiC CVD infrastructure. One of the major challenges associated with this undertaking was the complete replacement of the pancake RF coil (wherein the coil resides in a flat zone underneath the susceptor) with a barrel coil that completely wraps itself around the

cylindrical hot-wall growth zone. Despite the challenges, the NASA team was able to procure or fabricate all the custom parts needed to implement the major facility modification. Initial heat testing and trial depositions began in October 2010 (Fig. 6, right).

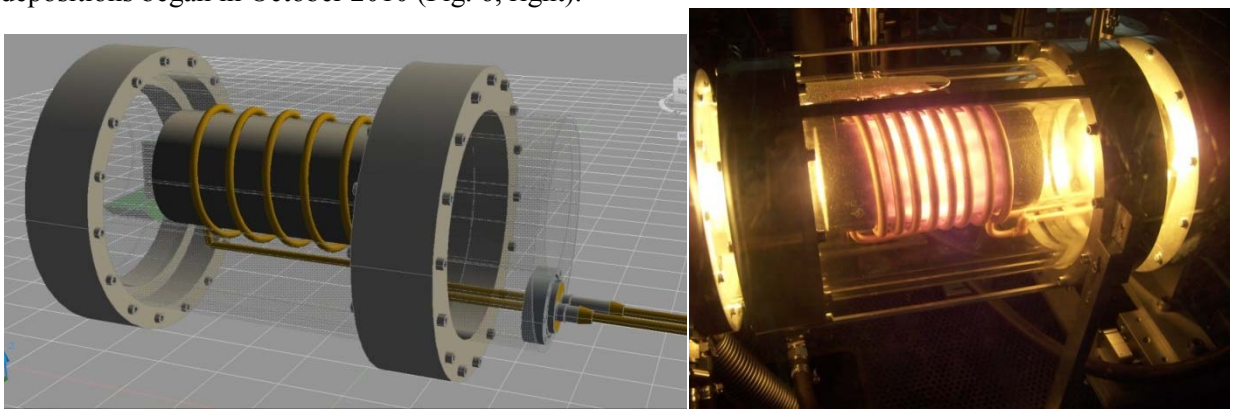

Fig. 6. (Left) Design drawing of hot-wall SiC epitaxial growth reactor custom-designed for integration into NASA Glenn SiC epitaxial growth facility. (Right) NASA Glenn hot-wall SiC reactor undergoing initial heat testing, October 2010.

Fig. 7 shows an optical micrograph close-up of part of a 6H SiC, a-plane polished pseudo-fiber following one of the very first (very recent) growth attempts in the modified hot-wall reactor. The small scribe line visible was cut into one of the a-face surfaces of sample (prior to growth). The sample morphology indicates that significant growth took place, as significant m-face facets evolved during the course of the 1-hour growth run. Such faceting is expected - as the crystal enlarges it should change from rectangular cross-section (initial sliced "flat toothpick" shape) to acquire the hexagonal shape cross-section consistent with its hexagonal crystal structure (e.g., Fig. 4).

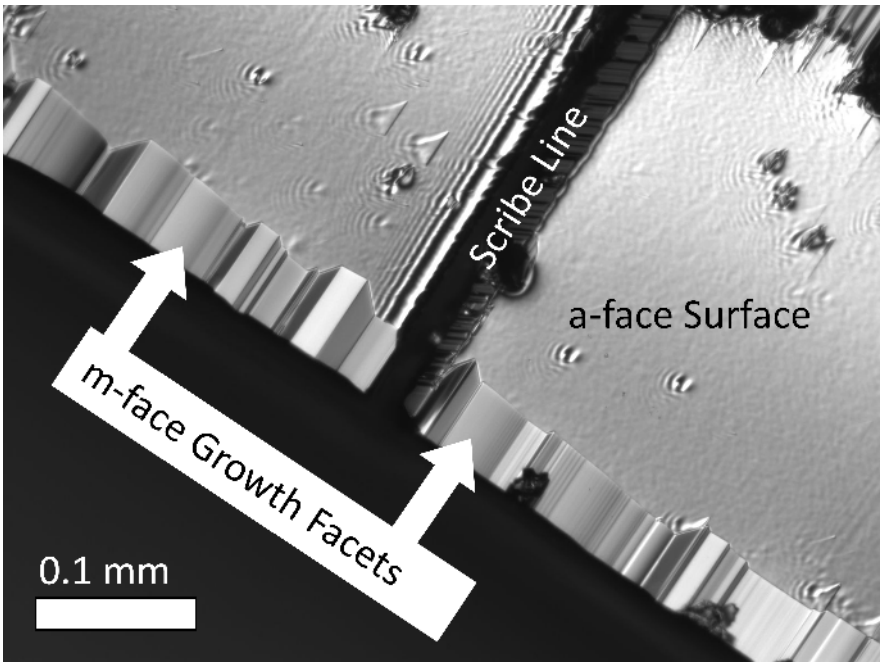

Fig. 7 Optical micrograph of portion of 6H-SiC pseudo-fiber following 1 hour of growth in NASA Glenn modified hot-wall SiC reactor.

With the hot-wall system becoming operational, much further growth, optimization, and characterization of "radial" SiC epitaxial films will be undertaken.

D. Solvent Melt Evaluation System

An ultra high vacuum system was assembled to evaluate possible solvents (for Solvent-LHFZ process) and their interactions (such as wetting properties) with a SiC pseudo fiber or other seed crystal. The system is pumped with a turbo drag pump and rough pumped with a rotary vain pump. The SiC pseudo fiber is held in an electrical isolated Ta rod with rotates at 10 rpm and can have its x, y, and z position manipulated by means of a vacuum bellow system. The solvent is place in a crucible which is placed inside a resistive heater. Multiple runs of just the heater and possible solvents have been completed. The system is currently undergoing modification to add additional cooling needed for more prolonged and high temperature melt experiments.

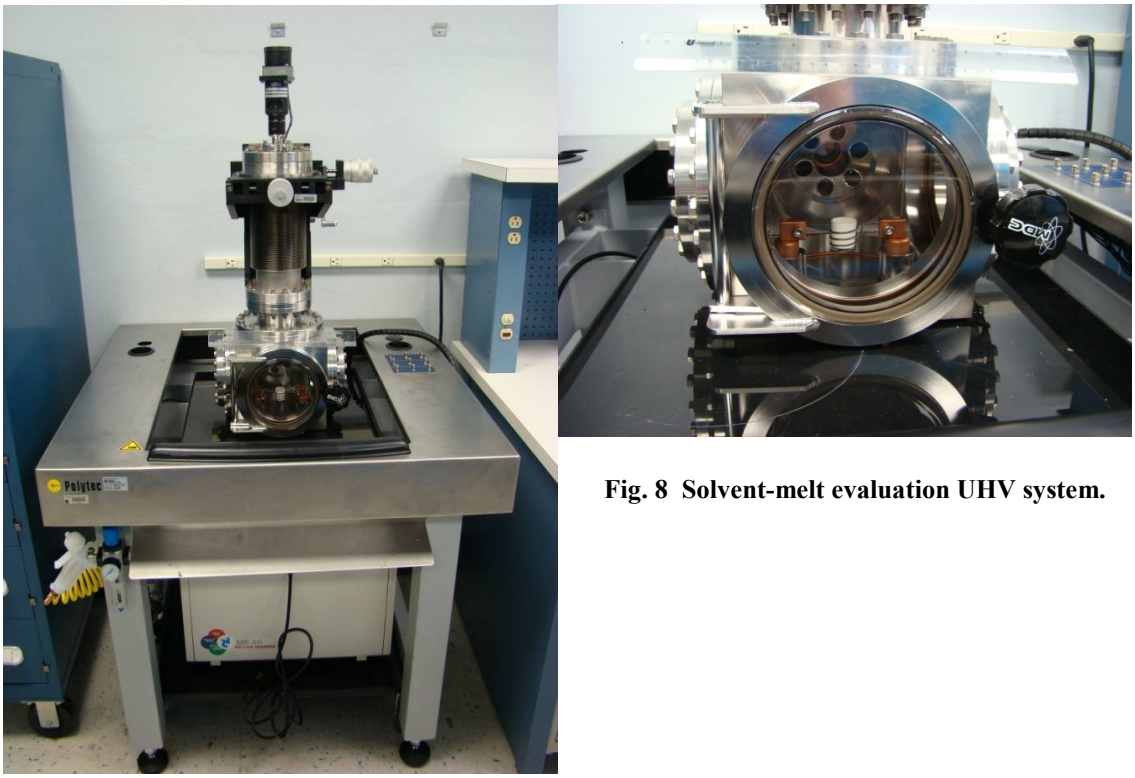

Fig. 8 Solvent-melt evaluation UHV system.

Conclusion

Extensive modifications to NASA Glenn crystal growth equipment have been accomplished since the Dept. of Energy project funding started less than a year ago. Over the next year these facilities will be used to demonstrate/develop the two critical (previously un-attempted) "fiber" and "radial" growth processes needed to realize Large Tapered Crystal (LTC) SiC boules. If successfully implemented, LTC boules promise to greatly improve the cost and quality of wide bandgap wafers that will become the basis for realizing much more advanced high-power semiconductor switches. These devices in turn offer high-impact benefits to power conversion/management systems including utility power transmission and electric/hybrid vehicles.

Publications

None this period – since this year was spent in build-up and modification of lab equipment.

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1. F. Ritzert and L Westfall, "Laser Heated Floating Zone Production of Single Crystal Fibers" NASA Technical Memorandum 4732 (1996)
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3. I. Chowdhury, MVS Chandrasekhar, P.B. Klein, J.D Caldwell and T.S. Sudarshan, "High growth rate 4H-SiC epitaxial growth using dichlorosilane in a hot-wall CVD reactor", accepted for publication in JCG
4. S. Leone, H. Pederson, A. Henry, S. Rao, O. Kordina, E. Janzen, "Growth of Thick 4H-SiC Epitaxial Layers on On-axis Si-face substrates with HCl Addition" submitted to Crystal Growth and Design (2010).
5. H. Tsuchida, M. Ito, I. Kamata, M. Nagano, T. Miyazawa, N. Hoshino, "Low-pressure fast growth and characterization of 4H-SiC epilayers" Mater. Sci. Forum, 645-648 (2010) 77-82

Patents

1. None this period. This project is based upon development of US Patent 7,449,065 Awarded 11 November 2008.

3. Electric Motor Research and Technology Development

3.1 A New Class of Switched Reluctance Motors Without Permanent Magnets

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Objectives

- Overall Objectives
  - Develop, design, build, and test an unconventional traction drive that
    - has no permanent magnet material,
    - has lower torque ripple and acoustic noise than that of a conventional switched reluctance motor (SRM), and
    - maintains the low cost, simplicity, and power density of the conventional SRM.
  - Obtain operational characteristics for finalized design and compare with targets:
    - power density: 5 kW/L (2015 DOE target),
    - specific power: 1.3 kW/kg (2015 DOE target), and
    - motor cost between $7/kW and $4.7/kW (2015 and 2020 targets, respectively).
- FY 2010 Objectives
  - Develop and refine control scheme.
  - Perform dynamic simulations.
  - Conduct structural and acoustic modeling.
  - Arrive at optimized design.

Approach

- Develop/refine control algorithms.
  - Develop software solutions needed to operate novel machine.
  - Investigate potential to introduce novel control techniques.
- Conduct electromagnetic, thermal, and structural/acoustic noise modeling.
  - Perform various types of finite element analysis (FEA) studies to critique overall design.
  - Perform acoustic modeling throughout vibration modes.
- Make necessary refinements.
  - Address any structural, thermal, or vibration issues.
  - Conduct electromagnetic FEA studies to confirm that mechanical implementations do not compromise performance significantly.
- Fully simulate finalized ORNL SRM design in dynamic simulations.
  - Determine torque and power versus speed characteristics.
  - Obtain accurate values for power density and specific power.

- Prepare a summary report to be incorporated into the annual VTP report that describes the
  - control algorithm;
  - FEA results, including torque and power capabilities and operational characteristics; and
  - finalized SRM design and converter architecture.

Major Accomplishments

- Verified through simulations that the design meets 2015 performance targets with less than 5% torque ripple.
- Developed custom software to accomplish various tasks.
  - Two universal dynamic simulators.
    - Parametric: efficient means to optimize control and design parameters.
    - FEA: capable of conducting dynamic electromagnetic and structural simulations.
  - Automated FEA-based geometric optimization.
  - Complex multivariable, multiobjective optimization of control waveforms as a function of speed and torque.
    - Near-zero torque ripple achieved for low and moderate torque levels (up to 150 Nm).
- Designed entire assembly, prepared drawings for fabrication, received all parts, and began assembling model verification prototype.
  - Verified mechanical structural integrity and performed qualitative acoustic analyses.
- Received positive feedback and significant interest from the Electrical and Electronics Technical Team and industry.

Future Direction

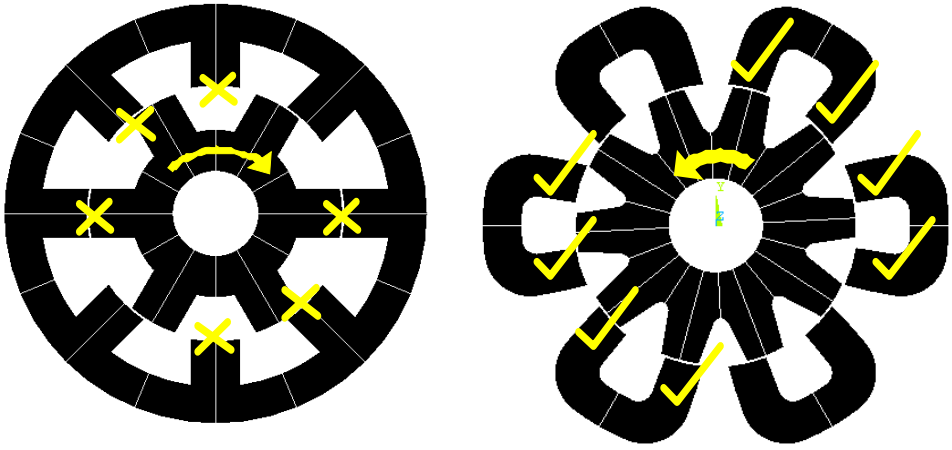
- Finish assembling model verification motor.
- Develop and apply means to obtain characteristics before and during testing.
  - Establish means to comprehensively obtain torque and flux linkage as a function of current and position for use in control algorithm.
  - Provide method to accurately measure torque ripple.
  - Assess impact of noise/vibration damping materials.
- Develop and prepare drive/controller hardware and software.
  - Implement control algorithm on digital signal processing or real-time system.
  - Choose inverter and build corresponding controller interface.
- Design, fabricate, and build final prototype.
  - Incorporate changes into design as determined from first construction and basic testing.
- Conduct comprehensive motor testing in dynamometer test cell.
  - Determine performance capabilities and efficiency characteristics throughout operation range for various operation modes.

Technical Discussion

Because of the high and unpredictable cost and availability of rare earth permanent magnets (PMs), which are used in most hybrid vehicle applications today, many automotive manufacturers have a common interest in the use of electric machines which do not use these PM materials. Although PM motors are not easily surpassed with respect to efficiency and power density, other competitive motor technologies exist which can have lower cost per power rating ($/kW). Of the alternative motor technologies, the SRM offers the simplest rotor configuration, which is advantageous in terms of material cost, manufacturing cost, speed capability, and reliability. The highly nonlinear behavior and unusual control methods associated with the SRM require the use of sophisticated and computationally intensive software programs to fully optimize its design and operation. Therefore, the SRM is a relatively young motor technology, in terms of research and development, as opposed to other technologies such as the induction motor. Two primary drawbacks of the SRM are the level of torque ripple and the acoustic noise inherently

associated with the SRM's doubly salient stator and rotor geometry. The intent of this project is to apply novel design techniques that significantly reduce torque ripple and acoustic noise while maintaining the intrinsic benefits of the SRM.

Existing torque ripple and acoustic noise reduction techniques typically incur significant compromises of things such as peak torque, torque/power density, material/manufacturing costs, and/or design complexity. A conventional SRM with eight stator teeth and six rotor teeth is shown in Fig. 1. If the rotor is assumed to be rotating clockwise, the two stator teeth without a superimposed yellow 'X' are the only stator teeth that would have excited windings if a conventional control scheme were used. That is, only two (25%) of the eight stator teeth are active during this instant. As the rotor position continues to increase in the clockwise direction, coils of two additional stator teeth are excited, and thus 50% of the stator teeth are active at that instant. However, this condition is maintained only for a short duration, and only 25% of the stator teeth are active beyond this short duration, giving a low average of active stator teeth.



(a) **(b)**

Fig. 1. Active stator teeth of a conventional SRM (a) and unconventional SRM (b).

After observing the low amount of active air gap area within the conventional SRM, it seemed that novel concepts could be used to increase the average number of active stator teeth that are producing productive torque in order to more readily distribute the torque production and thereby reduce torque ripple. Because the fundamental means in which torque is produced in an SRM relies on the magnetic saliency of the stator and rotor, it can be difficult to increase the number of active stator teeth without compromising the reluctance ratio between aligned and unaligned rotor positions. This is a result of introducing stator and/or rotor teeth within a closer proximity of each other, thereby promoting detrimental flux flow through undesired paths, which potentially decreases the overall torque capability of the machine. Therefore, the proposed general approach uses separate steel pieces and/or laminations to carry out the tasks mentioned above while seeking to minimize counterproductive flux flow by means of magnetic path isolation. Because the permeability of steel approaches that of air as magnetic saturation increases in the steel, it is not possible to have completely isolated magnetic paths in this type of application, particularly since the SRM often operates in the saturation region. Therefore, these types of hardware approaches must be incorporated carefully in such a way that the natural operation and control of the motor inhibits the detrimental tendencies of leakage and undesired flux paths.

In FY 2009, a wide variety of designs which use this technique were developed and analyzed for feasibility. Based on comparisons of estimated performance, size, cost, and manufacturability, the most

feasible geometry was chosen to be the focus of FY 2010 development efforts. As shown on the right in Fig. 1, 8 of 12 stator teeth are typically active at the indicated rotor position for counterclockwise motoring operation. As the rotor continues to rotate, only 4 of 12 stator teeth are active for a brief period of time and then 8 of 12 stator teeth are active again. Therefore, on average, at least 50% of the stator teeth are active in this unconventional SRM versus roughly 33% in a conventional SRM. While many more characteristics should be considered in making a direct comparison, this quick observation reveals the potential of the design to facilitate greater overlap of torque production among the phases compared with a conventional SRM.

Dynamic Simulators

To have the capability to fully assess the overall impact of the variation of a range of design parameters, two separate universal dynamic simulators were developed. The simulators are universal in the sense that they can simulate various motor designs, even other types of motors, with slight modification to the simulator. One of the simulators carries out the dynamic simulation and corresponding computations within FEA software by means of accessing the FEA solution database for each iteration and applying the appropriate constraints, constants, and relationships for the transient solution. This simulator is well suited for integration with other types of analyses such as integrated structural and thermal FEA. The other simulator is similar in nature, but entails a more parametric oriented approach to the transient solution and relies on parametric data from static FEA solutions. Extensive efforts were made to ensure that the impacts of saturation, mutual coupling, and other interactions between phases were fully realized. It is common for designers to neglect these phenomena, but the acknowledgement of these aspects is particularly important for this unconventional design approach. Both simulators have the capability to work in various modes such as current, torque, or speed regulated operation so that the simulation is conducted as if the design were in actual operation in a vehicle. Figure 2 shows a graphical user interface (GUI) that was developed to provide an effective way to operate the dynamic simulators and generate and edit waveforms which are supplied and returned from the simulator code.

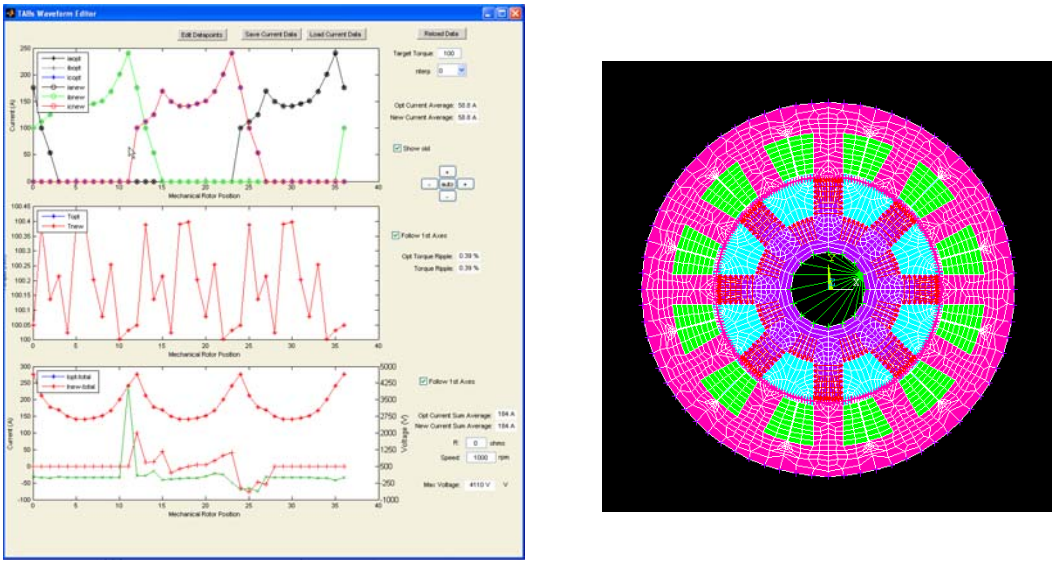


Fig. 2. GUI developed to operate dynamic simulators.

Control Algorithm Development

The parametric simulator is particularly useful for optimizing control conditions such as maximum torque per amp, minimum torque ripple, and maximum efficiency. A considerable amount of effort was devoted to the development of control optimization code for operation with near-zero torque ripple. Since torque

is a function of three currents and position, the currents at each position can be chosen to meet the desired torque reference, provided that current and voltage constraints are not violated. Therefore, this approach requires dynamic modeling to ensure that the required voltage does not exceed the amount available from the dc link. The resulting problem is nonlinear multivariable, multiobjective optimization with nonlinear constraints. Attempts were made to use optimization algorithms including various genetic and neural networking techniques, but computational times were tremendous and there was difficulty in obtaining globally optimal solutions, as local solutions were often presented, despite the use of a global algorithm. Therefore, an algorithm termed the "brute-force" method was developed, based on the unconventional manner in which the problem is approached using this method. The method involves the automated generation of an initial solution for the desired conditions followed by development of a series of solutions that fall within the given constraints. At this point, the brute-force method finds the optimal solution and verifies that it is a global solution, else another iteration is commenced. It is estimated that about 10,000 lines of code were written to carry out this task, in which recursive functionality is used to explore solution regions. The overall result is a collection of reference waveforms for points throughout the entire operation region.

Solutions obtained from the brute-force method were analyzed with the parametric dynamic simulator, with the results for less than 5% torque ripple conditions indicated by the blue trace in Fig. 3. Torque ripple can be defined in various ways, and in this case, it is based on the quadratic mean of the ripple divided by the average torque multiplied by 100. This method was used as opposed to using single values such as the maximum and minimum torque, which do not fully incorporate all aspects of the torque waveform. For example, a torque spike with very short duration could be present in the torque waveform and the latter torque ripple calculation would be greatly affected although the inertia of the system would most likely render the spike to be minimally consequential. A torque level of about 170 Newton meters (Nm) is achievable at low speeds with a torque ripple level of 5%. At 4,000 rpm, the machine is capable of producing 125 Nm, which is a power level of 52.4 kW, with a torque ripple of only 5%. Calculations which include copper and iron losses indicate that the efficiency of the motor under these conditions is about 94.5%. As speed increases, the power capability decreases if the torque ripple is limited to 5%. But at higher speeds, it may be possible to alleviate the torque ripple constraints based on the increased momentum associated with these speeds.

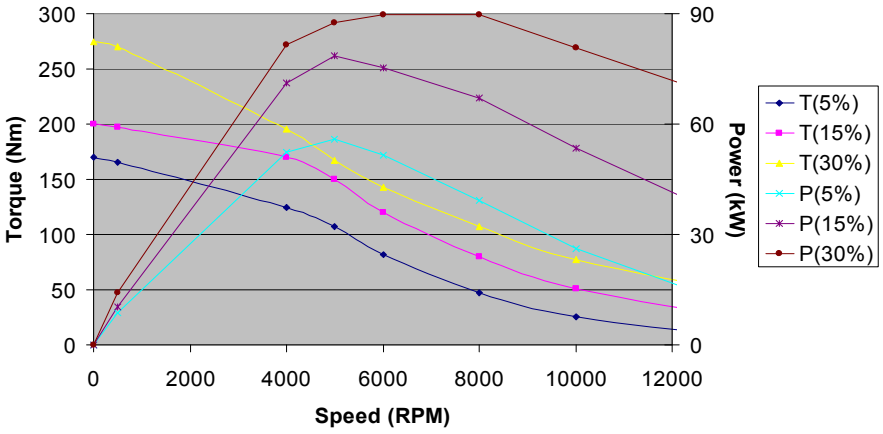


Fig. 3. Torque and power versus speed.

Continuous conduction control can greatly increase the output power of an SRM at moderate and high rotor speeds as a higher amount of current is applied during the torque production region (for the motoring operation mode). This is achieved by not requiring the current in each stator tooth to reach zero during each electrical cycle. Because current is not zero when the rotor rotates beyond the alignment

position, negative torque is applied to the shaft, and thus this control mode does not operate with utmost efficiency, but it can greatly increase the power capability of the machine. This is particularly relevant to vehicle propulsion applications, wherein the average required power is relatively low for normal driving conditions and only short durations of high power demand are required for situations such as passing other vehicles or merging with high-speed traffic.

The additional traces shown in Fig. 3 represent the torque and power capabilities of the machine with torque ripple percentages that are greater than 5%. Simulations indicate that the machine can produce about 75 kW at 8,000 rpm with a torque ripple of 20% and more than 90 kW at 8,000 rpm with a torque ripple of 30%. Simulations also show that the machine is capable of operating beyond 15,000 rpm. The size of the machine used in these simulations matches that of the second generation Prius, with roughly a 10 in. stator outer diameter and a 3.3 in. stack length. This particular design is well suited for an application similar to that of the primary motor of the Camry hybrid electric vehicle (HEV), where a gear reducer is used to increase the torque capability while the high speed operation results in improved power density. These results indicate that this design approach could potentially offer a competitive alternative to PM machines in HEVs.

Structural, Modal, and Acoustic Assessments

Mechanical analyses were conducted to perform design optimization and validation in terms of structural integrity and minimal acoustic signature. Force vector results from electromagnetic FEA studies were used to establish proper loading conditions and boundary conditions for these mechanical FEA studies. As peak loading conditions were applied, stress analyses were conducted on the components within the assembly, shown in Fig. 4. As structural improvements were incorporated into the design in response to these studies, the impacts upon the electromagnetic characteristics were assessed in separate analyses, as necessary.

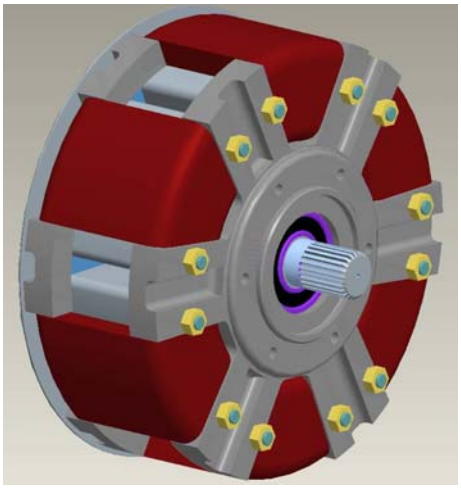


Fig. 4. Phase 1 motor assembly.

Initial studies indicated that a support pin for the stator laminations contained a stress concentration of about 100,000 psi (Fig. 5). As this stress is excessive, a method was integrated into the design which more readily distributes the stress along the stack of laminations and also allows the use of more substantial support hardware, thereby rendering it a stator support structure with maximum stress concentrations which are well below maximum yield strength.

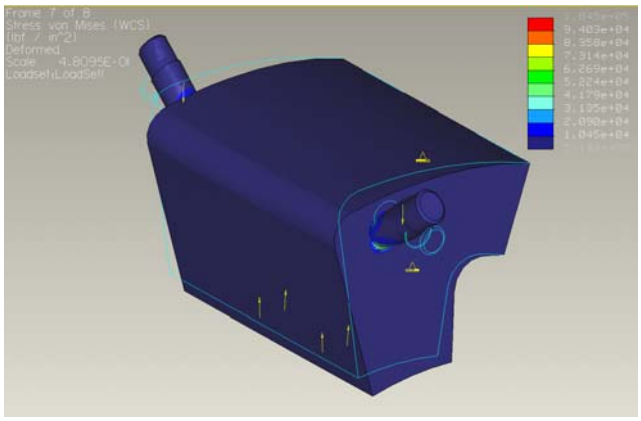


Fig. 5. Support pin stress analysis.

It is important to assess the displacement of the stator lamination stack under maximum load to ensure that it does not deflect and cause catastrophic failure due to interference with the rotor lamination stack. As shown in Fig. 6, the maximum displacement is located in the center of the lamination stack, where the model indicates a maximum deflection 0.0004 in. With an air gap of 0.03 in., the deflection extends about 1.3% into the air gap.

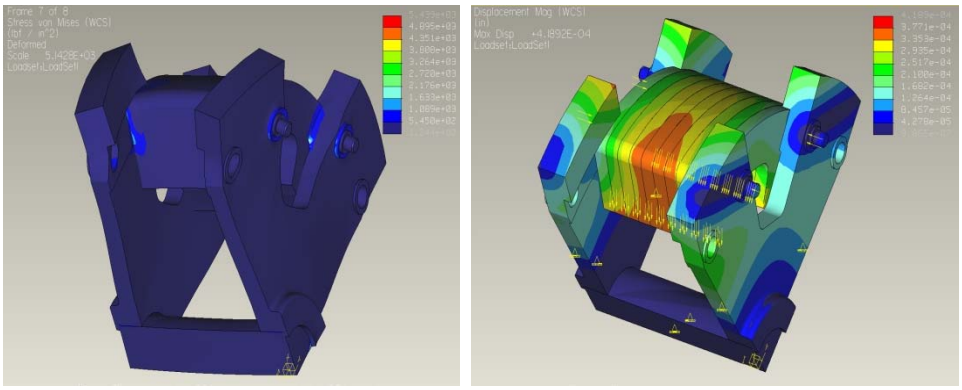


Fig. 6. Displacement analysis of support structure and stator lamination stack.

A separate stress analysis with peak loading conditions was performed on the crossbeam, shown in Fig. 7, which provides lateral support to the structure. Simulation results indicate a maximum stress of about 27,000 psi located in sharp crevices of the component. While these stress concentrations are not extremely high, they can be minimized with an appropriate radius in these locations.

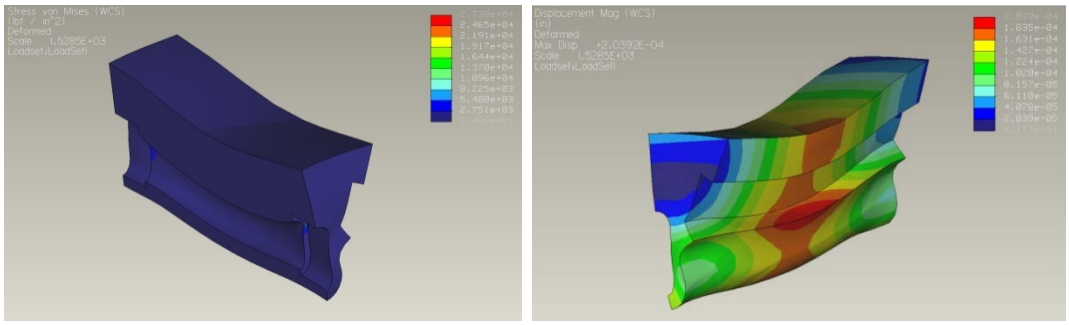


Fig. 7. Crossbeam stress analysis.

Although the rotor shown in Fig. 8 is of the conventional type, stress analysis was performed to assess the impact of centrifugal forces, which are a primary influence in the speed rating of the machine. A particular area of concern was the locating tab on the inner diameter of the lamination, where there is a stress concentration in the corners of the tab. This model was simulated at 20,000 rpm, and the stresses are well below the material yield strength with a factor of safety of about 1.7.

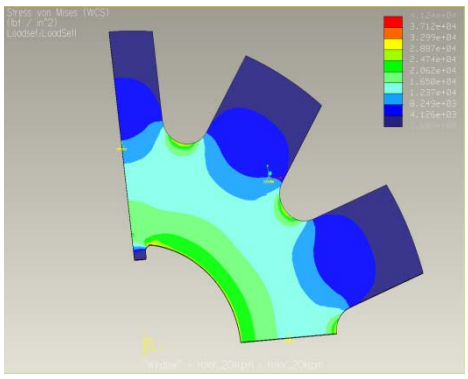


Fig. 8. Stress analysis of rotor lamination stack.

Various modal and qualitative acoustic analyses were conducted after the primary structural optimization efforts were concluded. While various modes exist, focus was placed on modes that correspond with frequencies associated with the operation of the design within the operating speed range. This includes forces which are directly related to the speed of rotation as well as other forces that are indirectly related to the speed of rotation which typically have higher excitation frequencies. The first mode shape of interest, shown in Fig. 9, occurs at 730 Hz. Deflections associated with this mode are essentially axial, and the structure would have good coupling to surrounding air like a speaker cone. However, driving forces for this mode shape should be minimal. For example, this mode shape may be excited if the rotor lamination stack had a significant misalignment with the stator lamination stack.

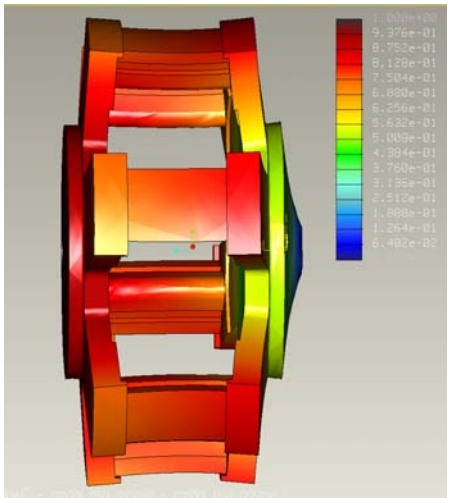


Fig. 9. Mode shape at 730 Hz.

Another mode of interest occurs at 1,250 Hz. As shown in Fig. 10, the deformation is essentially an axial mode with a twisting shape in the Y-Z plane. This mode would be highly attenuated by using a damping compound between the stator pole pieces and an outer shell which encompasses the outer perimeter of the crossbeams. The outer shell (not included in this simulation) would also add stiffness to reduce the amplitude of this mode shape.

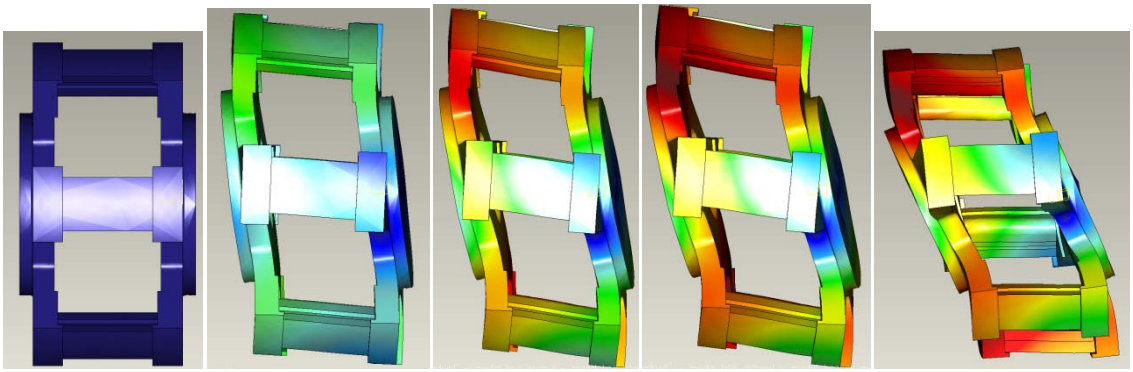


Fig. 10. Mode shapes at 1,250 Hz.

The next mode of interest occurs at 1,600 Hz, and consists of twisting deformations in the X-Y plane, as shown in Fig. 11. This mode would be significantly reduced by a cylindrical sleeve that is intended to be placed around the outer perimeter of the assembly. Damping material between the stator pole pieces and the outer sleeve will also mitigate these modal tendencies. Ultimately, this is a high modal frequency and it is not likely that there will be substantial driving forces within the range of operation of the machine.

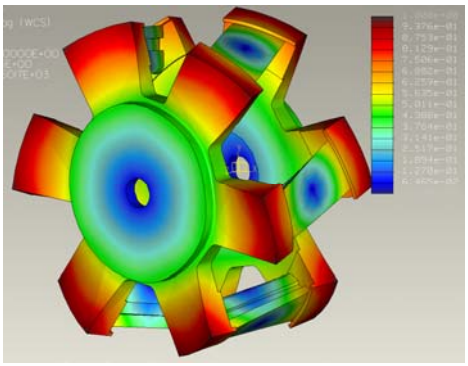


Fig. 11. Mode shape at 1,600 Hz.

Many other modal shapes exist and have been analyzed, and it was determined that there were no modes which caused significant concern in terms of structural integrity and acoustic signature. These studies are particularly useful in the determination of key areas to focus upon during the fabrication and assembly process. More specifically, a better understanding

has been established for the desired characteristics of the damping compounds that will be used throughout the assembly.

Thermal Analyses

A thermal model was developed using the layout shown in Fig. 12, and heat loads used in the analyses were obtained from modeled resistive heat as well as losses associated with hysteresis and eddy current effects. The model consists of the stator piece, which is made of electrical steel, copper windings, an insulation/damping layer, and the outermost cylindrical sleeve. The outermost sleeve provides structural support and is also used as a heat exchanger in the simulations, with heat transfer characteristics comparable to that of a typical water-ethylene glycol heat exchanger with a coolant temperature of 65°C. At low speeds most of the heat is generated by resistive losses in the stator winding, and at high speeds, most of the heat is generated by hysteresis and eddy current losses. Overall, the maximum amount of heat, by far, is generated at low speed, high-current operating points.

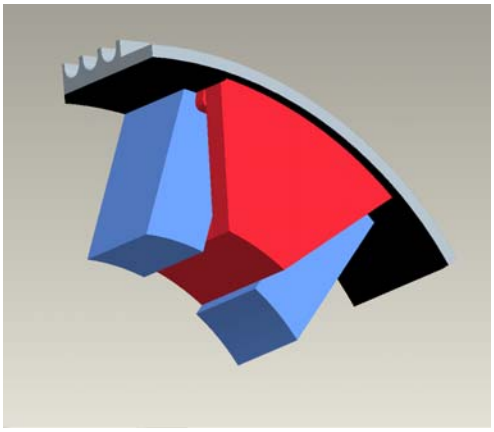


Fig. 12. Model used for thermal analysis.

While a conventional type of heat exchanger is used, this design has the distinct and substantial advantage of having the primary heat source (stator windings) located adjacent to the cooling apparatus. Additionally, the thermal conductivity of copper is at least 10 times that of the steel used in the laminations. Conventional motors of all types typically have stator windings enclosed by the steel laminations, and thus all heat must travel through the back iron of the stator laminations. Nonetheless, the current design approach requires the use of a compound between the stator winding and the outer sleeve for electrical isolation and the longevity of the winding. This compound is the primary inhibitor of heat transfer from the stator assembly to the heat exchanger. Studies were performed to assess the impact of the thickness of the compound. Figure 13 shows the results from two of the many scenarios that were investigated. For the maximum power condition with 5% torque ripple (52 kW), results indicate that a decrease in the thickness of the insulation compound from 0.06 in. to 0.03 in. has very little impact. Under these conditions, the steady state temperature for the 0.03 in. thickness is estimated to be 113°C, well below the temperature rating of the copper windings.

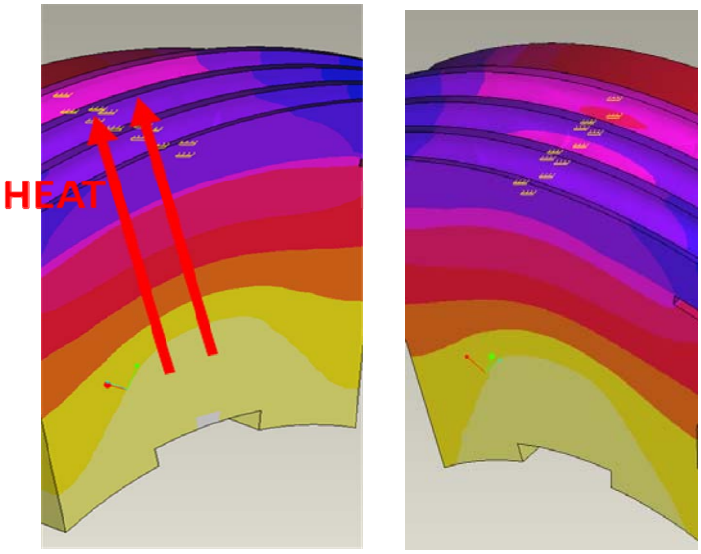


Fig. 13. Thermal gradient for electrical insulation compound thickness of 0.06 in. (left) and 0.03 in. (right).

First Phase Prototype

Although the final prototype is scheduled for fabrication and assembly in FY 2011, it became evident that there would be many benefits from building a preliminary

prototype. This first phase prototype will yield valuable information in various areas of the design and operation of the ORNL motor. From a modeling standpoint, empirical data can be used to verify (and adjust, if necessary) electromagnetic, structural, and thermal simulations. Additionally, quantitative empirical acoustic analyses will provide the opportunity to investigate the impact of various damping compounds. Various components in the first phase prototype, shown in Fig. 14, can be removed and replaced so that the effect of various types of compounds can be assessed. From a controls standpoint, it is important to have accurate motor parameters, which vary with rotor position, three currents, and temperature. ORNL will develop a means to measure these parameters and, because of the overall advantages to the program, will initiate this effort immediately in FY 2011 as opposed to waiting on the fabrication and assembly of the final prototype. Similarly, we will also begin integration and testing of the control algorithm and motor drive in the early part of FY 2011 without the final prototype. Therefore, the time constraint of completion for the final prototype assembly has been alleviated greatly and more effort can be placed on incorporating design improvements as observed throughout the fabrication, assembly, and testing of the first phase prototype.

Fig. 14. First phase prototype.

Conclusion

- Simulations indicate that the design meets 2015 performance targets with less than 5% torque ripple for a motor of the same size as that of the 2004 Prius.
  - Capable of 75 kW with only 20% torque ripple.
  - Capable of 90 kW with only 30% torque ripple.
  - Low cost due to absence of PM material.
- Automated control technique developed for near-zero torque ripple.
- First phase prototype designed, fabricated, and partially assembled.
- Improved upon and maintained characteristics of conventional SRM technology.
  - Significant reduction of torque ripple and acoustic noise.
  - Matches or surpasses performance of conventional SRM.
  - Robust with low manufacturing and fabrication costs.
  - Lower core losses due to localized flux paths.
  - Improved cooling due to unconventional winding technique.

3.2 Novel Flux Coupling Machine Without Permanent Magnets

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Objectives

- Finalize the design for a Novel Flux Coupling Machine without Permanent Magnets (PMs) and complete both electromagnetic and mechanical finite element analyses (FEAs).
- Complete engineering fabrication drawings.
- Analyze means of using field control to achieve a higher power factor, increasing both efficiency and torque capabilities.
- Begin fabrication of the prototype machine.

Approach

- Perform electromagnetic FEA simulations and compare the performance results to current industry standard PM machines.
- Add a field coil to provide an adjustable flux.
- Develop a novel flux path to function like a PM machine without the use of brushes.
- Use a hybrid cooling system with both internal oil channels and external water jackets in the motor housing.
- Perform field control simulations to ascertain the possibilities of achieving a higher power factor, increasing both efficiency and torque.
- Produce engineering fabrication drawings and begin prototype machine fabrication.

Major Accomplishments

- Demonstrated through finite element simulations on the prototype design that the PMs could be eliminated by using the novel stationary, brushless excitation coils, thus contributing to resolution of cost, temperature, performance, and speed issues typically associated with PMs.
- Analyzed 34 design iterations.
- Verified through simulations overall feasibility of the novel machine to meet DOE 2020 motor weight and volume targets.
- Verified significant cost reductions over PM machines can be realized by the novel machine.
- Integrated solid soft magnetic components for the rotor axial flux paths into the design.
- Achieved a design capable of operating at 14,000 rpm.
- Developed a MATLAB analytical program to provide performance versus speed curves under the voltage and current constraints.

Future Direction

- Complete prototype fabrication and testing in FY 2011.
- Compare the simulated results to the test results and develop a path forward for improvements.
- Bring the proven technology to the market.

Technical Discussion

Figure 1 shows a cutaway view of the prototype motor. No PMs are used in the motor; consequently, the permissible temperature of the motor is not restricted by their demagnetization.

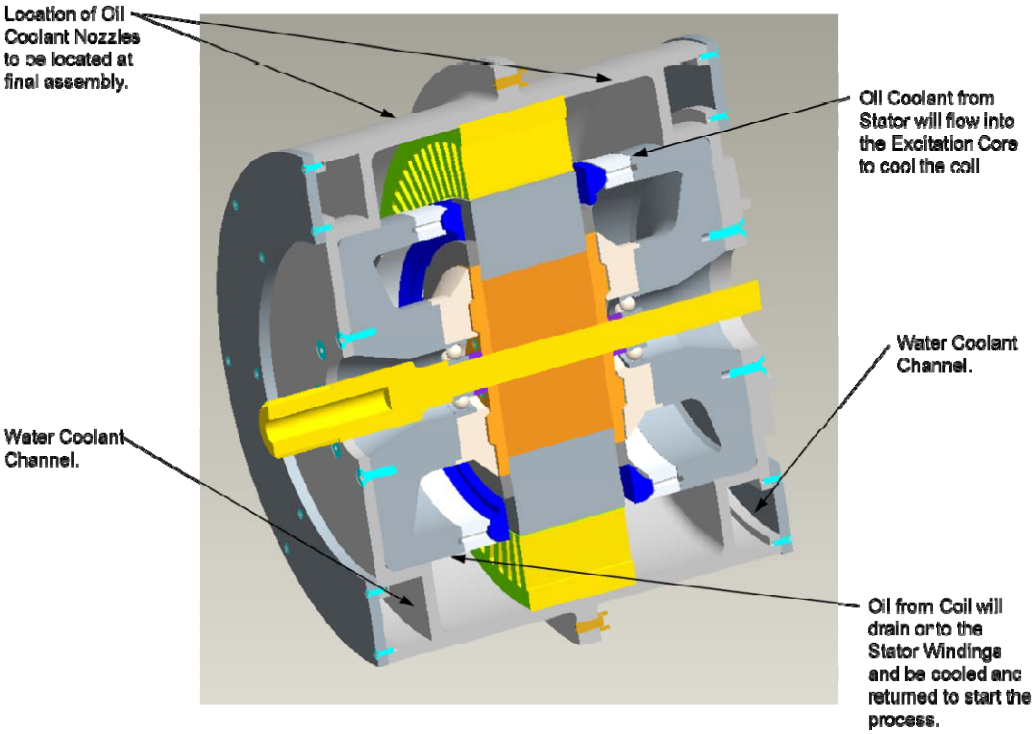

Fig. 1. Motor assembly cutaway view.

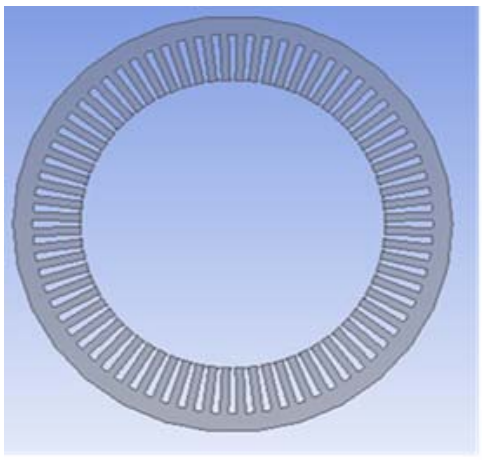

Fig. 2. Stator punching of prototype motor.

The stator punching of the flux coupling motor can be made for either a conventional distributed winding, such as the prototype punching shown in Fig. 2, or for a fractional-slot concentric winding type. The flow of flux is the same as the flux in a conventional two-dimensional stator core (i.e., no magnetic flux is designed to flow through the stator core axially).

The rotor direct current (dc) field flux is produced by two stationary excitation cores that transfer dc flux through the axial air gaps at each side of the rotor. Because the flux is dc, no eddy current is produced in the solid iron.

The inner and outer rings of the excitation core have opposite magnetic polarities. The inner ring of the excitation core carries one polarity of flux which goes through the axial gap to the rotor hub and subsequently distributes radial flux

to the laminated rotor poles as shown in Figs. 3 and 4. This flux then goes into the stator core and returns to the rotor wedges through the radial gap in an opposite polarity. This opposite polarity flux then flows axially to the rotor distributing rings that are only contacting the ends of the rotor wedges (shown in Fig. 5). The other side of a distributing ring is a complete ring without cutoffs. The dc excitation flux then returns to the excitation core to complete its magnetic path.

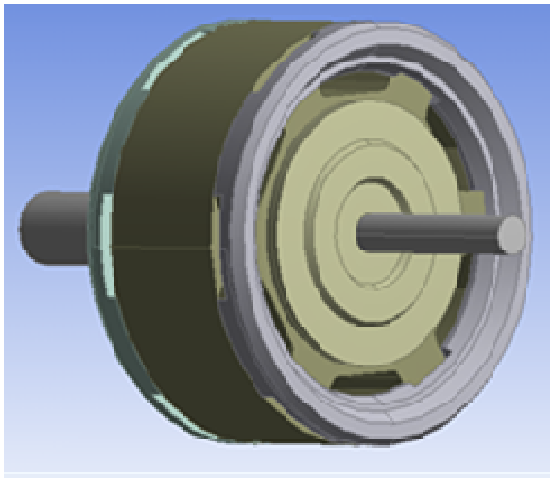

Fig. 3. Rotor of prototype motor.

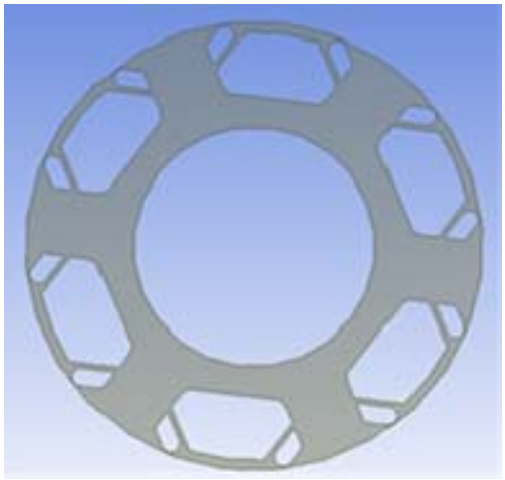

Fig. 4. Rotor punching.

Because the rotor distributing ring is not very thick in its axial direction, the saliency of the distributing ring may transfer to the smooth side of the ring and may produce core losses in the stationary outer ring of the excitation core. As the flux is dc, the local fluctuation of the space harmonics due to the saliency can be mitigated by the use of an equalizer ring made of a wrapped lamination. This will equalize the flux before going into the solid iron excitation core.

The major axial dc flux goes through the rotor solid hub and the rotor solid iron wedges that are located inside the cavities of the rotor punching and shown in Fig. 4. This solid iron path reduces the reluctance associated with the axial path of the laminated core.

Because the rotor solid iron wedges are shielded inside the rotor punching cavities, the high frequency slot harmonic flux is bypassed through the laminations on top of the wedges. This arrangement weakens the space harmonic flux that can go to the wedges. This core loss reduction effect will be measured and studied further FY 2011.

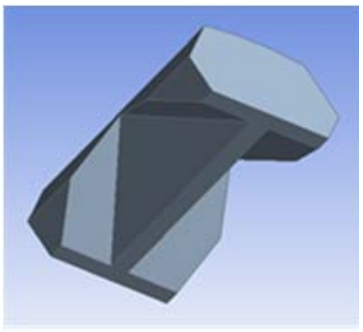

Fig. 5. Rotor solid iron wedge.

The overall motor performance curves for a motor with a wide range of magnetic saturation affected by the change of load and excitation should be calculated through the finite element flux linkages for each phase winding and at each operating point. Unfortunately, this would take excessive computation time and the available research time for this project was very limited. To address this, the saturated full load direct axis and quadrature axis inductances and the no-load flux linkage of the stator winding were computed and used to give a simplified overall estimation of the prototype motor's performance.

Figure 6 shows the simplified performance curves for the prototype motor. The corresponding parameters used in the analysis are peak phase voltage = 375 V, peak phase current = 233 A, stator phase winding flux linkage = 0.0875 Wb, excitation current = 8 A, direct axis inductance Ld = 0.289 H, and quadrature

axis inductance Lq = 0.386 H. The performance versus speed curves include peak phase voltage, power factor, direct axis phase current component, quadrature axis phase current component, peak phase current, motor torque, motor power, load angle delta, and current angle beta.

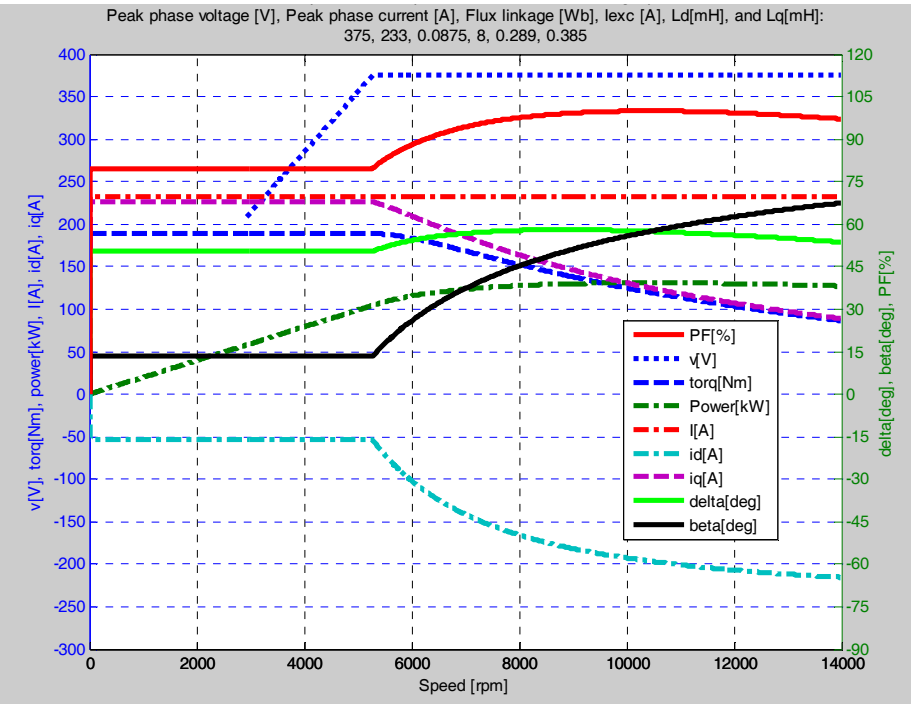

Fig. 6. Simplified motor performance versus speed curves.

As indicated in Fig. 6, the power factor at the highest speed region dips down. It can be improved by reducing the excitation current, resulting in weaker flux linkage (from 0.0875 Wb to 0.0788 Wb) as shown in Fig. 7.

Figure 8 shows the stator winding diagram for the prototype. The winding is capable of two dc bus voltages at either 600 V or 300 V. This is achieved by changing the lead connections. The magnet wire temperature rating was increased from the conventional class H (180°C) to class K (200°C) to take advantage of the elimination of the PM temperature restriction. The winding fill factor is 0.795, compared with 0.762 for the 2007 Camry motor. An optional stator winding would be to reduce the number of wires from 18 to 17, thus reducing the fill factor to a value of 0.751.

The 12-pole stator winding resistance is 0.052 Ohms per phase at 21°C, compared with 0.0354 Ohms for the 8-pole Camry motor. The stator copper loss at a root mean square current of 165 A is 4.2 kW at 21°C and 7.2 kW at 200°C. This is under the peak power condition with an 18 s operation time. The core loss and the efficiency map will be studied in detail in FY 2011 following the prototype motor build and test.

The excitation coil of the prototype motor has 1,000 turns of 19 AWG magnet wire. The resistance value is 10.6 Ohms at 20°C per coil and 18.1 Ohms at 200°C. During normal operation the excitation current is only a few amperes. The total 200°C excitation coil copper loss with 5 A excitation is 0.9 kW.

The torque quality of the prototype motor was evaluated through the torque value at each rotor angular position with the corresponding three-phase stator currents. The simulated results indicate good torque

quality as shown in Fig. 9. For comparison purposes, the torque quality is extremely poor with a 12-pole, 36-slot design of 1 slot per pole per phase.

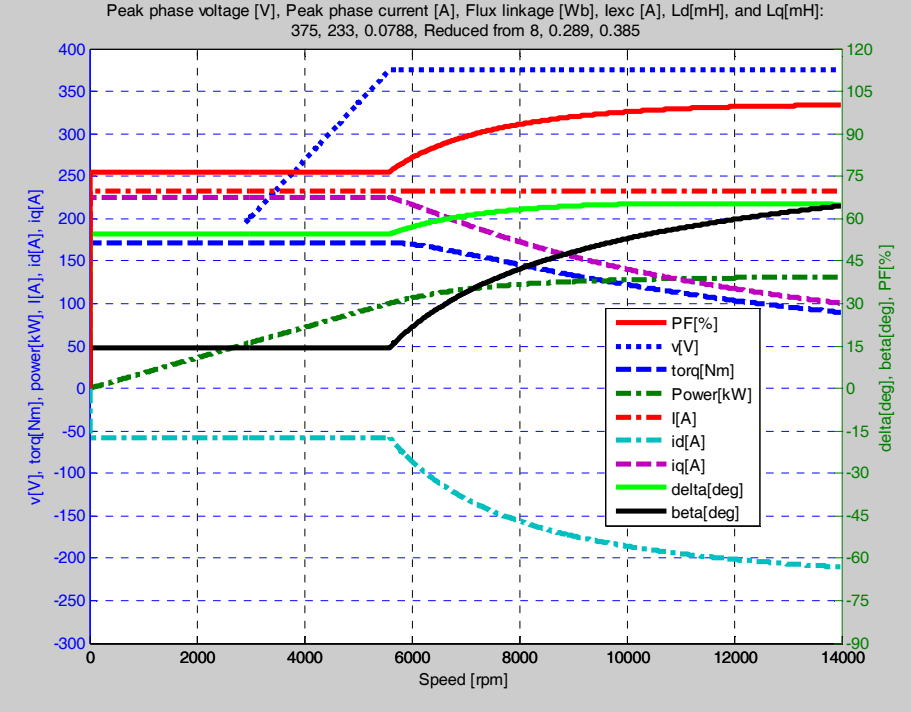

Fig. 7. Adjustable field can improve power factor.

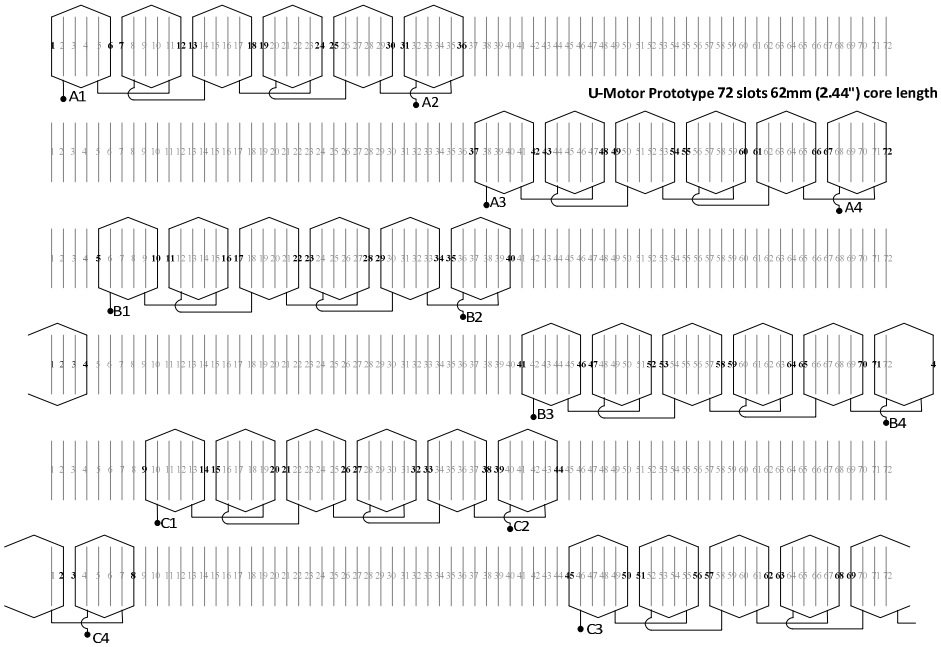

Fig. 8. Stator winding diagram.

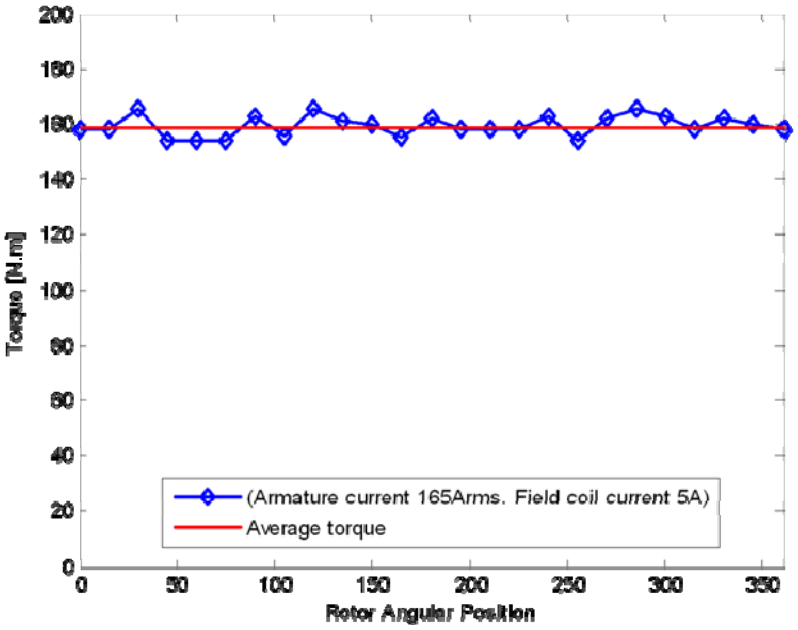

Fig. 9. Torque quality.

To achieve a 14,000 rpm rotor speed various design options were evaluated, many of which ultimately could not meet the stress and displacement requirements. The breakthrough came from shifting the focus from the rotor lamination alone to include the assembly of the flux distributing plate and the rotor hub end plate. ASTM A867, Alloy 2, a 2.50% silicon steel, was selected for the flux distributing plates, the rotor hub, and its end plates. This soft magnetic steel has sufficiently high mechanical strength (85 kSi tensile strength, mill annealed, and 80 kSi annealed for magnetic property) and magnetic properties equivalent to those of M-19 silicon steel.

The finite element simulation for the rotor stress at 14,000 rpm is shown in Fig. 10. The maximum rotor assembly stress at 14,000 rpm is 65,122 psi, located at the assembly of the flux distributing plate and the rotor-hub end plate.

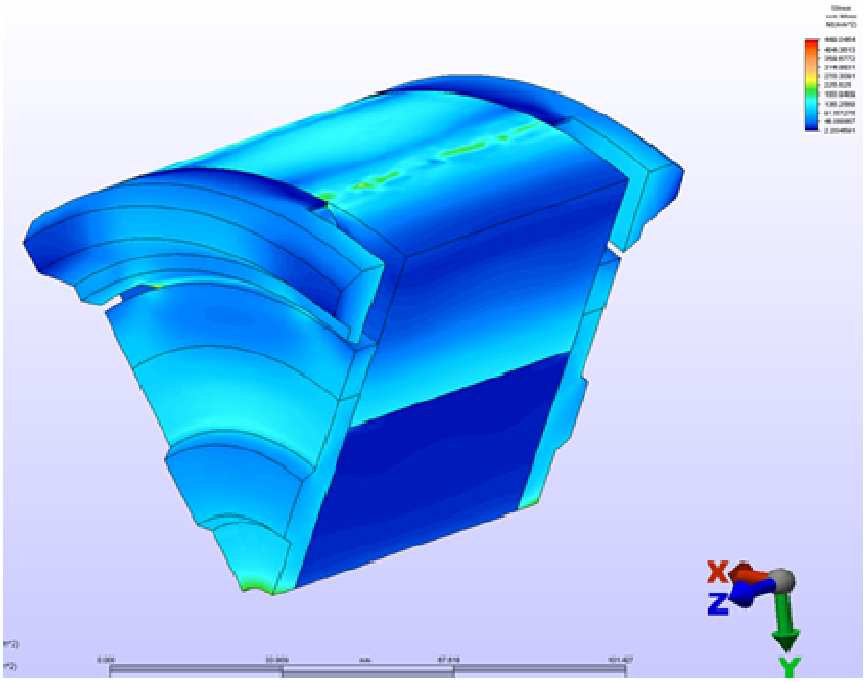

Fig. 10. Maximum Rotor Assembly Stress at 14,000 rpm = 65,122 psi.

The finite element simulation for the rotor displacement at 14,000 rpm is shown in Fig. 11. The maximum displacement of 0.002 in. is located at the rotor pole center of the rotor lamination stack. This displacement is acceptable with respect to the 0.029 in. per side of the radial air gap.

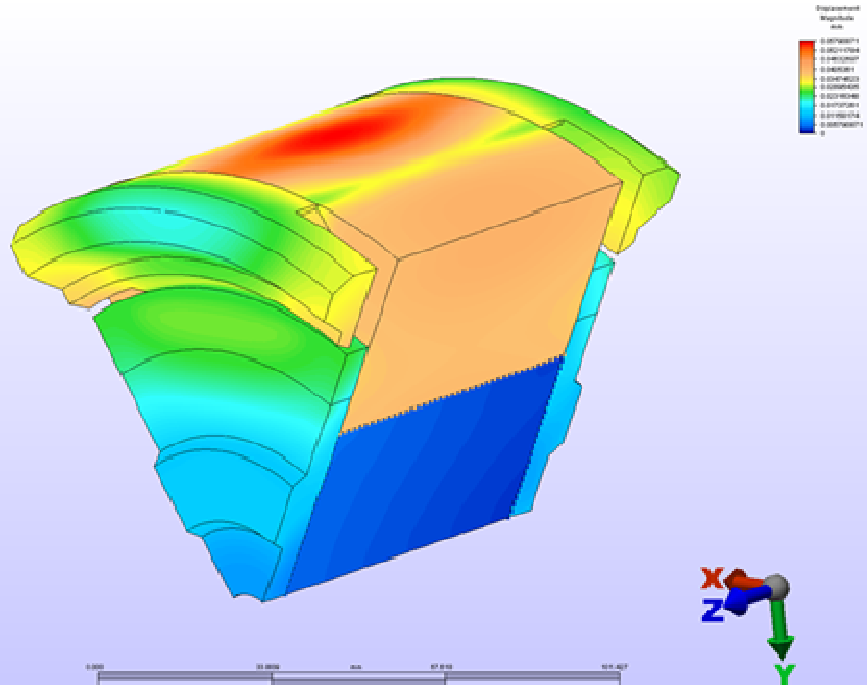

Fig. 11. Maximum rotor assembly displacement at 14,000 rpm = 0.002 in.

Table 1 shows comparisons among the novel flux coupling motor, the 2007 Camry motor, and the DOE FY 2020 targets.

Table 1. Comparisons Among Novel Flux Coupling Motor, Camry, and DOE 2020 Targets

Characteristic	Camry	Novel flux coupling motor	DOE 2020 Targets
Maximum power output (kW)	70 (tested)	115 (computed)	55
Weight (kg)	36.3	55.7	
Volume (L)	13.9	13.6[a]	
Specific power (kW/kg)	**1.9**	**2.1**	**1.6**
Power density (kW/L)	**5.0**	**8.5**	**5.7**
Power factor	0.61–1.00	0.75–1.00	
Cost ($/kW)/(total estimated cost)	**10.7**[b]/($749)	**6.1**[c]/($702)	**4.7**

[a]Volume calculation of new machine based on maximum height, width, and depth of motor components only (i.e., stator core, winding extensions, and rotor excitation cores).

[b]Requires 1 kg of high grade PMs at $90/kg.

[c]Includes additional cost of 11 kg steel and 3 kg copper wire (+$40.00) but eliminates 1 kg magnet (-$90.00).

Conclusion

- The prototype engineering design drawings for the novel flux coupling motor were completed, and the parts are being machined and fabricated.
- The prototype motor will be completed in early FY 2011.
- From the simulation results, the PM-less motor is feasible to meet the FreedomCAR 2020 motor targets for weight and volume while significantly reducing costs compared to current PM motors.
- Motor performance can be improved by using brushless adjustable field excitation.
- The breakthrough in the mechanical design enabled the motor speed to reach up to 14,000 rpm.
- Higher motor operating temperatures can be achieved. This benefit will be evaluated through the prototype tests in FY 2011.
- The prototype test results will help us to evaluate the shielding effects of the solid rotor wedges and the improvements needed for this type of flux coupling motor.

Publications

1. John Hsu and Randy Wiles, "Novel Flux Coupling Machines Internal Design Review," presentation to ORNL and outside industry reviewer, May 15, 2010, NTRC, Knoxville, Tennessee 37932.
2. John Hsu and Randy Wiles, "Novel Flux Coupling Machines," Presentation No. Ape-005, 2010 U.S. DOE Hydrogen Program and Vehicle Technologies Program Annual Merit Review and Peer Evaluation Meeting, June 7–11, 2010.

References

1. Nicola Bianchi and Thomas M. Jahns, "Design, Analysis, and Control of Interior PM Synchronous Machines," Tutorial Course Notes, IAS (copyright 2004).
2. J. S. Hsu, "High Strength Undiffused Brushless Machine and Method," US Patent 7,518,278, April 14, 2009.
3. J. S. Hsu, "Electric Machine for Hybrid Motor Vehicle," US Patent 7,270,203, Sept. 18, 2007.

Patents

Three 2010 patents were granted to this project by the U.S. Patent and Trade Mark Office.

1. John S. Hsu, "Permanent Magnet Machine and Method with Reluctance Poles and Non-Identical PM Poles for High Density Operation," U.S. Patent No. 7,719,153, May 18, 2010.
2. John S. Hsu, Laura D. Marlino, and Curtis William Ayers, "Method of Making Hermetic Seals for Hermetic Terminal Assemblies," U.S. Patent 7,695,663, April 13, 2010
3. John S. Hsu, and John W. McKeever, "High Pressure, High Current, Low Inductance, High Reliability Sealed Terminals," U.S. Patent 7,683,264 B2, March 23, 2010.

3.3 Permanent Magnet Development for Automotive Traction Motors
(co-funded with Project 13295 – Propulsion Materials Research)

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Objectives

- Develop the materials and processes needed to fabricate high performance permanent magnets (PM) that can be used for advanced traction drive motors with an internal PM rotor design to meet APEEM goals for enhanced performance at elevated temperature (180-200˚C) and reduced cost.
- Anisotropic magnets should be developed to satisfy the need for magnets with maximum magnetic energy density and minimum content of valuable materials. If possible, improved magnet forming processes and mechanical properties also should be developed to further reduce manufacturing costs and extend lifetime in service.
- While magnet materials meeting the technical specifications are most readily achieved using rare earth (RE) permanent magnets, the market factors of rising RE demand/cost and near total foreign control of RE supplies dictate that in the long term, alternative non-RE magnets must be developed.

Approach

This program consists of two major thrust areas.

- Continue investigation of ***RE anisotropic*** permanent magnets, as recommended in an industry expert study, placing effort on generating anisotropic particulate for bonded magnets and on novel processing of sintered RE permanent magnets, exploiting the improved high temperature tolerance of the Ames mixed rare earth (MRE)-Fe-B alloys.
- Develop aligned nano-structures in MRE-Fe-B magnet alloy particulate by enhanced control of crystal nucleation and growth or by controlled rapid solidification as a low cost route to make large gains in bonded magnet strength for simplified motor manufacturing.
- Further develop anisotropic sintered permanent magnets from micron-sized single crystal particles of MRE-Fe-B alloys using pressure-driven liquid phase sintering with intrinsic or extrinsic sintering additives for fully dense magnets of the highest magnetic strength, aiming for reduced Dy content.
    - This research thrust will be phased out as milestones are met and technology transfer is accomplished. It should also be noted that techniques being developed to produce anisotropic RE magnets probably can be used in the second thrust area, as well.
- New high strength ***non-RE anisotropic*** permanent magnets will be developed that meet the requirements for advanced interior PM electric traction motors. The investigation will involve theory and modeling efforts, as well as experimental synthesis of magnet compounds and prototype magnet fabrication and characterization.

- Development of non-RE anisotropic permanent magnets will include attempts to improve on known systems, by gaining enhanced knowledge of coercivity mechanisms with more sensitive characterization techniques and by innovative processing with greater control of microstructure.
- Non-RE anisotropic permanent magnets also will be pursued with help from theory and modeling, seeking to discover new phases with beneficial intrinsic properties, i.e., high Curie temperature, magnetization and magnetic anisotropy.
- If the new non-RE permanent magnet phases have insufficient magnetic properties as single-phase magnets, increased properties will be sought with further extrinsic manipulation, including use a soft magnetic second phase to produce enhanced exchange coupling.
    - It should be noted that this task area is extremely high risk, but if successful it will revolutionize the cost structure of permanent magnet motors and reduce the reliance on foreign controlled commodities for hybrid and electric vehicle production.

Major Accomplishments

- Solved problem with degraded high temperature performance of the segregated type of "core-shell" 2-14-1 phase structure (with Nd-enriched/Y-depleted shell or rim on each grain) in intrinsic (unmodified) sintered MRE-Fe-B magnet samples by adding uni-axial pressure assistance to the sintering process to permit reduced sintering temperature (<850˚C) for full density magnets.
- Demonstrated that a devitrification method with uni-axial applied pressure during annealing of glassy ribbon samples (as-spun) was successful at producing directional growth of aligned 2-14-1 nano-crystals with the a-axis (higher elastic modulus) perpendicular to the pressure vector direction, but with an unusual grain boundary disorder that appears to degrade magnetic anisotropy on this particulate for bonded anisotropic magnets.
- Performed preliminary electronic structure calculations of the Fe-Co system to determine the composition dependence of the magnetic moments, magnetic anisotropy and Curie temperature, where the original linear response scheme was modified and adjusted for this project. Results indicate that the maximum of each property occurs at a significantly different Fe-Co concentration.
- Used combinatorial synthesis on an appropriate model ternary alloy (Fe-Co-W) to search for single-phase magnetic compounds with anisotropic crystal structure and a minimum of Co content. Synchrotron micro-diffraction indicates that the main diffraction peak across the full spread corresponds to that of the (110) bcc phase. From MH (hysteresis) loop characterization of the lower W concentration region (~2%), we found several compositions where the out-of-plane (OOP) MH loop displays significant (promising) coercive field.
- Embarked on an extensive analysis of Alnico 5-7 samples by initial microstructural analysis in the SEM. Because the SEM samples were prepared to a high surface quality, orientation imaging microscopy (OIM) analysis could be performed. This verified that good alignment of the [001] direction was achieved in the growth direction of the grains, but that the grains were randomly oriented in the transverse plane of the casting. The SEM micrographs also determined grain size in the commercial samples, which will be important for TEM analysis during the coming year.

Future Directions

- Perform more focused work on improved processing of ***RE anisotropic*** permanent magnets, continuing to work on novel processing of sintered RE permanent magnets and on generating anisotropic particulate for bonded magnets, exploiting the improved high temperature tolerance of the Ames mixed rare earth (MRE)-Fe-B alloys.
    - Focus on development of anisotropic sintered magnets using pressure assisted intrinsic sintering at reduced temperature, exploring extrinsic additives to diminish Dy use.

  - Thoroughly develop pressure-driven anisotropic crystallization of amorphous magnet alloy ribbon to accentuate anisotropy in precursor particulate for bonded magnets.
- Accelerate effort to develop new high strength ***non-RE anisotropic*** permanent magnets that meet the requirements for advanced interior PM electric traction motors. It is critical that the investigation maintains close collaboration of theory and modeling efforts, of experimental magnet material synthesis work, and of detailed characterization studies on the new materials.
  - Develop theoretical tools for the investigation of potential new phases
  - Complete analysis of commercial Alnico
  - Understand texture development and develop control strategies in Alnico
  - Develop improved spinodal decomposition methods in Alnico
  - Complete combinatorial investigation of the Fe-Co-W system
  - Complete analysis of clusters in the Co-W system
  - Perform chemical synthesis of hard magnet particles for nano-composite magnets
  - Conduct Annual Workshop (Nov. 2010--completed) and Spring Workshop (May 2011)

Technical Discussion

Accomplishments in Rare Earth Anisotropic ($R_2Fe_{14}B$-type) Magnet Research

Anisotropic bonded or sintered magnets are the most cost effective for traction motor because they can obtain the highest maximum energy product $(BH)_{max}$ compared to isotropic magnets. This work builds on our earlier accomplishments in high temperature mixed rare earth (MRE) magnets of the isotropic type. There are several techniques to make anisotropic magnets, including aligned sintered magnets with micron-sized grains and melt-spun ribbons with nano-crystalline grain size and textures induced by controlling the solidification process or by hot-deforming glassy ribbons. Because the technical processes of anisotropic magnets are different from those of isotropic ones, new compositions, processes, and resulting microstructure need to be systematically studied and well understood in order to achieve good magnetic properties. In the past year, we mainly focused on four different aspects to approach our targets of anisotropic rare earth magnets. In addition, a 3-D reconstruction method for enhancing TEM results was applied to study the microstructure of melt-spun $MRE_2Fe_{14}B$ ribbons.

1. Optimization of composition and processes of sintered magnets made from $[Nd_{0.45}(Y_rDy_1)_{1/r+1*0.55}]_xFe_{14}Co_{0.3}B_{1.1}$ (r=1-5, x=2.4-2.6)

In our previous work, we have prepared aligned sintered magnets $[Nd_{0.45}(Y_3Dy_1)_{1/4*0.55}]_xFe_{14}B_{1.1}$ with improved magnet properties by adjusting alloy composition to introduce a liquid phase and using hydrogen decrepitation and conventional ball milling techniques. The $(BH)_{max}$ of new developed magnets with x=2.8 (WT220) reached to 25 MGOe. However, the magnet exhibits a strong temperature dependence for coercivity, similar to Nd-based magnets. Microstructural studies showed that the 2-14-1 grains form a core-shell structure with Nd segregation to the outer shell, negating the addition of Dy for bolstering the higher temperature magnetic properties after sintering at 1000-1100°C. In order to understand the complex partitioning behavior in the mixed rare earth system, the effects of composition and post annealing conditions on magnetic properties are systematically studied. In addition, the powder preparation and handling process have been greatly improved so as to control the Oxygen content to a level as low as possible. These improved processes make it possible to reduce the total RE content. Table 1 lists the changes of magnetic properties of $[Nd_{0.45}(Y_3Dy_1)_{1/4*0.55}]_xFe_{14}B_{1.1}$ when x decreases from 2.8 to 2.6. It is seen that the $(BH)_{max}$ increases from 25.4 to 29.3 MGOe with decreasing x=2.8 to 2.6. Unfortunately, the $(BH)_{max}$ drops dramatically at 400k due to a larger temperature coefficient of coercivity in those magnets. The temperature compensation effect which exists in the mixed RE melt-spun ribbons is not observed in the sintered magnets.

Table 1. Effect of RE ratio x and DyF_3 on magnetic properties of $[Nd_{0.45}(Y_3Dy_1)_{1/4*0.55}]_xFe_{14}B_{1.1}$

Ratio	2.8	2.6	2.6
DyF_3(wt%)	0	0	5
Mr (kGs)	10.8	11.4	10.7
Hc (kOe)	8.7	8.6	17.8
(BH)m (MGOe)@300k	25.4	29.3	26.0
(BH)m (MGOe)@400k	10.2	14.0	19.1
α (%/°C)	0.15	0.11	0.10
β (%/°C)	0.63	0.58	0.48

In order to improve temperature stability of sintered magnets, one of the most effective methods is to improve the coercivity by adding heavy rare earth elements, such as Dy or DyF_3. It is obvious that using DyF_3 is more economical. It is seen from Table 1 that the coercivity greatly increases from 8.6 to 17.8 kOe by adding 5% DyF_3. Although the $(BH)_{max}$ at room temperature decreases from 29 to 26 MGOe due to the addition of 5% DyF_3, the $(BH)_{max}$ at 400K increases from 14 to 19.1 MGOe. Therefore, the temperature stability and coercivity of magnets is obviously improved by adding DyF_3.

Since 2009, the improvement of magnetic properties of $[Nd_{0.45}(Y_3Dy_1)_{1/4*0.55}]_xFe_{14}B_{1.1}$ magnets is listed in Table 2. The best magnet obtains a $(BH)_{max}$ of 26 MGOe at 300K and 20 MGOe at 400K, respectively.

Table 2. Development status of magnetic properties of high temperature magnet $[Nd_{0.45}(Y_3Dy_1)_{1/4*0.55}]_xFe_{14}B_{1.1}$

Year	09	09-10	10
Mr (kGs)	10.8	10.4	10.6
Hc (kOe)	8.7	14.5	16.7
(BH)m (MGOe)@300k	25.4	24.4	26.0
(BH)m (MGOe)@400k	10.2	17.4	20.0
α (%/°C)	0.15	0.13	0.09
β (%/°C)	0.63	0.58	0.49

For comparison, the $(BH)_{max}$ values as a function of temperature for the experimental magnets and a commercial magnet are shown in Fig.1. The temperature coefficients of the experimental magnets are equal to or even better than that of the commercial magnet. However, their $(BH)_{max}$ values are still lower than that of the commercial magnet over the entire temperature range. In summary, if further processing improvements and composition adjustments can optimize the extrinsic parameters for $[Nd_{0.45}(Y_rDy_1)_{1/r+1*0.55}]_xFe_{14}B_{1.1}$ and make the ambient temperature $(BH)_{max}$ match the commercial magnet, the experimental magnets will be superior above 100˚C.

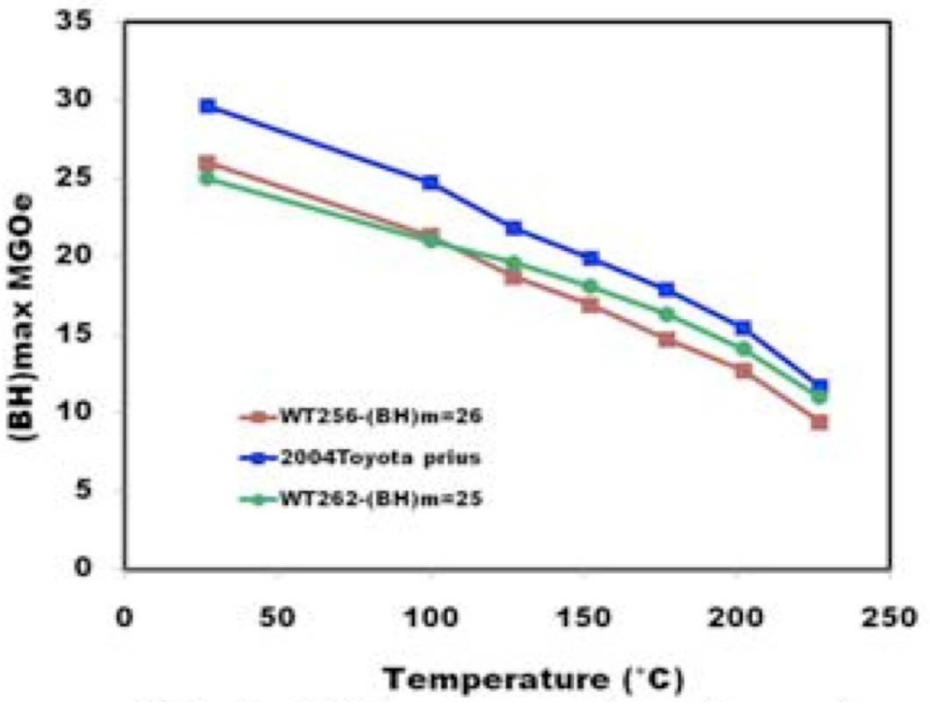

Fig. 1. $(BH)_{max}$ as a function of temperature for experimental and commercial magnets.

2. Study of microstructure and magnetic properties of sintered $[Nd_{0.45}(La_rDy_1)_{1/(r+1)*0.55}]_{2.6}Fe_{14}B$ magnets (r=1-3)

In this work, Y was replaced with La. La and Y are magnetically equivalent so that the magnetic properties of the alloy should be largely unchanged. On the other hand, since La is a light rare earth, the solidification behavior of the alloy should be similar to those of Nd-Fe-B alloys. Therefore, the replacement of Y with La should remove the driving force for partitioning and help to obtain a uniform microstructure, which is expected to promote sintered magnets with better temperature stability.

The microstructures and the composition profiles across grains of the magnet sample were studied as presented in Fig. 2a and b. The results of electron microprobe composition profiles across the second phase and grains (Fig.2b) show that the grain boundaries are rich in La and Nd but depleted in Dy while the La, Nd and Dy contents are constant across the 2:14:1 grains. Therefore, the core-shell grain structure observed in that of $(Nd\text{-}Y\text{-}Dy)_{2.6}Fe_{14}B$ alloy was eliminated. In addition, the areas at triple junction and grain boundaries are a RE-rich phase, and highly rich in La and moderately rich in Nd but depleted in Dy, which results in a lower coercivity. In order to strengthen these regions, to improve the coercivity, DyF_3 is added in the magnets.

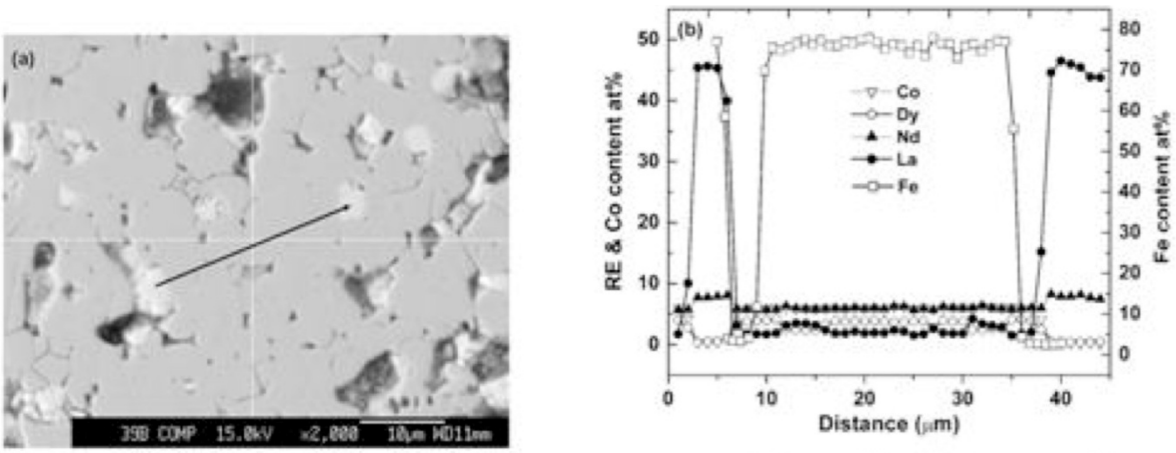

Fig. 2. Microstructure and electron microprobe composition profiles with La substituted for Y.

Table 3 lists the magnetic properties of magnets with the addition of 5%wt DyF_3 and different r (ratio of La:Dy). It is seen that the coercivity of the magnet with r=3 is greatly increased from 2.1 to 8.7 kOe after the addition of 5%wt DyF_3. In addition, the temperature coefficient of coercivity is significantly improved with increasing coercivity. At 100°C, the temperature coefficient α and β are as low as −0.06 and −0.48%/°C, respectively, while the typical values for the best high temperature Nd-based magnets are −0.10 and −0.48%/°C, respectively. The temperature coefficient values for the studied magnet are comparable to those of Nd-based magnets. However, the $(BH)_{max}$ of the studied magnet needs to be further improved.

Table 3. Magnetic properties of sintered $[Nd_{0.45}(La_rDy_1)_{1/(r+1)*0.55}]_{2.6}Fe_{13}Co_1B$ magnets with 5% DyF_3 addition and different r

r	3	2	1
M_r (kGs)	9.4	9	9
H_c (kOe)	8.7	9.7	15.1
$(BH)_{max}$ (MGOe)	20.2	19.0	21.1
α (%/°C)	0.084	0.080	0.060
β (%/°C)	0.632	0.608	0.470

3. Study of anisotropic melt spun ribbons devitrified during vacuum hot pressing

In pursuit of anisotropic powders for bonded magnets, studies applying uni-axial pressure during crystallization of $Nd_2Fe_{14}B$ are being performed. For uni-axial pressure crystallization, a $Nd_2Fe_{14}B$ + 3wt% TiC alloy was arc melted and melt-spun. Melt spinning was done at 25 m/s in order to form a mostly amorphous microstructure. The ribbons were hot pressed at 106 MPa in a graphite die while being heated to 640°C under vacuum. Fig. 3 shows an XRD pattern of the sample. The x-ray diffraction and SQUID measurements (not shown) both indicate that significant texturing was achieved through the application of uni-axial pressure during crystallization (ref.3). However, the annealing parameters need to

be adjusted since the coercivity of the samples was much lower than expected. It was suspected that the grains had grown too large to effectively pin domain walls.

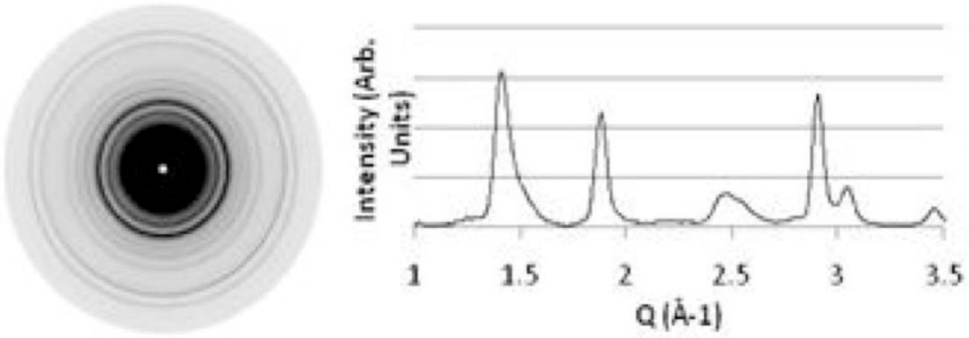

Fig. 3. XRD pattern of an amorphous ribbon that was crystallized during vacuum hot pressing.

A series of samples from the hot pressing experiments were also investigated using TEM in order to understand the crystallization behavior under applied pressure. The samples' nominal composition is $Nd_{0.8}Y_{0.8}Dy_{0.4}Fe_{14}B$ + 3% TiC, coded as NO-121-B (as-spun), NO-121-B-2 (580 ºC/60 min, 110MPa) and NO-121-B-3 (580 ºC/60 min, no applied pressure). Figure 4 gives the typical microstructures of the three alloys. The as-spun sample is almost fully amorphous with very few nuclei found in the matrix. EDS analysis didn't find any segregation/enrichment of TiC in the sample. The annealed sample without applied pressure shows a similar microstructure as other TiC added MRE samples (WT series). The average grain size of hard phase (2-14-1) is about 60 nm and many TiC particles (5–10 nm) formed along grain boundaries and triple junctions (Fig. 4 (right)). The sample annealed with applied pressure exhibits a quite unusual microstructure; see Fig. 4 (middle). The corresponding EDP can be indexed to either strong textured 2-14-1 or α-Fe, or both. A new series of the pressure-applied samples are under preparation for further verification/investigation for this effect.

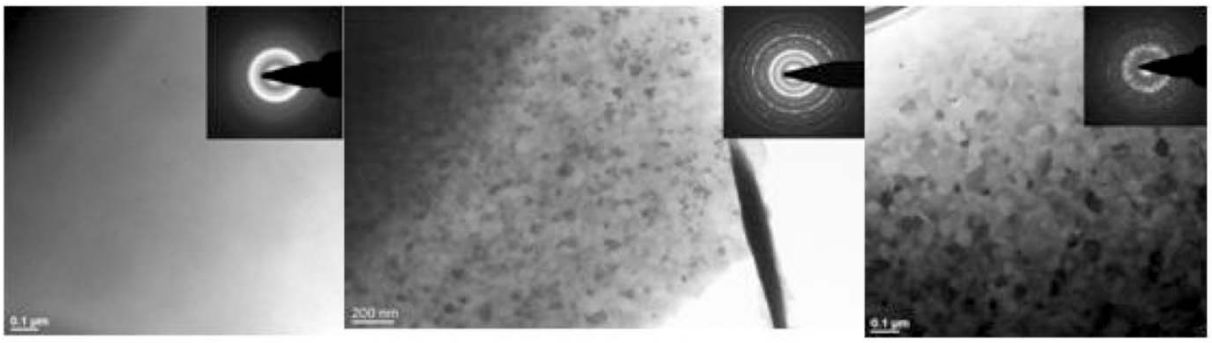

Fig. 4. TEM bright field images with corresponding electron diffraction patterns of (left) NO-121-B (as-spun), (middle) NO-121-B-2 (580˚C/60min., 110MPa), and (right) NO-121-B-3 (580˚C/60min., no applied pressure).

4. Study of new sintering technique on $[Nd_{0.45}(Y_3Dy_1)_{1/4*0.55}]_{2.6}Fe_{bal}B_{1.1}$ magnets

It is known that the microstructure of $[Nd_{0.45}(Y_3Dy_1)_{1/4*0.55}]_{2.6}Fe_{bal}B_{1.1}$ magnets after sintering at 1000°C or above shows a core-shell segregation structure in the 2-14-1 grains, which might be responsible for a strong temperature dependence. In a new sintering technique, the samples were sintered at 800-850°C for 1h with a uni-axial applied pressure up to 110MPa. Figure 5 shows a micrograph and electron microprobe composition profiles of the sintered sample. It is seen that the distribution of Nd, Y and Dy are basically uniform in the 2:14:1 grains. No obvious shell-core structure was observed. Sintered at 825°C for 1h under a 110MPa pressure, the sample has a density less than 7.0 cm^3/g, and its magnetic properties have

not been fully developed, indicating that the processing parameters still need to modified or optimized. However, the new sintering technique is very promising to develop high performance magnets with a composition much closer to that in Table 2. These investigations are ongoing.

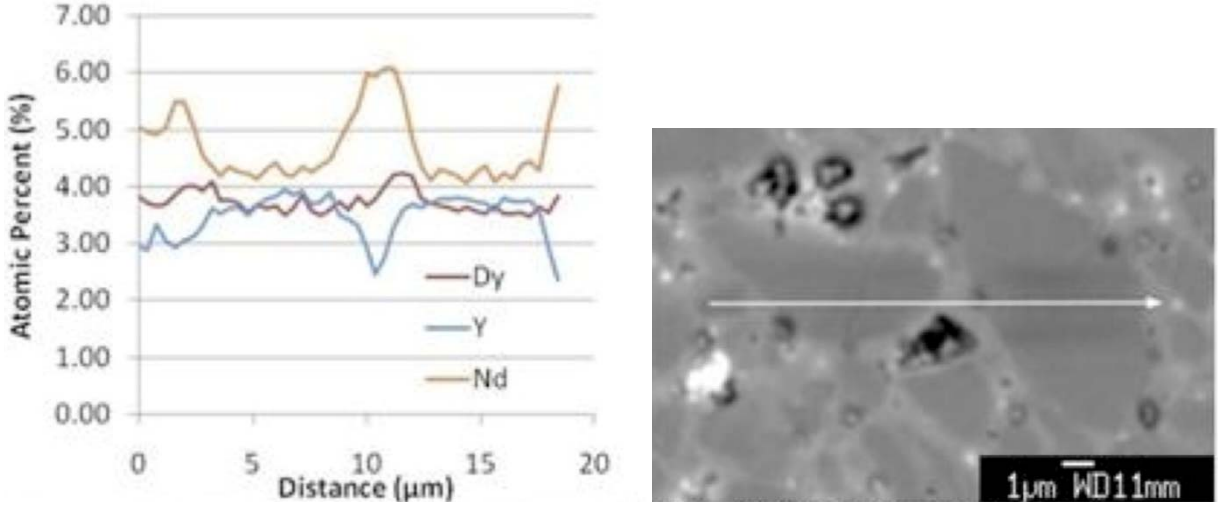

Fig. 5. Microstructure and electron microprobe composition profiles of sample sintered at 825˚C/1h with 110MPa applied pressure in vacuum hot press.

5. Study of reconstructed 3-D TEM images of $MRE_2Fe_{14}B$ ribbons

We successfully applied the STEM tomography technique to a ribbon sample (WT165) using the Tecnai G^2 F20 STEM. Figure 6 gives the STEM HAADF (Z-contrast) image and corresponding 3-D reconstruction results.

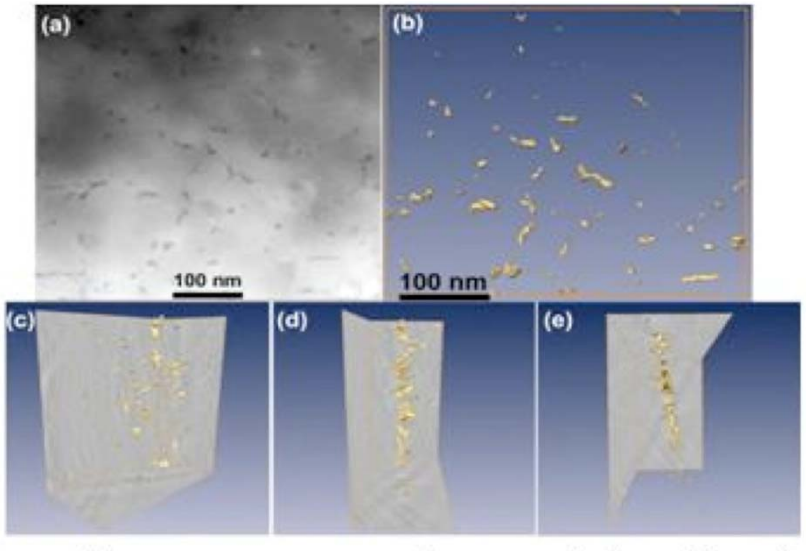

Fig. 6. (a) STEM HAADF image of the alloy (TiC particles in darker contrast) and corresponding ET 3-D reconstructed volume shown in (b) z-axis, (c) random, (d) x-axis, and (e) y-axis. The shape and morphology of the TiC particles are illustrated in yellow by using the iso-surface method.

Figure 7 gives the details at the center region of the reconstructed area. The majority of the TiC particles are oval or short rod-like in appearance and in a range of 5–10nm. During annealing procedure, excess Ti and C atoms are expelled from the formation of RE2-14-1 phase and then form TiC phase. The TiC grains

inhibit the hard phase to grow larger, therefore control microstructure. In this study, the 3D reconstructed sampled volume contains more than 20 grains of the RE2-14-1 phase and more than 70 TiC nano-particles. Therefore, there are ~1.7×10^8 TiC particles within a 1 mm^3 volume in the alloy, accounting for the strong pinning effect of the carbide addition. In summary, the STEM Tomography technique is a useful tool to explore and understand the details of magnet alloy microstructures.

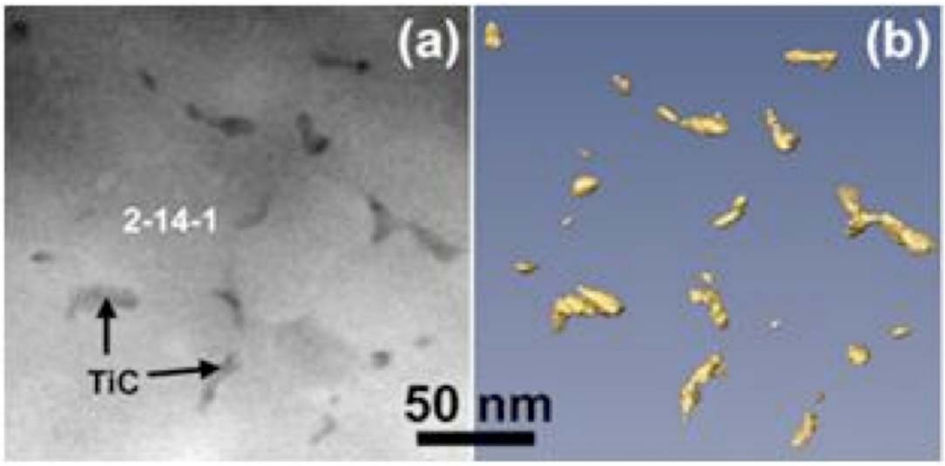

Fig. 7. (a) STEM HAADF image and (b) corresponding ET 3-D reconstructed volume, where the TiC particles are represented by the iso-surface.

Accomplishments in Beyond Rare Earth Magnets (BREM) Research

Accelerating rare earth cost pressure (resulting in a doubling of the cost of RE magnets in one year) and a recent glimpse of Chinese power (source for 97% of the world's RE supply) to impose RE supply limits outside of China have motivated a major augmentation of the original RE permanent magnet research project to include non-RE magnets. The new research thrust is an effort to elevate non-RE permanent magnet alloy designs to the realm of magnetic strength necessary for high torque PM motors. More specifically, this thrust will seek to develop permanent magnets based on Fe and Co with greatly increased coercivity and energy product, as well as a high Curie temperature, for advanced IPM traction motors. The investigation team includes first principles theory and modeling efforts (Theory Group), innovative synthesis of magnet compounds and prototype magnet fabrication (Synthesis Group), and highly detailed characterization with state-of-the-art instrumentation (Characterization Group). Drawing from US universities (Univ. Nebraska-Lincoln, Univ. Maryland, Brown Univ.), National Laboratories (Oak Ridge Nat. Lab., Ames Lab.), and commercial magnet producers (Arnold Magnetic Technologies), experts in magnetic materials from each area were formed into the team. Many team members belong to multiple groups as a natural coordination arrangement and the Ames Lab leadership core has structured numerous ways (including a team website, regular internet presentation/conference calls, and semi-annual face-to-face meetings) to ensure operation of the research team in a tight feedback loop.

After two workshop meetings the team developed and refined a plan that was followed in FY2010 and the accomplishments for the first partial year of work are summarized below, organized according to the task structure. The initial general plan is to explore two parallel research tracks, i.e., improvement of the best existing non-RE magnet system, Alnico, and discovery of new non-RE magnetic phases, focused on Fe, Co, and Fe-Co systems. The Alnico work will seek enhanced knowledge of coercivity mechanisms, increased control of microstructure and magnetic alignment, and beneficial composition modifications. New magnetic phase discovery will involve theory and modeling to guide the choices of base compositions and selection of minor additives to accentuate magneto-crystalline anisotropy, searching for maxima in intrinsic magnetization, magnetic anisotropy, and Curie temperature. Micromagnetics modeling will help specify extrinsic parameters for the new phases that optimize anisotropy, maximizing

shape, stress, surface, and exchange contributions to coercivity. As the experimental results from magnet synthesis work indicate promising directions, bulk magnet fabrication work will proceed to produce scale-size magnet samples for IPM motor testing and for development of magnet processing methods that can be scaled to industrial magnet production techniques.

Progress on the 4 tasks in the Theory Group studies:

Task 1. Literature Analysis for Assembly of Known and Promising Compounds
We have successfully initiated an effort in collaboration with Synthesis Partners (separately funded by VT) to identify appropriate search algorithms for assembling a database of non-rare earth (primarily) magnet compounds. Refined tests on a set of 5 papers selected from the literature showed that the computer algorithms can identify targeted data such as crystal structures and intrinsic magnetic properties (Curie temperature, magnetic moment, and magnetic anisotropy) . Some preliminary investigation of "machine reading" of literature for maximum efficiency and coverage of early work on non-RE permanent magnets is in progress. In the next stage, we will expand the scope of the database to encompass as many English language publications as possible, and add new publications to the database from all surveyed sources and further explore "machine reading" of literature. The beginning minimal database is now open for use by the entire project team members. Suggestions for improvement and changes will be coordinated for the team by the database oversight committee (Skomski, McCallum, and Antropov), but all team members are expected to contribute literature copies for analysis. Rehbein will perform the technical effort required to create and maintain database. We will also pursue the implementation of searchable annotations of literature to create an "expert" database.

Task 2. Theoretical Phase Diagram Exploration and Materials Structure Optimization
We have initiated the development of efficient computational algorithms to explore the crystal structure configuration space for a given set of compounds within a range of compositions of interest. To effectively search complex systems with multi-element (binary, ternary and beyond) compositions and a large number of atoms per unit cell (e.g. 50-100), it is necessary to search phase space with the use of fast empirical inter-atomic potentials. Since developing such potentials can be very time consuming, we adopted a strategy of developing algorithms that can provide a feedback mechanism to modify the accuracy of the inter-atomic potentials at the same time that the search is being performed. Candidate structures from such a search strategy will be further refined and validated by ab initio calculations. The success of such on-the-fly algorithms will enable the efficient and timely use of computational resources for materials discovery. One postdoctoral fellow will start in October 2010 to begin work on this project.

Task 3. Magnetic Properties Calculations
Initial studies of intrinsic properties of specific materials have been performed for several systems:

a. Fe-Co systems of ordered intermetallics and disordered alloys were studied. The magnetic moments, magnetic anisotropy and Curie temperature have been calculated using electronic structure methods and the original linear response scheme was modified and adjusted for this project. Preliminary results that we obtained indicate that the maximum of each property occurs at a different Fe-Co concentration (see Fig. 8). The ordered intermetallics demonstrated better magnetic anisotropy compared to disordered alloys at the same concentration. An experimentally unknown bcc phase of Co was found to have a very high Curie temperature. Such a Co crystal structure may exist in this films and clusters. Studies of Fe-Co alloys will be continued due to the importance of this prototype system for our project. We will consider the inclusion of the effects of different distortions, substitutions, defects and impurities.

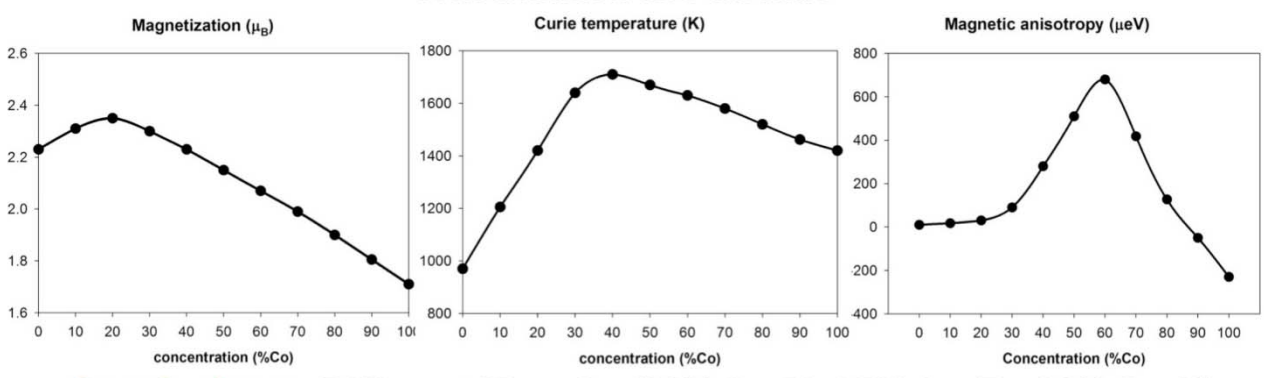

Fig. 8. Electronic structure calculation results for intrinsic magnetic properties of Fe-Co system.

b. The $Fe_{16}N_2$ system was studied, where the record magnetization has been reported. Our initial studies indicated no significant increase of magnetization with a moderate Curie temperature and significant magnetic anisotropy only in film geometry. These studies also will be continued to provide better argumentation about whether or not this material is suitable for our project.

c. We have studied the magneto-crystalline anisotropy energy of Fe atoms situated in the highly anisotropic environment of a single layer on a metal surface to establish the limit of how a strongly anisotropic environment can be used to enhance the magnetic anisotropy of a material.

d. We have investigated how interstitial C and N modify the magnetic anisotropy of iron. The effect has long been exploited in steel magnets, and there are many studies on the corresponding structural and mechanical properties and, to lesser extent, on magnetic properties such as magnetization. However, very little is known about the origin of the systems magnetic anisotropy. In cooperation with Arti Kashyap and her group, we have used a full-potential linear augmented plane wave (FP-LAPW) method with a generalized gradient approximation (GGA) for exchange and correlations. The carbon and nitrogen atoms, which occupy one set of octahedral interstitial sites in the tetragonally distorted bcc structure (see example of C in Fe in Fig. 9), yield a pronounced chemical contribution to the anisotropy, in addition to the well-known strain effect caused by long-range elastic interactions and martensitic ordering.

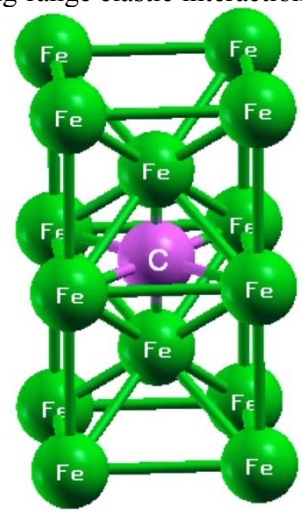

Fig. 9. Illustration of C in interstitial site of bcc-Fe lattice.

The magnetic moments of the Fe atoms are slightly reduced due to hybridization, but the system exhibits an appreciable magnetic anisotropy. Extrapolated to 100% C and N, respectively, the predicted anisotropies are 7.7 MJ/m3 and 3.9 MJ/m3, which is promising and consistent with available

experimental data. The calculated magnetic properties also are consistent with available experimental anisotropies, such as 0.40 meV and 0.32 meV per atom for C and N in martensitic Fe, respectively. Carbon contents in many steels are typically of the order of 0.9 wt.%, or 4 at.% ($Fe_{96}C_4$), which translates into an anisotropy constant of 0.21 MJ/m3.

Task 4. Micromagnetics modeling
At this early stage, we are still in the process of identifying suitable magnetic systems for our micromagnetics modeling study.

Progress on the 3 tasks in the Synthesis Group studies in FY2010:

Task 1. Synthesis of Model Magnet System Samples
Compilation of an inventory of thin film and nano-scale magnet material synthesis capabilities at each partner institution was begun for the project data library.

In concert with theoretical analysis, combinatorial synthesis experiments were performed on an appropriate binary alloy (Fe-Co) that is modified by a third element (W), searching for single-phase magnetic compounds with anisotropic crystal structure and a minimum of Co content. As Fig. 10 indicates, 3 separate sputtering targets were used to deposit several 500 nm thick films at room temperature with variable composition on a pre-oxidized Si substrate. Individual tiles that capture a limited composition sector were sliced from the deposited film and were prepared for characterization by annealing under vacuum at several temperatures. One set of samples that was annealed at 600˚C was subject to detailed characterization. A large composition region covering most of the ternary phase diagram was mapped (Fig. 10), and regions of lower W concentration (%W less than 40%) were studied in detail.

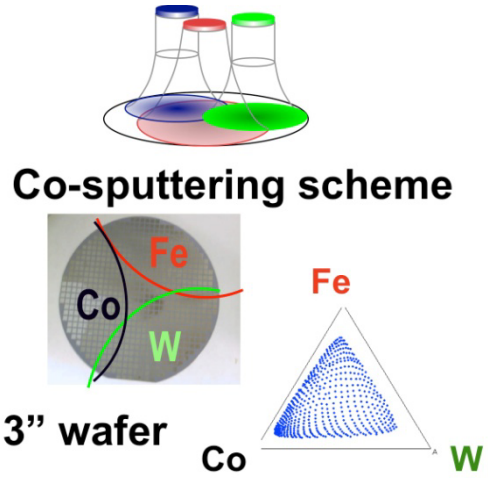

Fig. 10. Schematic of combinatorial synthesis experiment to generate composition field of Co-Fe-W.

In coordination with theoretical efforts, experiments on nano-particulate cluster deposition were started. We have measured the magnetic anisotropy constant (K_1) for cluster-deposited YCo_5 and $Co_{1-x}Pt_x$ (x ~ 0.1) nano-particles from the magnetic measurements carried out using a SQUID magnetometer. YCo_5 nano-particles were observed to be ferromagnetic with $H_c \sim 6$ kOe at 300 K and *M* vs. *H* curves reveal that the magnetization does not reach the saturation even at an applied field of 70 kOe. We estimated the value of K_1 to be $\sim 2.0\ 10^7$ ergs/cm^3 for YCo_5 nano-particles by fitting the experimental magnetization curves using the method "law of approach to saturation." $Co_{0.9}Pt_{0.1}$ nano-particles exhibit super-paramagnetic behavior with $H_c = 0$ and $M_r/M_s = 0$ at $T_{meas} \geq 50$ K and

show non-zero coercivities at T_{meas} 30 K. FC and ZFC magnetization curves also reveal the super-paramagnetic behavior of these nano-particles by showing a blocking at T_b = 50 K. We estimated the value of the magnetic anisotropy constant (K_1) of $Co_{0.9}Pt_{0.1}$ nano-particles using T_b to be 1.2 10^7 ergs/cm^3. Co-W nano-clusters also were produced by inert gas condensation. A composite target was used, with relative areas of Co and W designed to produce a composition of Co-25 atomic percent W, based on relative sputtering yields.

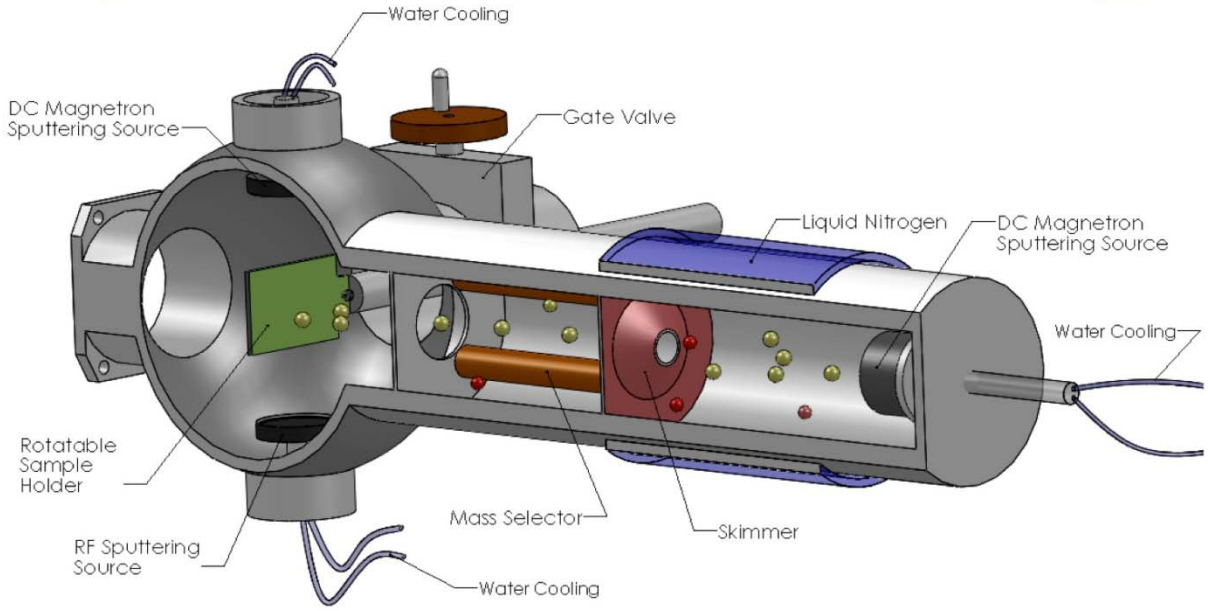

Fig. 11. Schematic of cluster deposition system for producing nano-particulate of magnet alloys.

In the past year, focus was placed on synthesis and self-assembly of ferromagnetic FePt and Fe nano-particles to demonstrate that self-assembly is a future approach to high performance dual phase exchange-spring nano-composite magnets containing non-rare earth nano-particles. Previously (Nature 2002), we have reported that self-assembly of FePt and Fe_3O_4 nano-particles followed by reductive annealing led to the formation of an exchange-spring FePt-Fe_3Pt nano-composite magnet with its $(BH)_{max}$ enhanced by 37% compared with the single component FePt nano-materials. However, the high temperature annealing step caused serious nano-particles aggregation/sintering and inter-particle Fe/Pt diffusion. As a result, it is difficult to control size and composition of both hard and soft phases. In the current efforts, we plan to make ferromagnetic FePt and Fe nano-particles first, then assemble them into nano-composites without the high temperature thermal annealing process. If it is successful, we will be able to make exchange-spring FePt-Fe nano-composite magnets with both size and composition controlled and $(BH)_{max}$ optimized.

Figure 12 outlines the general method we used for preparing ferromagnetic face-centered tetragonal (fct) FePt nano-particles. We first made super-paramagnetic face-centered cubic (fcc) FePt nano-particles via thermal decomposition of iron pentacarbonyl, $Fe(CO)_5$, and reduction of platinum acetyacetonate, $Pt(acac)_2$, with oleic acid and oleylamine as surfactant and diphylether as solvent. After the synthesis, we further coated fcc-FePt nano-particles with MgO by decomposing $Mg(acac)_2$ on the fcc-FePt nano-particle surface. With the robust MgO coating, the FePt/MgO nano-particles could be annealed at high temperature and the fcc to fct structure transformation was achieved within the MgO coating shell that was removed by washing with dilute HCl solution. Figure 12 A illustrates the synthesis. Figure 12 B and C are the TEM images of the 7 nm fcc-$Fe_{60}Pt_{40}$ and fct-FePt nano-particles, respectively. Although sintering was not excluded in these earlier tests, the fct-FePt nano-particles indeed were made by

removing the MgO coating and they do show ferromagnetic properties (Figure 12 D). Work to improve the quality of the fct-FePt nano-particles is underway.

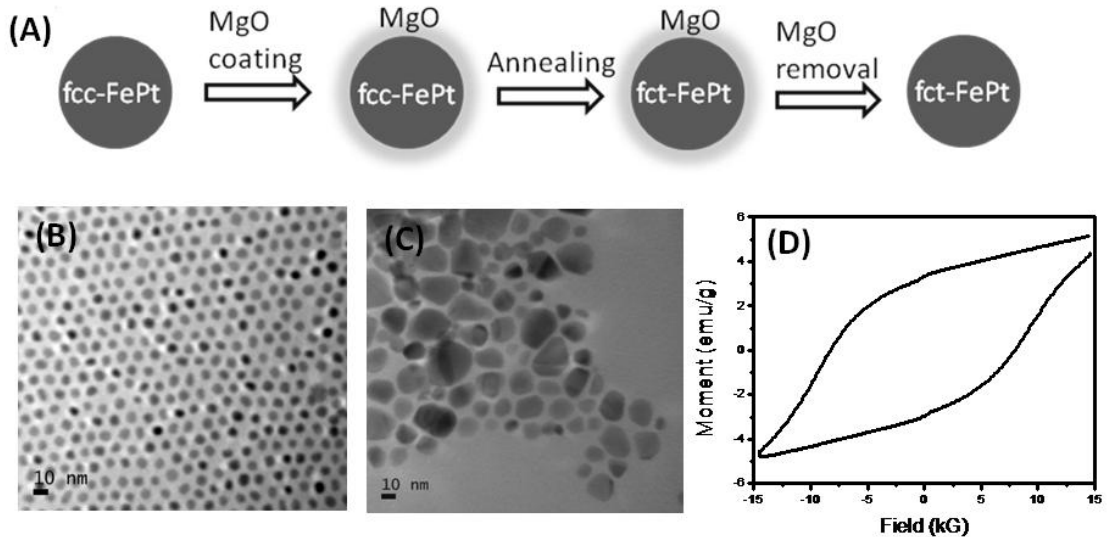

Fig. 12. (A) Schematic illustration of the synthesis of fct-FePt nano-particles; (B) TEM image of the 7 nm fcc-$Fe_{60}Pt_{40}$ nano-particles; (C) TEM image of the fct-FePt nano-particles after MgO removal; (D) room temperature hysteresis loop of the fct-FePt nano-particles.

To make high moment Fe nano-particles, we have developed a method via thermal decomposition of $Fe(CO)_5$ with oleylamine and hexadecylamine-hydrochloric acid as surfactants and 1-octadecene as solvent. The decomposition at 180°C yielded single crystalline monodisperse Fe nano-particles as proved by observation in the TEM (Figure 13 A) and XRD (Figure 13 B).

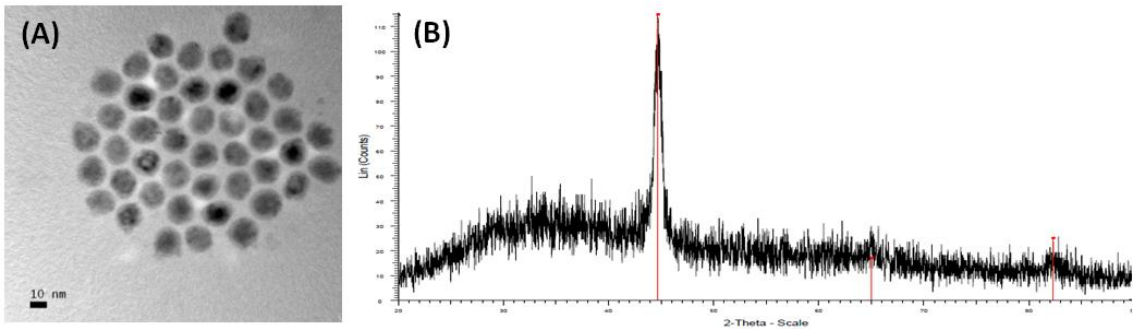

Fig. 13. TEM image of the 14 nm Fe nano-particles; (B) XRD of the 14 nm FePt nano-particles showing typical body centered cubic (bcc) structure.

Task 2. Experimental Magnetic Materials Fabrication
Compilation of inventory of material processing capabilities for bulk magnet fabrication at each partner institution was begun for the project data library.

Investigation of the coercivity contributions in Alnico (dual phase spinodal Fe-Co/Ni-Al alloys) was started with a literature review on the contributions of various alloying additions, microstructure evolution, and processing. From this review and discussions with Arnold Magnetic Technologies, the Alnico 5-7 alloy was selected for further analysis, since it has the highest energy product and a columnar microstructure. Alnico 5-7 samples were supplied by Arnold Magnetic Technologies at various stages of the heat treatment and thermal magnetization process and were sectioned and mounted for SEM characterization. A special sample of a finished magnet also was prepared from a section perpendicular to

the columnar growth axis for orientation imaging microscopy (OIM). The process of preparing TEM samples is ongoing, where a problem with demagnetization was recently solved, but determination of a suitable chemical etchant remains ahead. Full alloy sputtering targets also were prepared from larger arc-melted ingots for synthesizing experimental thin films of analogous Alnico compositions in a apparatus similar to that in Fig. 10. All samples have been distributed to the Characterization Group for collaborative microstructure and magnetic analysis.

A directional decomposition experiment is currently being developed, involving rods cut from finished Alnico 5-7 magnets. The intent of the experiment is to determine the effect of a thermal gradient on the microstructure of the magnet. The commercial production uses a magnetic field during the heat treatment to align the precipitates, improving the magnetic properties of the finished magnet. The experiment will examine if a thermal gradient can supplement or replace the magnetic field during the heat treatment.

The Theory Group was consulted on selection of a limited set of promising binary or ternary magnetic systems that are known to form anisotropic intermetallic phases or have other general interest for theoretical analysis.

Task 3. Analysis of Critical Magnet Material Constituents
A listing of potential magnet material constituents was compiled and representative commercial pricing and supply information was obtained for the purpose of preparing a position paper on the cost analysis and availability of several magnet constituents, starting with Co.

Progress on the 3 tasks in the Characterization Group studies in FY2010:

Task 1. Development of Data Sharing Mechanism for Characterization Results
Web-based data sharing methods and protocols were brought to the final stages of development to enable active comparison of results by all partners for the same materials that are characterized by a full spectrum of characterization tools.

Task 2. Advanced Characterization Methods
Collaborations have been initiated at synchrotron sources (SLAC and APS) to develop the capabilities for a variety of high-throughput materials characterizations studies. Team members have contributed jointly to an NSLS-II beamline proposal entitled: "Multiscale XRD," which was approved for NSLS-II at Brookhaven. Preliminary experiments have been performed on combinatorial libraries of Fe-Co-W at beamline 11-3 at SLAC in collaboration with A. Mehta (see below). Contacts have been made at port 8-2 at SLAC for the possibility of doing X-ray magnetic circular diachroism (XMCD) on selected samples.

Task 3. Structural and Magnetic Characterization
Compilation of a complete inventory of magnet material characterization capabilities at each partner institution was begun to add to the project data library.

Bulk structural and microstructural analysis and magnetic measurements on preliminary samples from the Synthesis Group have been performed and shared with the team members for analysis of potential magnetic material candidates. In the case of the Co-Fe-W thin film tiles that resulted from combinatorial synthesis, synchrotron micro-diffraction (see Fig. 14) of tile regions from the spread indicates that the main diffraction peak corresponds to that of the (110) bcc phase across the spread. Near the Fe-Co binary line, the lattice constant of the bcc phase changes in an expected manner, namely that the lattice constant increases as Fe concentration is increased. As the W concentration is increased beyond ~10%, the diffraction peak width increases substantially consistent with the fact that W has a much higher crystallization temperature (Fig. 14).

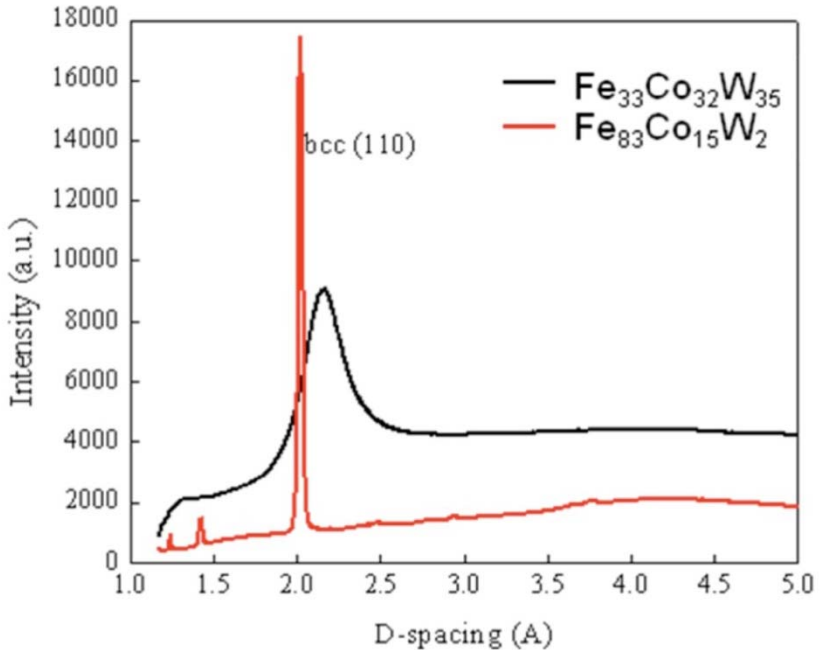

Fig. 14. Synchrotron diffraction results of selected compositions. Peak broadening at higher W concentration indicates that the material has not fully crystallized at the annealing temeprature of 600 ºC.

From MH (hysteresis) loop characterization of the lower W concentration region (~2%), we found several compositions where the out-of-plane (OOP) MH loop displays significant coercive field (see Fig. 15). In particular, $Fe_{83}Co_{15}W_2$ shows a coercive field higher than 3 kOe. By carrying out angular dependent hysteresis loops on selected compositions, we found that the magnetization reversal mechanism changes with changing W composition. We plan to repeat this experiment with new spreads where the composition region is focused to the lower W concentration and to study detailed composition dependent magnetic properties in order to confirm if there is indeed a promising high coercive field phase in this region.

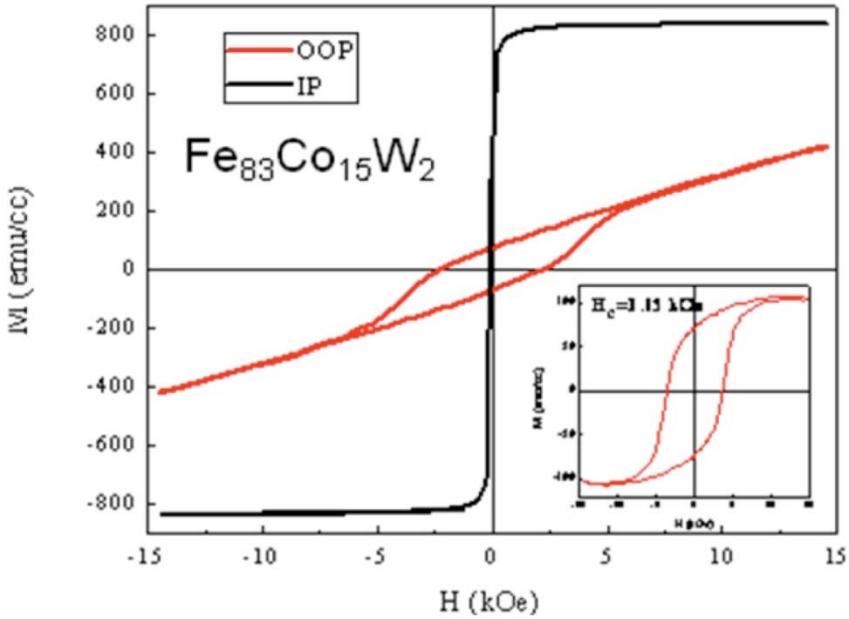

Fig. 15. MH loops of one of the compositions that displays a large coercive field in the out of plane (OOP) direction. The inset is the out-of-plane loop with the "linear" background subtracted.

A proof of concept experiment (with Co-W initially) was performed using advanced electron microcopy to connect (correlate) cluster synthesis experiments and large-scale modeling. Samples of the initial as-condensed Co-W particulate from the cluster deposition experiments were characterized by STEM, with an example shown in Fig. 16. From EDS measurements in the STEM, the average composition of all of the nano-particulate appeared to be Co-21 at.%W (near the intended composition), but significant composition segregation segregation also was evident. The finest particulate (about 1 nm) appeared to be Co-75W and the larger clusters (3-5 nm) appeared to be Co-15W and amorphous. STEM images also suggested that the ~ 5 nm clusters were agglomerations of several clusters, indicated by inhomogeneous contrast within the larger clusters. This is the first case that we have seen where two different cluster types precipitated from the gas phase. Modifications to the evaporation target and deposition parameters were made to address this issue, as well as a suitable annealing procedure to promote particulate homogenization and crystallization. The new clusters have yet to be analyzed.

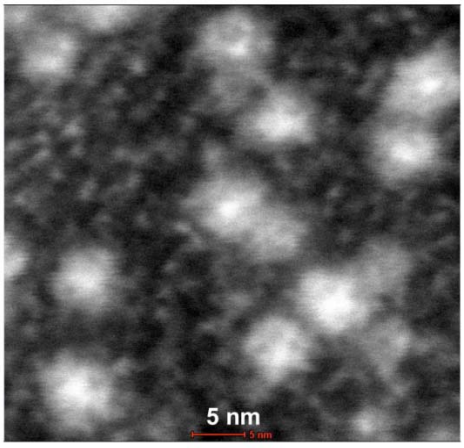

Fig. 16. High resolution STEM micrograph of as-deposited Co-W nano-particulate from cluster deposition experiments.

Alnico 5-7 samples were imaged in the SEM (see Fig. 17). The micrographs were used to determine if significant grain growth occurred during the heat treatment process, as well as to determine the extent of columnar growth in the casting. OIM analysis (Fig. 17) was performed on a wafer of finished Alnico 5-7. The results showed good alignment of the [001] with the growth direction of the grains, but random orientation of the grains in the transverse plane of the casting.

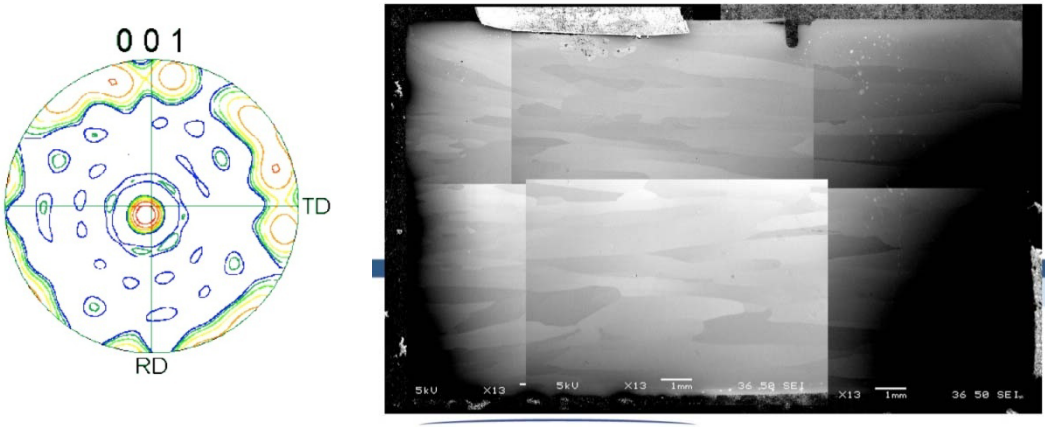

Fig. 17. OIM pole figure (left) from transverse section of Alnico 5-7 that shows excellent grain alignment along the magnetization direction, but random orthogonal alignment. Also, a composite SEM micrograph of the transverse section is shown (right), where very large aligned grains are visible.

Conclusion

To enable anisotropic sintered MRE magnet development, refinement continued of the processing steps needed to make particulate with an average particle size of ~3μm, with lower oxygen contamination, and with a reduced Dy content, along with progress toward significant reduction of excess rare earth in the MRE alloy to reduce alloy cost and to help enhance final energy product. In subsequent progress, a new pressure-enhanced sintering process was developed specifically for MRE magnet alloys that enabled reduced temperature (<850˚C) sintering to eliminate the deleterious "core-shell" segregation pattern in the 2-14-1 phase grains (with Y-enrichment around the rim of each grain) in the finished magnets and to restore high temperature stability by returning to the preferred Y addition to the MRE. To enable anisotropic bonded MRE magnet development, application of a uni-axial pressure gradient on ribbon samples during crystallization proved promising and will be pursued further. In response to a request to initiate a new research thrust that goes beyond rare earth permanent magnets, a large new thrust was started within the project. As described in the progress elements above, a detailed plan was developed in two planned workshop sessions and the full team of research partners began a highly collaborative research program in April of 2010. The initial general plan to explore two parallel research tracks was followed, i.e., seeking improvement of the best existing non-RE magnet system, Alnico, and discovery of new non-RE magnetic phases, focused on Fe, Co, and Fe-Co systems. The first Alnico efforts are still focused on enhanced knowledge of coercivity mechanisms, but we will begin studies of increased control of microstructure and magnetic alignment next year. Initial work on new magnetic phase discovery involved theory and modeling of Fe, Co, and Fe-Co base compositions and started into selection of minor additives to accentuate magneto-crystalline anisotropy, searching for maxima in intrinsic magnetization, magnetic anisotropy, and Curie temperature. Micromagnetics modeling will probably commence next year. Several of the experimental magnet synthesis efforts generated promising results and more detailed efforts will proceed next year. The suite of characterization tools for magnetic properties, microstructural analysis, and crystal structure determination proved very useful for feedback on the synthesis experiments and for general guidance to the theory and modeling efforts. Much more progress is anticipated in FY2011 since a full year of effort can be expended. It should be noted also that we have added a new industrial partner to our team, Arnold Magnetic Technologies, which should help to preserve our focus on eventual manufacturing and application of the non-RE permanent magnets that we develop.

Publications

1. W. Tang, Y. Q. Wu, K. W. Dennis, N. T. Oster, M. J. Kramer, I. E. Anderson, R. W. McCallum, *Magnetic properties and microstructure of gas atomized $MRE_2(Fe,Co)_{14}B$ powder with ZrC addition (MRE = Nd + Y + Dy),* Journal of Applied Physics (2009), 105(7, Pt. 2), 07A728/1-07A728/3.
2. Y. Q. Wu, W. Tang, M. J. Kramer, K. W. Dennis, N. T. Oster, R. W. McCallum, I. E. Anderson, *Correlation of the energy product with evolution of the nanostructure in the Y,Dy,Nd-(Fe, Co)-B magnetic alloy,* Journal of Applied Physics (2009), 105(7, Pt. 2), 07A720/1-07A720/3.

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1. D. Dadon, Y. Gefen, and M. Dariel, "The texture of melt spun $Fe_{76}Nd_{16}B_8$ ribbons," *Magnetics, IEEE Transactions on,* vol. 23, pp. 3605-3606, 1987.
2. M. J. Kramer, N. Yang, R. W. McCallum, K. W. Dennis, and L. H. Lewis, "In situ determination of Nd-Fe-B crystallization pathways," *J. Appl. Physics*, vol. 91, pp. 8156-8158, 2002.
3. W. B. Kamb, "Theory of Preferred Crystal Orientation Developed by Crystallization under Stress," *The Journal of Geology,* vol. 67, pp. 153-170, 1959.

Patents

1. R. W. McCallum, Y-W. Xu, I. E. Anderson, K. W. Dennis, and M. J. Kramer, U.S. Patent Application (PCT) filed November 18, 2002, "Permanent Magnet Alloy with Improved High Temperature Performance," under examination.

3.4 Scalable, Low-Cost, High Performance IPM Motor for Hybrid Vehicles

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Objectives

Electric drive systems, which include electric machines and power electronics, are a key enabling technology for advanced vehicle propulsion systems that reduce the petroleum dependence of the transportation sector. To have significant effect, electric drive technologies must be economical in terms of cost, weight, and size while meeting performance and reliability expectations.

The objective of the GE Global Research "Scalable Low-Cost, High-Performance IPM Motor for Hybrid Vehicles" program is to develop a higher power density IPM motor at a lower cost. Successful completion of this program will accelerate the introduction of hybrid electric vehicles into the U.S. road vehicle fleet and bring the added benefits of reduced fuel consumption and environmental impacts.

(A) Motor Development

- Develop advanced motor concepts including electromagnetic, mechanical, and thermal concepts.
- Build proof-of-principle machines to verify the design process as well retire the key risks.
- Design and build 55kW/30kW machines that meet the DoE specifications
- Develop cost model to estimate the advanced IPM motor based on 100000 units/year
- Investigate the scalability of the developed concepts by building and testing a 120kW/65kW machine

(B) Materials Development

- Demonstrate scalable processing of high resistivity permanent magnet and determine cost advantage
- Perform materials selection study for rotor components

Approach

(A) Motor Development

- Simplified stator windings will reduce end-turn length and losses, together with motor mass and volume and manufacturing cost.

- Advanced rotor concepts to achieve higher power density as well as meeting the high-speed requirement.
- Advanced scalable thermal management schemes for both the stator and the rotor to meet the required set of specifications.

(B) Materials Development

- Co-sintering process improvements to enhance reproducibility and scalability of high effective resistivity microstructures
- Scale-up to kilogram scale of high resistivity permanent magnets at domestic permanent magnet producer.
- Apply Asbhy material selection method to evaluate candidate materials for rotor component based on mechanical, magnetic, and thermophysical property constraints

Major Accomplishments

(A) Motor Development

- Two rotor and two stator electromagnetic (EM) concepts developed & analyzed in detail
- Scalable rotor and stator cooling concepts selected to meet performance, simplicity and scalability requirements
- Highest-performance EM concepts selected for proof-of-principle motors build.
- First proof-of-principle machine built and fully tested
- Second proof-of-principle machine (different rotor structure) built and fully tested
- Third machine design finalized, and build almost finalized.
- Development of cost model finalized (fine tuning is still needed)

(B) Materials Development

- Achieved kilogram scale production of $Nd_{15}Fe_{77}B$ permanent magnet powder for scaled processing
- Identified insulating layer compositions whose densification behavior approaches that of NdFeB with minimal reaction with NdFeB
- Completed materials selection study with changes recommended to rotor shaft material and magnet retaining elements.

Future Direction

(A) Motor Development

- Finish the building and testing of the third 30/55 kW machine
- Verification testing to be witnessed by the DoE
- Design and build scaled-up IPM > 65/120kW
- Receive and test scaled-up IPM
- Cost estimate for large-scale IPM motor production

(B) Materials Development

- Tune sintering behavior of insulation phase to match NdFeB
- Identify insulating phase composition with lowest raw material costs
- Demonstrate kg scale production of high-resistivity magnet at external vendor

Technical Discussion

(A) Motor Development

As previously mentioned, the first proof-of-principle (PoP) machine was down-selected based on highest EM performance. Fig. 1 shows the PoP machine on the dynamometer. The segmented stator with FSCW

is shown in Fig. 2 while the rotor is shown in Fig.3. Fig.4 shows a very close comparison of the measured versus predicted (using FEA) back emf at 100 rpm. The machine is designed to exceed the peak power of 55 kW for 18 seconds by 5 kW without exceeding the 400 Arms limit. The machine has been tested to 33 kW and 14000 rpm. This confirms the machine sizing. This also shows that the machine with its fundamentally novel rotor structure can run safely at 14000 rpm, which was one of the key risks. Also, this shows that the machine is capable of producing the rated power over the entire speed range.

Fig. 5 shows the various measured machine performance parameters at rated power as well as comparison of measured and predicted efficiency (including both electrical and mechanical losses). These measurements are based on steady state heat runs. It can be seen that the voltage limit is reached around 4000 rpm, which represents the machine corner speed. These results show that the machine exceeds both steady state and peak power requirements. Efficiency targets are met up to 9,000 rpm while the 105^{o}C coolant inlet temperature is met up to 7,500 rpm and more work is needed to meet these challenging targets at higher speeds. The machine efficiency at 14,000 rpm is around 88%, significantly higher than the state of the art, which is in the low 80s [1]. Fig.6 shows similar results at 20% of the rated torque.

Fig. 7 shows a comparison of the PoP machine measured (electrical and calorimetric) vs. predicted losses at rated power. It can be seen that calorimetric loss measurements and electrical input/mechanical output based loss measurements have reasonably good agreement. This gives more confidence in the measurements. Both have good match with predictions. The match is not as good at the 14,000 rpm. This is mainly due to the deterioration of a seal that created additional losses. Fig. 8 shows the machine heat run temperature rises at various speeds.

Temperature rises in various machine locations are as expected. This provides confidence in the stator and rotor thermal management schemes and predictions. The only exception is that the cooling jacket and stator yoke temperature rises indicate higher thermal resistance between them than expected. This has been investigated further and a potential reason found is that as the stator has a segmented structure, it might lead to poorer contact between the cooling jacket and the stator OD. Measures have been taken to improve this contact in the second machine that has been built and tested. These measure include:

(1) Sacrificial aluminum ring shrunk fit to achieve concentricity of the segmented stator
(2) Stator VPI (Vacuum Pressure Impregnation)
(3) Remove sacrificial ring and add thermal paste
(4) Shrink fit the lower cooling jacket

These steps are illustrated in Fig.9.

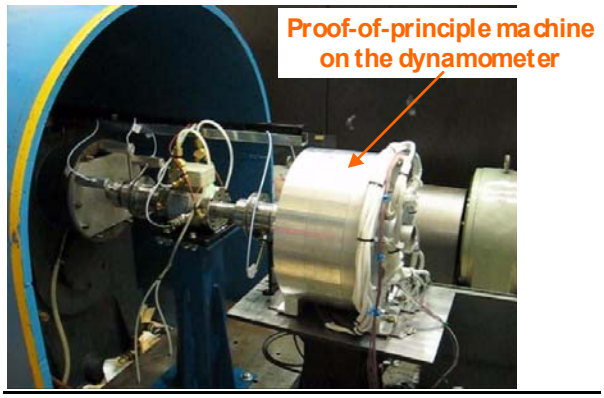

Fig. 1. Proof-of-principle machine on the dynamometer.

Fig. 2. Stator of the first proof-of-principle machine

Fig. 3. Rotor of the first proof-of-principle machine

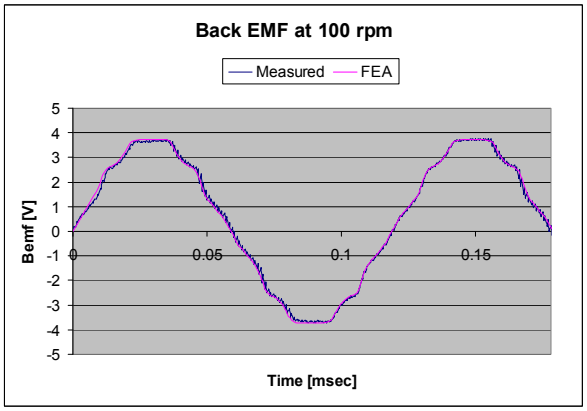

Fig. 4. Predicted vs. measured back emf of the first proof-of-principle machine at 100 rpm.

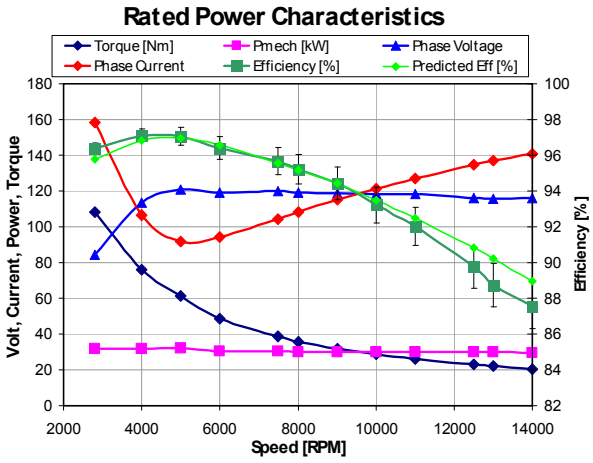

Fig. 5. First proof-of-principle machine measured performance at rated power

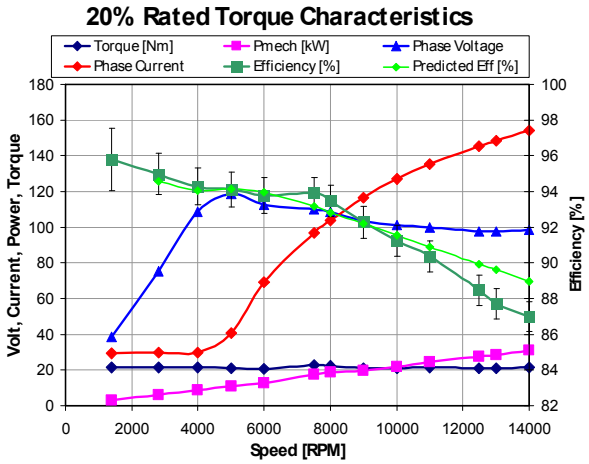

Fig. 6. First roof-of-principle machine measured performance at 20% rated torque

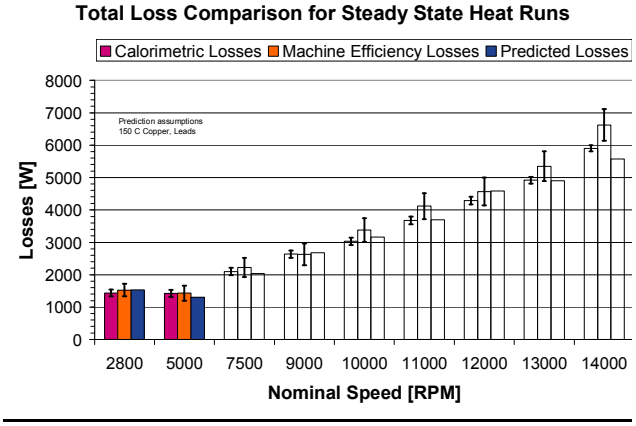

Fig.7. First proof-of-principle machine measured (electrical and calorimetric) vs. predicted losses at rated power

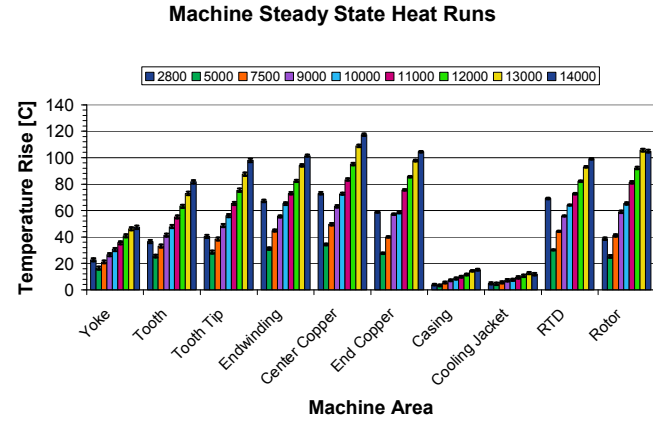

Fig.8. First proof-of-principle machine heat runs temperature rises in the various machine components at various speeds.

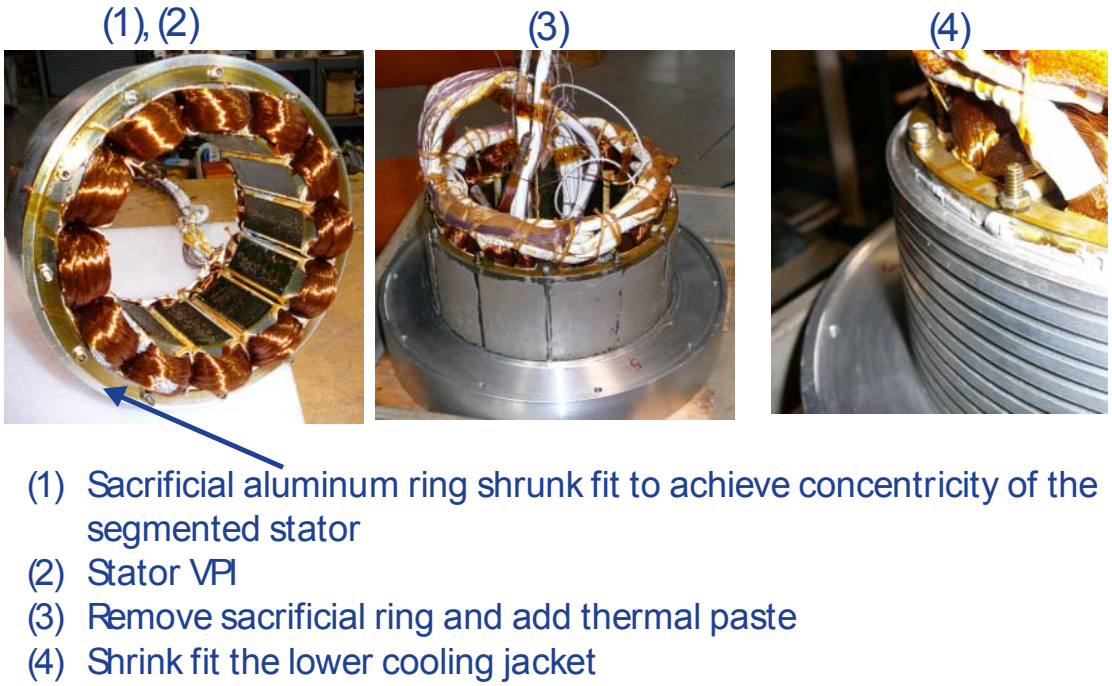

Fig. 9. Assembly steps to improve contact between the cooling jacket and the stator outer diameter

The second PoP machine has almost identical stator to the first PoP machine with the exception of a longer stack length and VPI. The rotor is the conventional one with v-shaped magnets shown in Fig.10.

In order to separate mechanical and electrical losses, the machine was first assembled unmagnetized. Fig. 11 shows the mechanical losses of this machine. Based on the test results, more modifications are planned to reduce mechanical losses at 14,000 rpm by ~35%. These include using low-loss bearings and seals as well as reducing rotor inner bore cooling related churning losses.

Next, the machine with magnetized magnets was tested. Fig. 12 shows the various measured machine performance parameters at rated power as well as comparison of measured and predicted efficiency. It can be seen that the voltage limit is reached around 5,000 rpm, which represents the machine corner speed. Similar to the first PoP machine, these results show that the machine meets both steady state and peak power requirements but the first machine can produce more power as will be discussed in the next section. Efficiency targets are met up to 9,000 rpm. The machine efficiency at 14,000 rpm is around 88%. Fig.13 shows similar results at 20% of the rated torque. In general, these results are comparable to the first machine.

Fig. 14 shows a comparison of the PoP machine measured (electrical and calorimetric) vs. predicted losses at rated power. It can be seen that calorimetric loss measurements and electrical input/mechanical output based loss measurements have reasonably good agreement. This gives more confidence in the measurements. Both have good match with predictions.

Fig. 15 shows the machine heat run temperature rises in its key locations at various speeds. Temperature rises in various machine locations are as expected. It can be seen that the temperature rise is lower than in the first PoP machine. This is partly because the second machine is bigger and has lower power density and partly because of the VPI of the stator which provides lower thermal impedance. Another important observation is that the temperature difference between the stator yoke and the cooling jacket has been reduced by ~50% compared to the first machine indicating a substantial reduction in the thermal contact resistance between the cooling jacket and the stator OD. This indicates that the steps illustrated in Fig.9 are effective.

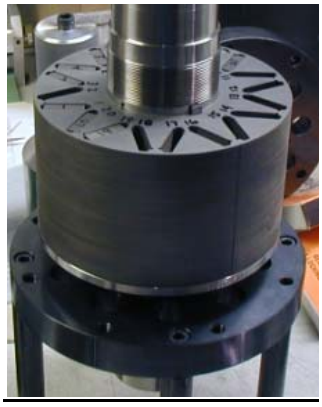

Fig. 10. Rotor of the second proof-of-principle machine

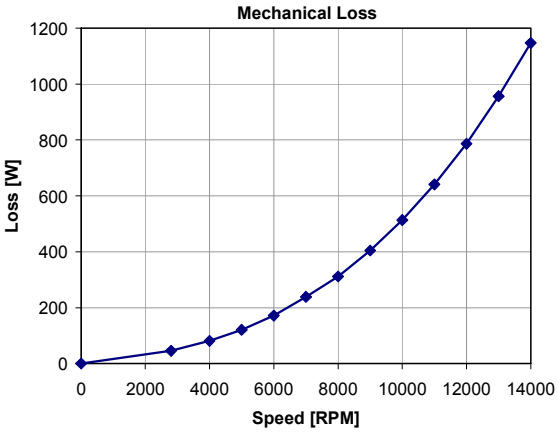

Fig.11. Mechanical loss test result of the second PoP machine with unmagnetized magnets

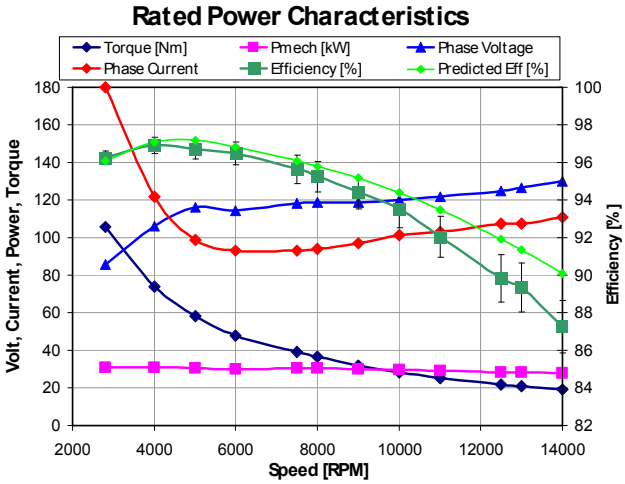

Fig. 12. Second proof-of-principle machine measured performance at rated power

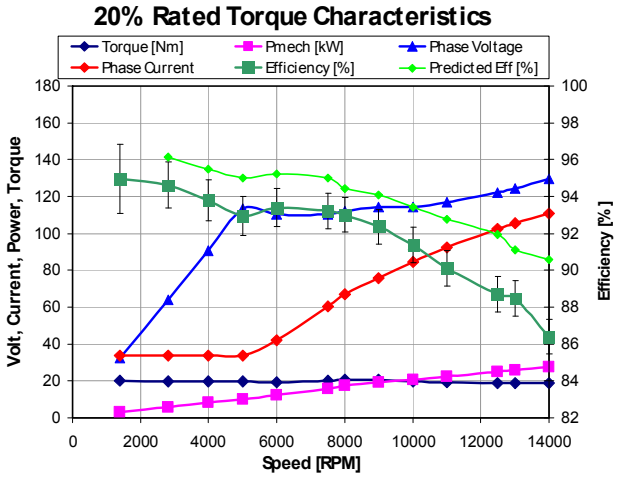

Fig. 13. Second roof-of-principle machine measured performance at 20% rated torque

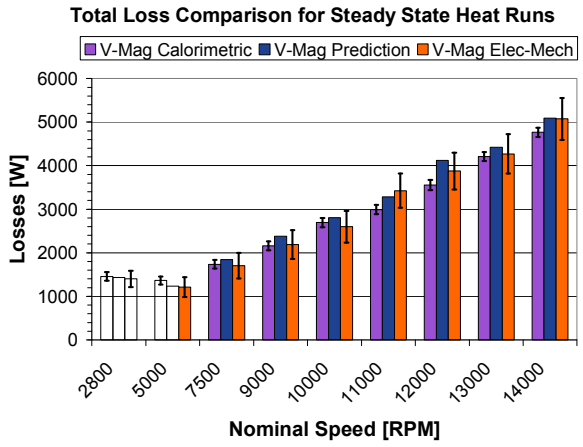

Fig. 14. Second proof-of-principle machine measured (electrical and calorimetric) vs. predicted losses at rated power

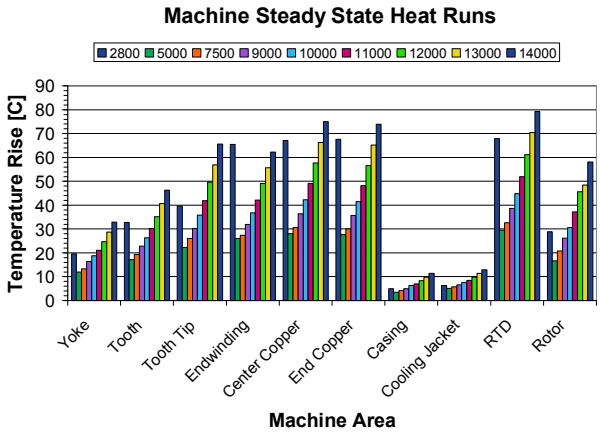

Fig. 15. Second proof-of-principle machine heat runs temperature rises in the various machine components at various speeds.

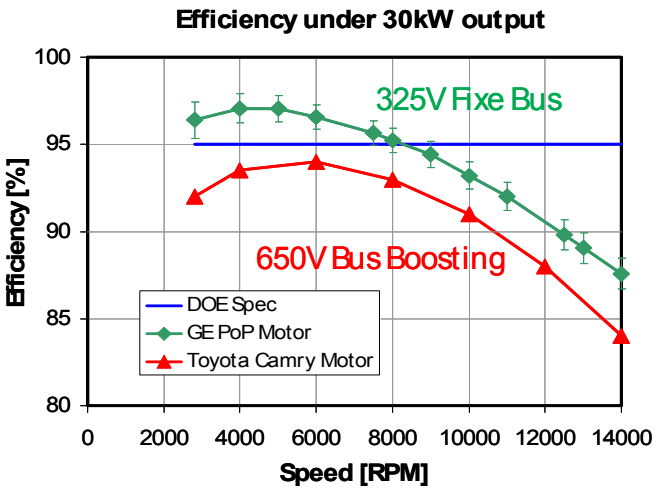

Fig.16. Comparison of efficiency

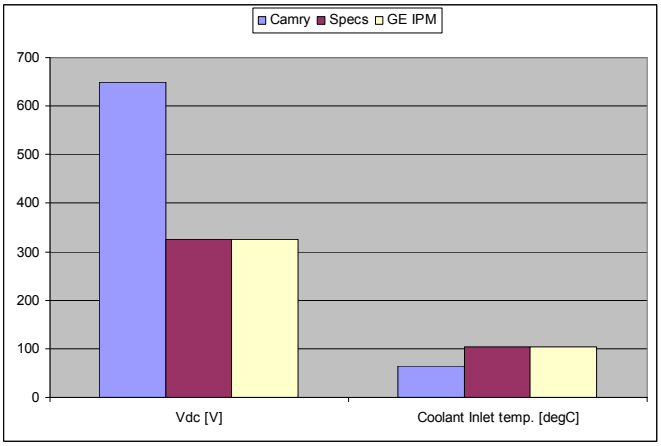

Fig.17. Comparisons of DC bus voltage and coolant inlet temperature

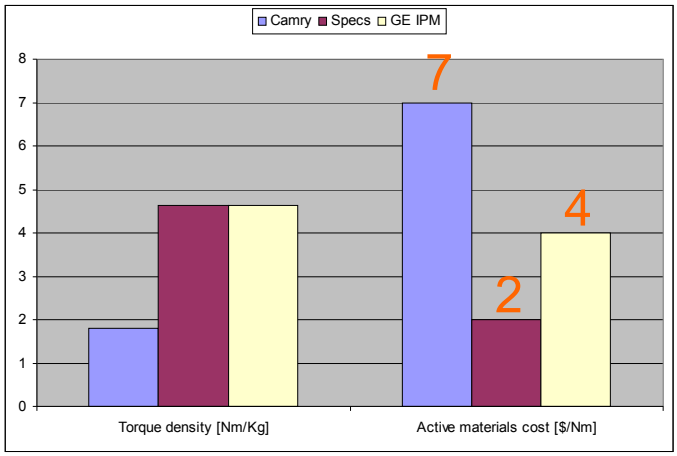

Fig.18. Comparisons of torque density and active material cost

Both machines have comparable efficiency. Even though the 95% efficiency target can be met only up to ~9,000 rpm, the efficiency at the maximum speed is significantly higher than the state of the art. Also, even though the machines have lower DC bus voltage and higher coolant inlet temperature, the first PoP machine has significantly higher continuous torque density (based on active mass) compared to the state of the art. Additionally, even though the cost cannot be met currently, the active material cost is significantly lower compared to the state of the art.

Table I summarizes the comparison of the required set of specifications vs. the performance of the two PoP machines. In addition, Figs 16 to 18 show comparison of the first PoP to the specifications and to the state of the art. It can be seen that the first PoP GE machine has higher power density (higher output power and lower mass).

BLE I
COMPARIOSN OF SPECS VS PERFORMANCE

Requirement	Target	Units	PoP1	PoP2
Minimum top speed	14000	RPM	14000	14000
Peak power output at 20% of maximum speed for 18 seconds and nominal voltage	55 @ 325 Vdc	kW	60	55
Continuous power output at 20 to 100% of maximum speed and nominal voltage	**30 @ 325 Vdc**	**kW**	33	30
Weight	<= 35	kg	<= 35 (22 Active)	>35 (27 Active)
Volume	<= 9.7	liters	<= 9.7	>9.7
Operating voltage (Vdc)	200 to 450	Vdc	200 to 450	200 to 450
Nominal Operating voltage (Vdc-n)	325	Vdc	325	325
Maximum per phase current at motor	400	Arms	400	400
Characteristic current	< Max current	Arms	< Max current	< Max current
Efficiency at 10 to 100% of maximum speed for 20% of rated torque	> 95	%	Refer to figs	Refer to figs
Back EMF at 100% of maximum speed, peak line-line voltage	< 600	Vdc	845	673
Torque pulsations - not to exceed at any speed, Percent of peak torque	< 5	%	< 5	< 5
Ambient (outside housing) operating temperature	-40 to 140	Deg C	-40 to 140	-40 to 140
Coolant inlet temperature	105	Deg C	Rotor up to 9000 rpm Satator up to 7500 rpm	Rotor and stator up to 9000 rpm
Maximum coolant flow rate	10	liters/min	10	10
Maximum coolant pressure drop	2	psi	2	2
Maximum coolant inlet pressure	20	psi	20	20

(B) Materials Development

High resistivity magnet microstructure

Multiphase layered composite permanent magnets have been developed that display an effective resistivity 3X that of sintered NdFeB (the resistivity of sintered NdFeB is 150 μΩ-cm). Magnet loss reduction is achieved by the insulating phase in the composite impeding the flow of eddy currents in the magnet structure. The insulating phase is introduced into the composite structure by co-sintering with NdFeB magnet powder, enabling a manufacturing cost reduction by avoiding the need for machining and assembling segmented permanent magnets. Fig. 19 shows the results of motor simulations that reveal that that the insulating phase must have an electrical resistivity of at 2000X that of the NdFeB magnet material to achieve a loss reduction similar to that achieved with mechanically segmented and reassembled magnets. Most oxide and fluoride compounds meet this requirement, providing a wide variety of candidate insulating phase compositions.

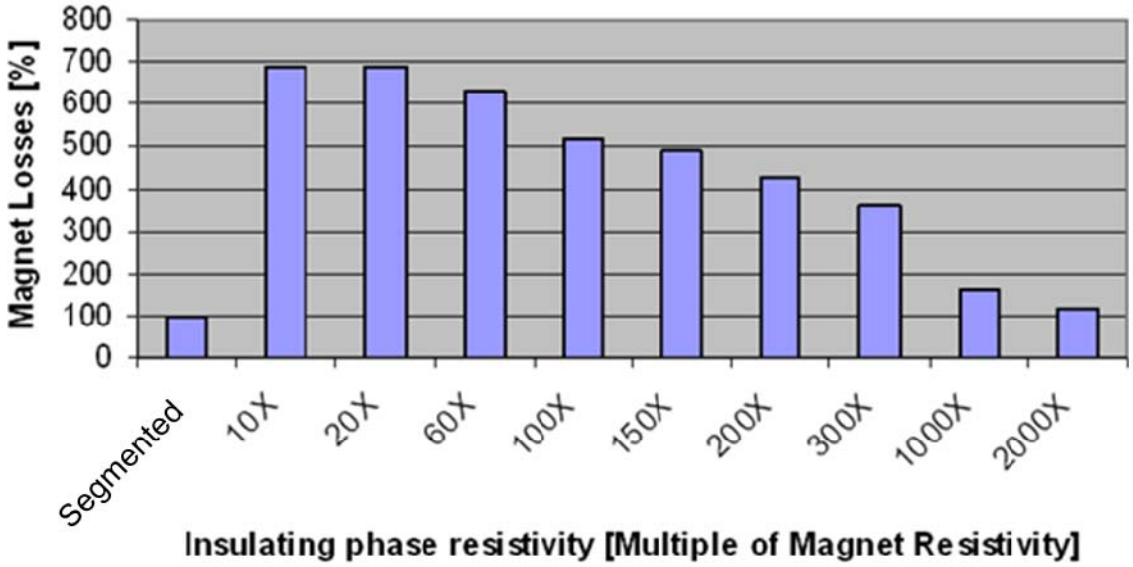

Fig. 19. Effect of insulating phase resistivity on magnet losses. An insulating phase with a resistivity with a resistivity of at least 2000X that of the resistivity of NdFeB is needed to approach the low magnet loss of mechanically segmented magnets.

Magnet powder production

A baseline composition of $Nd_{15}Fe_{77}B_8$ (atomic %) was chosen as the magnet powder for developing the high resistivity magnet compositions. This composition is well known and is in the public domain (Harris et al, 1985). Its physical properties and processing behavior are similar to high performance NdFeB compositions that are proprietary to permanent magnet producers. Pilot production of this material was performed in the materials production facility at GE Global Research. Approximately 500 gram ingots of the $Nd_{15}Fe_{77}B_8$ were prepared by vacuum induction melting of raw materials following by casting into split copper molds. Following a homogenization heat treatment, the ingots were loaded into a hydrogen pressure cell. Hydrogen is absorbed by the $Nd_{15}Fe_{77}B_8$ and the associated volume change causes the ingots to decrepitate into a coarse powder. The powder was dehydrided under vacuum to recover the $Nd_2Fe_{14}B$ phase.

Fine milling of the $Nd_{15}Fe_{77}B_8$ powder was achieved by planetery milling under Argon. The planetary milling was performed using steel media in steel milling container for a milling time of 24 hours. This was done for a total of 24 h. Milled material was unloaded in the glovebox and sieved through a 200 mesh

brass sieve before being stored in an HDPE plastic bottle. The planetary milling process achieved the 3-5 µm particle size needed for sinter processing.

Plasma emission spectroscopy analysis of two samples of the planetary milled fine NdFeB powder indicated compositions of 14.5 mol% Nd, 76.6 mol% Fe, and 8.9 mol% B and 14.1 mol% Nd, 78.1 mol% Fe, and 7.8 mol% B. Whether this variation is batch-to-batch or measurement-to-measurement is not known. Typical oxygen contents measured by inert gas fusion on planetary milled powders were in the range of 0.2 to 0.3 weight%. The maximum desirable oxygen content for sinterability is 0.4%. Fig. 20 is an image of the finely milled $Nd_{15}Fe_{77}B_8$ powder.

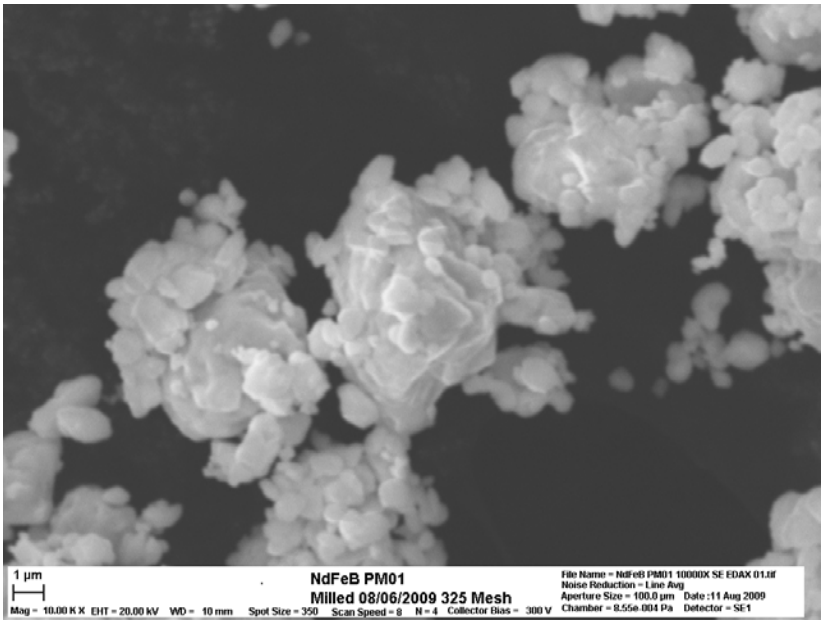

Fig. 20. Scanning Electron Microscopy image of hydrided and planetary milled $Nd_{15}Fe_{77}B_8$ powder produced at GE Global Research. Average particle size is 3 to 5 µm, with some finer particles agglomerated to larger particles.

Thermogravimetric analysis (TGA) of the $Nd_{15}Fe_{77}B_8$ powder was performed under gettered argon at a heating rate of 10°C/min and the results are shown in Fig. 21. Mass changes during heating appear to be less than 0.25 wt% indicating complete desorption of hydrogen as well as minimal oxidation. Differential scanning calorimetry (DSC) shown in Fig. 22 show that a liquid phase forms above 664°C, in close agreement with the 665°C according to the phase diagram of Sagawa, et al. (1987). This liquid is a low melting point, Nd-rich minority phase that is needed to achieve full densification during sintering. According to the same phase diagram in Sagawa's paper, the rate at which the fraction of liquid phase increases as temperature increases goes up significantly above ~1040°C, forming the lower specification limit for the sintering temperature for this material.

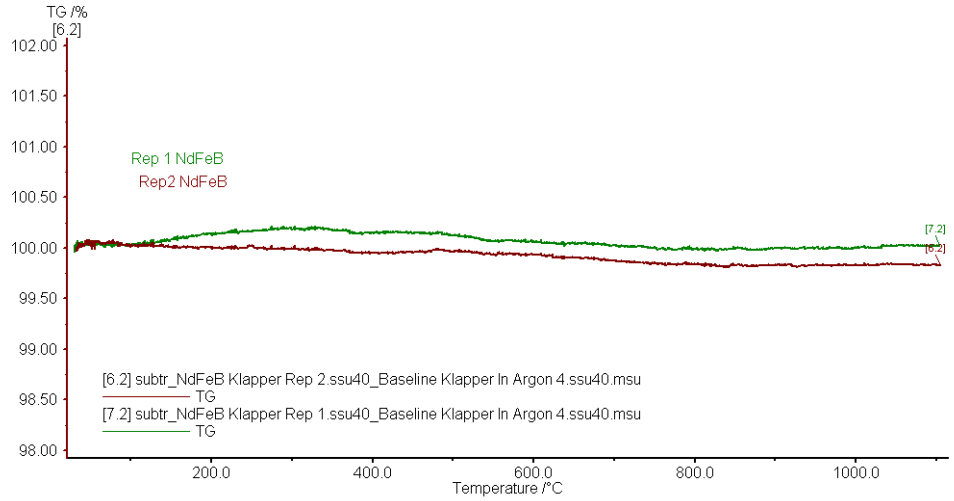

Fig. 21. Thermogravimetric analysis (TGA) on $Nd_{15}Fe_{77}B_8$ powder heated at 10 °C/min under gettered Argon.

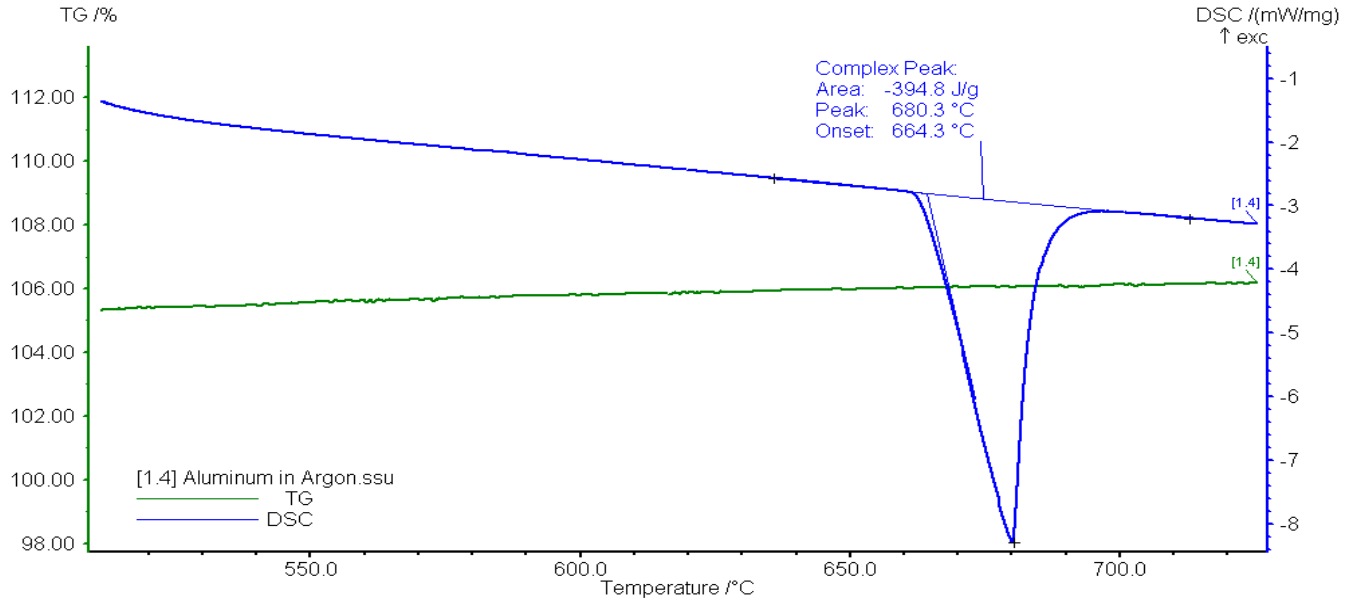

Fig. 22. Differential scanning calorimetry (DSC) of Nd15Fe77B8 powder under gettered argon at 10 °C/min. The onset of melting of the Nd-rich minority is observed at 664.3 °C, close to the published values. Melting of this phase is required to achieve full densification during sintering.

Insulating phase development

Screening of candidate compositions for the insulating phase considers several factors, including:

1) Electrical resistivity of at least 2000 times that of NdFeB
2) Raw material cost comparable to NdFeB
3) Densification rate during sintering matched to NdFeB
4) Not infiltrated/completely de-oxidized through reaction with NdFeB
5) CTE match with NdFeB when cooling from the sintering process

These criteria enabled the selection of a set of insulating phase mixtures whose sintering behavior could be tuned to match that of NdFeB. The densification behavior was systematically explored using dilatometry and sintering trials. The electrical behavior was verified using four point probe resistance measurements and the microstructure was probed with scanning electron microscopy.

Initial sintering trials of the multiphase insulating/magnet structure showed good bonding at low magnification, but cracks along the phase interfaces are evident at higher magnifications. The insulating phase did not densify as much as the NdFeB, leading to bulging near the edges of the part, and residual porosity in the NdFeB material closest to the phase interfaces, where the NdFeB would have been pulled into tension during sintering.

Further refinement of the insulating phase composition was observed to have result in densification behavior that was better matched to the NdFeB composition. A complete match has not yet been found, as there are still some vertical cracks evident in the microstructure. Fig. 23. Shows a macro image of a pressed and sintered composite magnet made using this composition, demonstrating the improved densification behavior.

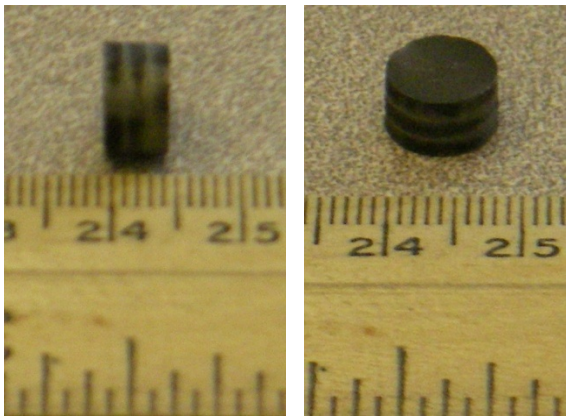

Fig.23. Optical image of a 3/8" multilayer pressed and sintered NdFeB magnet with three magnet layers (dark contrast) and two insulating layers (light contrast)

Sintering experiments are continuing to improve the sintering behavior of the high resistivity permanent magnets as well as to find insulating materials with the lowest possible raw material costs. Experiments to scale up the processing of the multilayers to kilogram scale will be conducted at a domestic permanent magnet producer in the first half of 2011.

Materials selection study

A review of the machine design developed in Phase I identified four rotor components whose performance is limited by mechanical, magnetic, or physical properties such as thermal conductivity. The Ashby material selection method (Ashby, 1999). The method identifies key engineering properties; their specification limits, and develops appropriate metrics that quantify the trade-offs between them. These metrics are then applied to a database of materials properties to provide candidate materials. These candidates are compared to existing selections and evaluated in terms of cost, manufacturability, and impact on system performance.

The three components that were identified for the study were selection analyses of the magnet-retaining elements, the rotor shaft material, and the rotor laminates have been completed. For the magnet-retaining elements, an alternative material has been identified. The alternative has better mechanical strength and

creep performance at maximum operating temperature than the original selection, and also has comparable electrical and magnetic properties and comparable cost to the original selection. For the rotor shaft, an alternative material with improved thermal conductivity and lower-cost fabricability, and comparable strength and creep resistance, to the original selection has been identified. The original material selection for the rotor laminates has been retained, while the properties of an alternative material are being studied for longer-term applications.

Conclusion

(A) Motor Development

- Significant progress made since last year
- Two advanced proof-of-principle machines were built. Both were fully tested
- Major risks including spinning the novel rotor concept at 14000 rpm have been retired
- Test results closely match predictions. This provides confidence in design process
- Torque and power density requirements are met
- Efficiency requirements are met up to 9000 rpm. Achieved efficiency values at higher speeds exceed the state of the art.
- Alternate rotor materials identified to enhance thermal management and efficiency capabilities of the final 30kW/55kWpk machine
- 12 US patent applications filed to date

(B) Materials Development

- A multiphase permanent magnet microstructure has been developed that exhibits high effective resistivity by component magnetic and insulating phases in a multilayer geometry.
- Insulating phases with densification behaviors approaching that of NdFeB have been identified and laboratory scale multilayer magnets have been produced/
- Kilogram scale production of NdFeB powder has been achieved to support scaled magnet synthesis at a domestic permanent magnet producer
- Work is underway to improve the match of the densification behavior of the insulation phase with the permanent magnet phase, identify lowest raw material cost insulation material, and to achieve kilogram scale production of high resistivity NdFeB magnet at a domestic permanent magnet producer.

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4. Systems Research and Technology Development

4.1 Benchmarking Competitive Technologies

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Objectives

- Provide status of nondomestic hybrid electric vehicle (HEV) technologies through assessment of design, packaging, fabrication, and performance during comprehensive evaluations.
  - Compare results with other HEV technologies.
  - Distribute findings in open literature.
- Support FreedomCAR program planning and assist in guiding research efforts.
  - Confirm validity of the program technology targets.
  - Provide insight for program direction.
- Produce a technical basis that aids in modeling/designing.
- Foster collaborations with the Electrical and Electronics Technical Team (EETT) and Vehicle Systems Analysis Technical Team (VSATT) on benchmarking activities.

Approach

- Choose vehicle subsystem.
  - Evaluate potential benchmarking value of various HEVs.
  - Consult with original equipment manufacturers (OEMs) as to which systems are most beneficial.
- Tear down power converter unit (PCU) and electronically controlled continuously variable transmission (ECVT).
  - Determine volume, weight, specific power, and power density.
  - Assess design and packaging improvements.
  - Conduct tests on magnets and capacitors.
- Prepare components for experimental evaluation.
  - Develop interface and control algorithm.
  - Design and fabricate hardware necessary to conduct tests.
  - Instrument subsystems with measurement devices.
- Evaluate hybrid subsystems.
  - Determine peak and continuous operation capabilities.
  - Evaluate efficiencies of subsystems.
  - Analyze thermal data to determine assorted characteristics.

Major Accomplishments

- Selected the 2010 Toyota Prius for evaluation based on anticipated automotive manufacturer interest in the system due to the integrated cooling technique used in the PCU.
- Conducted design/packing studies of the 2010 Prius PCU and ECVT and determined various improvements and tradeoffs when compared to the 2004 Prius and Camry hybrid designs.
- Bypassed the 2010 Prius PCU motor inverter controls to allow full control over testing conditions.
- Mounted intensive efforts to disassemble and evaluate key components within the PCU/ECVT.
- Assessed mass, volume, power density, and specific power of various PCU/ECVT components.
- Evaluated efficiency, performance, and continuous capabilities of the 2010 Prius subsystems.
- Communicated effectively with EETT and VSATT to develop project direction and test plan and convey test results.

Future Direction

- Focus benchmarking efforts on technologies of interest to DOE, EETT, and VSATT.
- Adopt approaches similar to those of previous benchmarking studies while working to meet the universal need for standardized testing conditions.

Technical Discussion

Much like the 2007 Camry and 2008 Lexus LS 600h PCU designs, the size and proportions of the 2010 Prius PCU, shown in Fig. 1, are similar to those of a conventional 12 Vdc car battery. The 2010 Prius PCU weighs 13.0 kg versus about 17.4 kg and 17.9 kg for the 2007 Camry and 2008 LS 600h PCUs, respectively. A reduction of mass is expected when considering the lower power rating of the 2010 Prius. Another explanation for the reduction in mass is that the 2010 Prius uses a lightweight aluminum cooling infrastructure, whereas the 2004 Prius and 2007 Camry designs use a cast aluminum heat exchanger. Interestingly, the 2010 Prius PCU volume of 16.2 L is significantly greater than that of the 11.7 L and 13.7 L volumes of the Camry and LS 600h PCUs.

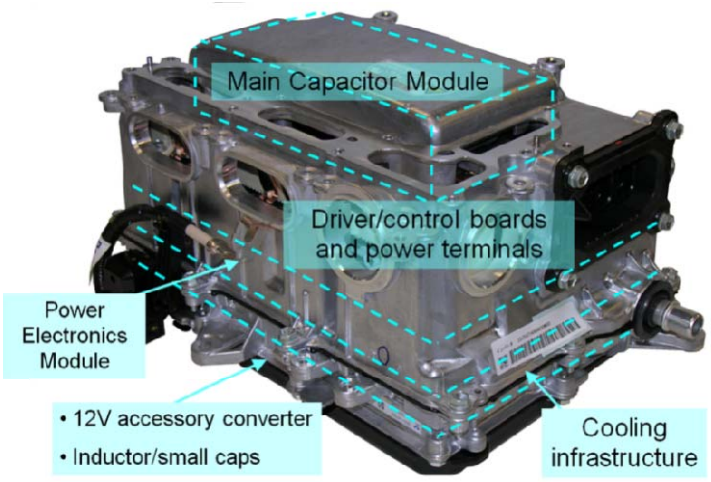


Fig. 1. Compartments of the 2010 Prius inverter and converter assembly.

It should be noted that both second and third generation Prius PCUs include a 202 V to 12 V direct current-direct current (dc-dc) converter for the accessory voltage supply, replacing the alternator. Connector terminals are connected to the 202 V battery supply, and additional connector terminals provide a fused link from the 202 V battery supply for the external inverter which drives the air conditioning (A/C) compressor. This small, three-phase inverter for the compressor is located within the

2004 Prius PCU. One coolant port is located below the interface to the vehicle electronic control unit (ECU) and the other coolant port is located on the opposite end of the PCU. The ethylene-glycol and water mixture flows from the PCU output port through a heat exchanger on the ECVT and subsequently to a radiator which is separate from the high temperature internal combustion engine (ICE) coolant radiator. Motor and generator interconnections differ significantly: in the Camry design only three bolts secure the cable harness to the PCU whereas the 2010 Prius and LS 600h designs include bolts which secure the cables directly to terminals in addition to the mechanical support from cable harness bolts.

Within the 2010 Prius PCU are components associated with a bidirectional dc-dc converter, motor inverter, and generator inverter; their general locations are shown in Fig. 2. Contrary to the Camry PCU design described in reference [1], but similar to the LS 600h {reference [2]}, the 2010 Prius controller, power supply, and driver electronics for the bidirectional dc-dc converter and inverters are grouped together onto two printed circuit boards located in the uppermost compartment (Fig. 2). The Camry PCU design includes four separate printed circuit boards dedicated to these functions, and the bidirectional dc-dc converter printed circuit boards and power electronics are located in a separate compartment. The main capacitor module shares the uppermost compartment and includes many small capacitors which are combined to serve as two large capacitors, one at battery level and one on the output of the boost converter. Similar to the 2004 Prius, the main capacitor module is a separate unit and is not molded with the housing of the PCU, as are the Camry and LS 600h capacitor modules. Attached to the side of the main capacitor module is a small 54 kΩ ceramic resistor that is connected across the high voltage (HV) dc link capacitor terminals and is located on the side of the PCU. The resistor, sized the same as those in the Camry and LS 600h, functions as a voltage bleed off for the capacitor and may contribute some filtering effects.

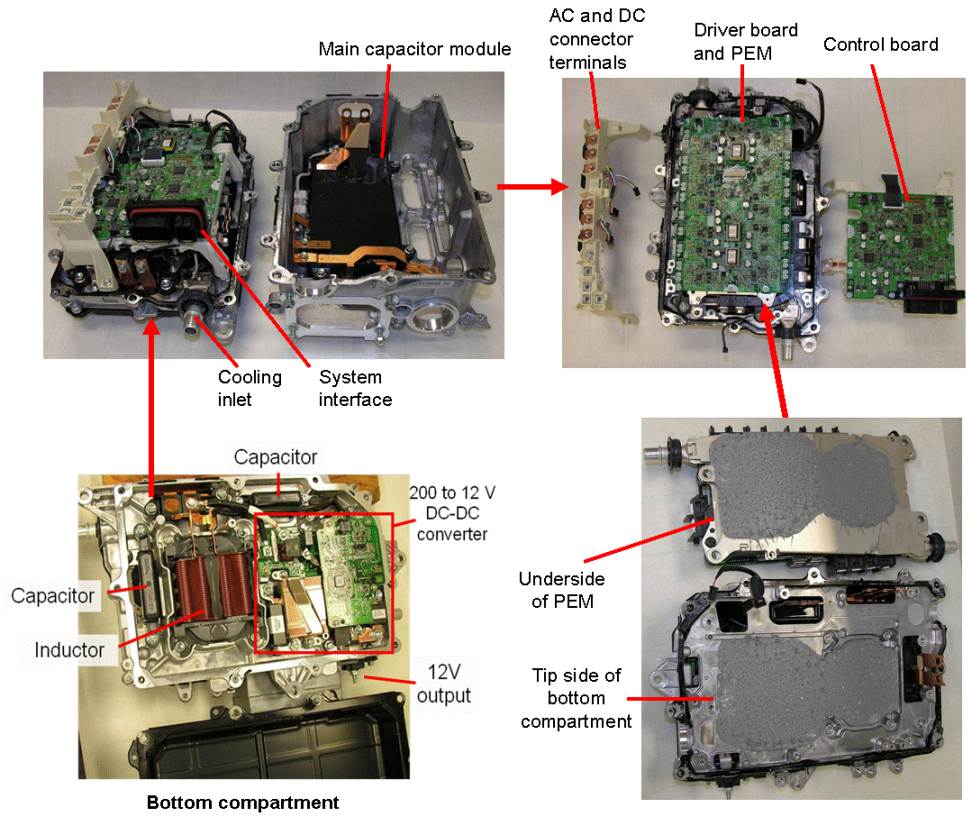


Fig. 2. 2010 Prius PCU teardown.

The 2010 Prius and LS 600h power electronics devices are located in the compartment below the controller and driver electronics, and the bidirectional dc-dc converter power electronics are grouped together with the inverter power electronics. While the power electronics module (PEM) and cooling infrastructure are one unit, separate sections are shown in Fig. 2 because the lowermost compartment also uses the heat exchanger. The lowermost compartment houses the 200 V to 12 V dc-dc converter as well as the large inductor and small capacitors associated with the bidirectional dc-dc boost converter which supplies the motor and generator inverters.

Because the nickel-metal hydride battery is rated at 27 kW, it is assumed that the bidirectional dc-dc converter will not operate at power levels exceeding 27 kW. Similarly, it is assumed that the motor inverter has a peak power rating that matches the measured power rating of the motor. A 201.6 Vdc battery supplies power to the PCU, which is connected to the low voltage (LV) side of the boost converter. A 470 V, 315 μF, capacitor is connected across the input with a 225.6 μH inductor between the battery and the boost converter PEM. A small 53.8 kΩ resistor is in parallel with an 860 V, 0.562 μF, capacitor, which is integrated into the main capacitor module. Additionally, separate 900 V, 0.8 μF, and 950 V, 0.562 μF, filter capacitor modules are located in the bottom portion of the PCU, and a 750 V, 888 μF, smoothing capacitor, which is connected to the HV side of the boost converter, is a part of this parallel configuration. This HV bus serves as the dc link for the motor and generator inverters. The boosted voltage ranges from 202–650 Vdc depending on driving conditions such as desired acceleration and required regenerative braking and is controlled accordingly by commands from the motor-generator (MG) ECU and the vehicle ECU.

Power Converter Unit Teardown

Figure 2 shows the 2010 Prius PCU with the upper half of the housing removed and placed beside it. Eleven bolts hold the assembly together with a compound similar to room temperature vulcanizing silicone applied to the mating surfaces to seal the unit. The main capacitor module is secured in the housing with four bolts, and the small white ceramic resistor is fastened to the side of the module. The copper bus bars (near the bottom-right side of Fig. 2) connect directly to the hybrid battery supply. The common bus bar immediately enters the capacitor module while the positive input traverses the width of the PCU and then enters the capacitor module and is also connected to the inductor in the bottom compartment by means of long vertical bus bars.

The control/interface circuit board and the dc input, dc output, motor, and generator connection terminals were removed, as shown in the upper left portion of Fig. 2. This circuit board, shown on the right in Fig. 2, is multilayered and includes power regulation electronics; two identical MG microprocessors; a boost-converter microprocessor; two Tamagawa AU2802 integrated circuits for MG speed/position detection; and hardware for vehicle communication, MG current measurement, safety interlock devices, and temperature feedback. The design of this circuit board is very similar to that of the 2007 Camry. The circuit board seen in the middle portion of Fig. 2 is the driver/power supply board, and it is also similar to that of the Camry. The driver board includes regulated isolation power supplies; isolated driver electronics; hardware to prevent faults and overlapping; and voltage, current, and temperature sensing circuitry for each insulated gate bipolar transistor (IGBT). There are 22 groups of five pins for driving and sensing purposes for each IGBT.

The ac and dc connector terminals are visible in Fig. 2. As copper bus bars extend from the motor and generator inverter outputs, two of the three phases pass through black current transducers before reaching the connection terminals at the top of the assembly. Two interlock devices are located on the connection terminal assembly to disable the system if the terminal cover or battery connector is removed. In the lower right portion of Fig. 2, the PEM with integrated cooling has been removed and placed beside the bottom compartment. Input and output ports for the cooling system have rubber seals to prevent moisture

from entering into the interior of the PCU assembly. A significant amount of gray thermal grease is used between the bottom side of the cooling structure and the bottom compartment. Four small, cylindrically shaped pieces are associated with the four bolts that are used to mount the large inductor in the bottom compartment. The footprint of the 200 V to 12 V dc-dc converter is larger than the inductor footprint, and more thermal grease is used in this area of the mating surface. Two separate capacitor modules (900 V, 0.8 μF, and 950V, 0.562 μF) have two copper bus bars which extend vertically from the bottom compartment. The bus bars are substantially thick (probably to reduce inductance and resistance) and bolt directly to the PEM. Three copper bus bars are grouped together, two of which are for each terminal of the inductor. The other bus bar provides a common for the 200 V to 12 V dc-dc converter, and the positive supply for this converter is connected to the input terminal of the inductor, which is visible in the lower left portion of Fig. 2. The location of the two capacitors is indicated, and the top of the inductor is also visible in this image. In all of the previous PCU designs, the inductor is completely enclosed with potting compound, with no copper visible. The output of the inductor is connected to the middle point of the dc-dc converter leg and the leg is in parallel with the motor and generator inverter legs, thereby connecting directly to the dc link. Circuitry for the 12 V converter is also indicated in this image.

Mass and volume measurements were made for the 2010 Prius motor inverter, dc-dc converter, and their subcomponents; however, for certain components the dimensions and volumes are approximate as the geometries are sometimes irregular. Many of the components of the PCU are shared between the inverters and dc-dc converter. Thus, the mass and volume of these items were tallied separately and then divided accordingly. As explained in more detail in publication [1], based on device count about 55% of the power electronics are dedicated to the motor inverter, 27% to the generator inverter, and 18% to the dc-dc converter. Because the devices in the bidirectional dc-dc (boost) converter are larger, the percentage of PEM area devoted to each component is about 49%, 29%, and 22% for the motor inverter, generator inverter, and dc-dc converter, respectively. It is therefore reasonable to distribute the mass and volumes of the shared items across the motor inverter, generator inverter, and dc-dc converter according to the percentages 50%, 30%, and 20%, respectively. For example, about 50% of the driver board is dedicated to the motor inverter because about 50% of the IGBTs are included in the motor inverter. Likewise, 20% of the mass and volume of the shared items is attributed to the dc-dc converter. The large capacitor module is the largest and heaviest PCU component.

The peak density and peak specific power of both the motor inverter and the bidirectional dc-dc converter were calculated to be 11.1 kW/L and 16.6 kW/kg and 5.7 kW/L and 5.3 kW/kg, respectively. Because the mass of the 2010 Prius PCU is much lower than that of the other systems, the inverter specific power is significantly higher than that of the Camry, and especially the 2004 Prius. Even so, the specific power calculation seemed quite large upon initial inspection. However, considering that about 2 kg is devoted to the accessory converter, the mass of the inverters and boost converter sum up to only 11 kg. The LS 600h has the highest power density since the power capability of the LS 600h motor inverter is much higher than that of the other systems while their sizes are relatively similar. Because the 2010 Prius PCU volume is reasonably high, the inverter power density is lower than that of the LS 600h and Camry. Although the power capability of the 2010 Prius bidirectional dc-dc converter increased by about 35% in comparison with the 2004 Prius, the mass only increased by about 6% and the volume decreased by about 6%. Thus, there was an improvement of the specific power and peak density of the boost converter, but not as significant as that of the motor inverter.

The main capacitor of the 2010 Prius PCU is shown in the upper left portion of Fig. 2. The 2010 Prius and LS 600h capacitor modules contain both capacitors, which are connected to the HV and LV side of the bidirectional boost converter, whereas the corresponding Camry capacitors are housed in separate modules. The main capacitor was x-rayed to determine capacitor characteristics. The x-ray shows that there are three discrete submodules in parallel that form the 888 μF capacitor, with each submodule having a capacitance of 296 μF. The equivalent Camry and 2004 Prius capacitor has 12–87 μF and 8–

142 µF submodules in parallel to provide a total capacitance of 2,098 µF and 1,130 µF, respectively. The x-ray also shows that there are two 157.5 µF submodules which are in parallel and form the 315 µF battery level filter capacitor. The cells which form these capacitors span the entire width of the module, whereas the Camry and 2004 Prius capacitors are much smaller and only span half of the module's width. The LS 600h cells are also small, yet they are vertically oriented. The fuse for the 202 V supply to the A/C compressor is secured to the side of the capacitor module. The small 0.562 µF capacitor is on the opposite end of the module.

A primary function of these capacitors is to attenuate voltage transients and surges which are associated with the buildup and collapse of the energy stored in the 329 µH inductor (shown in Fig. 2). The lower switch (three IGBTs in parallel) of the dc-dc converter cycles at 5 or 10 kHz with a variable duty cycle to build up and store energy in the inductor. As the duty cycle is varied, the output voltage of the inductor also varies accordingly. Because of the inherent voltage ripple and potentially high voltage produced by the collapsing inductor field, these capacitors serve to stabilize the battery voltage and dc link voltage and protect the power electronics devices from potential overvoltage conditions. The inductor has two coils in series, and the core was secured with bolts and immersed in a potting compound.

A total of 22 IGBTs and antiparallel diodes are located in the PCU, all sharing the same dc link. As indicated in Fig. 3, the motor, generator, and bidirectional boost converter power electronics are combined into one package. All the upper devices are displayed in the lower half of the image, and likewise, all of the lower devices are seen in the upper half of Fig. 3. The motor inverter comprises 4 IGBTs and diodes in each phase, with 12 IGBTs and 12 diodes in its entirety. The generator has only two IGBTs and diodes for each phase, with a total of six IGBTs and diodes. While the boost converter devices only total up to four IGBTs and diodes, they are much larger than those of the motor and generator inverters. Coolant hose connections are located on each end of the heat exchanger, allowing coolant to enter one side and absorb heat as it traverses across the width of the PEM and exits the other port. As seen in Fig. 4, the cooling infrastructure runs beneath the drive and sense pins of the IGBTs, thereby facilitating flow along the length of the PEM before passing through the thin cooling channels. This promotes more uniform heat transfer among the power electronics devices. A thermistor is located on the coolant inlet just inside the PCU. Although the thermistor is secured to the coolant inlet, the actual sensing device is not flush with the aluminum surface of the inlet.

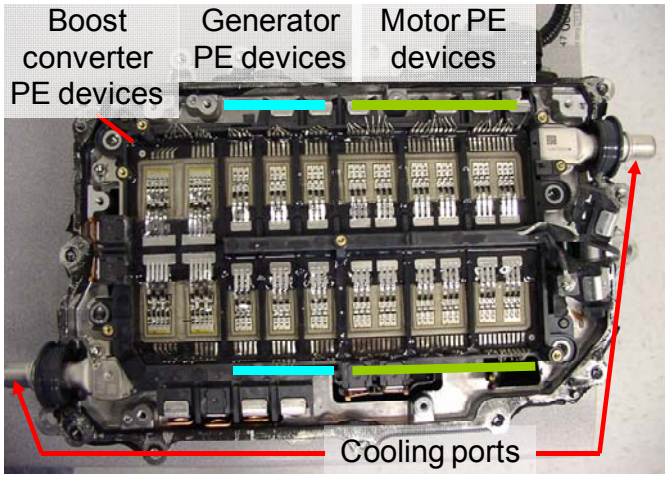


Fig. 3. 2010 Prius PEM.

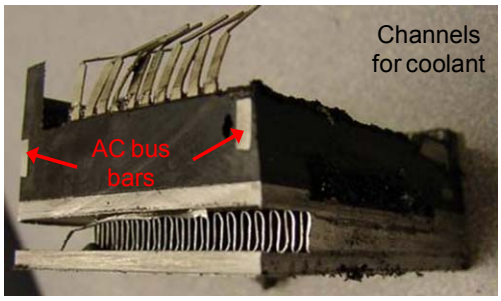


Fig. 4. Cross section of 2010 PEM.

One of the most noticeable discrepancies between the 2010 Prius PEM and previous PEM designs is the orientation of the power electronics devices. In the 2010 Prius, the power electronics devices are oriented in a manner such that the drive and sense pins are on the outer perimeter of the module. While this likely presents opportunities to improve the layout of the driver circuitry, it more importantly allows more phase legs to be placed along the length of the dc bus bar. The Camry and 2004 Prius designs have the motor and generator inverters on opposite sides of the dc bus, with the three-phase outputs also on opposite sides and on the outer periphery of the PEM. By contrast, the upper and lower IGBTs of each inverter are on opposite sides of the dc bus in the 2010 Prius. The black dividers between each phase are thicker on the top than on the bottom portion in the 2010 Prius PEM (Fig. 3). This is because the alternating current (ac) bus bars (indicated in Fig. 4) are molded in this black material and are fed to the two three-phase terminal outputs on the side of the PEM.

To help portray the layout, it is advantageous to trace the path from the positive dc link through one phase leg to the negative dc link. There are two layers of ribbon bonds on each side of the dc link; three on the top layer and three on the bottom layer, which is slightly visible in Fig. 5. The bidirectional boost converter uses five ribbon bonds per device. There are also several layers of bus bars for the dc link and ac outputs, extending completely through the middle of the PEM, a few of which are visible in the left side of the cross section in Fig. 5. In Fig. 5, the bottom bus bar on the right side of this group of bus bars in the middle is the positive dc link, which is connected with the three lower ribbon bonds to the collectors of the upper phase legs (all on the right). If the IGBT is activated, current flows out the emitter through the three upper ribbon bonds to the upper bus bar. The collector of the lower IGBT (shown in Fig. 3) is connected by three lower ribbon bonds to this horizontally oriented bus bar, as is the ac output bus bar, which is vertically oriented and placed between each phase. If the lower IGBT is activated, current passes through the IGBT and out the emitter to the three upper layer ribbon bonds which attach to the negative dc link.

The 2010 Prius layout appears to be more orderly and is advantageous in ways such as fewer attachment points and shorter overall conductor length, perhaps improving the parasitic parameters of the devices in addition to the improved parasitic parameters of ribbon bonds versus wire bonds. While there are some inherent benefits to this packaging approach, there are also some negative aspects. For example, the 2007 Camry PEM contains six IGBTs and diodes for each phase leg of the motor inverter (versus four for the 2010 Prius). In the Camry PEM described in reference [1], a third IGBT is located beneath the dc link bus bars in the middle. An interesting comparison could be made if three more phase legs were added (one for each phase) to the 2010 Prius motor inverter to make an even comparison with the Camry PEM. It seems to be that the 2010 Prius packaging approach requires parallel IGBTs to be placed along the length of the dc link. This is one particularly attractive aspect of the LS 600h design, which consists of vertically oriented PEMs. Nonetheless, the 2010 Prius PEM sufficiently includes the bidirectional boost converter, as opposed to having separate modules such as those of the Camry and 2004 Prius.

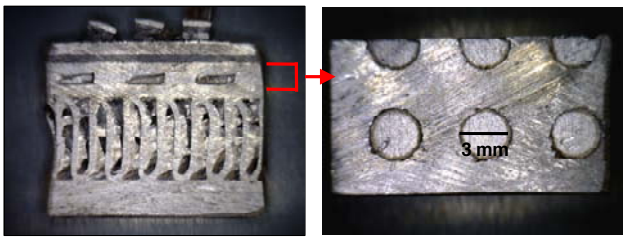
Fig. 5. Cross-section of boost converter modules 2010 Prius.

External dimensions of the 2010 Prius, 2007 Camry, 2008 LS 600h, and 2004 Prius power electronics devices were measured for comparison. The size and appearance of the LS 600h IGBTs and diodes are similar to those of the bidirectional dc-dc converter of the Camry. The square area of silicon (Si) for each IGBT has decreased from 131.9 mm^2 to 109.4 mm^2, and the total square area of Si used on the motor inverter has decreased from 1,583 mm^2 to 1,313 mm^2, a 17% reduction in moving from the 2004 Prius to the 2010 Prius design.

The 2004 Prius IGBT consists of a planar gate structure and includes areas in the drift region below the emitter "n+" and "p" regions which do not pass as much current as the drift region areas below the gate. This inefficiency is due to the shape of the inversion layer which is formed when using a planar gate structure. The Camry, LS 600h, and 2010 Prius IGBTs consist of a trench gate structure which forms a more uniform inversion layer during on-state operation, and therefore higher current densities are created in the drift region. All IGBTs include leads for semiconductor junction temperature measurement feedback, gate voltage control, current measurement, and emitter voltage feedback. These signals are used to control the devices and prevent fault conditions from occurring.

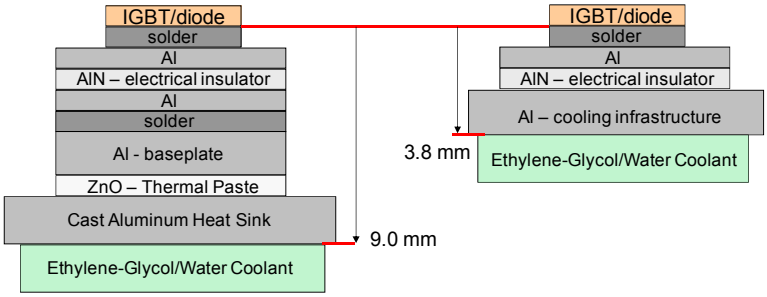
An overall view of the layers within the PEM is given in Fig. 6. Despite the sacrifice of thermal conduction characteristics, numerous 3 mm diameter holes are introduced to alleviate stresses associated with thermal expansion, which are particularly high at the interface of materials with differing coefficients of thermal expansion. Figures 6(a) and 6(b), cross sections through the vertical and horizontal planes of the module, show these perforations (red indicator).

Figure 7 shows a comparison of the thermal conduction paths in the 2004 and 2010 Prius from the power electronics devices to the ethylene-glycol-water coolant. Both systems have the power electronics devices soldered directly to an aluminum substrate and both use aluminum nitride (AlN) ceramic insulators for electrical isolation from the cooling infrastructure. Below the AlN insulators, the 2010 Prius has an aluminum layer which has been brazed to the cooling infrastructure, while the 2004 Prius PEM has an aluminum layer below the insulator that has been soldered to a thick aluminum baseplate, which is bolted to a cast aluminum heat sink with zinc oxide thermal paste between the baseplate and heat sink to fill any voids between the mating surfaces. Ultimately, the length of the conduction path from the bottom of the power electronics devices is 3.8 mm for the 2010 Prius versus 9.0 mm for the 2004 Prius, a 58% decrease in length. Additionally, a solder layer and thermal paste layer have been eliminated, both of which have relatively low thermal conductivities (compared to aluminum), and therefore the overall thermal conductivity has greatly increased.



(a) **(b)**

Fig. 6. Cross-sectional views of extracted 2010 Prius PEM: (a) side; (b) top.



(a) **(b)**

Fig. 7. Comparison of thermal conduction path in 2004 Prius (a) and 2010 Prius (b).

ECVT Teardown

The overall functionality of the 2010 Prius ECVT, shown in Fig. 8, is similar to the Camry and Prius, yet there are significant differences between the subsystem designs. All systems use the sun gear of a planetary gear that is connected to the generator with a hollow rotor shaft, through which a shaft connected to the ICE passes and connects to the planetary carrier. The ring of the planetary gear is connected directly to the motor output in the 2004 Prius and to the motor through a high-speed reduction gear in the 2010 Prius and 2007 Camry. The 2010 Prius, 2004 Prius, and Camry planetary rings drive the differential output through a series of drive gears.

One of the most noticeable differences between the 2010 Prius electric motor (Fig. 9) and previous Toyota designs is the design of the rotor. While the PMs are in a 'V' shaped orientation, the x-ray in Fig. 9(b) indicates the presence of large openings in the rotor laminations. These openings certainly reduce the overall mass of the rotor and may have other design implications such as effecting the reluctance component of the torque, which could be impacted by these large interior air gaps. Additionally, the design may have reduced eddy current losses at the shaft, as the large voids would deter flux transients from occurring in this area. An additional design feature of interest is the small inner diameter of the rotor lamination, and thus the outer diameter of the rotor shaft. Previous designs consist of a rotor shaft with a much larger outer diameter. The outer diameter of the LS 600h motor, 2010 Prius motor, and Camry motor stator laminations are 7.88 in., 10.395 in., and 10.395 in., respectively. Stator lamination stack lengths for the LS 600h, 2010 Prius, and Camry motor are 5.33 in., 2.0 in., and 2.4 in., respectively. As the diameters of the 2010 Prius and Camry motor stators and rotors are identical, the stator core mass per unit stack length (without copper) of the 2010 Prius stator is roughly equal to that of the Camry; 10.36 kg/2 in. = 5.18 kg/inch versus 12.38 kg/2.4 in. = 5.16 kg/inch, respectively. However, the rotor mass per unit length of the 2010 Prius is slightly lower than that of the Camry; 6.7kg/2 in. = 3.35 kg/inch versus 9.03 kg/2.4 in. = 3.76 kg/inch.

Another significant design difference in the ECVT is the generator shown in Fig. 10. While the rotor is similar to previous Toyota designs (note the large inner diameter), the stator is significantly different, with 12 stator teeth versus a typical count of 48 teeth and concentrated windings all encapsulated within a mold. The light grey mold was analyzed for material composition, and it is composed of 58.11% Al, 39.42% O, and 2.47% Na, by mass with fibers that are 49.3% O, 30.1% Si, 12.22% Al, and 8.34% Ca, by mass.

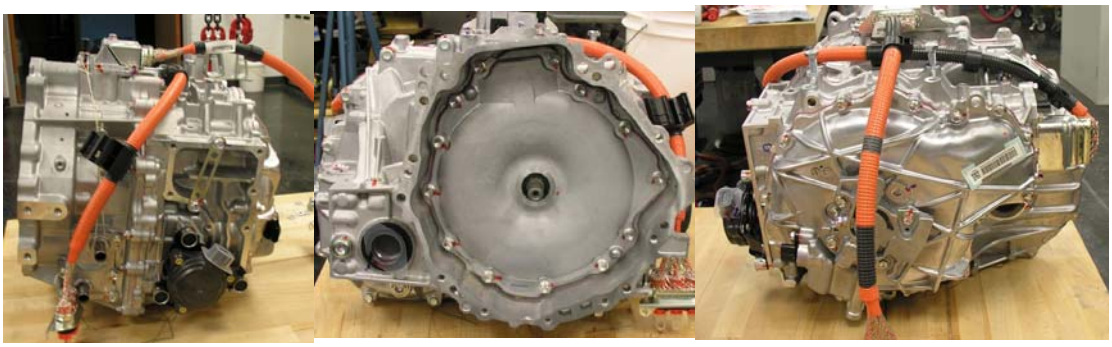
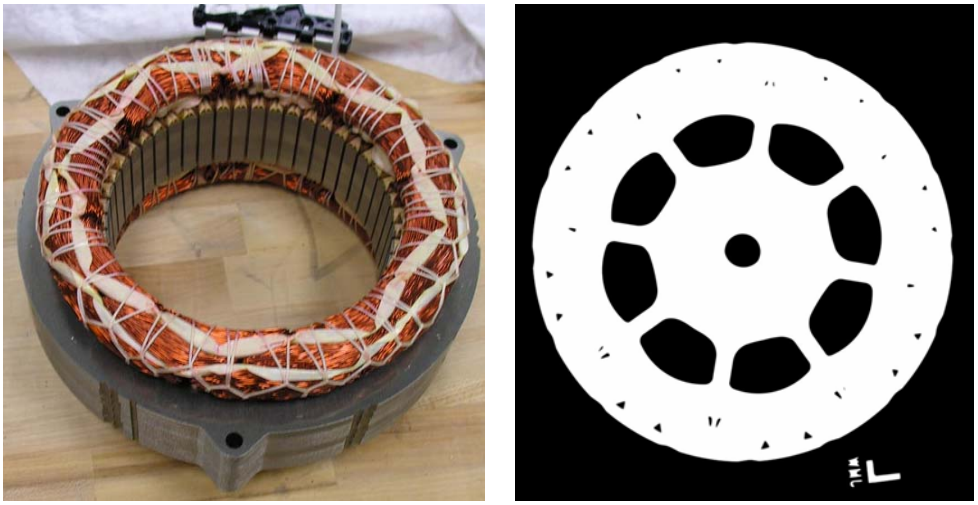


Fig. 8. 2010 Prius ECVT



(a) **(b)**

Fig. 9. 2010 Prius motor stator (a) and x-ray of motor rotor (b).

Fig. 10. 2010 Prius generator.

A comparison of the specific power and power density of four HEV systems, the 2010 Prius, 2004 Prius, 2007 Camry, and Lexus LS 600h, is provided in Table 1. Note that the heat exchanger and speed reducer were accounted for in the motor mass and volume calculations. The results indicate that the peak power density of the 2010 Prius motor has improved over that of the 2004 Prius but is significantly lower than that of the Camry. This is because the motor volume is relatively similar with only a 0.4 in. reduction of stack length, yet the peak power is lower. Mass reductions in the 2010 Prius yield nearly equal specific power numbers in comparison with the Camry motor. The LS 600h has high values of power density and specific power. Peak power capabilities were used in these calculations, and the use of continuous ratings may yield closer results for the motor assessments. However, it is difficult to generalize continuous power ratings as they are based upon a variety of conditions such as coolant temperature, stator temperature limit, and motor speed. Nonetheless, the double-sided cooling technique has an apparent advantage over previous designs.

Table 1. Comparison of Specific Power and Power Densities for Various HEV Components

Component and parameter	2010 Prius (60 Kw)	Lexus LS 600h (110 Kw)	2007 Camry (70 Kw)	2004 Prius (50 Kw)
Motor				
Peak power density (kW/L)	4.8	6.6	5.9	3.3
Peak specific power (kW/kg)	1.6	2.5	1.7	1.11
Inverter (excluding generator inverter and buck/boost converter)				
Peak power density (kW/L)	11.1	17.1	11.7	5.7
Peak specific power (kW/kg)	16.6	14.8	9.3	5.7

Experimental Evaluation

We conducted various evaluations to determine PCU and ECVT operational characteristics such as efficiency, continuous capability, and performance. Initial tests included measurement of back electromotive force voltage, no-load losses, and locked rotor torque. These tests provide parameters and characteristics of the motor which are useful for approximating the capabilities of the motor. Secondary evaluations included efficiency, performance, and continuous analyses upon the subsystems. Before any tests could be conducted, the ECVT had to be modified to provide access to the motor shaft. The only shafts externally accessible are the engine input shaft and the differential output shafts. Although the differential gear is indirectly connected to the motor, power measurements through these gears would not be accurate enough to make precise motor efficiency calculations. A shaft was designed and fabricated to provide external access to the motor rotor. The fabricated shaft was fed directly to a speed and torque transducer. The other side of the torque transducer was coupled to a speed reduction gearbox. The

gearbox is capable of handling speeds up to 18,000 rpm and the dynamometer can operate at power levels of up to 400 hp. All hardware on the high speed portion of the shaft was designed to have face mount couplings, which prevents alignment issues and provides extra safety as the shafts are shorter and aren't exposed.

Extensive efforts were made to ensure that the ECVT modification did not impact cooling or lubrication characteristics by inadvertently hindering or enhancing oil flow. The system depends greatly on proper oil circulation for heat conduction and lubrication. Oil is circulated with a mechanically driven trochoid oil pump and an electrically driven trochoid oil pump. Consideration of proper shaft support was also an important part of the process to ensure that no bearings were overloaded. A heat exchanger located at the side of the ECVT is in series with the inverter. Thermocouples were tactically placed to monitor stator, inner/outer case, and oil temperatures both near and far from the heat exchanger. Additional instrumentation was added to the ECVT and PCU, and a data acquisition system was developed to collect thermal, mechanical, and electrical data such as coolant temperatures, heat sink temperatures, torque, speed, currents, and voltages. These data were collected and fed into an immense spreadsheet and saved for future use. An optimal control scheme was developed to ensure the most efficient operation of the motor throughout the entire operation range. The controller uses speed, position, and current feedback to regulate the output conditions supplied by the inverter. The OEM motor inverter controls were bypassed to allow full control over the inverter, enabling uninhibited testing of the system over various operating conditions.

Efficiency measurements of the motor and inverter were taken over the entire operation range of the motor. The efficiency contour map in Fig. 11 represents the steady state efficiency characteristics of the motor for efficiencies above 60%. The peak efficiency is 96%, and efficiencies above 88% are spread over a large area of the operating region. For much of the high torque regions, a coolant temperature of ~10°C was used to permit extensive testing in this region. Otherwise, the torque levels nearing 200 Nm could only be maintained for extremely short periods of time before reaching stator temperature limits. Figures 12, 13, and 14 show the combined motor and inverter efficiency maps for dc link voltages of 650 Vdc, 500 Vdc, and 225 Vdc, respectively. The same scale was used in all of these figures to portray the phenomenon of improved efficiencies for lower dc link voltages. The peak combined efficiency for 650 Vdc in Fig. 12 is 95%. Although the peak combined efficiency for 500 Vdc is only 94%, this peak efficiency region has shifted to a lower speed and efficiencies are ultimately higher than that of the 650 Vdc efficiency map in low speed and medium torque regions. Similarly, the combined efficiency map for 225 Vdc has higher efficiencies than that with 500 Vdc and 600 Vdc in low speed and low torque regions of the map. The primary reason for this is the inverter efficiency, where switching losses decrease with decreasing voltage. Additional data, further analyses, and more elaborate documentation of the findings and results from the FY 2010 benchmarking efforts can be found in [1] in the publications list at the end of this section.

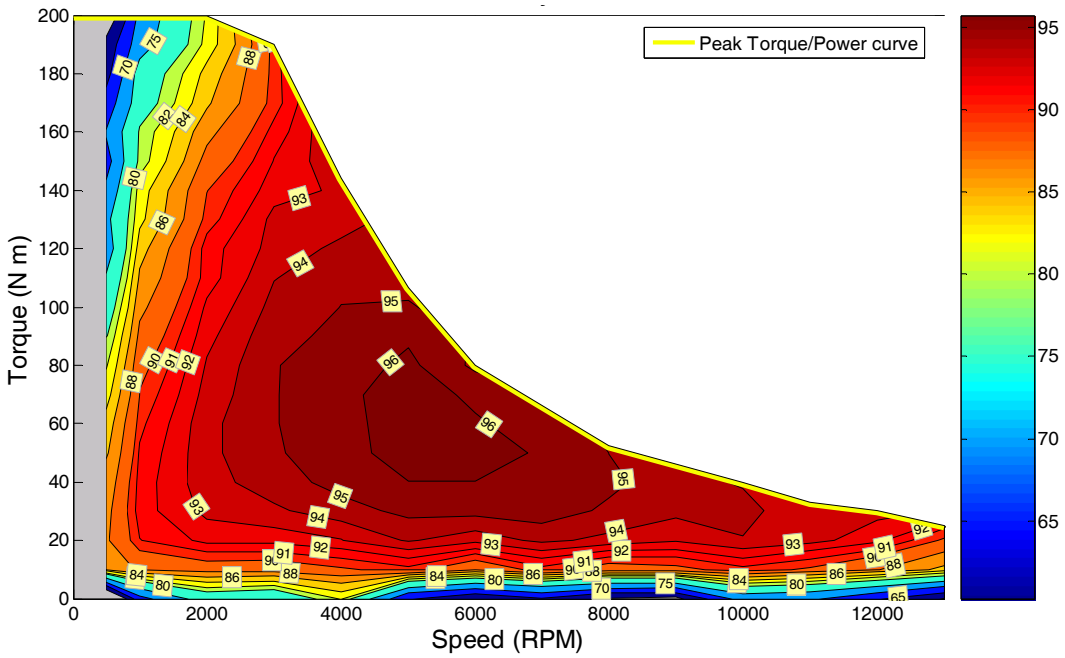


Fig. 11. 2010 Prius motor efficiency map for 650 Vdc.

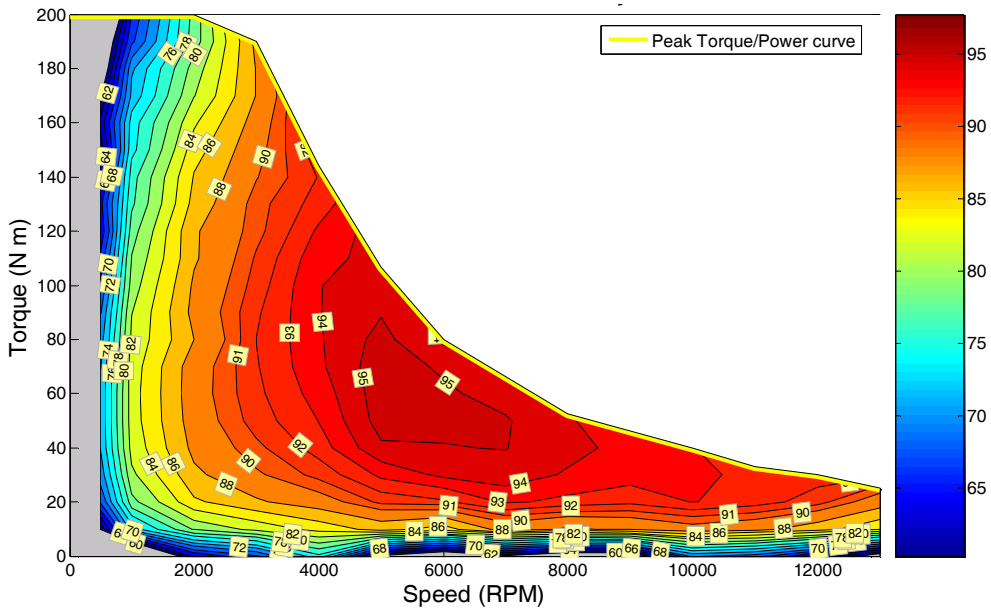


Fig. 12. 2010 Prius combined motor-inverter efficiency map for 650 Vdc.

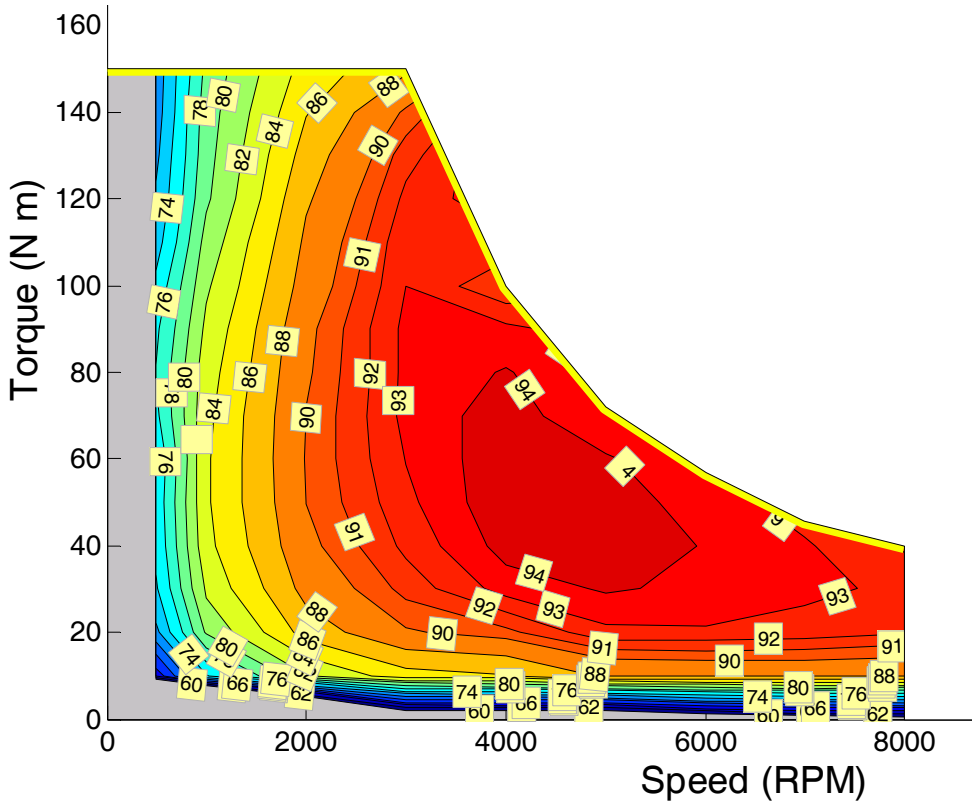


Fig. 13. 2010 Prius combined motor-inverter efficiency map for 500 Vdc.

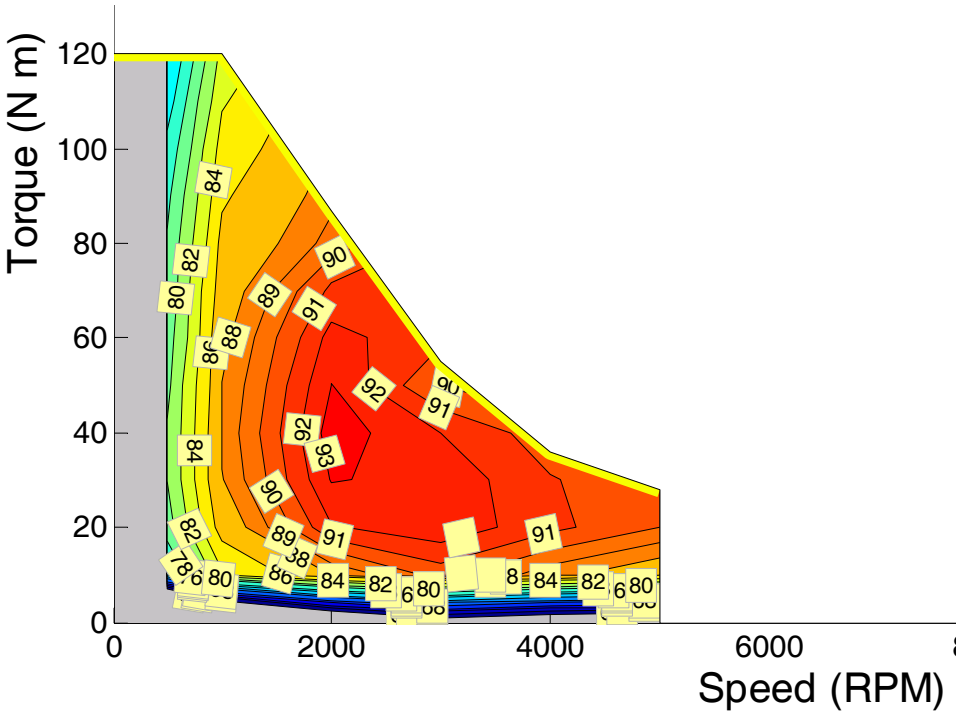


Fig. 14. 2010 Prius combined motor-inverter efficiency map for 225 Vdc.

Conclusions

Our evaluation of the 2010 Toyota Prius uncovered the following.

- Benefits of the integrated cooling technique used in the 2010 Toyota Prius lead to a significant increase in specific power in comparison with the Camry (78% increase), while the power density actually decreased slightly.
- Reduced IGBT and diode count in boost converter, which was integrated into the same module as motor and generator inverters, leading to lower costs.
- Cooling technique not as effective as LS 600h double sided cooling technique but is likely more cost effective.
- Motor stator rotor has similar PM arrangement to other models used for comparison, but overall lamination is significantly different.
- Motor lamination stack length is 2 in. versus 2.4 in. for the Camry.
- Power density of the 2010 Prius motor is slightly lower than that of the Camry and LS 600h.
- Specific power of the 2010 Prius motor, while higher than that for the 2004 Prius, is still slightly lower than that of the Camry and LS 600h.
- Motor efficiencies are above 90% for a great portion of the operation range, even more so than the Camry.
- Low dc link voltages facilitate increased efficiency for low speed and moderate torque operation regions because of reduced inverter switching losses.
- High torque and high power operation points are best suited with 650 Vdc operation.
- Peak efficiencies reached 96% for the motor.

Publications

1. T. A. Burress, et al., *Evaluation of the 2010 Prius Hybrid Synergy Drive System*, ORNL/TM-2010/253 Oak Ridge National Laboratory, 2010.

References

1. T. A. Burress, et al., *Evaluation of the 2007 Toyota Camry Hybrid Synergy Drive System*, ORNL/TM-2007-190, Oak Ridge National Laboratory, 2007.
2. T. A. Burress, et al., *Evaluation of the 2008 Lexus LS600h Hybrid Synergy Drive System*, ORNL/TM-2008/185, Oak Ridge National Laboratory, 2008.

4.2 High-Power-Density Integrated Traction Machine Drive

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Objectives

- Overall objective is to develop a reliable, fault-tolerant, integrated modular motor drive (IMMD) capable of operating at 200°C junction and 150°C ambient temperatures.
- For FY 2010, the objectives are to
  - design a demonstrator version of the IMMD with fault-tolerant controller using the most promising configuration to verify performance characteristics including power density and fault tolerance and
  - evaluate silicon (Si) insulated gate bipolar transistor (IGBT) and suitable packaging at 200°C, considering device characteristics, loss, cooling, and reliability.

Approach

- Analyze alternative fault-tolerant machine and controller configurations to identify the most promising candidates for future demonstration in prototype hardware.
- Apply the results of the initial analysis to design and build a preliminary10 kW prototype integrated traction drive in FY 2011 followed by a full-scale 55 kW (peak) prototype unit in FY 2012 and FY 2013.
- Evaluate selected Si IGBT for operation at 200°C, considering device characteristics such as loss, thermal limits, and reliability. These devices will potentially be used in device modules for IMMD to be developed in FY 2011 and FY 2012.
- Develop suitable phase-leg device module packaging concept through analysis and simulation, aiming for 200°C junction and 150°C ambient operation. The device module concept will be the basis for prototyping in FY 2011 and implementation in IMMD in FY 2012 and FY 2013.

Major Accomplishments

- Analyzed and compared a variety of alternative modular motor configurations, leading to identification of a 6P, 10 pole permanent magnet (PM) machine as the most promising configuration for further development.
- Analyzed and compared several alternative distributed controller configurations, leading to selection of a heterarchical control architecture as the best candidate for achieving fault-tolerant operation.
- Tested static and switching characteristics of IGBT at various temperatures, concluding that device losses are acceptable for operation at 200°C, but the ruggedness of the devices needs further evaluation.

- Designed a baseline 10 kW phase-leg power module package through die selection, material selection, layout design, parasitic extraction, and thermal characterization. The commercial two-pass tube cold plate is selected for cooling the phase-leg power module. Thermal performance of the packaging design with liquid cooling was analyzed. The effects of different coolants (water-glycol and transmission oil) and 150°C ambient on junction temperature were compared. The results show the baseline device module can meet the required power and temperature performance need for IMMD.

Future Direction

- In FY 2011, build and test a 10 kW demonstrator IMMD to evaluate drive system performance and fault tolerance; develop the 10 kW phase-leg power modules needed for implementing the full power IMMD. The modules should be based on low cost Si and able to operate in ambient temperatures of 150°C with junction temperatures up to 200°C.
- In FY 2012 and 2013, scale up the power level of the IMMD technology and combine with the high temperature modules to achieve high-density integrated traction motor drive.

Technical Discussion

1. Machine Performance Comparisons

1.1 Optimal Slot/Pole Combinations for Different Numbers of Phases

In this section, the set of criteria for choosing the optimal slot/pole combination for different numbers of stator phases is presented. The basic building block of the IMMD consists of a stator pole-piece fitted with a concentrated winding and a dedicated power converter unit. Considering the nature of the application, the optimal slot/pole combinations can be chosen according to the following criteria.

1. Choose a high value of the fundamental winding factor K_{w1} to maximize torque production.
2. Choose the highest least common multiple (LCM) of the number of slots, N_s, and the number of poles, N_m, to minimize cogging torque. LCM(N_s,N_m) indicates the number of cogging torque periods per full mechanical rotation.
3. Choose the greatest common divisor (GCD) of N_s and N_m that is greater than one and even. GCD(N_s,N_m) indicates symmetries in winding layout and magnetic pull between the stator iron and the rotor magnets.
4. Consider the magnetic motive force (MMF) space harmonic distribution to minimize the rotor losses.

Table 1. Key Metrics of Machines with Different Phase Numbers

	3P	4P	5P	6P
Poles	10	14	14	10
Slots	12	16	15	12
SPP	2/5	2/7	3/14	1/5
LCM	60	112	210	60
GCD	2	2	1	2
Winding factor	0.933	0.962	0.980	0.966
Max elec. freq. (Hz)	1167	1633	1633	1167
Overrating factor (%)	n/a	33	25	20
Number of modules	6	8	5	12

Reference [1] includes tables presenting the synchronous winding factor, LCM(N_s,N_m), and GCD(N_s,N_m) for 3, 4, 5, and 6P slot/pole combinations that support fractional-slot concentrated windings. These tables were used as a source for Table 1, which presents optimal slot/pole combinations for fractional slot concentrated winding (FSCW) surface PM (SPM) machines. Phase numbers between 3 and 6 were selected, and basic performance features of these

designs were compared to a baseline 12 slot, 10 pole, 3P SPM machine (Table 1). These designs are referred to as 3P, 4P, 5P, and 6P, where the number represents the number of phases.

Table 2 presents the key machine dimensions and magnet characteristics that were held constant for all of the machine designs. Figures 2 to 5 provide key graphical information for each of these four machine designs including a machine cross-sectional view, a plot of the winding function for a single phase winding, and a plot of the spatial harmonic components that are present in the winding function. The highlighted entries in Table 2 identify the strengths of each candidate. The 3P design has a relatively low electrical frequency and an even value of GCD. Since the 6P design has the same stator and rotor structure as the 3P design, their characteristics are quite similar. However, the higher winding factor and reduced torque ripple of 6P are advantages due to the increased number of phases. The slot/phase/pole (SPP) value of 2/7 is highlighted for the 4P design because previous work has shown that the families of SPP=2/5 or SPP=2/7 are particularly well suited for high speed SPM machine achieving optimal flux weakening conditions [3]. The 5P design has the highest LCM value and winding factor and the minimum number of modules.

Table 2. Machine Dimension and Material Constraints

Stator OD (mm)	274	Rotor OD (mm)	142
Active axial length (mm)	75	Magnet thickness (mm)	11
Air-gap thickness (mm)	1	Magnet remanent flux density (T)	1

1.2 Effects of Stator MMF Space Harmonics on Candidate Design Performance

Because the stator MMF distributions of FSCW machines generally contain a rich set of spatial harmonics, the magnet eddy-current losses in modular PM machines are typically larger than those in conventional PM brushless ac machines. The torque in modular PM machines is produced by the interaction of a higher-order synchronous harmonic component with the permanent magnets. Harmonic component analysis of the phase winding functions was conducted to compare the spatial harmonics. In the comparison, a constraint was introduced requiring the same magnet flux-linkage in all of the candidate designs. With this constraint, the amplitude of the synchronous frequency component in Figs. 1–4 is the same for all of the candidate designs. As a result, all the machines produce the same torque when the windings are excited with a current that is inversely proportional to the number of phases.

1.3 FEA Validation of Machine Performance

Finite element analysis (FEA) was used to design the four candidate machines presented in Figs. 1–4 and to analyze their performance. Table 3 provides a summary of the key performance predictions for the candidate machines.

Figure 5(a) presents comparisons of the predicted phase back-EMF waveforms for all 4 machines operating at maximum speed (14,000 rpm), emphasizing the electromagnetic similarities of these four machines. The predicted average torque for these machines is plotted in Fig. 5(b) as a function of the phase current, with both variables plotted in per-unit to simplify the comparisons. All four machines begin to exhibit the effects of magnetic saturation at elevated phase current amplitudes between 1.5 and 2.0 pu, although the nonlinearity is mildest for the 3P machine. Finally, Fig. 5(c) compares the predicted torque ripple for the four machines during peak torque operation (i.e., 55 kW at 2800 rpm), demonstrating that the torque ripple is modest for all the machines (note the suppressed zero in the torque axis), with the highest ripple appearing in the 3P machine.

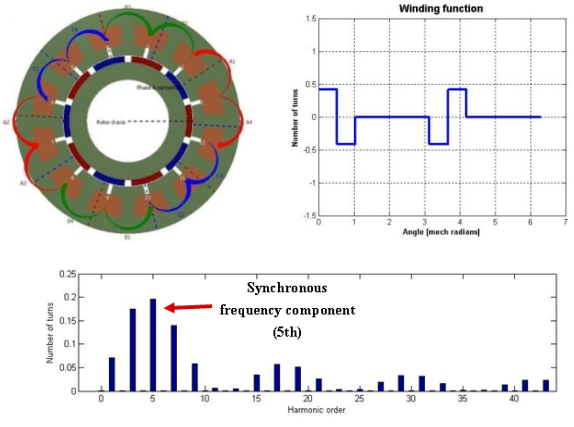


Fig. 1. Three phase (3P) machine: 12 slots/10 poles.

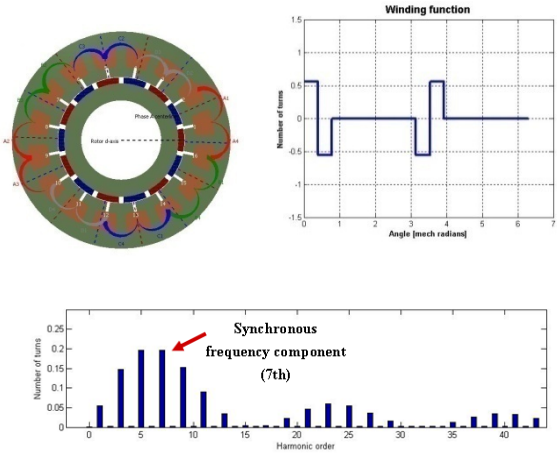


Fig. 2. Four phase (4P) machine: 16 slots/14 poles.

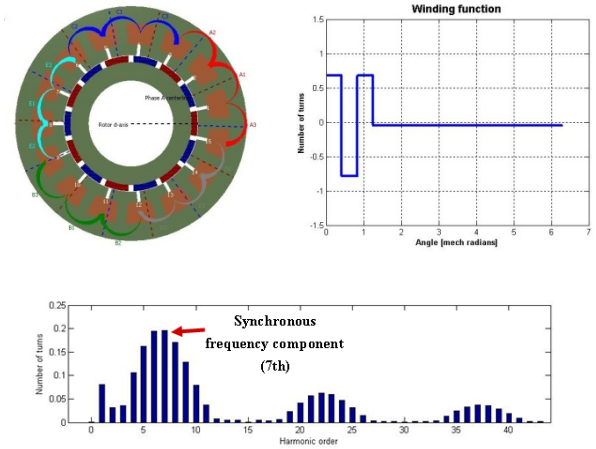


Fig. 3. Five phase (5P) machine: 15 slots/14 poles.

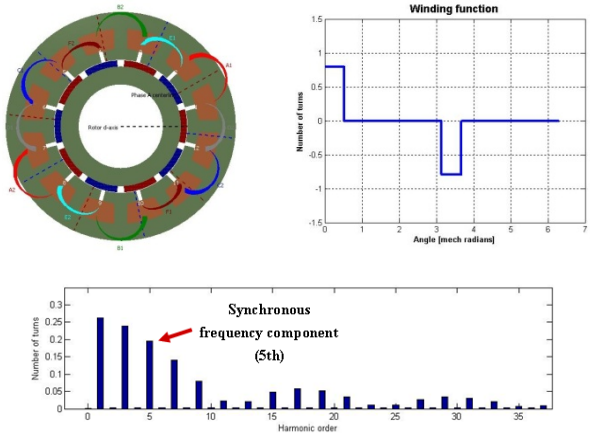
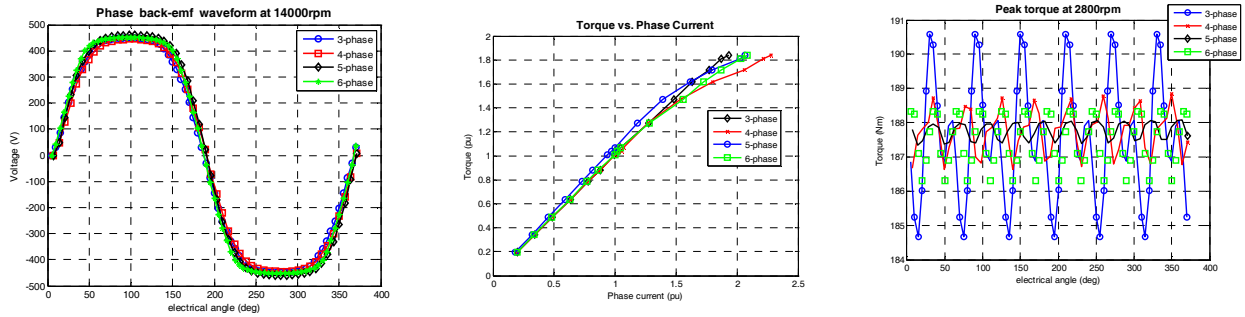


Fig. 4. Six phase (6P) machine: 2 slots/10 poles.

Table 3. Comparative Machine Performance Metrics

Feature	3 Phase	4 Phase	5 Phase	6 Phase
Series turns/phase	32	32	33	32
Rated current density @ A/mm^2	5.64	5.69	5.16	5.75
Peak current density @ A/mm^2	10.89	11.84	11	11.74
Rated current (A rms)	150	118	82.2	76.6
Phase back EMF @ 14,000 rpm (V_{peak})	458	455	460	458
Torque ripple @ peak power conditions (%)	5.9	2.0	0.7	2.3
Copper mass (kg)	6.8	7.8	10.4	13.6
Iron mass (kg)	19.1	18.3	18.1	19.2
Magnet mass (kg)	2.3	2.2	2.2	2.3
Total mass (kg)	28.2	28.3	30.7	35.1
Peak PM flux linkage (mWb)	71.5	53.8	43.4	35.9



(a) (b) (c)

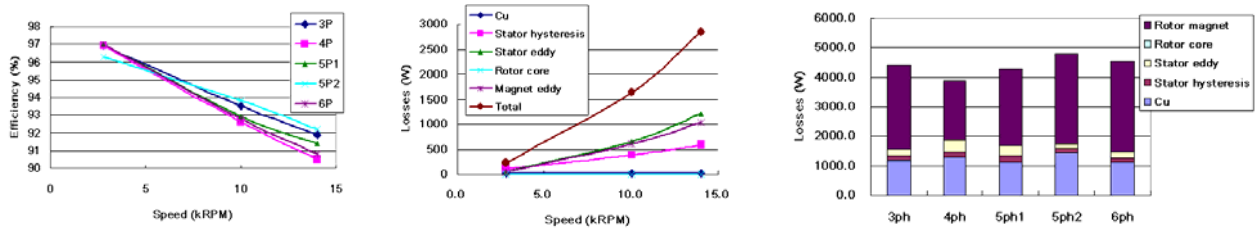
Fig. 5. (a) FEA-predicted phase back-EMF waveforms at 14,000 RPM; (b) predicted torque vs. phase current plot in per unit; and (c) predicted torque ripple during peak torque operation.

1.4 Soft Magnetic Composite Stator Core Replacement

The preliminary evaluation of soft magnetic composite (SMC) material was carried out in a non-optimal fashion. Instead of developing new machine designs tailored to the SMC material properties, the M19 material in the laminated-core designs was simply replaced with SMC material. The results of this material replacement exercise showed that the predicted average torque produced using the SMC core is 11% lower than that of the same machine with 0.35 mm-thick M19 laminations. In addition, the predicted core loss of the SMC core is higher than the loss of conventional laminated cores using M19 steel by 40 to 50% at maximum speed.

1.5 Predicted Machine Losses and Efficiency

The predicted efficiencies of the candidate machine designs with different phase numbers were evaluated at three operating points at speeds of 2,400, 10,000, and 14,000 RPM using sinusoidal current excitation. Figure 6(a) shows the predicted efficiency values vs. speed for partial load (20% of rated torque) conditions, exhibiting efficiency values that monotonically decrease from values in the vicinity of 90% at low speeds to values in the range of 91 to 92% at the maximum speed of 14,000 rpm. Figure 6(b) shows the corresponding loss breakdown for the 5P1 machine (note that 5P1 and 5P2 correspond to two 5P designs with different stator winding configurations), indicating that losses in the stator core and magnets increase with speed and dominate the losses at high speeds. Figure 6(c) provides more details about the predicted loss breakdown in the five machines under peak output power conditions (55 kW at 2800 rpm), indicating that magnet losses dominate under this condition.



(a) (b) (c)

Fig. 6. (a) Predicted efficiency at 20% rated torque vs. speed for machines with 3 to 6 phases; (b) predicted loss components of 5 phase machine vs. speed at 20% rated torque; and (c) predicted loss breakdowns at 55 kW and 2,800 rpm.

1.6 Results of Comparative Machine Evaluation

The results of the analytical machine study were carefully evaluated in order to select the most promising candidate machine for the 10 kW preliminary prototype drive planned for construction and testing in FY 2011. The selection is made more complicated by the fact that no single configuration emerged as being the best in every category, which requires considering engineering tradeoffs. After the evaluation process, the decision was made to select a variant of the 3P machine reconfigured with 6 phases instead of 3 as the preferred candidate for further development. As noted in Table 1, the 3P machine actually uses 6 separate phase modules, making it possible to operate this machine as a 6P unit if each module is treated as an independent phase module. Figure 1 shows that each of these 6 phases occupies a 60 degree arc along the stator periphery.

The major factors favoring the 3P (or 6P) machine over the other candidates for this application include its even GCD value of 2, which eliminates unbalanced magnetic pull on the rotor, lower machine mass, and lower fundamental frequency (1.16 kHz) at maximum speed that is critical to achieving high efficiency values at elevated speeds. Although its winding factor and LCM values are not the highest among the candidate machines, the overall evaluation of the 6P configuration gave it a net advantage over the other alternative machine configurations that ultimately led to its selection as the preferred topology for further development.

2. Fault-Tolerant IMMD Controller Development

Two alternative controller architectures that were evaluated and compared for the IMMD application are hierarchical and heterarchical controllers presented as block diagrams in Fig. 7. Of these two architectures, the hierarchical controller [Fig. 7(a)] represents the more familiar and conventional control configuration adopted in many machine drives. In this hierarchical controller, a master centralized controller is in charge of controlling the machine operation, interacting directly with the encoder (or resolver), IGBT gate drivers, current sensors, and user interface. Clearly, if the centralized controller fails, the whole system fails, making this hierarchical controller architecture a poor choice for fault tolerance.

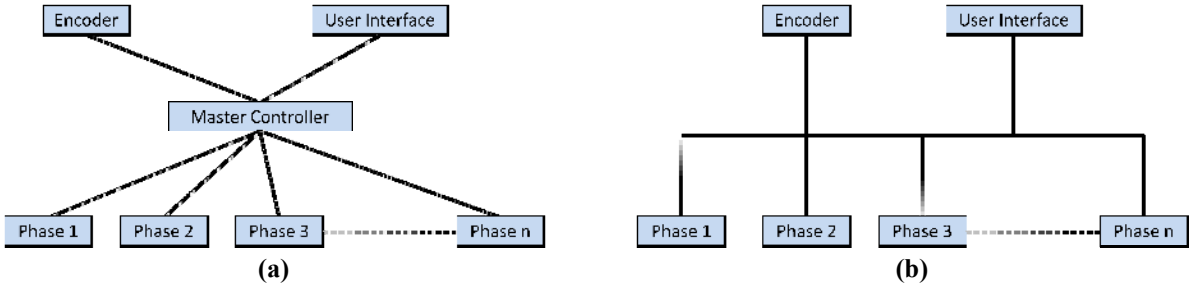


Fig. 7. Two alternative controller architectures for the IMMD: (a) basic hierarchical control architecture and (b) basic heterarchical control architecture

In the alternative heterarchical controller [Fig. 7(b)], each phase module has its own dedicated controller. All of the phase controllers are connected to each other as well as to the drive sensors (i.e., rotor position sensor and current sensors) and user interface via a digital network. In contrast to a master-slave configuration, the individual controllers in the heterarchical architecture operate in parallel as independent peers, with each controller having control of only its own associated module. If one of these controllers fails, all of the *n-1* remaining phase module controllers are able to continue operating.

A block diagram using this type of controller configuration to implement field-oriented control for a 5P IMMD is shown in Fig. 8. Although shown for a 5P machine, this configuration can be generalized to control an *n*-phase machine in the same manner.

The incremental encoder will have its A, B, and index pulse pins connected to the on-chip quadrature encoder module in each controller by means of a 3 wire digital bus. The individual phase current readings are available to each modular controller through an *n*-wire analog bus, and each modular controller's on-chip A/D converter will have real-time information from all of the phase current sensors available through this analog bus. An on-chip UART or CAN module will be used to connect each controller to the user interface and to exchange other information among the phase module controllers. Although not shown in Fig. 8, a ring topology could be adopted for the digital network.

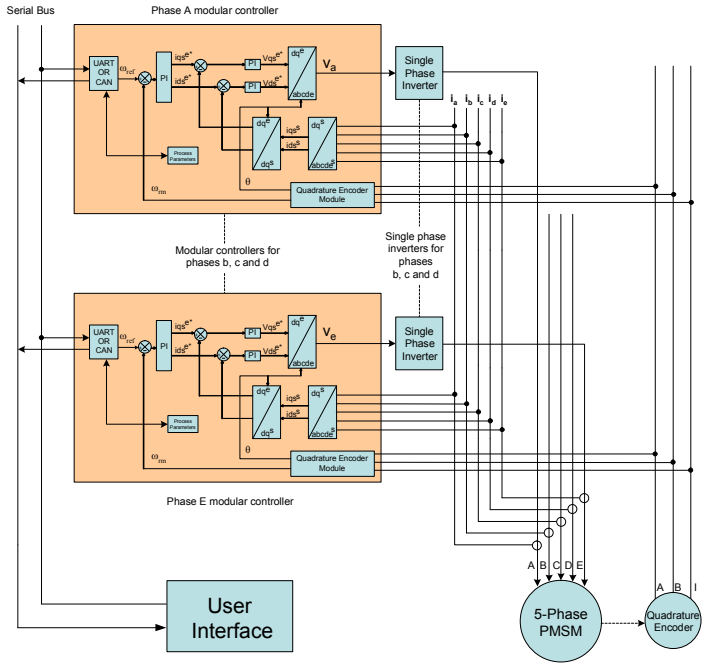


Fig. 8. Heterarchical controller implementation for field-oriented control of a 5 phase IMMD.

Controller/DSP Selection for IMMD Fault-Tolerant Control

A variety of 16 and 32 bit microcontrollers offered by leading semiconductor manufacturers were reviewed for the IMMD application. After careful consideration, the Texas Instruments Piccolo 32 bit TMS320F28035 microcontroller was selected as the best candidate for this project.

3. Si IGBT Operation at 200°C

IMMD offers a promising new approach for integrating motor drive power electronics into the machine housing in a modular fashion. To be integrated into the machine housing, the power electronics need to work in ambient temperatures up to 150°C. For low cost, it is desirable to use Si devices. Given that the current commercial Si devices usually have a maximum junction temperature rating of 150°C, with some devices rated at 175°C, it is desirable to investigate the possibility to push the Si device junction temperature to 200°C with increased loss-handling capability and higher power density. [9]

An IGBT with soft, fast recovery antiparallel diode from Infineon (IKW40N120H3) is selected for characterization and thermal study of IGBT operating at high temperatures (Fig. 9). Table 4 shows the basic parameters in the datasheet. The main issues with Si device operating beyond 150°C to 200°C include excessive loss and possible thermal runaway due to excessive leakage current, the change of the safe operating area boundaries due to the decreased latching current and second breakdown, and corresponding long-term reliability issues. [10] In this report, IGBT is investigated in terms of static and switching characteristics, device losses, and thermal limits.

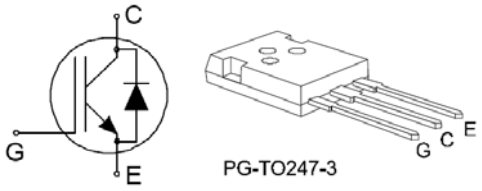


Fig. 9. IKW40N120H3-Si IGBT with antiparallel diode.

Table 4. Specifications of IKW40N120H3

Type	V_{CE}	I_C	V_{CEsat}, T_{vj}=25°C	T_{vjmax}	Package
IKW40N120H3	1200V	40A	2.05V	175°C	PG-TO247-3

3.1 IGBT Static Characteristics

Figure 10 shows the static characterization setup. Figure 11 shows the IGBT output characteristics at 200°C. RCE(on) represents the on-state resistance and VT0 represents the threshold voltage, both significant parameters for conduction loss. Table 5 shows the parameters of IGBT output characteristics at different temperatures. As the temperature rises, the on-state resistance increases because of mobility reduction while the threshold voltage decreases. As a result, the conduction loss has a positive temperature coefficient when Ic is large.

Fig. 10. Static characterization setup with curve tracer.

Table 5. Parameters of IGBT Output Characteristics at Different Temperatures

	25°C	100°C	175°C	200°C
V_{T0}	1V	0.9V	0.8V	0.7V
$R_{CE(on)}$	0.026Ω	0.037 Ω	0.049 Ω	0.052 Ω

For the loss calculation, the leakage current is measured when 650 V is applied to the collector and emitter of device under test (DUT). Figure 12 shows the IGBT leakage current as a function of junction temperature. At high temperatures, especially above 175°C, the leakage current increases rapidly (double every 5 degrees), which contributes to the total loss and might cause thermal runaway.

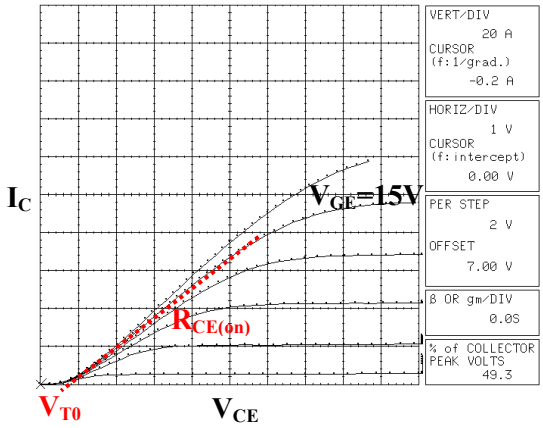


Fig. 11. IGBT output characteristics at 200°C.

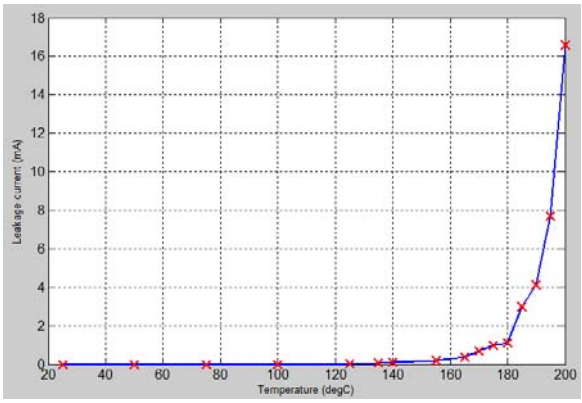


Fig. 12. IGBT leakage current at 650 V as a function of junction temperature.

3.2 IGBT Switching Characteristics

The inductive-load double pulse tester was built to test the switching characteristics of Si IGBT. Figure 13 shows the circuit schematic of double pulse test (DPT) with overcurrent protection. The double pulse is generated by Agilent 33220 arbitrary waveform generator. The DUT is driven by a high speed, high current gate driver IXDD414 from IXYS, with gate voltage from 0 V to 15 V.

To measure the switching characteristics of IGBT at high temperatures, DUTs are connected to the hot plate through the copper connector, as shown in Fig. 14. The glass wool and fan are used to keep the PCB board (especially for shunt resistors and gate drivers) under 50°C. Thermal couples are used to monitor and adjust the temperature of DUT case and PCB. Since the switching loss caused by two pulses is negligible, it is assumed that DUT junction temperature is the same as the case temperature. Figure 15 shows the hardware testbed for high temperature switching experiments.

Fig. 13. High temperature experiment setup for switching characteristics test.

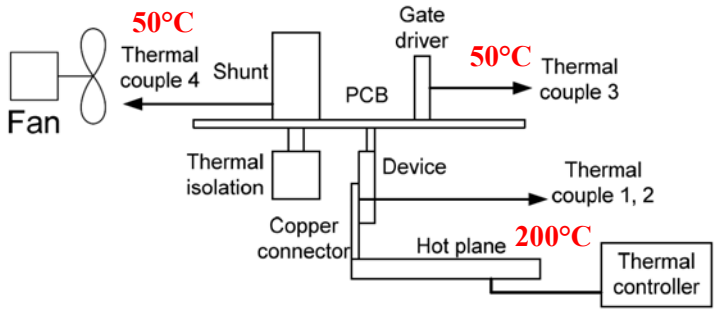


Fig. 14. High temperature experiment setup for switching characteristics test.

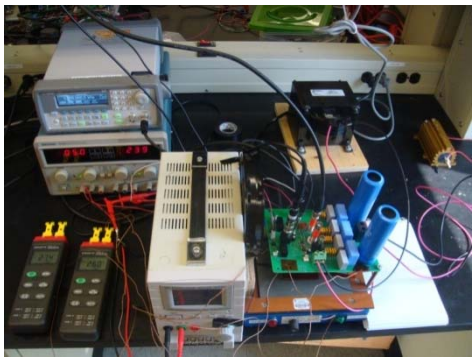


Fig. 15. Hardware testbed for high temperature switching experiments.

With the DPT hardware testbed, the IGBT switching characteristics are tested at 25°C, 100°C, 175°C, and 200°C. The test conditions are: VCC=650 V, IC=40 A, VGE=0.0 V/15.0 V, RG=10.0 Ω. Figure 16 shows the DPT waveforms of IGBT at 200°C.

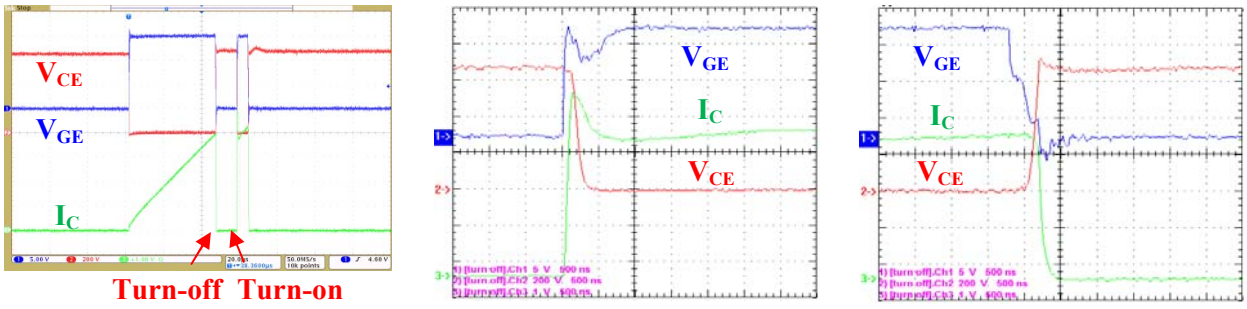


Fig. 16. Waveforms of IGBT switching characteristics at 200°C: (a) double-pulse waveforms, (b) turn on transient, and (c) turn off transient.

Based on the switching waveforms, the parameters of IGBT switching characteristics at different temperatures are calculated and shown in Table 6. The experimental parameters at 25°C and 175°C are very close to that in the datasheet. Both the switching time and switching energy increase as the temperature goes up.

Table 6. IGBT Switching Parameters at Different Temperatures

Parameter	25°C	100°C	175°C	200°C
Turn on delay time $t_{d(on)}$	24.4ns	21ns	23.6ns	20ns
Rise time t_r	60.4ns	62.6ns	78.4ns	80ns
Turn off delay time $t_{d(off)}$	278ns	311.2ns	380ns	400ns
Fall time t_f	38.8ns	79.2ns	120ns	140ns
Turn-on energy E_{off}	3.19mJ	3.99mJ	4.50mJ	4.61mJ
Turn-off energy E_{off}	1.31mJ	2.05mJ	2.83mJ	3.02mJ
Total switching energy E_{ts}	4.50mJ	6.04mJ	7.33mJ	7.63mJ

3.3 Power Losses and Thermal Analysis

To calculate the motor drive losses based on the device characteristics, the specifications of the system are assumed in Table 7.

Table 7. System Specifications

Power rating (for 1 phase leg)	P_B=10 kW	**DC link voltage**	V_{dc}=650 V
Nominal voltage (l-n rms)	V_B=217 V	**Modulation index**	M=0.994
Nominal current (rms)	I_B = 46 A	**Modulation scheme**	Continuous space vector modulation (SVM)

The total loss generated from power devices consists of conduction loss, switching loss, and leakage current loss. In our case, the diode reverse recovery loss is neglected since it is very small. Table 8 and Fig. 17 show the total losses in one phase leg, which increase with temperature.

Table 8. Power Losses in One Phase Leg at Different Temperatures (f_s=5kHz)

(Unit: W)	25°C	100°C	175°C	200°C
IGBT conduction loss	91.66	110.31	131.0	133.28
IGBT switching loss	23.34	31.3	38	39.6
Leakage current loss	0	0	0.65	10.8
Diode conduction loss	3.07	3.22	3.28	3.31
Total loss	118.07	144.86	172.95	186.95
Efficiency (%)	98.82	98.55	98.27	98.13

The device is cooled by the water-ethylene-glycol (WEG) coolant at 105°C. Keeping the junction temperature below 200°C requires a certain thermal transfer ability, which is represented by thermal resistance and depends on the semiconductor material and packaging. Figure 18 shows the temperature curve with the power dissipation line. The rate of the thermal load line is thermal conductance. The cross point of the thermal load line and the zero loss line is the coolant temperature. From Figure 18, the thermal resistance from junction to ambient of IGBT should be no more than 1.04 K/W if the switching frequency is 5 kHz, which provides the baseline for packaging design. Some failures were observed during DPT at 200°C, and the ruggedness of the devices needs further evaluations.

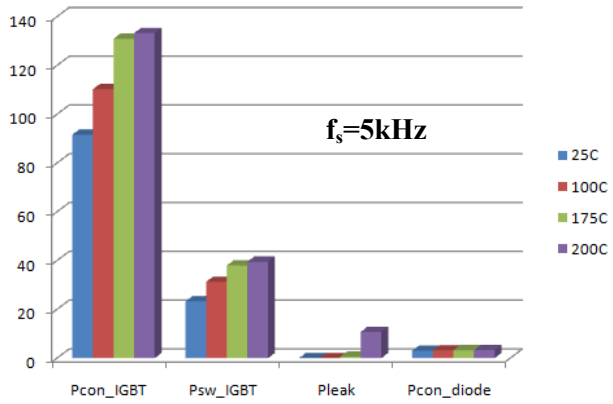


Fig. 17. Power losses in one phase leg at different temperatures (f_s=5kHz).

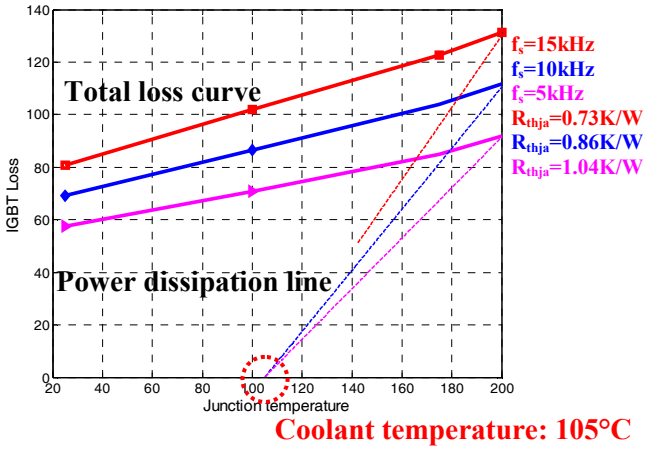
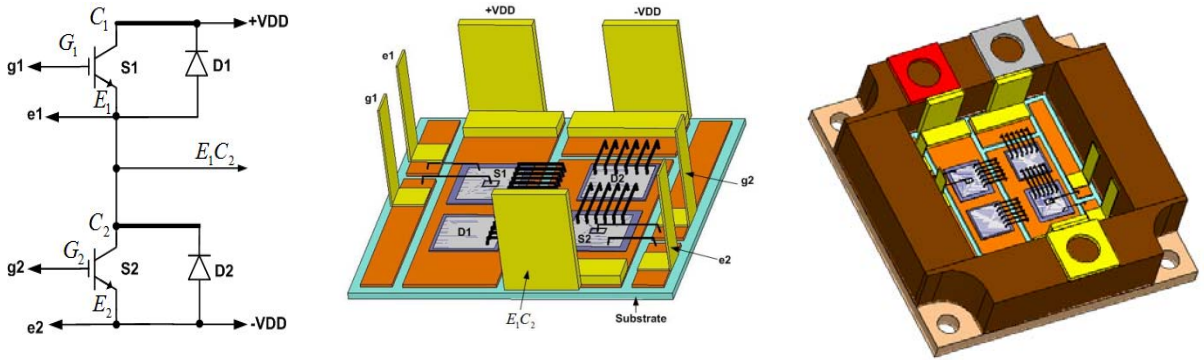


Fig. 18. IGBT power losses and thermal analysis at different frequencies.

4. Device Packaging and Cooling

Wire-bonding technology is adopted for the baseline design of the 10 kW phase-leg power module, as shown in Fig. 19. Meanwhile, Table 9 lists the detailed materials selection and the corresponding dimensions. Two Si IGBT and two diode dies from Infineon, with maximum ratings of 1,200 V/50 A/175°C, are selected. To enhance reliability, copper lead frame is used as connection terminal instead of pole connection. Solder Au80Sn20 is used as the die attachment, with an optimized thickness of 200 μm. Essentially, this package is a conventional design [11].

Hence, the baseplate and case are also included, as shown in Fig. 19(c). Note that in future applications we may remove the baseplate to directly connect the substrate to the heatsink to achieve smaller thermal resistance.



(a) **(b)** **(c)**

Fig. 19. Baseline design of a 10 kW phase-leg power module: (a) phase-leg schematic, (b) layout design, and (c) power module design.

Thermal resistance of each device from junction to case is of importance for cooling system design because the maximum junction temperature of each device should not exceed 200°C [12]. An FEA simulation tool, Comsol Multiphysics, was used to characterize the thermal performance of the proposed package. Table 10 lists the thermal conductivity values used in the simulation.

Table 9. Materials Selection

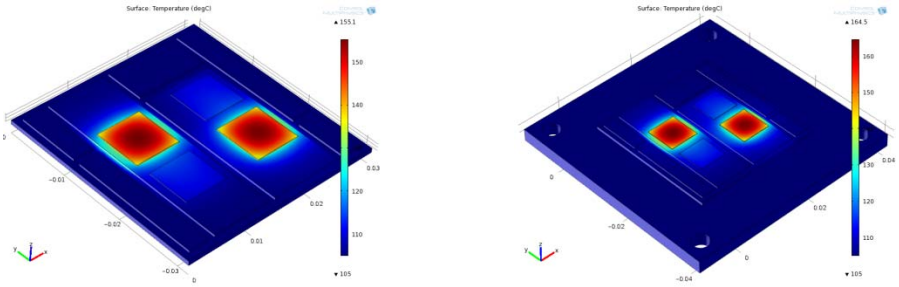
Component	Dimensions (mm)
IGC50T120T6RL	7.25 × 6.84 × 0.115
Emitter pad	5.36 × 5.74 × 0.004
Gate pad	1.31 × 0.81 × 0.004
SIDC42D120F6	6.5 × 6.5 × 0.12
Anode pad	5.78 × 5.78 × 0.004
Substrate	30.6 × 30 × (Cu: 0.3, Ceramic: 0.635)
Aluminum wires	Gate pad 5 mils, others 10 mils × 6
Bus	Copper: 1 × 7 × 9
Lead	Copper: 0.2 × 3 × 9
Die attachment	Au80Sn20: thickness 0.2
Base	Copper: 52 × 53 × 3
Encapsulant	Silicone gel
Case	Torlon 5030

Table 10. Thermal Conductivities

Material	Thermal Conductivity W/(m°C)
Al_2O_3	24
Cu	393
Al	237
Au80Sn20	50
Si	90

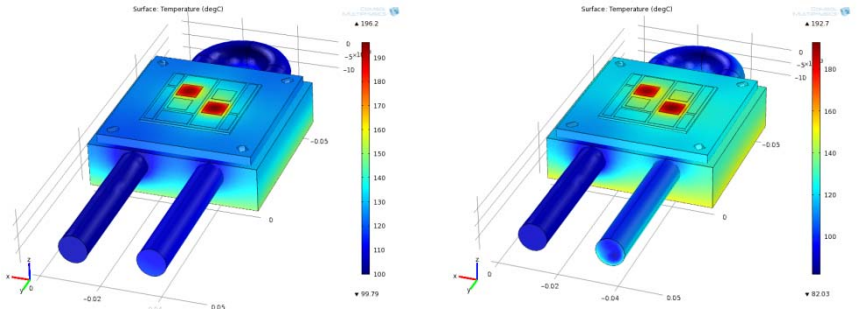
Figure 20 shows the thermal performances of the packaging design without and with baseplate when the modulation index of the inverter is 1.0. As can be seen, the use of the baseplate and the solder layer between substrate and baseplate increase the temperature rise of IGBT about 9.4°C. Here, the IGBT has the largest power loss, and the diode has the smallest loss, hence the temperature rise of the IGBT is the largest.

Thermal management system is another key challenge in motor drive. At present, the inverter and motor use different cooling loops and coolants. Specifically, for inverter cooling, an individual 65°C WEG cooling loop is used, whereas transmission oil circulation with a WEG heat exchanger is used for motor cooling. Our objective is to use one liquid cooling loop and one coolant to cool the inverter and motor together. Figure 21 shows the thermal performance of the packaging design with liquid cooling for two different coolants. In comparison with Figs. 15(a) and 15(b), the junction temperature of the IGBT for the transmission oil (192.7°C) is a little lower than that for WEG (196.2°C). Although the transmission oil has larger dynamic viscosity, the cooling performance of the transmission oil is acceptable in our design due to its lower inlet temperature. Therefore, to further improve the thermal performance of the whole system, we can optimize the packaging design in terms of: (1) selecting high thermal conductivity substrate (e.g., AlN), (2) removing the baseplate, (3) using solder instead of thermal interface material, and (4) designing a more powerful cooling structure (e.g., pin-fin heatsink).



(a) **(b)**

Fig. 20. Thermal performance of the package when IGBT loss is 90 W and diode loss is 10 W. Without baseplate (a), the temperature rise is 50.1°C. With baseplate (b), the temperature rise is 59.5°C.



(a) **(b)**

Fig. 21. Thermal performance of the packaging design with liquid cooling: (a) WEG coolant with inlet temperature 105°C and (b) transmission oil coolant with inlet temperature 90°C.

Conclusion

Significant progress has been made during the first year of this project towards identifying the most promising machine and controller architectures for inclusion in the integrated traction drive system. A variety of fractional-slot concentrated-winding PM machine configuration with 3 to 6 stator phases were evaluated and compared to determine their suitability for this special drive application. After considering all of the engineering tradeoffs, a 6P variant of a 3P, 12 slot, 10 pole machine has been identified as the candidate machine demonstrating the highest potential for achieving the demanding performance objectives of the integrated traction drive system. Also, alternative controller architectures for the integrated traction drive have been evaluated and compared. A heterarchical control architecture is identified as the most promising configuration for achieving the desired high levels of fault tolerance. According to this preferred architecture, the *n-1* healthy controllers are unaffected by the loss of any one of the controllers, providing the basis for a robust control of the integrated traction drive.

The static and switching characteristics of selected Si device have been tested with a hardware testbed built specifically for device characterization at high temperature. The results show that the loss and leakage current at 200°C are acceptable. However, the ruggedness of such devices at 200°C requires further evaluation. Based on the losses and thermal study, an Si-device-based 10 kW phase-leg packaging design together with a 2-pass tube coldplate is proposed. Detailed thermal performance characterization has been conducted for different packaging structures, operating conditions, and coolant selections. The proposed packaging design and cooling approach can maintain the Si IGBT junction temperature below 200°C with the ambient temperature of 150°C.

Publications

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1. M. EL-Refaie, M. R. Shah, R. Qu, and J. M. Kern, "Effect of number of phases on losses in conducting sleeves of high speed surface PM machine rotors," in *Conf. Rec. 42nd IEEE IAS Annu. Meeting*, New Orleans, LA, Sep. 2007, pp. 1522–1529.
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4.3 Advanced Integrated Electric Traction System

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Objectives

- Develop and demonstrate advanced technologies for an integrated ETS capable of 55kW peak power for 18 seconds and 30kW of continuous power.
- The ETS is to cost no more than $660 (55kW at $12/kW) to produce in quantities of 100,000 units per year, should have a total weight less than 46kg, and have a volume less than 16 liters with a nominal 105°C coolant and >93% efficiency.
- The cost target for the optional Bi-Directional AC/DC Converter is $375.

Approach

- Develop accurate system specifications to reduce cost and increase reliability of system.
- Increase motor power density to reduce cost, less material needed for same power.
- Board centric power electronics to increase flexibility to adapt to vehicle applications, simplify manufacturing process, while improving electrical performance.
- Power module, improve design with new switched with on-chip current and temperature sense, reduced packaging inductance, and improved joint.
- Dc bus capacitor design to eliminate housing, minimize potting and bus structure to reduce cost by eliminating non value added material and increase flexibility of scaling capacitance

Major Accomplishments

- Technology/Component Development
  - IGBT with on chip current and temp sense has been tested for accuracy over operating temperature, current, and voltage
  - Heavy copper board and press fit pin connection, insertion force, formed joint, circuit noise issues, layout constraints, and current capability
  - Power module joint technology tests (1800 cycles)
  - Sintered joints with different combinations of substrate (AlN, Si_3N_4 and Al_2O_3) and base plate, metal injection molded Cu cold forged Al, material being evaluated using three sources
  - Critical factors in successful joint are, plating, thickness of paste applied across joint, joint area, and uniform pressure
  - High temperature solder
  - Developed capacitor capable of meeting high temp environment using polypropylene film and has been verified through testing
  - Film thickness, width, metallization, and resin evaluated
  - Testing
  - Verified through life testing at temperature and voltage
  - Humidity, temperature rise with current, ESL, and ESR

- Thermal
  - Cooling methodologies have been studied and compared for cost and performance

- Motor designs and builds for dyne testing, FEA verification and controls development:
  - Designed an optimized, application-specific, radial insertion bar-wound 5-Phase machine, and built an expedited version with a traditional stranded wire stator to provide an early approximation of the final machine.
  - Completed mechanical design including thermal and stress analyses of the radial insertion bar-wound 5-Phase machine to minimize manufacturing and tooling costs.
    - Developed dual coil concept to reduce quantity of welds by 50%.
    - Developing insertion tools and stator build processes.
    - Forming stator coils and fabricating slot liners.
  - Bar wound 5-Phase machine built and under test

- Inverter
  - Thermal analysis of the inverter completed.
    - All temperatures are within limits
  - Modal and CFD analysis complete
    - Meets GMW3172
  - Completed design, released drawings, ordered parts, manufacturing assembly instructions and fixtures developed
  - Power Module, Gate Drive (includes DC capacitance), and control card have been tested and verified
  - First units built and under test
    - Bench testing
    - Dyne testing
- System
  - Controls development complete

- Charger (AC/DC Converter)
  - Modal and CFD analysis complete
  - Meets GMW3172
  - Built early proto hardware
  - Functionality has been verified
  - Completed design, released drawings, ordered parts, manufacturing assemble instructions and fixtures developed
  - First units built and under test
  - Established collaboration with EPRI for battery to grid

- Program
  - Technologies assessed : 29
  - Configurations/Types: 36
  - Topologies, bus, EMI filtering, components, and concepts
  - Patents: 35
  - Compatibility with vehicle production

Future Direction

- Dyne testing will provide 5-Phase system efficiency map, and torque speed curves necessary to determine validity of simulate data and meets the FreedomCAR objectives
- Environmental testing will confirm hardware improvements in power modules, capacitors, heavy copper boards, press fit pins, and that AIETS meets the FreedomCAR objectives

Technical Discussion

Electric Traction System

This cooperative development project develops an Advanced Integrated Electric Traction System. This program is divided into two phases: a research phase and a development and demonstration phase. The research phase is for experimentation and evaluation of technologies and manufacturing processes. The development and demonstration phase utilized the learning's from the research phase to design, built, and test an Electric Traction System and a bi-directional Charger.

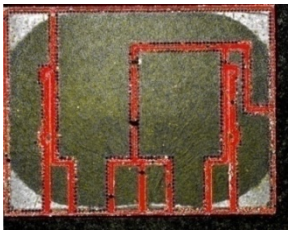
A study of key system requirements was performed. Vehicle operating points and conditions were identified, evaluated, and defined. A topology study was then performed. Topologies that were considered were a conventional 3-phase, boosted system, z-source, and multi-phase were studied. The topology chosen was a 5-Phase because of its opportunity to increase torque density.

Development of components for the electric traction system was undertaken to improve performance and flexibility/scalability. Components that have been the focus of this project are power modules, capacitors, heavy copper boards, current sensors, and gate drive and controller chip sets. Working with suppliers, detailed component specifications have been developed. Current, voltage, and operation environment during the vehicle drive cycle was evaluated to develop the component specifications.

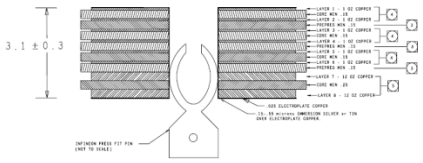
Examples of this area of work are:

1. Capacitors – GM and AVX worked to define in detail accurate component specifications for the DC bus capacitor. Detailed drive cycle information was used to determine voltage, current, and time duration at key points. Additionally environmental conditions were overlaid onto the voltage, current, and time duration information. Analysis was performed to determine best possible candidate materials. Appropriate tests were performed to evaluate candidate films and potting materials. Material recommendations were made based on testing and several types of prototype capacitors were fabricated and tested. Final selection was made based on test data and final system specifications. This yielded a low cost high temperature capable capacitor.
2. Power Module – GM worked with Infineon and Semikron separately to define an accurate detailed specification for a half bridge module. Designs were proposed by each supplier and evaluated for electrical thermal and structural performance by GM. Each element of the power module was studied: silicon; substrate; joining die to substrate and substrate to heat sink; high power and signal interconnects. Evaluations of designs in traction system operating conditions were done. Data was provided to both Infineon

High Temp DC Bus Capacitor



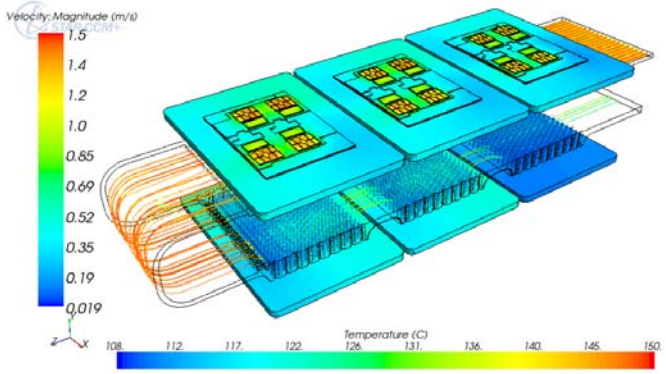
Sintered Joint Evaluation



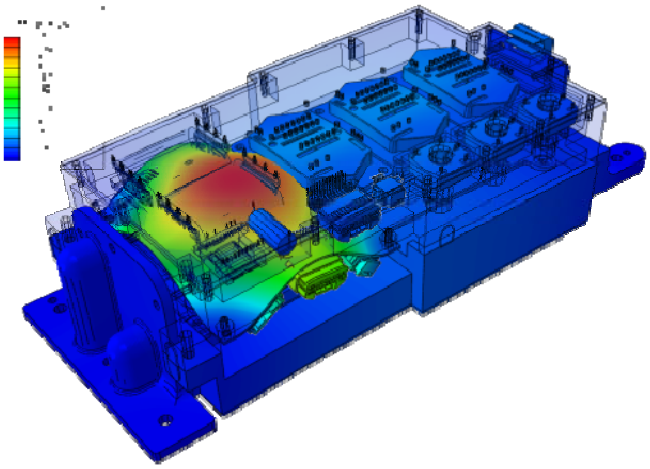
Press Fit Pin Interface

and Semikron, and appropriate changes were made to each respective design. Prototype power modules were fabricated, delivered, and tested. Deficiencies in fabrication processes and design were identified, (i.e. hv press fit pin bridge frame support and symmetry of pins, part plating issues for sintering) and changes made if feasible.

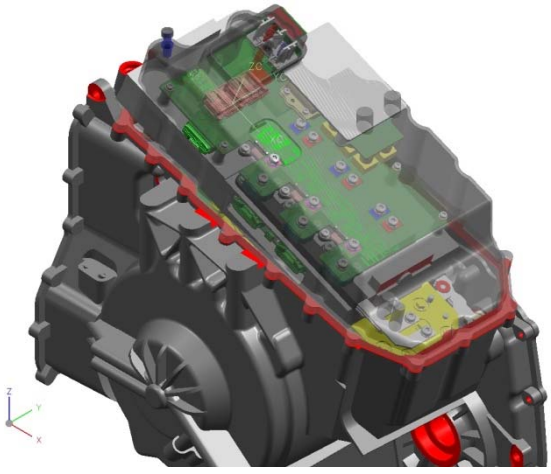
The integrated electric traction system packaging presented significant complexity with space limitations, extreme temperature and vibration conditions along with high voltage and manufacturing concerns in along with cost reduction needs. Additionally vehicle packaging and assembly constraints were taken into account. Several design concepts were generated of the electric traction system. Each concept was evaluated through analysis and when necessary bench testing of key elements was performed. Strengths and weaknesses were identified along with cost assessments and reviewed with a program team that included design engineering, manufacturing, test engineering, and suppliers. A design concept was chosen that utilized a printed circuit board centric design. This concept allowed for components to be placed through automation and for more design flexibility for vehicle applications. Detailed design was completed and a Preliminary Design Review was held and then a Critical Design Review. Drawings were then released, parts ordered, and unit build and test started. Tests have been designed to characterize technology and unit performance over the vehicle operating conditions. Electrical, temperature, vibration, motor torque and speed, and efficiency performance will be documented.



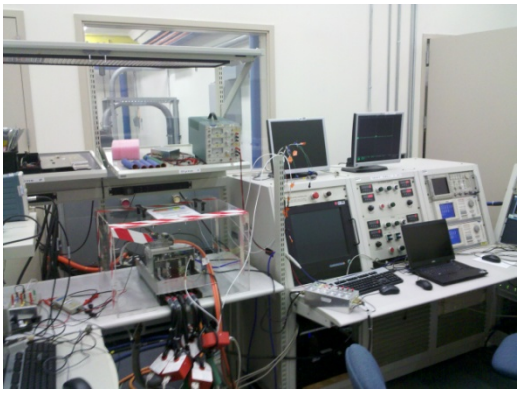
Thermal Analysis



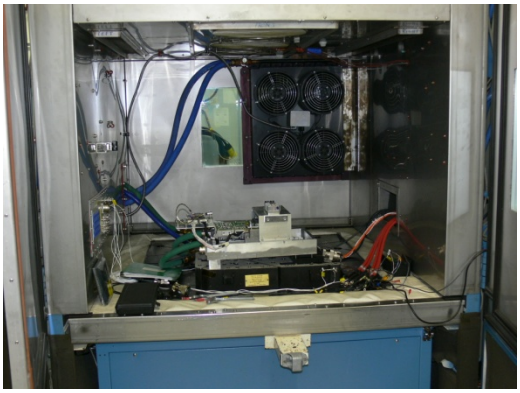
Modal Analysis



Integrated Electric Traction System



Dyne Testing



ESS Inverter Testing

Bi-Directional AC/DC Converter

Electric Range Extend Vehicles and Battery Electric Vehicles provide transportation and societal benefits, but additional consumer benefits can be created. The ability to provide true sinusoidal 120Vac/220Vac electric power from the vehicle battery system would enable the consumer to run any household tools or appliances. Additionally in the future, with the same power electronics, services may be provided to the electric grid to help enable smart grid. These additional benefits will be considerations in the purchase of an EREV or BEV.

The current industry approach is to process energy from grid to the vehicle Electrical Storage system as shown in figure 1. The Charging system is based on two power converters design namely;

- **Front End Boost Converter** which provides power factor correction, low THD and high voltage bus, usually 400VDC.
- **Isolation Buck Converter** which provides galvanic isolation between the grid / ESS and regulates charging voltage and current.

Figure 1 illustrates two stages charging system. Benefits: the two stages can be optimized individually, Drawbacks: Two power stages, less efficiency, not cost effective, unidirectional power flow

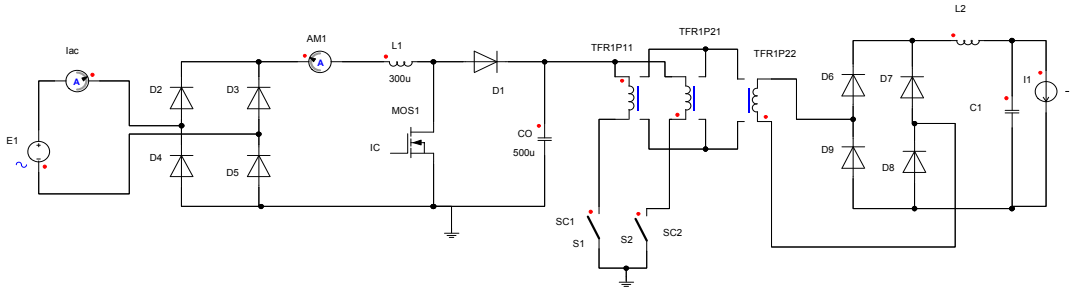


Fig. 1. Industry Current Approach Two Stages Isolated Unity Power Factor Battery Charger

GM Novel Approach: Single Stage Isolated Bidirectional Unity Power Factor Matrix Converter, BMC. The BMC system power topology is illustrated in figure 2.

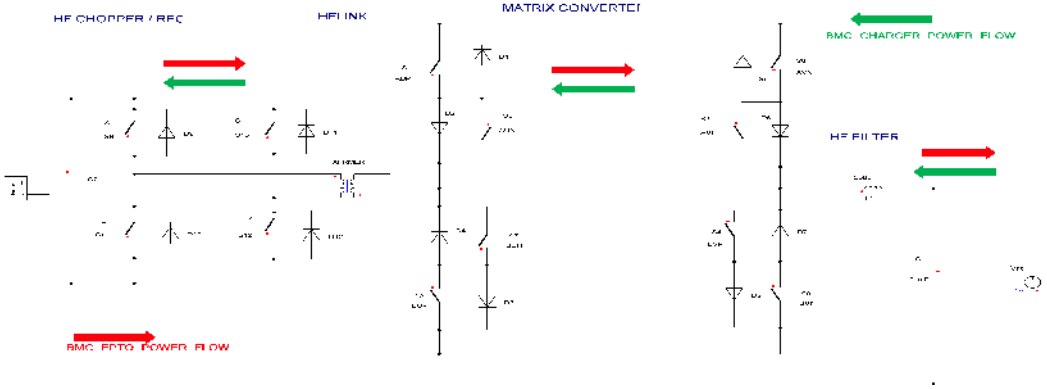


Fig. 2. BMC Power Architecture

General Motors has developed a Bi-Directional Matrix Converter that provides two modes of operation; First Mode is charging, CM. in this mode the BMC processes energy from the grid to charge the vehicle electrical storage system, EES. The second mode is Electrical Power Take off, EPTO. In this mode the BMC processes energy from the ESS to provide AC output power for consumer usages, e.g. home appliances, construction tools, emergency power, ext. Also the converter could be configured to supply

energy from vehicle ESS to the Grid and be integrated in smart grid. It is a building block in smart grid/ green energy applications. The BMC is a single stage 3.3Kw bidirectional isolated unity PFC matrix converter architecture that can be scaled up to a 10kW system

Conclusion

This program directly addresses FreedomCAR program gaps by reducing cost, mass, and volume. An integrated electric traction system has been developed that has taken advantage of advance technology in power modules, capacitors, current sensors, gate drive, and control card. Extensive collaboration between GM, its suppliers, and the National Labs has taken place. While GM's objective was to meet all of DOE's 2015 goals and objectives cost was not meet, but it did meet DOE's 2010.

Publications

Program Kickoff October 30, 2007

PEEM FY'08 Kickoff November 6, 2007

2008 Merit Review February 27, 2008

AIETS Phase 1 Review July 17, 2008

PEEM FY'09 Kickoff November 18, 2008

2009 Merit Review May 22, 2009

PEEM FY'10 Kickoff October 27, 2009

2010 Merit Review June 10, 2010

PEEM FY'11 Kickoff November 17, 2010

Patents

1. Plastic lead frame with distributed-force substrate support
2. Hermetic plastic overmolding of substrate
3. Sensor Mount Assemblies and Sensor Assemblies
4. Three Modes PWM Control Strategy for AC/DC Matrix Converter
5. Electrical System for Pulse-Width Modulated Control of a Power Inverter Using Phase-Shifted Carrier Signals and Related
6. Crossed, overlapped power module bus structure
7. Single fastener, overlapped power module bus structure
8. Charging System with Galvanic Isolation and Multiple Operating Mode
9. Surface Enhancement Utilizing Boundary Layers with Indirect Jet Impingement
10. Systems and Methods for Bi-Directional Energy Delivery with Galvanic Isolation
11. Direct IGBT Die Y-Capacitors to Control Electromagnetic Compatibility
12. Battery Pack Filter to Control Electromagnetic Compatibility
13. Control Algorithm for 2 machines with 1 inverter
14. Boost inverter with 2 machines
15. Dual Leg Inverter Drive System with Anti-polarity Phase Connections
16. Method of Fast Approximation of Peak Summed Fundamental and Third Harmonic Voltages
17. Fractional slot multiphase machines with open slots for simplified conductor insertion in a bar wound
18. Hairpin winding configuration for fractional slot multiphase machines

19. Fractional slot multiphase machines with open slots allow preformed/combined coils insertion from inner diameter, weldings reduction, decrease weldings failure, eliminate weld-end twisting/bending steps, eliminate costly/complex twisting/bending tooling
20. Maximum Voltage usage for Multiphase Machines in Field-weakening region
21. Electromagnetic Interference Filter for Automotive Electrical Systems
22. Power Module Assemblies with Staggered Coolant Channels
23. Integrated, High Performance, Low Inductance Power Inverter Module
24. Groove heat sink to improve power semiconductor module reliability
25. Inverter Gate Drive PCB Inner Core High Current Access
26. Synchronouos Current Regulator for 5-phase Machine with One Faulted Phase
27. Over-modulation Strategy for 5-phase Machine
28. BIOS Extensions to Control Multiple Motors with Single-Motor Application Code
29. PWM strategy to minimize DC-link current ripple
30. Forced Current Commutation Techniques in Isolated Current Fed Matrix Converters
31. Over Modulation PWM compensation
32. Bidirectional Matrix Converter Battery Charger Control Strategy
33. Compensation Strategy for Bidirectional Matrix Converter Nonlinearities
34. Method to Enhance THD and PFC in Single Phase ac/dc Boost Converter
35. Adaptive Compensation Startegy for Bidirectional Matrix Converter Nonlinearities

4.4 Small Business Innovative Research (SBIR) Projects

Principal Investigator: Steven Boyd
Vehicle Technologies Program – DOE Office of Energy Efficiency and Renewable Energy
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DOE Technology Development Manager: Susan A. Rogers
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Objectives

- Use the resources available through the Small Business Innovation Research (SBIR) and Small Business Technology Transfer (STTR) programs to conduct research and development of technologies that can benefit the Advanced Power Electronics and Electric Motors (APEEM) effort within the Vehicle Technologies Program.
- Achieve the four SBIR objectives: (1) to stimulate technological innovation; (2) to increase private sector commercialization of innovations; (3) to use small business to meet federal research and development needs; and (4) to foster and encourage participation by minority and disadvantaged persons in technological innovation.

Approach

- The Small Business Innovation Research (SBIR) program was created in 1982 through the Small Business Innovation Development Act. Eleven federal departments participate in the SBIR program and five departments participate in the STTR program, awarding a total of $2billion to small high-tech businesses.
- A 1982 study found that small businesses had 2.5 times as many innovations per employee as large businesses, while large businesses were nearly three times as likely to receive government assistance. As a result, the SBIR Program was established to provide funding to stimulate technological innovation in small businesses to meet federal agency research and development needs. After more than a decade, the STTR program was launched. The major difference is that STTR projects must involve substantial (at least 30%) cooperative research collaboration between the small business and a non-profit research institution.
- Small Business Innovation Research (SBIR) and Small Business Technology Transfer (STTR) are U.S. Government programs in which federal agencies with large research and development (R&D) budgets set aside a small fraction of their funding for competitions among small businesses only. Small businesses that win awards in these programs keep the rights to any technology developed and are encouraged to commercialize the technology.
- Each year (typically around the beginning of October), DOE issues a solicitation inviting small businesses to apply for SBIR/STTR Phase I grants. It contains technical topics in such research areas as energy production (Fossil, Nuclear, Renewable, and Fusion Energy), Energy Use (in buildings, vehicles, and industry), fundamental energy sciences (materials, life, environmental, and computational sciences, and nuclear and high energy physics), Environmental Management, and Nuclear Nonproliferation. Grant applications submitted by small businesses MUST respond to a specific topic and subtopic during an open solicitation.
- SBIR and STTR have three distinct phases. Phase I explores the feasibility of innovative concepts with awards up to $100,000 for about 9 months. Only Phase I award winners may compete for Phase II, the principal R&D effort, with awards up to $750,000 over a two-year period. There is also a Phase III, in which non-Federal capital is used by the small business to pursue commercial

applications of the R&D. Also under Phase III, Federal agencies may award non-SBIR/STTR-funded, follow-on grants or contracts for products or processes that meet the mission needs of those agencies, or for further R&D.

Phase I Topics for 2010

Subtopics in FY 2010 were included in a single topic for APEEM, detailed below:

6a. High-Performance DC Bus Capacitors for Power Inverters in Electric Drive Vehicles
6b. Alternative Production Techniques for Homogenous Magnet Alloys
6c. High Temperature Packaging
6d. Non Obtrusive Semiconductor Die Temperature Measurements

Phase I Awards Made in 2010

Advanced Film Capacitors for Power Inverters in Electric Drive Vehicles

Strategic Polymer Sciences, Inc.
200 Innovation Blvd, State College, PA 16803

Principal Investigator: Dr. Shihai Zhang, szhang@strategicpolymers.com

Statement of the Problem: Capacitors are critical components in power inverters for electric drive vehicles. Current capacitors have low temperature stability below 105 °C, low energy density below 0.2 J/cc. they occupy ~35% of the inverter volume, contribute to ~23% of the weight, and add ~25% of the cost. They represent a barrier to the reduction of the cost/weight/volume of electric drive vehicles.

Technical Approach: We propose to develop new polymer resin compositions with high dielectric constant, low dissipation factor, and high temperature stability, and low cost.

Commercial Applications and Other Benefits: The advanced film capacitors with high reliability will enable the miniaturization and reduce the cost of EDV power inverters and many power electronic devices. Potential applications include capacitors for hybrid electric vehicles, plug-in electric vehicles, high power strobe lights, defibrillators, and uninterruptable power supplies, and military pulsed power systems.

A Low Cost Continuous Process to Produce Magnet Alloys

Materials & Electrochemical Research (MER) Corporation
7960 S. Kolb Road, Tucson, Arizona 85756

Principal Investigator: Dr. James C. Withers, jcwithers@mercorp.com

Statement of the problem: The current processes to produce Nd-Fe-B alloy powders for producing high magnetic strength permanent magnets for application in electric traction motors for use in electric vehicles requires a significant number of steps resulting in high cost. To meet the cost goals for these motors to expand the availability of electric vehicles, substantial reductions in cost to produce the Nd-Fe-B alloy powders must be achieved.

Technical Approach: Starting from the rare earth oxide Nd2O3 it is possible to produce the alloy Nd2Fe14B which is the highest magnetic strength composition utilizing similar processing that has been

demonstrated to produce high purity low cost titanium alloy powder. A chloride base process utilizes a carbothermically treated oxide to produce an intermediate that fully chlorinates to produce NdCl3 that when combined with FeCl2 and BCl3 can be metallothermically reduced to the alloy powder Nd2Fe14B with a byproduct metal chloride that is readily vacuum separated at a low temperature for recycle to produce the reductant and chlorine for making NdCl3. The only off gas is CO2 as all other reactants are recycled leading to a continuous process to produce high purity Nd2Fe14B alloy powder at low cost.

Commercial Applications and Other Benefits: Substantially reducing the cost and energy in an environmentally friendly process to produce low cost Nd2Fe14B alloy powder provides the material to produce high quality permanent magnets at low cost that translates to producing more electric vehicles. The greater use of electric vehicles reduces pollution, reduces the need for oil/petroleum and the attendant advantages of reduced importing of oil. A greater use of electric vehicles emanating from low cost permanent magnets is a benefit to the entire Nation. The low cost Nb2Fe14B is also applicable for magnets for wind generation of electricity.

Low Thermal Resistance Integrated Package and Heat Sink for HEV IGBT Modules

Advanced Thermal Technologies, LLC
91 South St.
Upton, MA 01568

Principal Investigator: Dr. James Connell, jconnell@charter.net

Statement of the Problem: There is a growing demand for power electronics that can operate under the high temperature and high power conditions that will be encountered in Hybrid Electric Vehicles (HEV). As the coolant temperature used to dissipate heat from electronics increases, the operation of power semiconductor devices such as Insulated Gate Bipolar Transistors (IGBTs) becomes severely limited in order that the safe operating temperature limit of the semiconductor devices not be exceeded. There is a need for high efficiency low-cost heat sink technology to support next generation high power, high reliability HEV IGBT power modules.

Technical Approach: The proposed effort is focused on the development of a unique, high efficiency integrated package and heat sink technology for application to IGBT power modules. The heat sink is enabled by a dielectric-graphite-metal composite material which provides for electrical isolation of the electronic components and circuitry, minimizes the thermal resistance between the electronics and the heat sink fluid and provides CTE matching of the composite material stack-up to minimize thermal stresses resulting from power and temperature cycling. There is a critical need for advanced active cooling solutions with improved thermal properties capable of meeting the thermal management requirements of current and future high power HEV IGBT modules. The research objectives of this project are the development of the design and manufacturing process for the components of the proposed heat sink assembly; and the demonstration of the heat sink's thermal performance. The technology developed in this Phase I research program will enable the cost effective manufacture of a heat sink based upon a dielectric-graphite-metal material that enables thermal management solutions for high HEV IGBT power modules.

Commercial Applications and Other Benefits: The unique dielectric-graphite-metal materials technology will provide lower thermal resistance and thus enable thermal management solutions that improve the operating range and efficiency for a wide variety of power electronic systems. The commercial applications of the proposed package and heat sink technology include IGBTs and MOSFETs used in switching devices; RF power amplifiers used in communication systems; high brightness light emitting diodes used in solid state lighting and power electronics for harsh environment operation.

Nanomaterials for High Performance Thermal Packaging

Applied Nanotech, Inc.
3006 Longhorn Blvd., Suite 107
Austin, TX 78758

Principal Investigator: Dr. James P. Novak, jnovak@appliednanotech.net

Statement of the Problem: Modern electrical systems operate with high power consumption and as a result of the power dissipation generate much heat that can damage components and limit application lifetime. Even with the specialty materials currently used in both the electronic package as well as the mounting buss for heat dissipation, most systems still require additional cooling mechanisms. ANI proposes adaptation of a high thermal conductivity carbon aluminum composite and a Cu nanoparticle based solder to generate next generation high thermal capacity electronic packaging which will reduce or eliminate the need for external cooling loops. This new material is expected to show increased performance over traditional direct bonded copper substrates. Successful development of our novel thermal management solution will provide increased options for power electronics and overall thermal management solutions.

Phase II Topics for 2010

Under the SBIR/STTR process, companies with Phase I awards from FY 2009 are eligible to apply for a Phase II award in FY 2010. The FY 2009 Phase I subtopics were:

24a. Eddy Current Loss Calculation
24b. High-Power-Density, Non-Permanent-Magnet, Electric Motor Development for Hybrid, Plug-in Hybrid, and Fuel Cell Vehicles
24c. High Temperature Packaging
24d. Development of an Accelerated Life Test for HEV/PHEV Power Modules

Phase II Awards Made in 2010

Six Phase I awards were made in FY 2009 as Phase I projects, and resulted in the following Phase II award for FY 2010.

High-temperature Packaging of Planar Power Modules by Low-temperature Sintering of Nanoscale Silver Paste

NBE Technologies, LLC
2200 Kraft Drive, Suite 1425, Blacksburg VA 24061

Principal Investigator: Dr. Susan Luo, sluo@nbetech.com
Primary Contact: Dr. Guo-Quan Lu, gqlu@nbetech.com

Statement of the Problem: This proposal addresses the Department of Energy's need for high temperature packaging technologies to help automotive manufacturers to reduce costs of hybrid electric vehicles and future plug-in hybrid electric vehicles. A specific technology barrier to be removed calls for the development of a new die-attach method for joining power semiconductor chips. This die-attach technology is necessary to make double-side cooled power modules working reliably at high temperatures to meet the challenge of 105oC inlet coolant that is risen from the need to eliminate extra cooling loops in future electric vehicles.

Technical Approach: An emerging lead-free die-attach solution, termed low-temperature joining technology by silver sintering, will be introduced for making high temperature power modules. And, the small business's nanoscale silver paste technology will be used to greatly simplify the joining technology's implementation for fabricating planar, double-side cooled power modules.

What was done in Phase I: The small business's nanomaterial was successfully demonstrated as an enabling technology for making planar, double-side cooled power modules. The module was shown to be operational at chip junction temperatures over 175oC. Other testing results show that the nanosilver sintered joints are thermally better in heat dissipation and more reliable than their soldered counterparts.

What is planned for Phase II: Research activities of the Phase-I program will be expanded to include design, selection, and testing of substrate and encapsulation materials for making high-temperature planar, double-side cooled power modules. Multiple power modules will be fabricated and integrated with gate-driver electronics to construct inverters rated for a typical electric vehicle. Demonstration and testing results of the inverters will be used to guide the Phase III effort for manufacturing high-temperature inverters or converters in future electric vehicles.

Commercial Applications and Other Benefits: The United States' automakers would directly benefit from the successful completions of this Phase II program on the high-temperature packaging technologies. The cutting-edge technologies would provide them competitive advantage to offer consumers cost-effective, fuel-efficient vehicles. This, in turn, will help reduce the nation's reliance on petroleum and petroleum imports and decrease carbon emissions. Furthermore, the successes would allow this small business to rapidly grow its business by marketing its nanomaterial products to the auto industry. In so doing, it would create significant number of high-tech jobs for the region of Southwest Virginia which has been suffering extreme economic hardship.

Phase III Topics for 2010

DOE released a funding opportunity announcement for its Phase III program entitled "The DOE FY2010 Phase III Xlerator Program for Energy Efficiency and Renewable Energy, Electricity Delivery and Energy Reliability, Fossil Energy, and Nuclear Energy" on July 9, 2010. Only DOE SBIR or STTR Phase I and Phase II grantees from FY 2005 to FY 2009 were eligible to apply to this announcement. The APEEM program listed two subtopics under the Vehicle Technologies topic:

1. Technologies to Address Internal Heating in DC Bus Capacitors
2. Improved Magnetic Materials for Motors

Phase III Awards Made in 2010

Two Phase III awards were made in FY2010 as Phase III projects described below.

High Performance Permanent Magnets for Advanced Motors

Electron Energy Corporation
924 Links Ave, Landisville PA 17538

Principal Investigator: Jinfang Liu, jfl@electronenergy.com

Statement of the Problem: This proposal addresses the interest in developing new permanent magnets, to improve the performance of advanced motors for hybrid electric vehicles.

Technical Approach: The overall objective of this program is to develop high performance permanent magnets with improved magnetic properties at temperatures up to 240oC, high electrical resistivity to reduce eddy current losses in advanced motor applications, and low cost.

What was done previously: In the phase I and Phase II effort, we successfully prepared samples in the lab with high resistivity and high magnetic performance. The approaches comprised of compositional and process optimization, such as atomic substitutions and additions in conjunction with process parameter optimization to yield the highest magnetic properties, and the use of dielectric constituents to increase the electrical resistivity. The research was extended to both Sm-Co and Nd-Fe-B rare earth permanent magnets. EEC has filed two patents applications on related technologies so far.

What is planned for Phase III: The Phase III effort will be dedicated to further optimization of the identified feasible approaches, development of standard grades of high resistivity magnets, pilot production and beta site testing. Cost reduction will be addressed by further development of automated production processes. Moreover, the dielectric constituents of the new *composite / hybrid* magnets as well as the simple fabrication process will also contribute to achieving the goal of more affordable high-performance magnets. The Phase III effort will be focused on exploring opportunities to commercialize the high resistivity and high performance magnets developed in this program. Beta site testing will provide much needed data to show the reduction of eddy current and increase of motor efficiency.

Commercial Applications and Other Benefits: If this program is successfully completed, it will have significant impact on hybrid vehicle markets as well as wind energy industries. It will also re-vitalize the U.S. manufacturing base in permanent magnets, which is currently dominated by China and Japan.

Compact High Temperature DC Bus Capacitors for Electric Vehicles
Using High Performance Electroactive Polymers

Strategic Polymer Sciences, Inc.
200 Innovation Blvd. Suite 237, State College PA 16803

Principal Investigator: Shihai Zhang, szhang@strategicpolymers.com

Statement of the Problem: Power electronics are a key technology for hybrid and plug-in electric drive vehicles (EDV) and represent 20% of the material costs. DC bus capacitors are one of the critical components in EDV power inverters and they can occupy ~35% of the inverter volume, contribute to ~23% of the weight, and add ~25% of the cost. Current polypropylene (PP) film capacitors cannot be reliably operated above 105°C and an additional cooling system must be added to cool down the capacitors.

Technical Approach: We propose to develop compact film capacitors with high dielectric constant and high temperature stability using our proprietary electroactive polymer dielectric compositions. The capacitors will be able to operate at above 140°C with a size that is more than 60% smaller than current PP DC bus capacitors.

What was done previously: We have developed electroactive polymer dielectric compositions with dielectric constant above 5 and melting temperature above 240 □C. We have also accumulated unique experience in producing ultrathin free-standing polymer capacitor film with thickness down to 2 μm using inexpensive melt process.

What is planned for Phase III: We plan to develop advanced compact DC bus film capacitors for electric vehicle power inverters using novel electroactive polymer dielectric compositions with high temperature

stability (>140°C), high dielectric constant, low dielectric loss tangent, low leakage current. Prototype capacitors will be developed for customer test at technology readiness level 7 (System/subsystem model or prototype demonstration in a relevant environment). The EAP film capacitors will meet the DOE FreedomCAR targets and enable significant reduction in EV power inverter size and cost.

Commercial Applications and Other Benefits: The ultrahigh energy density film capacitors with high reliability and high temperature stability will enable the miniaturization of many power electronic devices. Potential applications include DC capacitors for hybrid electric vehicles, grid-tied photovoltaics, wind turbine generators, and motor control systems.

4.5 Technology and Market Intelligence Regarding:

- **Wide Bandgap Semiconductors: A Case For and Against Silicon Carbide for Automotive Applications**
- **Recycling of Automotive Motors, Power Electronics and Rare Earths**
- **Rare Earth Market Update**

Principal Investigators:Christopher Whaling, Frank Williams and Richard Holcomb
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Objectives

Synthesis Partners was tasked by the Department of Energy (DOE) Vehicle Technologies Program to collect, integrate, and analyze open source technology and market research information to assess specific questions in three fields:
1) Wide Bandgap Semiconductors (SiC)
2) Recycling of Automotive Motors, Power Electronics and Rare Earths
3) Rare Earth Markets and R&D

In addition, Synthesis began the first phase of framing an HEV Power Inverter Cost Analysis study. This initial work focused on developing requirements with Steven Boyd of DOE, collecting background information from commercial and government sources on power inverter cost drivers, and identifying primary sources for follow-up interviews. There were no reports issued by Synthesis on this topic in FY10.

Regarding Wide Bandgap Semiconductors (WBGS): A Case For and Against Silicon Carbide for Automotive Applications (June 2010), Synthesis addressed:

- Current WBGS technology R&D activities relevant to automotive power semiconductors
- Near-military specifications at significantly lower costs
- WBGS commercial R&D and developments relevant to devices with the following characteristics:
  - 600-1200 V
  - 5-20 A or higher if possible, up to ~70 A
  - 200-300°C operating temperatures
  - Large wafer sizes preferred for lower cost

Regarding Recycling of Automotive Motors, Power Electronics and Rare Earths (June 2010), Synthesis addressed:

- The nature of emerging trends in automotive recycling and related market sectors
- Automotive recycling approaches under consideration or being implemented
- Emerging potentially successful economic and business models for automotive recycling

- Potentially promising disruptive game-changers for automotive recycling, including new approaches and technologies, and
- Barriers to the implementation of current and emerging approaches and technologies in the US market, including economic, regulatory, and others

Regarding Rare Earth (RE) Markets and R&D (July 2010), Synthesis addressed:

- Developments in RE markets
- Developments in RE minerals exploration, mining, processing and refining
- Developments in RE magnet production
- Developments in RE-materials substitution
- Recent US legislative and government actions.

The information in this RE Market Update is provided in an outline format. This targeted research followed Synthesis' detailed Rare Earth Materials and Rare Earth Magnets report, issued in August 2009.

Approach

Synthesis employed targeted and responsive research methodologies under this tasking to access a range of secondary and primary sources during the October 2009 to September 2010 timeframe. These efforts led to the production of three published reports and several briefings, each of which provided key findings, as well as information on key sources identified. At each briefing Synthesis sought questions, feedback, and guidance concerning refinements of the research.

Deliverables (Major Accomplishments)

Synthesis delivered three concise written reports and several oral briefings on same under this Task. The reports are entitled:

- Wide Bandgap Semiconductors: A Case For and Against Silicon Carbide for Automotive Applications (June 2010)
- Recycling of Automotive Motors, Power Electronics and Rare Earths (June 2010)
- Rare Earth Market Update (July 2010)

Future Direction

Synthesis' FY11 efforts are primarily focused on a HEV Power Inverter Cost Analysis study. Other technology and market research topics are under consideration by DOE. Synthesis anticipates beginning work in an additional field in the latter half of FY11.

The HEV Power Inverter Cost Analysis will address the main drivers of the cost of both key components and system-level configurations of the HEV power inverter. In-depth interviews, secondary sources, and case-based analytical approaches will be used to provide a detailed assessment of the present cost-of-production baseline for power inverters and their components. Using that baseline as a starting point, Synthesis will assess current costs and cost-drivers and will also work to identify plausible future approaches to reducing costs in the design and manufacturing of power inverters. The goal is to identify, characterize, and report on methods with the potential of achieving greater than 20% cost reductions in power inverters.

Primary and secondary source collection is on-going, and employs Synthesis' expert approach to leveraging commercial, government, non-profit and proprietary databases of sources worldwide.

Synthesis is also providing targeted assistance with literature search activities in support of the AMES Beyond-Rare Earth Magnets (BREM) initiative.

Technical Discussion

The published market research reports produced the following selected key findings. Please see the reports for more detailed findings, information on sources, and additional market projections.

1. Wide Bandgap Semiconductors (SiC): A Case For and Against Silicon Carbide for Automotive Applications
2. Recycling of Automotive Motors, Power Electronics and Rare Earths
3. Rare Earth Markets and R&D

WBGS Report: A Case For and Against SiC for Automotive Applications (June 2010)

This research was conducted during the November 2009 through February 2010 timeframe.

Key Findings:

- While the experts disagree on the SiC – Si cost differential at which SiC components will begin to be adopted by the automotive industry, they all agree that the cost of SiC and relatively limited supply of SiC are the prime reasons for the continuing use of Si.
- At current market prices, using SiC is cost-prohibitive in mass-produced vehicles. However, with improvements in manufacturing processes and increased demand leading to volume production, the cost could drop enough within the next 3 - 5 years to make SiC a viable alternative to Si. For this to come to pass, the price of SiC components would need to be reduced to only a small premium (e.g., 20-30%) over Si components. However, one key source (Friedrichs, Peter et al, eds.: Silicon Carbide, 2010, Chapter 1, p. 12), concerning Toyota written by Kiminori Hamada of Toyota's Electrical Engineering Division, states: "[I]t must be understood that despite these superior material properties, SiC has little chance of being used unless it can be obtained at a cost that is the same as or lower than that of Si, which currently dominates nearly all semiconductor applications for rational economic reasons."
- At the current rate of development it will be at least five years before SiC MOSFET prices are low enough to interest automakers in replacing Si devices in large volumes.
- Above 2000V, “there is no competition for SiC, and this will be its sweet-spot.”, according to Abas Goodarzi of US Hybrid Corporation.
- SiC power modules will not be useful for any automotive applications below 500V.
- Japanese government agencies, automakers and associated industry partners are actively pursuing SiC technology developments.
- In May 2010, the Japanese Ministry of Economy, Trade and Industry (METI) announced the start of the "New Material Power Semiconductor Device Project Toward Achieving a Low-Carbon Society" (budget for FY 2010: 2 billion yen, or approx. $22.6 million). The project includes the expansion of the R&D Partnership for Future Power Electronics Technology (FUPET) and the establishment of the SiC Alliance. FUPET and the SiC Alliance “will play important roles in promoting SiC research and development and introducing SiC to society,” according to reports. METI is clearly actively supporting research towards practical applications of SiC.
- Japanese automakers are currently using a variety of substrate materials, including SiC, to work on power modules in the 1200V range and may be pushing beyond it. For example, Nissan claimed to have developed the world's first inverter using SiC diodes for vehicle use in September 2008, and implemented it in the XTRAIL FCV (Fuel Cell Vehicle). Mitsubishi is actively pursuing SiC

technology R&D for their HEV/EVs, and Honda/ROHM appears poised to bring a SiC power module to the market.

- Bridgestone Corporation of Tokyo (the world's largest tire and rubber company), commenced production of silicon carbide wafers in 2010. It is reported that the PureBeta™ SiC Single Crystal Wafer being produced by Bridgestone extends the company's experience in using polymer technology and nanotechnology in developing tires.
- As currently implemented, Si power modules perform effectively due to a dedicated cooling system. There are no indications that eliminating this cooling loop will increase efficiency or reduce weight of current designs. However, as manufacturers design future automobiles, SiC provides an alternative to employing these dedicated cooling systems and will allow greater weight reduction with more efficient packaging and placement of components.
- While a Si-only solution could provide an approach to handling increased operating temperatures, the penalties of increased size and weight do not make it an optimum solution. In the long-run, alternative technology approaches, including SiC, are anticipated.
- At current market prices, eliminating the secondary cooling loop does not compensate for the increased cost of SiC. Realizing the full benefits of SiC, including higher operating temperatures and weight savings, will involve redesigning the vehicle to take advantage of the characteristics of SiC components. A detailed assessment of the implications of these changes at the system level has not been identified in the public domain.
- Using a hybrid Si MOSFET/IGBT-SiC diode device may provide an entry point for SiC, allowing increased production which should lead to lower costs. However, there is debate regarding the technical merits of transitioning from Si-SiC devices to an all-SiC device.
- While the American automakers do not appear to be interested in using voltages above the 600V-700V range, the Japanese manufacturers are working in that direction. This is one of the primary reasons they are interested in wide bandgap materials.
- Most indicators point to SiC as the best wide bandgap material for use in hybrid vehicle power electronics. However, Toyota is pursuing GaN as an alternative to Si. It is possible, though no evidence was found to confirm, that Toyota is developing a breakthrough technology which would allow cost-competitive production of GaN devices.
- US HEV sales are not sufficient to drive automotive OEMs to transition to SiC at this time. Thus, it appears that OEMs will need to consider the both HEV and non-HEV vehicle sales to achieve the necessary economies-of-scale to drive SiC costs to a competitive premium over the costs of Si.
- The current state of demand for SiC MOSFETS is a chicken-and-egg challenge: Dramatic reductions in the cost of SiC MOSFETS for automotive applications depend on large-volume production runs. However, without the high volumes, producers can't achieve the price-points required by automotive users. Automotive applications are particularly demanding, with a low-to-zero tolerance for price premiums.
- Non-automotive industries (e.g., wind, solar, and civilian/military aerospace applications) will drive SiC production growth over the next several years.
- SiC's adoption in the automotive sector will also be affected by other factors outside the automakers' control, such as efficiency and emission mandates.

Recycling of Automotive Motors, Power Electronics and Rare Earths (June 2010)

This research was conducted during the October through December 2009 timeframe.

Key Findings:

- A recurring theme discovered among sources addressing recycling of hybrid vehicles is that there are too few hybrid or electric vehicles on the road to justify investment in specific technologies, processes, or guidelines for recycling them.
- While Ford and General Motors have subsidiaries and partners in Europe and Japan, their American operations do not seem to be closely linked in with the efforts in those regions toward improving vehicle recyclability, according to comments from the Automotive Recyclers Association (ARA) and Institute of Scrap Recycling Industries (ISRI).
- Synthesis did not find that any of the organizations which oversee or govern the automotive or electronics recycling industries in the US have made clear efforts toward addressing the recycling of hybrid vehicle components, other than the batteries.
- As hybrid vehicles increase in numbers and begin entering the recycling stream, it may be necessary for regulators and professional organizations to take an active role and set incentives to treat hybrids and electric vehicles differently from conventional vehicles, if the goal is to recapture the materials used in the motors and power electronics.
- The ARA and the National Center for Electronics Recycling are apparently not aware of one another's efforts, but that both expressed interest in taking action on hybrid vehicle component recycling.
- The recycling industry in the US is based on a business model which is at least twenty years old, as it is designed to address the age of automobiles that are typically recycled (approximately 20 years old). Their business model will inevitably change to reflect the significant increase in recoverable electronic materials and other technologies contained in hybrid and electric-drive vehicles.
- Synthesis assesses that there may be an emerging market opportunity for recycling automobile power electronics. We assess that the total value of automobile power electronics otherwise discarded as part of the ASR (automotive shredder residue) will be in the range of $700M to $3.5B over the past ten years. Furthermore, as the number and complexity of automobile electrical systems increase, this market opportunity will grow, possibly producing up to $7B in revenues over the next ten years.
- In a notable market development regarding rare earth magnet recycling, it was reported by the organization Japan for Sustainability (www.japanfs.org) in May 2010 that Hitachi has launched a project to develop rare earth magnet recycling technologies. According to the report, Hitachi is developing devices to recover rare earth magnets from motors, will explore technologies for recycling used magnets and plans to launch a business in these fields in 2013.
- As indicated by the Hitachi report, market-driven activity has a high likelihood of driving significant new developments in the recycling automotive electronics industry, and will likely transform the current industry landscape over the next five years.
- Significant factors argue for the sparing use of rare earth magnets in electric motors over the next five years from a recycling and material reclamation perspective (though, as Hitachi developments suggest, there are innovative approaches being developed to address these constraints), including:
  - The difficulty in mechanically separating magnets from the motors
  - The difficulty of separating the electric motors from the transmissions and other car systems),
  - The complexity of recycling magnetic materials and/or their constituent materials, and
  - The lack of near-term market for the re-use of magnets.

Rare Earth Market Update (July 2010)

The research was conducted during the April through June 2010 timeframe.

Synthesis Partners conducted rapid secondary and primary source research on the rare earth mining and magnetic sectors and reported the results in outline form. The collection effort leveraged the primary source contacts and secondary sources developed by Synthesis and DOE in the course of prior RE market research.

In terms of primary source contacts, the following table depicts the key companies, industry associations and industry consultants contacted in the course of our research.

Table 1: Primary Contacts

Source	Contact
Companies	
Adams Magnetic Products	Jack Powell
Arafura	Alistair Stephens
Avalon Ventures	Ian London
Electrodyne	Kevin Cook
Electron Energy Corp.	Peter Dent
Hitachi Metals	Brian Brilinski
J.A. Green & Co.	Jeff Green
Jack Lifton, LLC	Jack Lifton
Less Common Metals	David Kennedy
Lynas Corporation	Dr. Matthew James
Magnet Applications	Dr. James Bell
Molycorp	Mark Smith
Thomas & Skinner	Ed Richardson
UQM Technologies	Jon Lutz
Walt Benecki LLC	Walt Benecki
Wings Enterprises, Inc	Jim Kennedy
Associations	
U.K. Magnetics Society	J. Ward
Rare Earth Industry and Technology Association	Keith Delaney
Rare Earth Magnetics Association	

The Rare Earth Market Update includes information and analysis on the following North American and Australian companies and activities:

- Rare Earth Exploration
  - American Companies
  - Canadian Companies
  - Australian Companies
- Rare Earth Mining/Processing (ore/rare earth oxide production)
  - American Companies
  - Australian Companies
- Rare Earth Refining (processes ore/oxide into metal)
  - American Companies
  - Canadian Companies
  - Australian Companies
- Rare Earth Magnetic Material Producers
  - American Companies
  - Canadian Companies

- Rare Earth Magnet Producers
  - American Companies
  - Canadian Companies
- Rare Earth/Magnetics Organizations in the US

The RE update also includes information on the Chinese RE industry. Selected information included in the brief report includes:

- The Chinese rare earth industry is undergoing consolidation as large companies merge and buy out smaller companies. Development plans from The National Development and Reform Commission show a reduction to fewer than 20 refiners by 2020.
- One goal of the industry consolidation is to stabilize prices, as competition between producers resulted in "unreasonably low" prices of exports. Since 1990, China's rare earth exports have grown nine-fold while the price has dropped by 36 percent. China is cutting this year's exports by 8.1 percent, to 31,300 tons. Future plans call for capping exports at 35,000 tons per year in 2010 to 2015. Twenty-five percent of China's rare earth exports go to the US and 50 percent to Japan.
- The global economic slump has hit the Chinese rare earth industry hard. Over the past 10 years Bayan Obo of Inner Mongolia has supplied about 80 percent of the world's rare earth materials. The rare earth industry in this region was at its peak in 2008, with an industrial output value reaching 9.88 billion Yuan ($1.48 billion) and export volume totaling $131.3 million. However during first quarter of 2010, sales revenues totaled 375 million Yuan – a 47 percent drop from the same period last year. Its losses exceeded 78 million Yuan, and export volumes dropped more than 70 percent.
- The world's largest research institute for the industry, Baotou Research Institute of Rare Earth, initiated seven projects applying new refining technologies at a cost of 1.34 billion Yuan in 2008. They predict that, when the technological applications are all realized, the industry's annual output will reach 4.17 billion Yuan.
- Exploration outside of China has changed the RE picture. In the 1990s, China held 88 percent of the world's known rare earth reserves. That dropped to 52 percent in 2008. Zhou Hongyu, a deputy to the National People's Congress, stated, "At the present rate of mining, China will have no rare earth to mine in the next 20 or 30 years, and then we will have to import rare earth at great cost." Note that he is referring to mining, not rare earth production. Refining the ore could take years beyond the point at which mines are exhausted.
- A report titled 2008 Report on China's Magnetic Material Market states: "There are now 1,096 magnetic materials producers in China, of which 359 focus on ferrite, 226 on rare-earth and metallic magnets, with the rest producing associated equipment and auxiliary raw materials." The report was published in January 2009.
- Xu Guangxian, a 90-year-old chemist with Peking University, known as China's "father of rare-earth", suggested that China should "establish a national reserve system for rare-earth." China's Ministry of Industry and Information Technology (MIIT) has approved Inner Mongolia Baotou Steel Rare-earth (Group) Hi-tech Co., Ltd to carry out a rare-earth strategic reserve program. The company will build 10 rare-earth oxide reserve projects with over 200,000 tons of total capacity.
- In late May 2010, China announced it will tighten controls over mining rare earth minerals. According to a report in the *New York Times*, China's State Council "is weighing a proposal to put the government in control of private and unauthorized mines that produce rare earth minerals." While some companies and governments have expressed concern that this is a move to tighten China's control on the rare earth industry, in June 2010 Chinese officials said they are tightening control "because the mining has led to environmental ruin and chaotic development."

Chinese Rare Earth companies of interest include:

- China Minmetals Non-Ferrous Metals Co.
  - Expects to "become the largest global rare earth enterprise in the next five years."
  - In February 2009, the company listed its processing capacity at 8,500 tonnes. According to the company's plan, when the company is listed on the stock market in three to five years, the capacity will reach 13,500 tonnes.
  - In February 2010 Zhou Zhongshu, president of Minmetals, said "We aim to be the world's largest rare earth supplier."
- HEFA Rare Earth Canada Co. Ltd.
  - North American subsidiary of Baotou HEFA Rare Earth, "one of the world's largest and most experienced producers."
  - Owns five rare earth processing factories with 5000+ metric ton rare earth oxide production capacity
- Inner Mongolia Baotou Steel Rare-Earth Hi-Tech Co., Ltd
  - Taking over smaller rivals in Inner Mongolia to consolidate rare earth operations into one company
- Tianjiao International
  - American supplier for products from Baotou manufacturers

Chinese institutes and societies focused on rare earths include:

- Baotou Research Institute of Rare Earth
  - The largest rare earth research and development institution in China; "focuses on the comprehensive exploitation and utilization of rare earth resources and the researches on rare earth metallurgy, environmental protection, new rare earth functional materials, rare earth applications in traditional industry."
  - Owned by Baotou Iron & Steel.
- The Chinese Society of Rare Earths
  - A rare earth science and technology organization. Claims more than 100,000 registered experts, which would make it the biggest academic community on rare earth in the world.
  - No news updates, articles or research updates have been published to their web site since 2006.

Conclusions

Each market research study provides the results of the research, analysis, and important context for interpretation of the data. Please note that the information developed by Synthesis is based on information available at the time of the research.

Publications

Please see published reports.

References

Please see published reports.

Patents

None

5.0 Thermal Management Research and Technology Development

5.1 Air-Cooling Technology for Power Electronics

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Objectives

The overall project objective is to develop and apply air-cooling technology to improve power electronics thermal control design and influence industry, enhancing system performance to meet FreedomCAR technical targets for weight, volume, cost, and reliability. This overall objective includes the following:

- Develop and demonstrate commercially viable, low-cost air-cooling solutions for a range of vehicle applications and assess their potential for reducing the cost and complexity of the power electronics cooling system.
- Enable long-term goal of elimination of liquid coolant loop.
- Reduce cost, weight, and volume of the power electronics system.
- FY 10 Objectives:
  - Develop system-level analysis approach to match cooling technology, package mechanical design, and balance of system with vehicle applications.
  - Investigate advanced air-cooling heat transfer technologies.
  - Develop experimental and analytical capabilities to enable advanced heat transfer technology research.
  - Establish and strengthen collaboration with industry, university, and national laboratory partners.

Approach

- Use a system-level approach that addresses the cooling technology, package mechanical design, balance of system, and vehicle application requirements.
- Research each of these areas in depth and apply findings to develop effective system-level designs.
- Develop experimental and analytical/numerical tools and processes that facilitate high quality and rapid research results.
- Work closely with industry, university, and national laboratory partners to ensure relevant and viable solutions.

Major Accomplishments

- Developed system-level modeling approach that accounts for the interactions of cooling technology, package mechanical design, balance of system, and the vehicle application. Applied this approach to example charging applications and showed the feasibility of air-cooling.

- Developed the Air-Cooling Technology Characterization Platform for researching single-target fundamental heat transfer of air-cooling technologies. This includes a high-accuracy, constant-temperature anemometry system and calibrator for quantifying flow behavior.
- Investigated steady and synthetic jets. Demonstrated that synthetic jets can have equal or better performance compared to steady jets without the complexity of ducting and a remote prime mover.
- Developed computational fluid dynamics models which capture the important flow structures.
- Established industry collaborations
  - Oak Ridge National Laboratory (ORNL) – Established collaboration plan with ORNL to develop needed thermal system knowledge for a FY12 high temperature inverter project.
  - GE Global Research – Air jet heat transfer research collaboration.
  - Momentive Advanced Materials – Recently established for FY11 to look at advanced materials for air-cooling.

Future Direction

- Develop promising advanced air-cooling technologies at the single-target level and begin applying them to the system-level.
- Characterize effect of different heat spreaders and enhanced surfaces on air-cooling.
- Match air-cooling technologies to appropriate vehicle applications and develop understanding of the system-level design trade-offs.
- Analyze and improve efficiency of balance of system technologies for air-cooling (e.g., fans, ducting, filters).
- Continue to work with industry partners to develop relevant and viable solutions.
- Complete heat transfer foundational work for FY12 high-temperature, air-cooled inverter project with ORNL.

Technical Discussion

Approach

The objective of NREL's Air-Cooling Technology for Power Electronics Thermal Management project is to assess, develop, and apply air-cooling technology to improve power electronics thermal control design and influence industry's products; thereby enhancing system performance to meet FreedomCAR technical targets for weight, volume, cost, and reliability. With the notable exception of the low-power Honda Insight, commercially available hybrid vehicles use liquid-cooled power electronic systems. All the heat from a vehicle, however, must ultimately be rejected to air. For liquid-cooled systems, heat from the power electronics is transferred to a water-ethylene glycol coolant via a heat exchanger and then pumped to a separate, remote liquid-to-air radiator where the heat is rejected to air. This research effort seeks to develop the necessary heat transfer technology and system-level understanding to eliminate the intermediate liquid-cooling loop and transfer heat directly to the air. The relative merits of air-cooled high-heat-flux automotive power electronic thermal management systems will be quantified, evaluated, and demonstrated under steady state and transient conditions.

Effectively and viably accomplishing these goals requires an air-cooled system thermal design understanding and approach. As shown in Fig. 3, this project will analytically and experimentally address each aspect of the system: heat transfer cooling technology, power electronics package thermal design, balance of system (prime movers, ducting, etc.), and their interconnected interactions. It is also critical to account for and understand the effects of constraints and inputs into the air-cooled thermal management system: thermal environment, device type, and vehicle context. The thermal environment constraints have a direct impact on the driving temperature difference available for air-cooled heat transfer and can vary depending on design targets and system location in a vehicle. Under-hood temperatures are approximately 100°C –140°C and are therefore unsuitable for cooling. External ambient air at 30°C – 45°C is highly suitable for cooling, and some additional benefit can be gained from using cabin air, but it

must be balanced with the added parasitic load. The device type will determine both the maximum junction temperature and efficiency and thus influences the maximum allowable package surface temperature and heat load. Advanced power semiconductors, such as silicon carbide and gallium nitride, have the potential to greatly expand the air-cooling feasibility range by increasing the allowable junction temperature from 125°C to 200°C or higher while possibly improving efficiency. Vehicle context determines the power electronics duty cycle, affecting the total heat rejection needs and also imposing constraints on the system volume and weight. Understanding the in-vehicle demands on the power electronics systems will allow for modulated designs to meet cooling needs, reducing system overdesign and minimizing parasitic losses.

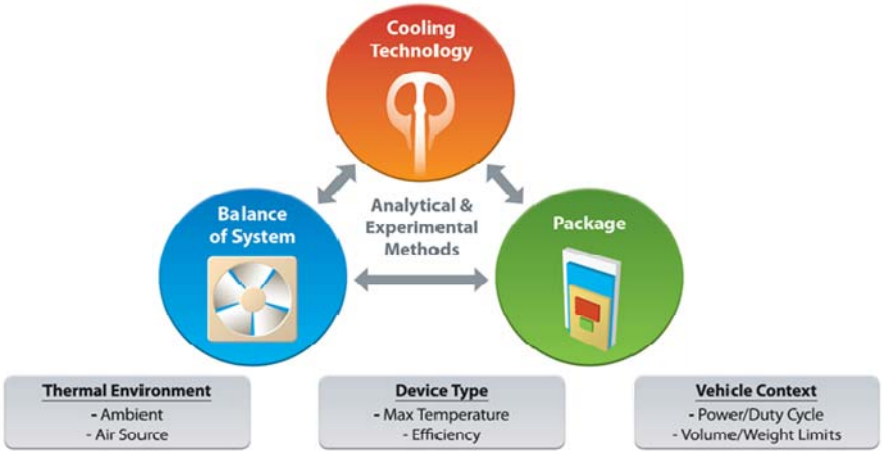

Fig. 3. Power electronics air-cooled thermal management system research and design approach

To move ideas from concept to implementation, four levels of research, development, and demonstration will be used: novel cooling technology fundamental heat transfer, system-level heat transfer and balance of system, inverter-level application, and vehicle-level demonstration with partners (Fig. 4). This process will both ensure that each level of complexity assists in achieving the overall objectives and will serve to screen ideas so that only the best approaches pass to the next level.

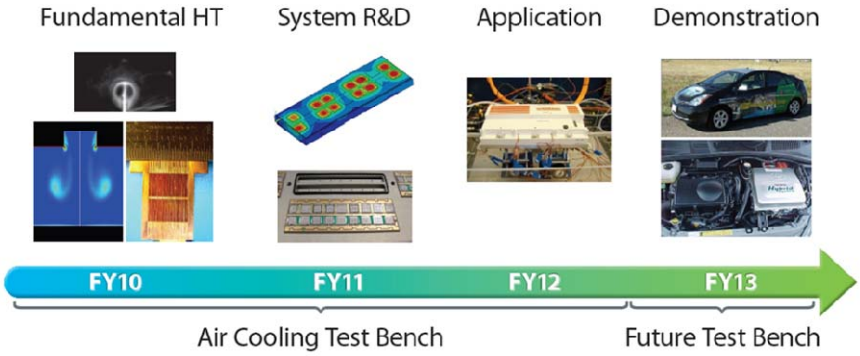

Fig. 4. Air-cooling system research, development, and demonstration approach

System-Level Analysis

A high-level system analysis software program was developed in MATLAB to capture interactions of the three thermal management system components and their inputs from Fig. 3. This tool can be used to explore the design space and match cooling technology, thermal package designs, and the balance of system with vehicle application requirements. These results will relate high-level Advanced Power Electronics and Electric Motors (APEEM) specification goals or targets to thermal management system

improvements. Fig. 5 provides a high-level overview of the system analysis program inputs, calculation models, and outputs. Further details regarding the cooling technology model, balance of system, and package mechanical design can be found in their respective sections of this report. Additional information on the overall process and application specification can be found in the Thermal Control of PHEV/EV Charging Systems report.

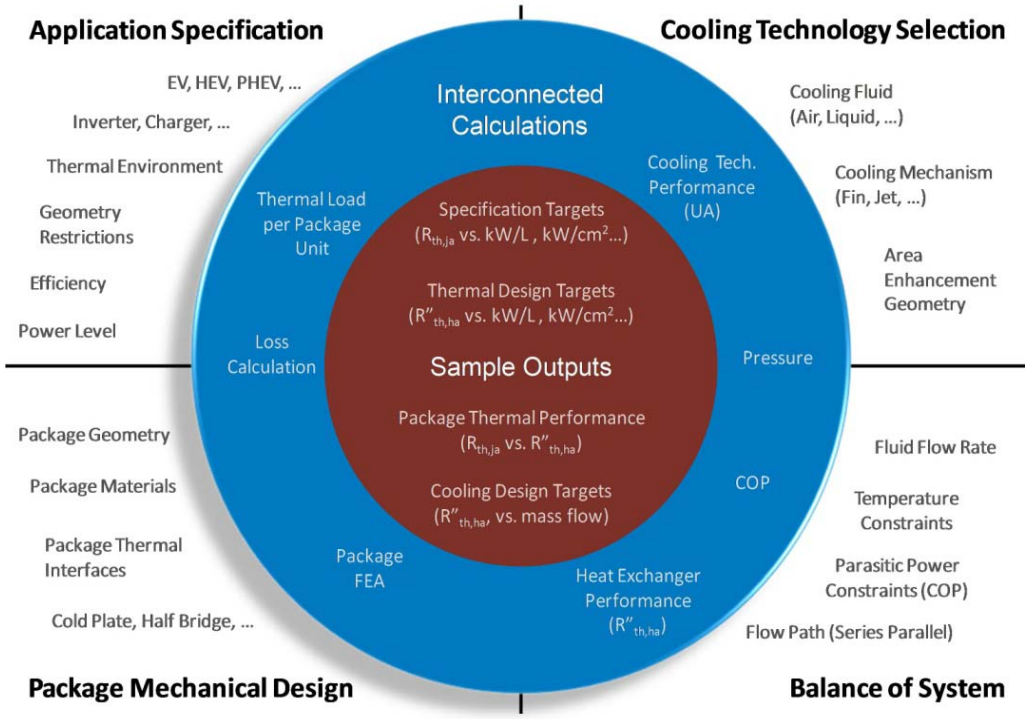

Fig. 5. Power electronics system analysis parameter overview

As a case study, this model was applied to two air-cooled plug-in hybrid electric vehicle (PHEV) and electric vehicle (EV) charging applications: a general cold plate and a DC-DC converter. The goal was to determine the required air-cooling technology performance to meet the given application specifications. Details regarding these two applications are provided in the Thermal Control of PHEV/EV Charging Systems report. Definition of the cooling technology, mechanical package design, and flow path for these test cases is covered in the Cooling Technology, Mechanical Package Design and Balance of System sections of this report.

In this example study, it was found that conventional air-cooled fin designs could be used to meet level 1 (1.44 kW) and level 2 (6.66 kW) vehicle charging targets. These results are provided in the Thermal Control of PHEV/EV Charging Systems report. Fig. 6 shows results for the DC-DC converter case study. Here, the tool was used to evaluate the ability of air-cooling to cool insulated gate bipolar transistor (IGBT) modules used within the DC-DC converter for a high-power DC charging application. The DC-DC converter is configured to operate as a buck converter, which converts a high-voltage DC charge source into a lower voltage compatible with the vehicle energy storage device. In this study, a small heat sink area and an extended heat sink area were modeled. Modifying the heat sink area affects the available cooling area and thus the fin length. For the same mass flow rate, the fin height was adjusted to match the same thermal performance. Also note that although the cooling technology heat exchanger resistance looks constant on this log-log plot, it is in fact, curving due to increased heating of the coolant with increasing power. This example illustrates how the interaction between the package and cooling

technology can be captured by this model. Also note how the number of components (IGBT/diode pairs) used in parallel affects the cooling requirements. This program has the capability to do sensitivity studies on all the input variables, providing a framework to investigate the system-level thermal management design and match cooling approaches with vehicle applications.

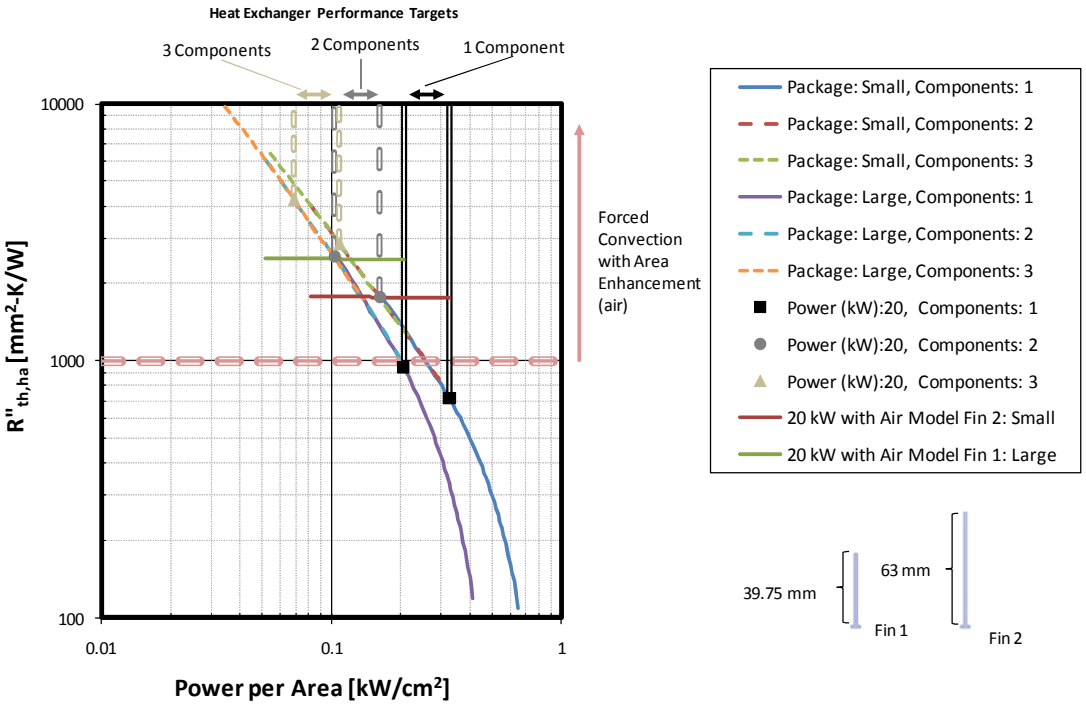

Fig. 6. Example system analysis, air-cooled 20 kW DC-DC converter for vehicle charging application

Cooling Technology

Improving convective heat transfer from a surface for a fixed driving temperature difference requires improving the heat transfer coefficient and/or increasing the wetted surface area. This must be achieved, however, without increased parasitic losses caused by either increased pressure loss or additional work requirements. For electronics cooling, it is also critical to maximize the available driving temperature at the surface by minimizing the temperature drop from the semiconductors to the wetted surface where it can be rejected. The focus of the cooling technology work is to research and develop innovative approaches to achieve these goals. One possible way of accomplishing this is to use synthetic jets and extended surfaces.

A synthetic jet is a type of fully pulsatile jet that results from the formation and interaction of vortex rings [1]. A common method of generating a synthetic jet in a single-phase fluid is the application of a threshold periodic pressure gradient across an orifice. With each cycle, a shear layer forms at the orifice edge and rolls up into a vortex ring that travels downstream due to its self-induced velocity. Fig. 7 shows a schematic of the suction and ejection strokes that constitute a cycle in this synthesis. Further, Fig. 8 shows the development of the leading vortex ring captured with a high speed camera. The roll-up of the shear layer (a-b), the trailing jet (b), break down (c), and the ensuing entrainment of air during suction (d) are observed. In this repeated fashion, a train of vortex rings moving away from the orifice occurs, whereupon the coherent structures interact, coalesce, and break down in a transition towards a turbulent jet directed downstream.

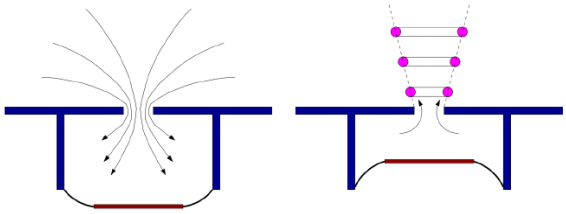

Fig. 7. Schematic of synthetic jet operation displaying the suction and ejection strokes [2]

This operational principle allows for a synthetic jet to be synthesized entirely from the surrounding medium, thereby circumventing the need for a remote prime mover and any external plumbing that is required to create a steady jet. In addition to eliminating the external pump requirement, synthetic jets have several advantages, including simple fabrication, high reliability, low weight, and the ability to aggressively influence the surrounding medium. Electronics cooling is one application where the use of synthetic jets has been shown to enhance heat transfer, both in direct impingement and in combination with conventional fans [3-5]. This enhancement is primarily due to coherent structures inherent in the synthetic jet flow that increase momentum and energy transfer, and as a consequence, increase the heat transfer rate.

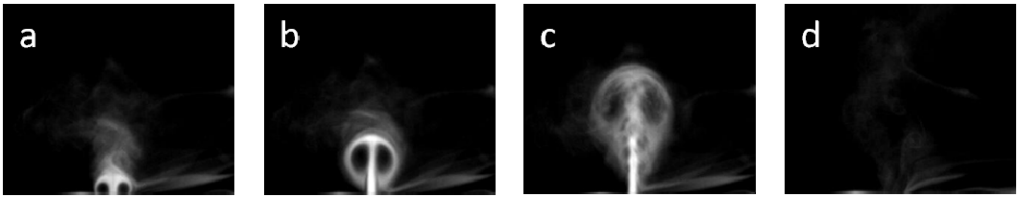

Fig. 8. Synthetic jet smoke visualization showing the progressive evolution of the leading vortical structure

Extended surfaces such as fins of various geometric and material configurations have long been used to enhance convective heat transfer, primarily through the increase of surface area exposed to the convective flow [6-8]. Graphite-based, open-pore structure foams have shown particular promise [9]. They are lightweight, have high strength and rigidity, are nontoxic, have a high surface area to volume ratio, and the graphite struts themselves possess a high thermal conductivity. Overall, the specific thermal conductivity (conductivity divided by density) of pitch-derived carbon foam is 6 times greater than the thermal conductivity of copper, making the pitch-derived carbon foam attractive for weight-sensitive thermal applications. In addition, unsteady and turbulent flows occur within the porous structure at Reynolds numbers of about 100, providing additional fluid mixing. Moreover, the foam may be fabricated in such a manner that the pressure drop across the heat exchanger is modest [Fig. 11].

With both synthetic jets and extended surfaces individually showing improved heat transfer capability, it suggests that a combination of both could further improve performance. This, in addition to the simplicity of the components, is anticipated to help achieve target program goals of cost, weight, and volume. A synthetic jet/extended surface would likely be designed to work in conjunction with a prime mover (e.g., a blower) and not replace it. The synthetic jet serves to locally enhance the heat transfer coefficient, thereby decreasing the power required by the prime mover to dissipate the same amount of heat. Fig. 9 shows three possible ways the technology may be implemented. Fig. 9(a) and 7(b) illustrate two configurations where a heat sink (foam or metal fin type) is placed on the electronics package and a synthetic jet actuator lies either above or to the leading edge of the heat sink. The entire system is then placed in a cross flow generated by the prime mover. The third design (Fig. 9c), based on reference [10], incorporates the synthetic jet actuators within the heat sink itself, resulting in the periodic jets emerging from within the heat sink. While these configurations illustrate future concepts, the first step is to characterize the fluid and heat transfer performance of synthetic jet actuators and extended surfaces.

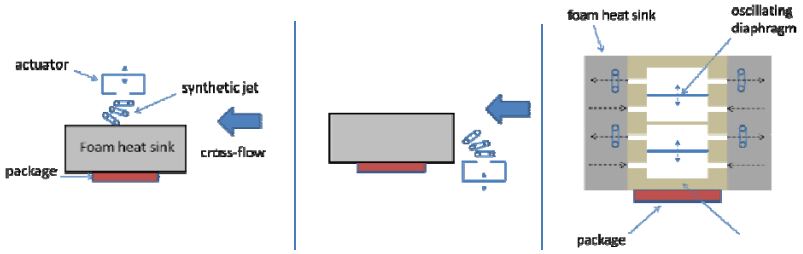

Fig. 9. Schematic (above) and CAD model (below) of possible cooling configurations

Both experimental and analytical/numerical tools were used to research advanced air-cooling technology in FY10. To enable experimental evaluation of advanced cooling technologies, the Air-Cooling Technology Characterization Platform was developed. This is a single-target air-cooling test bench for fundamental-level heat transfer testing, and is shown in Fig. 10. This test bench provides accurately measured and controlled air flow to a target heater. The air is both dried and temperature controlled. The heater's surface temperature is also controlled to simulate an electronics package, and the heater power is measured. The target heat loss is measured with a guard heater apparatus in a separate test and then subtracted for high-accuracy heat transfer performance measurement. Thermal numerical models were used to design and confirm the accuracy of this approach. The test bench flow, heater temperatures, and relative target position are computer programmable to allow rapid testing of advanced heat transfer technologies.

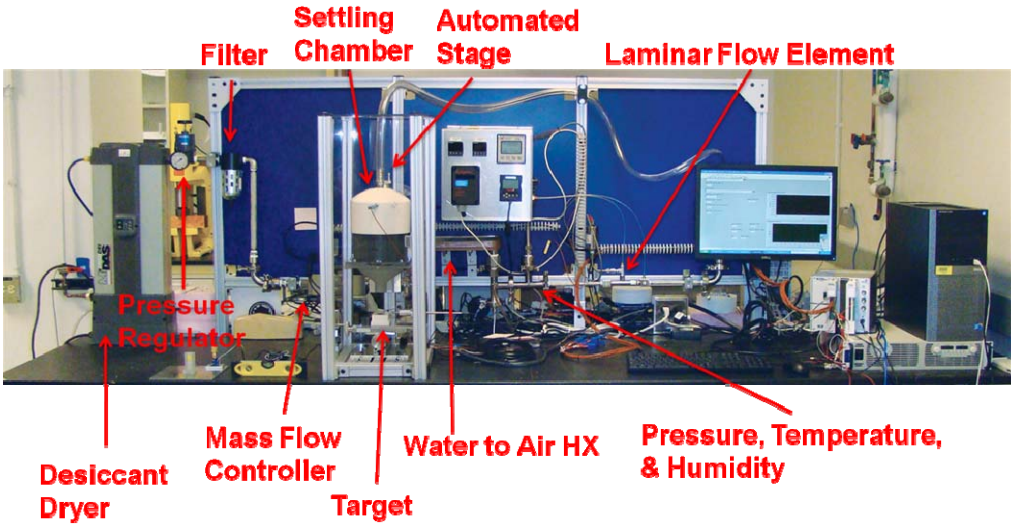

Fig. 10. Air-cooling technology characterization platform

The Air-Cooling Technology Characterization Platform was used to study both steady and synthetic air jets for enhanced localized heat transfer and will be used to study a variety of technologies in FY11 including cross flow, heat spreaders and enhanced surfaces. To study steady air jets, a settling chamber attachment was designed and fabricated based on wind tunnel correlations. The settling chamber outlet is designed to accept interchangeable nozzles; both converging and slot nozzles were fabricated. The settling chamber reduces turbulence intensity and provides a more uniform flow to the nozzle entrance. To study synthetic jets, a synthetic jet actuator was fabricated. This actuator is an electromagnetic speaker with an interchangeable orifice plate on the open end. The speaker is driven by a power supply where the input signal frequency and amplitude are controlled. Piezoelectric synthetic jet actuators will be considered as research moves from heat transfer to system-level application. The synthetic jet actuator and the settling chamber are interchangeable, as are their nozzle plate attachments. This allows direct comparison of nozzle designs.

For measurement of velocity and flow behavior, a high-accuracy constant-temperature anemometry system for 1, 2, and 3 component measurements is used. Probes are calibrated using a purpose-built constant-temperature anemometer calibrator. A three-axis programmable stage is used to position the anemometer and characterize flow field behavior.

To develop a better understanding of both the flow mechanics and heat transfer, computational fluid dynamics (CFD) models were created using the ANSYS Fluent software package. The synthetic jet/ extended surface concept has a large number of parameters that influence the performance. This design space is too large to fully explore experimentally; therefore, models are needed to help screen parameters and focus experimental work. Free and impinging jet configurations for both round and rectangular slot geometries are being modeled. As a first step in developing an experimentally validated model, a round synthetic jet, impinging upon a flat surface was modeled. To simplify the model, the cavity and diaphragm motion are excluded from the solution domain and a sinusoidal velocity boundary condition is imposed at the orifice throat. An axisymmetric approximation is also made to further reduce the model domain. Synthetic jets are turbulent in nature, however, a laminar model is considered for the first step. Fig. 11, shows one representative solution and compares it with the smoke visualization. Qualitatively, the laminar model captures the larger pertinent features. The roll-up and evolution of the leading vortical structure is clearly observed (a, b), and the propagation of the laterally moving vortical structure after impingement is seen as well. This initial step gives some confidence in the modeling approach; the next step will be the addition of turbulence. Both Reynolds-Averaged Navier-Stokes (RANS) and Large Eddy Simulations (LES) turbulence models are being considered. Once turbulence is added, validation of both the fluid flow field and the thermal performance will be completed using anemometry and temperature measurements, respectively.

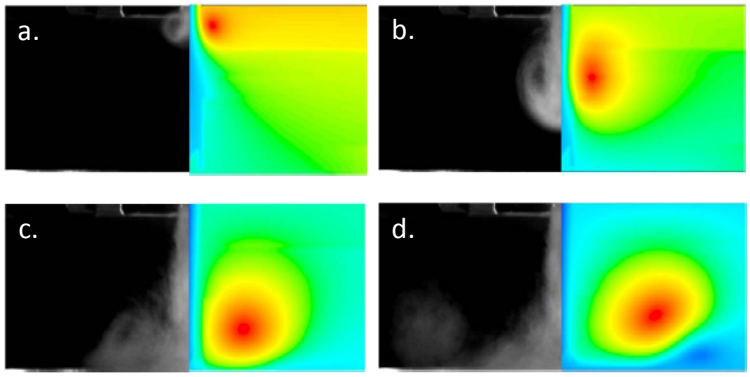

Fig. 11. Comparison between experiment and numerical modeling for an impinging jet

Synthetic jets are primarily influenced by two non-dimensional variables, the stroke ratio and the Reynolds number [1]. The stroke ratio may be thought of as the scaled length of a theoretical slug of fluid emerging from the orifice during the ejection stroke. The Reynolds number definition requires a characteristic velocity. For a steady jet, the mean exit velocity is used. In contrast, the period nature of the synthetic jet requires a characteristic velocity to be defined. Conventionally, the velocity signal at the orifice exit is integrated over the ejection stroke (half the period) and averaged over the full period [1]. To obtain this characteristic velocity, the exit velocity time history needs to be acquired. Towards this end, a single calibrated hot-wire probe was placed at the exit of the orifice. Fig. 12a shows the velocity at the exit as a function of time for an actuator operating at 60 Hz. Since a single-component hot-wire probe cannot discern direction, two positive peaks are seen. The larger peak is associated with the ejection stroke, while the smaller one is linked to the suction stroke. Fig. 12b shows the power spectral density of the signal, which indicates the dominant modes in the flow. The driving frequency (60 Hz) and the subharmonics are captured. It is these periodic disturbances that disrupt the boundary layer and promote mixing of momentum and energy.

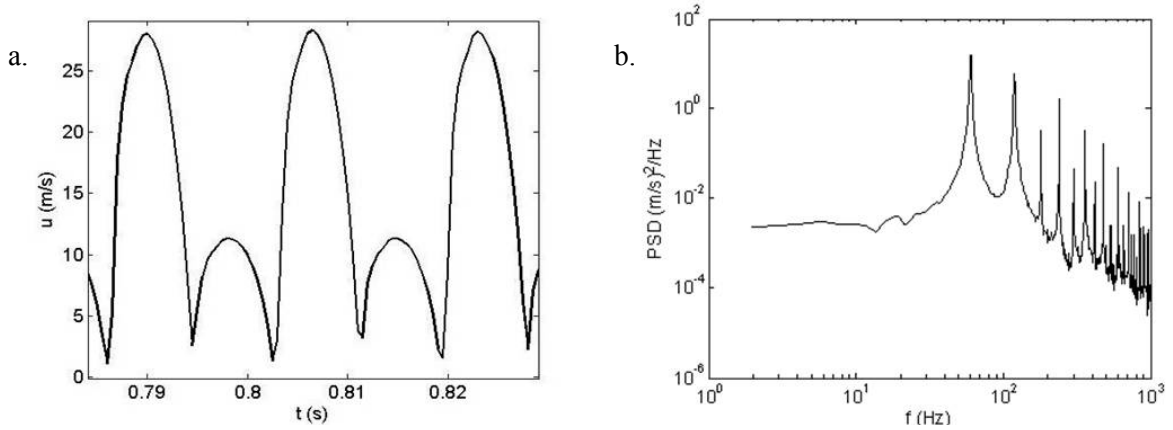

Fig. 12. Synthetic jet orifice exit velocity measurements: a. Time history b. Power spectral density

The influence of frequency on the time averaged velocity is shown in Fig. **13**a. For the frequency range tested, there exists an optimal frequency that maximizes the velocity. The location of this optimum is related to the resonant frequencies of the cavity and driving membrane system [11]. If parasitic losses are not considered, operating the actuator at this optimal frequency results in the most favorable fluid performance. That being said, the power consumption will be addressed in future experiments. At a fixed frequency, increasing the driving amplitude, results in an increase in exit velocity, as shown in Fig. **13**b. It is important to note that the mean velocity is dependent on both frequency and amplitude. Therefore, different combinations of the frequency and amplitude may yield the same mean velocities and consequently, the same Reynolds numbers.

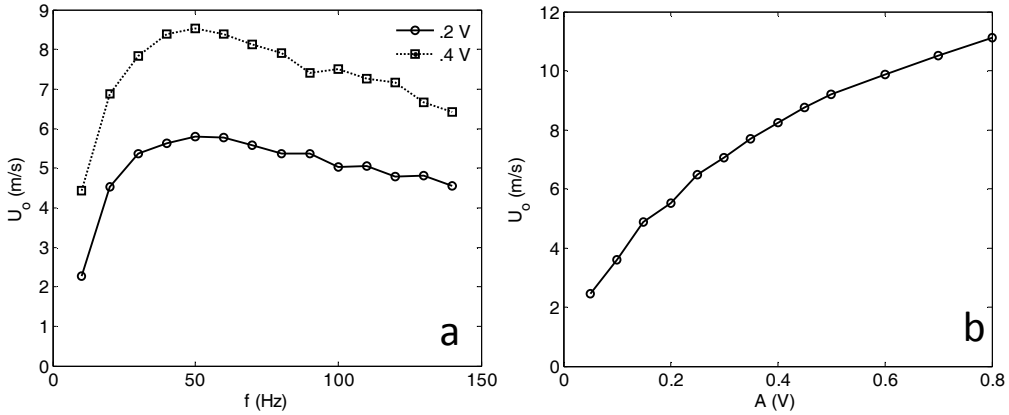

Fig. 13. Average velocity at the orifice as a function of actuator driving a. frequency b. amplitude

To better understand the benefits of synthetic jets their performance was experimentally compared to steady jets. Fig. 14 shows the heat transfer coefficients for both impinging continuous and synthetic jets for the same Reynolds numbers, orifice-to-heater height, and orifice dimensions. It appears that for this particular configuration (actuator, geometry, etc.) the synthetic jet marginally outperforms the continuous jet. This result agrees generally with literature, which asserts that synthetic jets either perform as well or better than their steady jet counterparts [4, 5, 12]. It should also be noted that the synthetic jet used for this experiment has not yet been optimized, and further improvements are anticipated. Additionally, an initial comparison done with an industry partner indicates that synthetic jets outperform steady jets by more than a factor of two under some conditions and designs. Based on these initial comparisons and literature, synthetic jets are anticipated to have equal or better performance than steady jets. This is encouraging considering that synthetic jets are more self-contained and do not require a remote prime mover or any ducting. In principle, synthetic jets have simple operation and fabrication procedures,

making them potentially highly reliable and cost effective while still giving the same or better heat transfer performance as compared to steady jets.

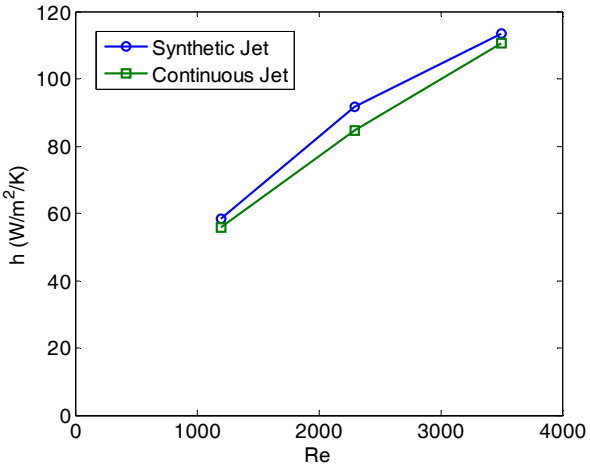

Fig. 14. Comparison of the thermal performance of synthetic and continuous jets for an orifice diameter (d) of 5 mm and an orifice-to-heater distance of 5d.

For the system analysis discussed previously in Fig. 6, a fin in cross-flow model was developed. The heat transfer for this model is based on semi-empirical fin performance models from literature [13, 14]. For fully developed channel flow, Nusselt number is constant, depending only on channel geometry. This model, however, allows for temperature dependent fluid properties. Therefore, the heat transfer coefficient, which is dependent on fluid conductivity, is not necessarily constant as coolant flow and temperature variables change. The fins are treated with a standard fin efficiency approach [13]. To account for the rise in temperature as the fluid passes down the length of the fin surface, the Effectiveness-NTU (NTU is number of transfer units) method is implemented as discussed in [15] and [16]. The heating of air can have a significant impact on the thermal performance. Fig. 15 shows the ratio of the NTU-based thermal resistance divided by the idealized constant-temperature thermal resistance as a function of mass flow rate for the larger heat sink DC-DC converter system analysis described previously. A ratio of one would indicate constant temperature behavior.

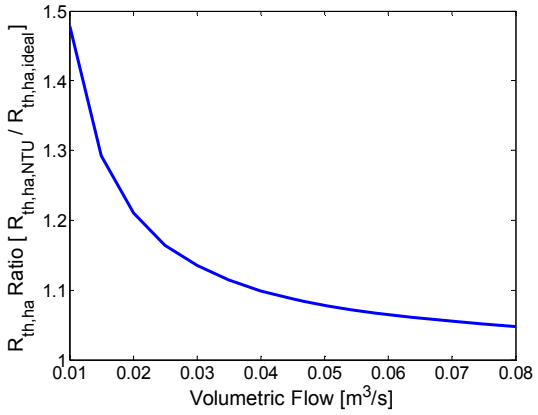

Fig. 15. Heat exchanger to air thermal resistance ratio, $R_{th,ha,NTU}/R_{th,ha,ideal}$

Package Mechanical Design

Detailed finite element analysis (FEA) models for a range of commercial power semiconductor package configurations were developed. Each package consists of an IGBT and diode pair, direct bonded copper (DBC), heat spreader, thermal interface material, and heat sink. This approach captures the details of how

the mechanical design decisions, such as material selection, semiconductor placement, and base plate area, affect the thermal performance of the package system. These models have been integrated into the system analysis modeling described previously. Please see the Power Electronics Thermal System Performance and Integration report for further details on the mechanical package modeling approach.

Balance of System

A balance of system model was developed as part of the power electronics system modeling process. The balance of system model provides a flexible structure to define the cooling system, including flow rate and flow paths. The next version will also allow definition of ducting, filters, and prime movers. For this model, the heating source is divided into regions and packages which, in the context of an inverter, correlate to inverter switches and IGBT/diode pairs. For example, a three-phase inverter could be divided as shown in **Fig. 16**a, with six regions, each representing a switch and each region having two packages each representing an IGBT/diode pair. Currently, from the coolant perspective, the package level can either be in parallel or in series. The mechanical package analysis does contain more detail regarding arrangement; however, the coolant only sees the package base plate areas. The heat generation and cooling technology are solved at the package-level and scaled to the region-level by the number of packages. The region-level flow is defined using flow branches. For example, in **Fig. 16**a, there are three branches, each two regions long. Adding two-sided cooling simply requires adding branches for the other side. At this time, all branch flow rates are assumed to be equal, and all branches must be the same. More flexibility will be added in the future.

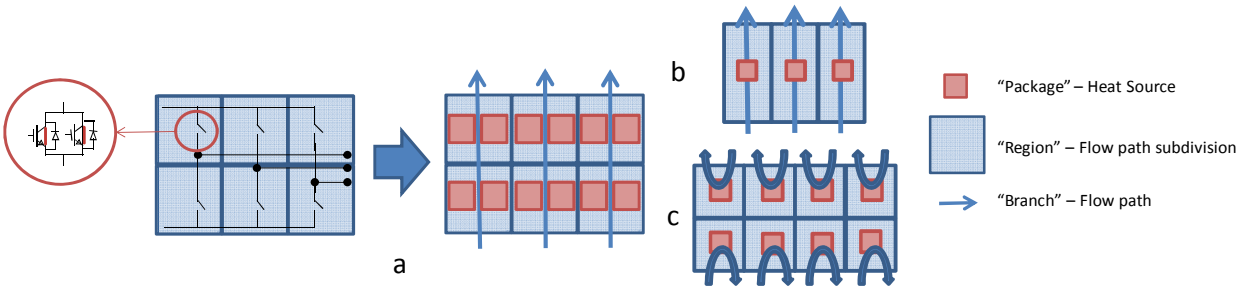

Fig. 16. a. Coolant system flow path abstraction and definition; b. Cold plate; c. DC-DC converter

Fig. 16b and 14c show the region, package, and flow paths used for the PHEV and EV charging application studies described in the system analysis section. The cold plate, **Fig. 16**b, has three parallel flow paths that cross the short side of the device. **Fig. 16**c shows the DC-DC converter, which has eight regions, each with its own cooling. This represents a centerline to outside edge coolant flow configuration.

Conclusion

Significant progress was made toward the project's objective to develop and apply air-cooling technology to improve power electronics thermal control design and influence industry; thereby enhancing system performance to meet FreedomCAR technical targets for weight, volume, cost, and reliability. A system-level approach to research was developed that addresses cooling technology, package mechanical design, balance of system, and vehicle application specifications. A high-level system model was created to investigate each of these components and understand their complex interactions. Application of this model was demonstrated for a simplified cold plate charger and a more detailed DC-DC converter. This model will be expanded and applied to a range of applications in FY11, including collaborative investigations with ORNL. The Air-Cooling Technology Characterization Platform was developed, which enables a single-target fundamental heat transfer experimental research. This includes a high-accuracy constant-temperature anemometer system and calibrator. Results from this test bench have shown promise for synthetic jet technology. Several synthetic jet based approaches were conceptualized,

and a screening process will be used to identify the most promising. This capability was leveraged to establish an air-cooling heat transfer collaboration with GE Global Research. In addition to experimental work, progress was made in creating detailed computational fluid dynamic conjugate heat transfer models of steady and synthetic air jets, capturing important flow structures. These models will help improve the understanding and design of new advanced cooling methods. FY10 laid the foundation for developing promising cooling technology in FY11 and applying these new approaches to a system in FY12.

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Additional thanks to: Charlie King, Sreekant Narumanchi (NREL)

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Patent

1. Micro-fin–based novel air-cooled heat sink concept is under review by NREL patent committee.

5.2 Characterization and Development of Advanced Heat Transfer Technologies

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Project Objectives

The overall objective of the advanced heat transfer technologies task is the development of cooling methodologies to enable high heat flux dissipation while maintaining low die operating temperatures with the aim of achieving the Advanced Power Electronics and Electric Motors (APEEM) program goals of weight, volume, and cost. Existing hybrid automotive power electronic systems can rely on single-phase, channel flow cooling systems that provide relatively low heat transfer capability. Consequently, these cooling systems tend to be bulky and add significant mass and volume to the system.

In this project, we investigate efficient cooling schemes such as single-phase liquid jet impingement and two-phase heat transfer in combination with enhanced surfaces, with the overall goal of helping decrease the size and weight of automotive power electronics cooling systems. The enhanced surfaces are either coatings or surface structures that are applied or fabricated onto the heated surface to increase heat transfer efficiency. The intent of this work is to find a potentially simple yet effective means of improving heat transfer efficiencies that may lead to increases in specific power and power density of automotive power electronics.

Approach

In this project, we evaluate the effectiveness of enhanced surfaces for augmenting heat transfer in both single- and two-phase heat transfer for potential power electronics cooling applications. Various surface coatings/structures were studied, including some novel enhanced surfaces synthesized by industry and university partners as well as by NREL. Collaborations were established with the various institutions to obtain samples of their enhanced coatings/surfaces.

The thermal performance of the coatings/surface structures was quantified through their heat transfer coefficients, critical heat flux (CHF) (two-phase only), and boiling incipience superheat (two-phase only) values. These values were obtained experimentally within test loops designed to conduct these experiments. The thermal performance of the enhanced coatings/structures was then compared to that of a plain/baseline surface as well as simple surface roughening techniques (single-phase only).

The following test parameters are specific to either the single-phase study or the two-phase study.

Single-Phase Study

- Experiments were conducted in the submerged jet and free jet configurations. Experiments were also conducted in channel-flow type configuration to determine the effectiveness of the enhanced surfaces when utilized in cooling configurations similar to those used in existing automotive hybrid power electronics cooling systems.
- We investigated the effect of fluid velocity on performance.

Two-Phase Study

- We conducted experiments in pool boiling (immersion/passive cooling) and spray impingement boiling configurations.
- For the spray impingement boiling study, we investigated the effect of flow rate and subcooling on thermal performance.

Major Accomplishments

Single-Phase Study

- A total of 11 different surface coatings/structures were investigated in the channel flow, submerged jet, and free jet configurations.
- Results indicate that the enhanced surfaces investigated would not be effective at enhancing heat transfer in channel flow configurations with relatively large passages/channels at velocities less than 2 m/s (i.e., in existing automotive power electronics cooling configurations).
- Within the free jet impingement configuration, the copper microporous coating (3M) produced the largest heat transfer enhancement, about 130% as compared to free jet impingement on a plain surface. However, at lower flow rates, the MicroCool finned surface (Wolverine Tube, Inc.) outperformed all coating/surfaces.
- Within the submerged jet impingement configuration, the MicroCool surface produced the largest heat transfer enhancement, about 100% as compared to impingement on a plain surface.

Two-Phase Study

- Three enhanced surfaces/coatings were tested in both pool boiling and spray impingement boiling configurations.
- The copper microporous coating (3M) increased nucleate boiling heat transfer rates by 100%–500% and increased the critical heat flux by 7%–20% in the pool boiling and spray impingement boiling configurations.
- The microporous coating (3M) was found to be very effective at enhancing heat transfer to the extent that nucleate boiling heat transfer is found to be the dominant heat transfer mode and is insensitive to forced convection effects. This indicates that passive two-phase cooling implemented with this type of coating can perform similar to spray cooling.
- The 20-μm-long copper nanowire coating (University of Colorado at Boulder) provided an approximately 100% increase in heat transfer coefficients and about a 5% increase in the CHF.

Future Work

- In the future, we will conduct system-level tests to investigate the effectiveness of the enhanced surfaces in cooling an actual power electronics module.
  - For the single-phase study, a copper cold plate utilizing the MicroCool micro-fin structure (Wolverine Tube, Inc.) has been fabricated and will be used to cool a Semikron SKM power electronics module. The performance of the enhanced surface will be compared to an equivalent cold plate with no surface enhancement.
  - For the two-phase study, a Lexus/Denso power electronics module will be cooled using immersion/pool boiling. Experiments will be conducted using a module with the copper

microporous coating (3M), and the results will be compared to an equivalent module with no coating. This will allow us to quantify the potential of both immersion/pool boiling and the enhanced surfaces to cool an actual power electronics module.
- For the single-phase study, additional experiments will be conducted using a combination of finned structures (surface area increase) with enhanced surfaces/coatings.
- We will investigate the reliability of enhanced surfaces by subjecting the surfaces/coatings to a constant water–ethylene glycol jet and evaluating for erosion and potential changes to their thermal performance.

Background / Technical Discussion

Prior studies relevant to this project are discussed below. This discussion is divided into two parts: single-phase and two-phase investigations.

Single-Phase Jet Impingement Heat Transfer

The thin boundary layers (hydrodynamic and thermal) associated with jet impingement cooling can provide relatively large heat transfer coefficients, which makes them an attractive cooling solution for high heat flux applications [1]. Moreover, studies have demonstrated that jet impingement heat transfer can be further enhanced through the use of surface roughening techniques for both air [2] and liquid [1-4] jets.

Gabour and Lienhard [3] investigated the impact of surface roughness on jet impingement heat transfer. Their results demonstrate that stagnation point heat transfer increases with increasing roughness, with the roughest surface producing 50% greater heat transfer than the baseline surface. Moreover, the roughness enhancement increases with increasing Reynolds numbers. The enhancement is associated with the roughness structures protruding through the thermal boundary layer within the stagnation zone. Sullivan et al. [4] also reported enhancement using roughened heat sources in the submerged jet configuration. In this study [4], the heat transfer enhancements of the roughened surfaces are associated with mechanisms occurring within the wall jet region. It is speculated that roughened surfaces increase heat transfer by advancing the transition to turbulent flow and by disrupting the viscous sublayer within the turbulent region.

Two-Phase Heat Transfer

Extensive research has been conducted on characterizing the performance of enhanced surfaces in the pool boiling configuration. A review by Honda and Wei [5] summarizes the pool boiling performance of a variety of enhanced surfaces. They report that, in general, micro-fins are more effective at increasing CHF while microporous structures are more effective at increasing nucleate boiling heat transfer. In an earlier investigation, Bergles and Chyu [6] conducted pool boiling experiments using a commercially available porous surface that consisted of copper particles brazed onto a heated surface. Experiments revealed that the coating significantly increased the heat transfer coefficients by as much as 800% and 250% for R-113 and water, respectively.

The use of enhanced surfaces in conjunction with spray impingement boiling has received little attention as compared to their application to pool boiling. Silk et al. [7, 8] used finned and porous tunnel structured surfaces to enhance spray cooling. Enhancement from these structures was mostly a result of the fin effect (increased surface area). Studies investigating the effect of microporous coatings on spray cooling were carried out by Kim et al. [9] using air-assisted water sprays. Enhancements to both heat flux and dry-out were reported using the coating and were attributed to the wicking effect within the coating.

Enhanced Surfaces

As mentioned above, the primary goal of this project was to evaluate the use of enhanced surfaces as a means of enhancing single- and two-phase heat transfer. A variety of surface structures were evaluated; however, the main focus was on evaluating the more novel coatings/surface structures. These novel coatings/structures consisted of a copper microporous coating, MicroCool micro-finned surface, copper nanowires, and spray pyrolysis-based copper coating. Scanning electron microscope (SEM) images of these coatings/surfaces are provided in Figure 1. A more detailed description of each surface coating/structure is provided below.

- The copper microporous coating was developed and patented by 3M. It consists of sub-20-μm copper particles fused onto a surface at elevated temperatures (~850°C) to form a ~150-μm-thick porous coating.
- The MicroCool micro-finned surface was created by Wolverine Tube, Inc. using its patented micro-deformation technology. Fin specifications: fins per cm=77, pitch=127 μm, fin thickness=67 μm, fin gap=65 μm, and fin height=725 μm.
- The copper nanowires were generated at the University of Colorado at Boulder and were grown on the copper surface by means of electroplating, using a porous anodic alumina as the template [10]. Two nanowire coatings were studied, one with nanowires of length of 2–3 μm and another with nanowires of length ~20 μm (two-phase only). The diameter of the nanowires was 250–300 nm with an inter-wire gap of ~50 nm. The diameter of the nanowires was a function of the pore diameter in the template, and the length was controlled by the duration of the electroplating.
- A copper coating was created at a laboratory in the NREL photovoltaics center using a spray pyrolysis process. The coating was created by spraying an ink consisting of copper formate, ethylene glycol, and ethylene diamine onto a heated surface. The final thickness of the coating was not measured.

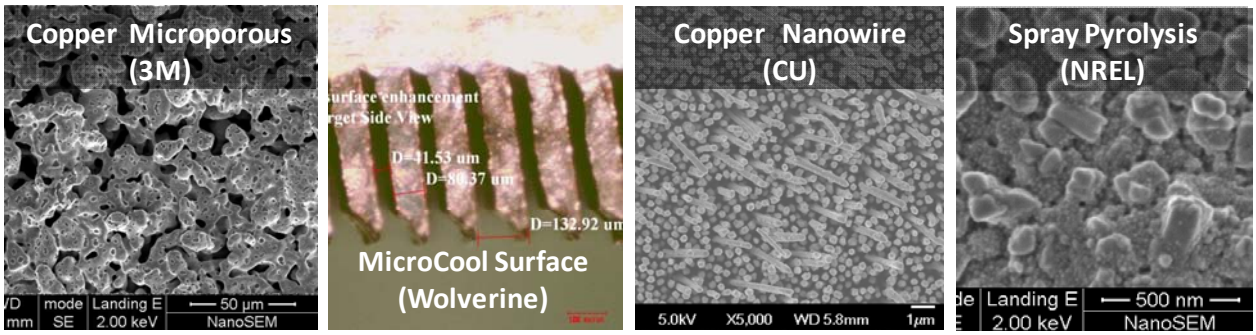

Fig. 17. SEM images of the enhanced surfaces tested

Single-Phase Heat Transfer Enhancement through Enhanced Surfaces

Experimental Apparatus & Procedures

A schematic of the flow loop used for the single-phase heat transfer experiments is shown in Figure 2. These experiments were performed using deionized water, which is contained within the reservoir tank. The liquid is circulated through the loop using a gear pump that has a maximum capacity of 600 cm^3/s. Precise flow control is achieved by controlling the pump speed via a variable frequency drive and by throttling the needle valves to direct flow to the test section or through a bypass line. A turbine flow meter, located downstream of the pump, is used to measure fluid flow rates. For all tests, the nozzle inlet liquid temperatures were maintained at 25°±0.5°C through the use of a temperature-controlled immersion heater and chilled water loop that are located within the reservoir tank.

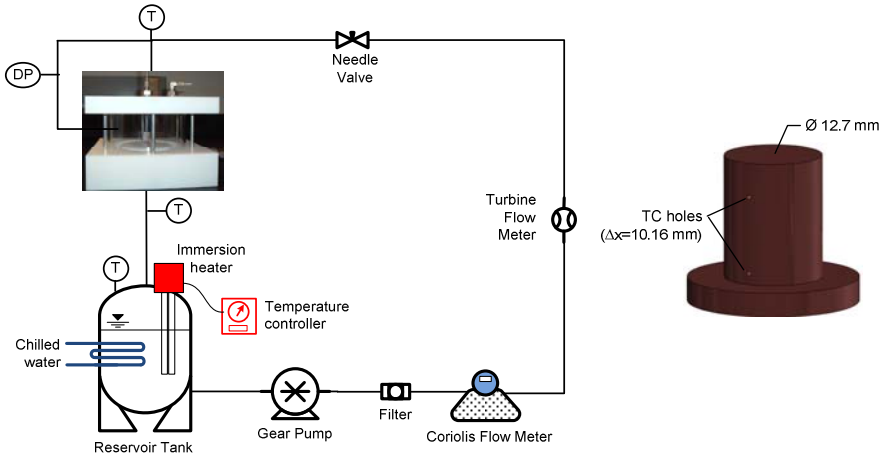

Fig. 18. Schematic of the single-phase flow loop (left) and 3-D rendering of the test heater block (right).

A drawing of the test heater, which is machined from oxygen-free copper, is shown in Figure 2. Power to the heater is provided through a thick film resistor attached to the bottom side of the copper piece. Insulation is provided with Teflon, which surrounds the copper piece exposing only the top 12.7-mm-diameter surface. Heat flux and surface temperature measurements are calculated, assuming one-dimensional steady-state heat transfer, via two K-type thermocouples embedded within the copper block.

Table 2. Estimated Heat Transfer Uncertainties at Various Nozzle Velocities

U (m/s)	***Error ± h*** *(W/m^2-K)*	***Error ± %***
2	1,199	6.3%
7	2,437	6.8%
12	4,268	8.0%

Uncertainty Analysis

A detailed uncertainty analysis was carried out according to the procedures described in Dieck [11] to quantify the uncertainty in the experimental heat transfer coefficients. The procedure involves gathering uncertainties in all variables (eight total) required to calculate the heat transfer coefficients. The uncertainty in the heat transfer coefficient was then calculated using the propagation of error equation, including both systematic and random uncertainties. The random uncertainties were obtained experimentally through test repetitions using the plain/baseline data. Table 1 summarizes the calculated heat transfer coefficient uncertainties (95% confidence interval) at various nozzle velocities. After calibration, the uncertainty in the thermocouple measurements is estimated to be ±0.03°C, while the uncertainty in the fluid velocity is estimated to be ±1%.

Results and Discussion

This single-phase heat transfer study was primarily focused on evaluating the effect of enhanced surfaces on jet impingement heat transfer in both the free and submerged jet configurations. Jet impingement cooling is a more aggressive cooling scheme associated with high heat transfer rates, which makes them an attractive cooling solution for high heat flux applications [1]. However, experiments were also conducted to test the performance of the enhanced surfaces in a channel flow (flow over a heated surface) configuration. Detailed schematics for the channel flow, submerged jets and free jet test configurations are shown in Figure 3. This figure provides the relevant dimensions for each test. A 1.24-mm-diameter nozzle was used for the jet impingement tests.

For single-phase heat transfer experiments, roughened surfaces were also created using simple roughening techniques such as sandblasting and sandpaper scoring. The roughness of these surfaces was

characterized using a Fowler Pocket Surf surface roughness gauge providing average surface roughness measurements of Ra=4.16 µm and Ra=4.1 µm for the sandblasted and sandpaper-roughened surfaces, respectively. Tests were also conducted using a variety of finned surfaces. Various fin structures were created and tested, including rectangular and pyramidal pin fins. Due to the large amount of data generated, only the data for the best performing fin structure (pyramidal fins with fin height=1.27 mm) will be shown. This fin's structure provided a ~140% increase in area as compared to the baseline sample. The performance of the finned and roughened (sandblasting and sandpaper) samples was then compared to the performance of the novel coatings/surfaces.

For these experiments, the thermal performance was characterized by measuring the heat transfer coefficients defined as $h=q''_{calc}/(T_w-T_{inlet})$, where q''_{calc} is the calculated heat flux, T_w is the temperature of the heater surface/wall and T_{inlet} is the temperature of the liquid exiting the nozzle.

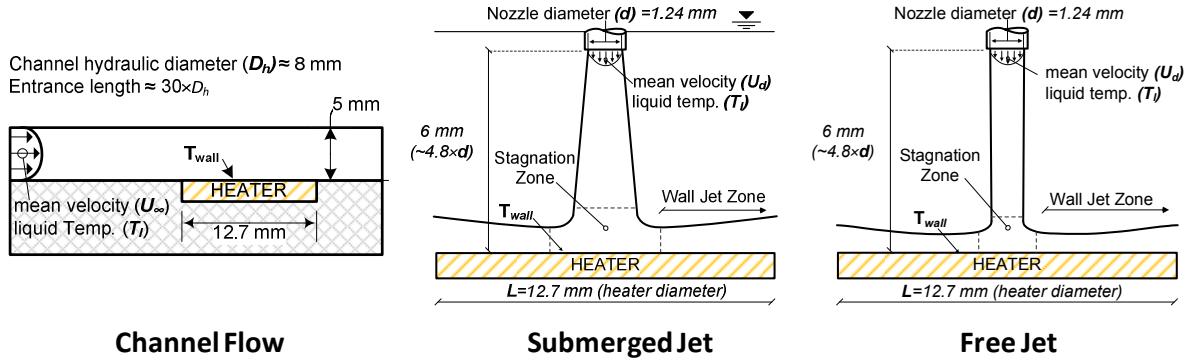

Fig. 19. Schematics, with relevant test parameter dimensions, for channel flow, submerged jet, and free jet experimental setups

Channel Flow: The performance of all samples tested in the channel flow configuration is shown in Figure 4. This figure shows the plot of the heat transfer coefficients as a function of the mean channel velocity. The velocity range tested was intended to encompass practical operational velocities where the lower velocities tested are more typical of standard fluid velocities within automotive power electronics cold plates. The higher velocity was limited to 1.6 m/s given that a study by Lytron [12] reports that erosion-corrosion issues may occur if velocities exceed about 1.8 m/s and 2.4 m/s for aluminum and copper, respectively. For these tests, the power dissipated was 20 W.

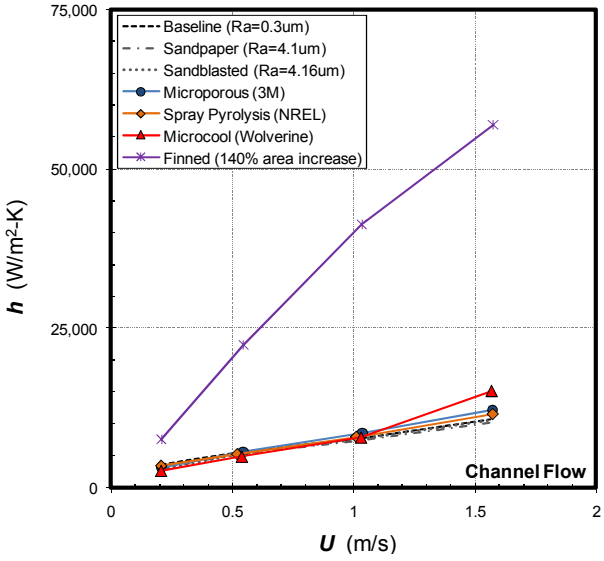

Fig. 20. Heat transfer coefficients versus fluid velocity for the various surfaces in the channel flow configuration

As shown in Figure 4, none of the enhanced surfaces produced any substantial enhancement in the heat transfer coefficients in the channel flow configuration. Similarly the roughened surfaces also had no effect on performance. In this configuration, only the samples with finned surfaces enhanced heat transfer—a result of an increase in the heated surface area. These findings indicate that the enhanced surface tested would have minimal, if any, effect on

performance if applied to existing automotive power electronics cooling systems, which utilize channel flow type configurations at relatively low velocities and with relatively large channel sizes.

Submerged Jets: Results for the submerged jet impingement tests are provided in Figure 5a. For these experiments, the power dissipated was 70 W. In this configuration, the Wolverine MicroCool surface produced the highest heat transfer enhancement of as much as ~100% at the highest velocity tested. Even though the greatest enhancement was achieved at the highest velocity, this surface was found to produce substantial enhancement at all flow rates tested. The superior performance of this surface is likely a result of the increased surface area (not measured), as well as potential interactions of the finned structures protruding through the thermal boundary layer within the stagnation zone, similar to the behavior postulated by Gabour and Lienhard [3] in their study.

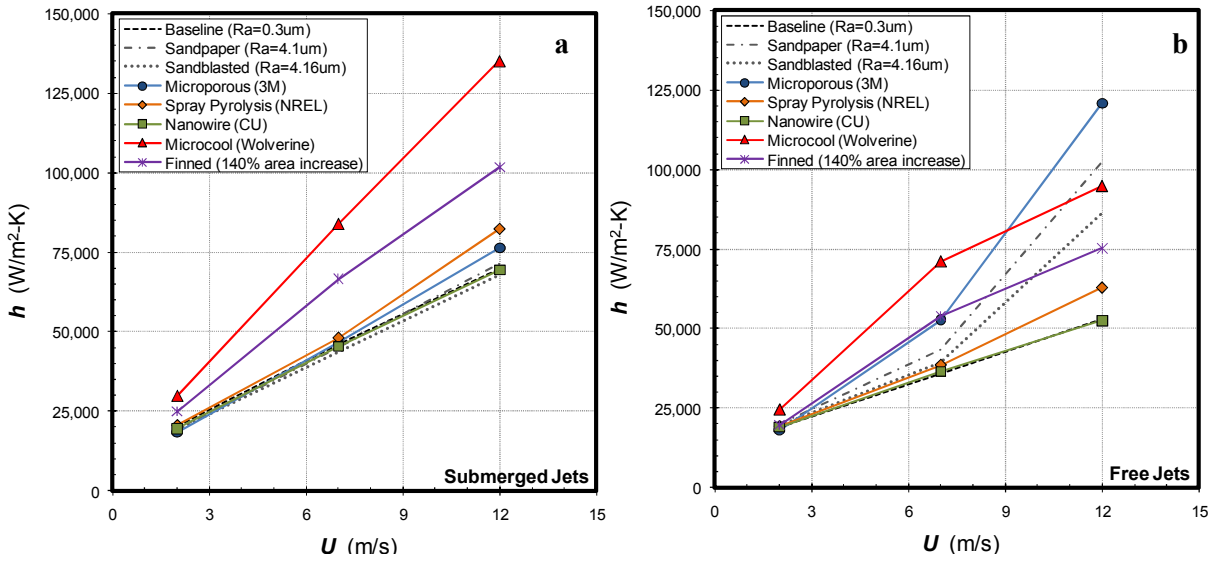

Fig. 21. Heat transfer coefficients versus fluid velocity for the various surfaces in the submerged (left) and free (right) jet configuration

The other enhanced surfaces (microporous, nanowire, and spray pyrolysis) were found to have minimal effect on performance: their performance curves are close to that of the baseline surface. The small enhancement seen for the spray pyrolysis curve at the highest flow rate falls within the 95% confidence interval uncertainty estimates and therefore is not considered statistically significant.

Free Jets: Results for the free jet impingement tests are provided in Figure 5b. For these tests, the power dissipated was 70 W. As seen from this figure, the performance data in this configuration is more intriguing as compared to the prior two configurations discussed. The highest enhancement, of ~130% as compared to the baseline, is achieved with the 3M microporous coating at the highest velocity tested. Interestingly, the simple roughened surfaces also demonstrated significant heat transfer enhancements of about 90% and 60% for the sandpaper scored and sandblasted surfaces, respectively. An interesting feature in the data for the microporous coating and the simple roughened surfaces is found in the manner in which their performance increases exponentially as the velocity increases. As the velocity increases, the boundary layers (both hydrodynamic and thermal) will decrease. This thinning of the boundary layer would likely allow for greater interaction between the boundary layers and the surface structures as the surface structures are able to protrude further into and potentially beyond the boundary layers. This effect could then allow increased heat transfer by providing a heat conduction path through the surface structures to the cooler liquid beyond the thermal boundary layer.

Although the microporous coating produced the greatest enhancement, the MicroCool surface outperformed all surfaces at the lower flow rates tested (2 and 7 m/s). It is also worth noting that all finned samples tested were observed to suffer from significant fluid splatter at higher flow rates and consequently their performance suffered.

Two-Phase Heat Transfer Enhancement through Enhanced Surfaces

Experimental Apparatus and Procedures

A schematic of the two-phase flow loop is shown in Figure 6a. The loop is designed to deliver the fluid at the desired pressure, temperature, and flow rate to the spray nozzle located inside the test chamber. The liquid is stored within the test vessel and is circulated through the loop using a speed-controlled gear pump. Additional system components include a plate-type heat exchanger, a positive displacement flow meter, and a filter. System temperature measurements are made using K-type thermocouples, and system pressures are collected using pressure transducers. The spray nozzle used in the spray cooling experiments is a Unijet full cone pressure nozzle with an orifice diameter of 1.7 mm and spray angle of 48.5°, made by Spraying Systems, Inc.

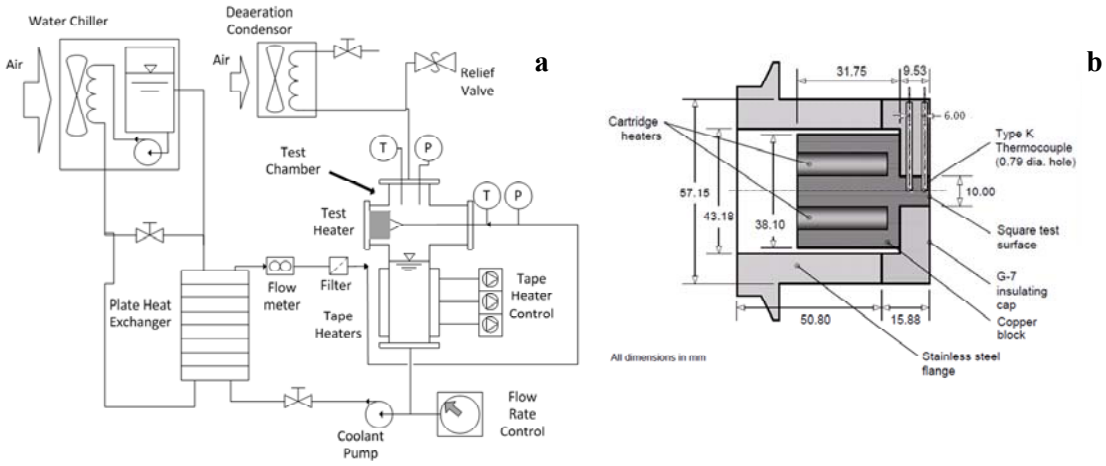

Fig. 22. Schematic of the two-phase flow loop (left) and heater (right)

In all the experiments reported in this study, the chamber vapor and liquid temperatures are maintained at ~61°C, corresponding to a pressure of 1 atmosphere at sea level (~101 kPa). Before each experiment, the fluid was deaerated for 20 to 45 minutes to remove any dissolved non-condensable gases. For the spray experiments, two levels of liquid temperatures in the nozzle are considered: 31°C (subcooling ΔT_{sub} = 30°C, henceforth referred to as "subcooled"), and 60°C (subcooling ΔT_{sub}~1°C, henceforth referred to as "near-saturated"). Boiling curves were generated by raising the voltage through the cartridge heaters in small increments and allowing the temperatures to achieve steady state, which was determined by less than 0.1°C change in 5 to 10 minutes, depending on the surface. For accurate determination of the CHF, the flux increment is kept very small, near the CHF. The highest heater power with a stable target surface temperature is considered to be the CHF, beyond which a sudden, large surge in the temperature measurement occurs with only a small increment in the heat flux. Once the CHF is detected, the heater voltage is cut off, and the target is allowed to cool down.

Figure 6b shows the construction of the test heater used to simulate a 1-cm^2-square chip. The heater block is machined from oxygen-free copper. Heat is provided using three cartridge heaters embedded in the base of the heater and is dissipated at the 1-cm^2 surface. Insulation to the heater block is provided using a fiberglass (G7) block that surrounds the heater. Heater surface temperatures and heat flux through the target surface are calculated assuming one-dimensional steady-state conduction using two K-type thermocouples embedded within the heater block.

Uncertainty Analysis

The uncertainty in the flow rate is estimated to be ±0.17 cm^3/s in the range 1.25 to 17 cm^3/s while the uncertainty in the pressure measurements is estimated to be ±350 Pa. The uncertainty in the temperature measured is within ±0.03°C. Due to the uncertainty in the positions of the two target thermocouples (estimated to be ±0.125 mm from the centerline of the holes) and hence the temperature measurements in the target block, it is estimated that the heat flux measured has an uncertainty of ±6 %.

Results and Discussion

Similar to the single-phase study, the two-phase study was focused on evaluating the use of enhanced surfaces as a means of two-phase cooling enhancement. For this study, three enhanced surfaces were evaluated: a copper microporous (3M) coating and two copper nanowire (University of Colorado at Boulder) coatings. The two nanowire coatings differed only in the length of the nanowires, which were 2–3 μm for one coating and ~20 μm for the other. The copper microporous coating and the shorter nanowire coating (2–3 μm) were identical to the coatings used in the single-phase study.

Two-phase heat transfer experiments were conducted in both pool boiling and spray impingement boiling configurations. The effect of the enhanced surfaces on heat transfer coefficients, boiling incipience, and the CHF was evaluated and compared to that of a baseline/plain surface. The influence of flow rate and subcooling on the boiling heat transfer was also investigated.

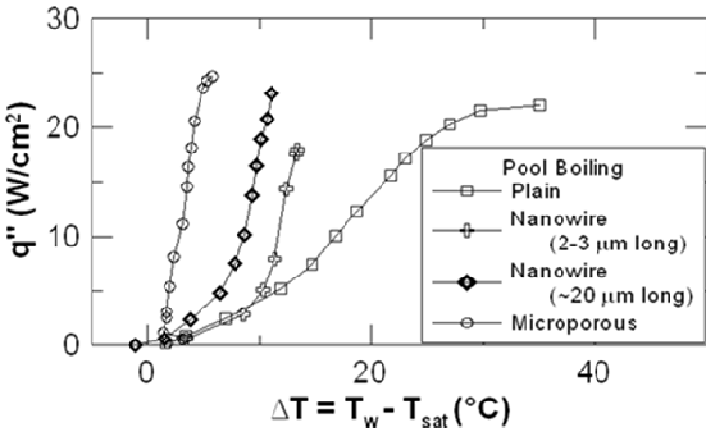

Fig. 23. Pool boiling curves

Pool Boiling: The pool boiling curves for the four surfaces are shown in Figure 7. Evident from this figure is the dramatic heat transfer enhancement of over 500% produced by the microporous coating as compared to the plain surface. This dramatic enhancement is likely associated with the many micro-sized cavities within the porous coating, which increase the number of active nucleation sites and facilitate nucleation. By promoting nucleation, the microporous coating also decreases the boiling incipience superheats to only ~3°C as compared to ~5°C in the long nanowire surface, ~8°C in the short nanowire surface, and ~12°C in the plain surface. The CHF is also enhanced by 10% for the microporous surface with respect to the plain surface.

Table 3. Spray Cooling Experiment Test Matrix

Surface	Flow rate (cm^3/s)	Mean velocity (m/s)	Subcooling level
Plain	4.7 10.2 15.8	2.1 4.5 7.0	30°C, 1°C
Microporous	4.7 10.2 15.8	2.1 4.5 7.0	30°C, 1°C
Nanowire	4.7	2.1	30°C, 1°C

Two nanowires surfaces, using nanowires of different lengths, were evaluated. The shorter nanowire surface (2–3 µm long), while showing an improvement in *h* of about 60% for the same heat flux near the CHF, resulted in a lower CHF than the plain surface. The surface with the longer nanowires (~20 µm long) showed a 100% increase in *h* near CHF and a 5% increase in the CHF. The increase in the heat transfer with the length of the nanowires at the same superheat is probably due to the increased number of nucleation sites at the microscale cavities formed at the top layer by agglomeration of the nanowires.

Spray Cooling: Experiments with spray impingement were performed on the different surfaces for the combination of parameters shown in Table 2. The mean velocity shown in the table is simply the ratio of the volumetric flow rate of the liquid to the area of the nozzle orifice (1.7 mm diameter). It should be noted that the surface with the nanowire coating showed degraded performance due to the spray even at the lower flow rate. Therefore, spray cooling results for the nanowire surface are not shown in this report but are available for the lowest velocity (4.7 m/s) tested.

Figure 8 shows the spray boiling curves for the plain/baseline and microporous coated surfaces at the highest flow rate tested (15.8 cm^3/s). In this figure, the spray boiling curves for both subcooled (T_{nozzle} = 31°C) and near-saturated (T_{nozzle} = 60°C) conditions are shown. As was the case with pool boiling, the microporous coating also produced substantial heat transfer enhancement of about 100%–300% in spray cooling for both near-saturated and subcooled conditions. Additionally, the microporous coating was found to increase the CHF between 7% and 20% for the various spray cooling experiments.

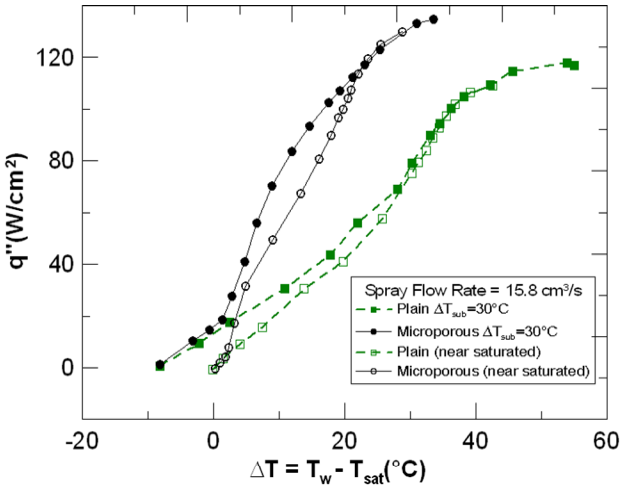

Fig. 24. Spray boiling curves for both near-saturated and subcooled conditions

The favorable effect of the liquid subcooling is clearly seen at lower power levels for both the surfaces where subcooling produced lower temperatures (Figure 8). However, at higher power levels within the fully developed nucleate boiling regime, subcooling is found to have minimal effect on performance as is evident in the convergence between the subcooled and near-saturated boiling curves. This is the case for both the microporous coated and plain surfaces. The convergence of the near-saturated and the subcooled curves at the higher heat fluxes demonstrates that the phase-change heat transfer is the dominant heat transfer mechanism.

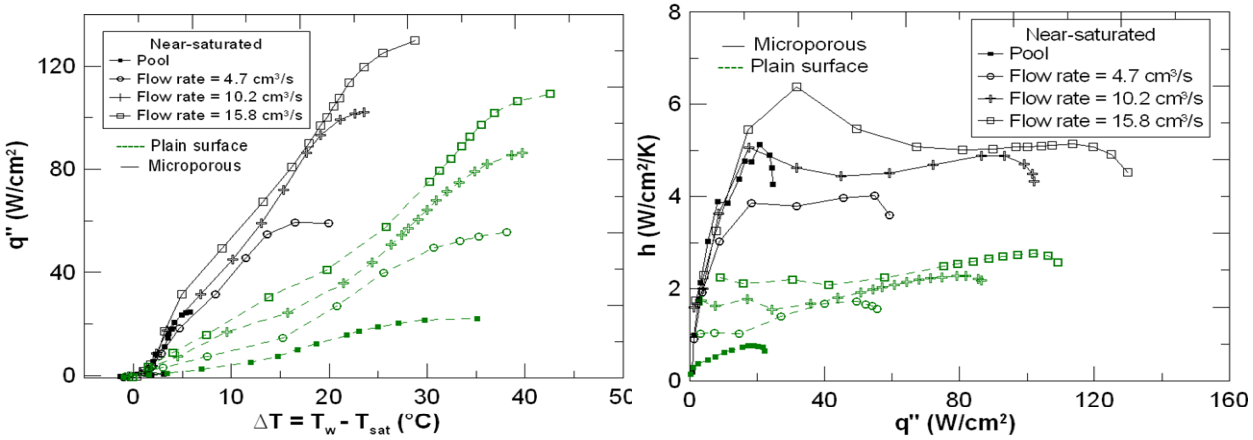

Fig. 25. Spray boiling curves (left) and heat transfer coefficients (right) for plain and microporous surfaces

Figure 9 shows the boiling curves (left) and heat transfer coefficients (right) for plain and microporous coated surfaces for the near-saturated conditions. With regard to the plain surface, the effect of increasing flow rate (from pool boiling to 15.8 m^3/s) is a distinct increase in heat transfer coefficients and CHF. This is due to the increasing forced convection effects. However, the same is not true for the microporous coated surface. At lower heat fluxes, the pool and spray boiling curves for the microporous coating essentially overlap each other, thus demonstrating minimal difference in performance. Therefore, the results suggest that for the microporous coating, nucleate boiling heat transfer is the dominant heat transfer mechanism and is therefore less sensitive to forced convection effects. These results are very promising because they imply that passive two-phase cooling implemented on a microporous coated surface (at zero pumping power) can produce the same heat transfer performance as spray cooling. However, the added forced convection effects of spray cooling do significantly increase CHF for both the coated and plain surfaces.

System/Package-Level Implications

An analysis was then conducted to estimate the effect of the enhanced surfaces on the system/package level thermal performance. This process consisted of running finite element model simulations to quantify the total package thermal resistance (junction to liquid) at various magnitudes of cooling (i.e., varying the convection coefficient applied to the cooled surface). A Semikron SKM power electronics package was used for these simulations. Two package configurations were considered: the entire package configuration where cooling is provided by a cold plate attached to the package base plate, and a direct-cooled direct-bond-copper (DBC) configuration where cooling is provided directly to the backside of the DBC. The resulting plots are shown in Figure 10. In this plot the total package thermal resistance (junction to liquid) is plotted as a function of the inverse of the heat transfer coefficient.

Two different cooling schemes utilizing enhanced surfaces were considered: one implementing single-phase jet impingement cooling with a MicroCool surface and one implementing two-phase immersion boiling with the microporous coating. The performance of the enhanced surfaces was simulated by using the experimentally measured heat transfer coefficients and compared with the performance of a channel flow cooling configuration (Figure 10). The results show that implementing single-phase jet impingement cooling with a MicroCool surface can decrease the total thermal resistance by 11% and 39% in the entire package and direct-cooled DBC configurations, respectively. Similarly, implementing two-phase cooling with a microporous surface can decrease the total thermal resistance by 16% and 61% in the entire package and direct-cooled DBC configurations, respectively.

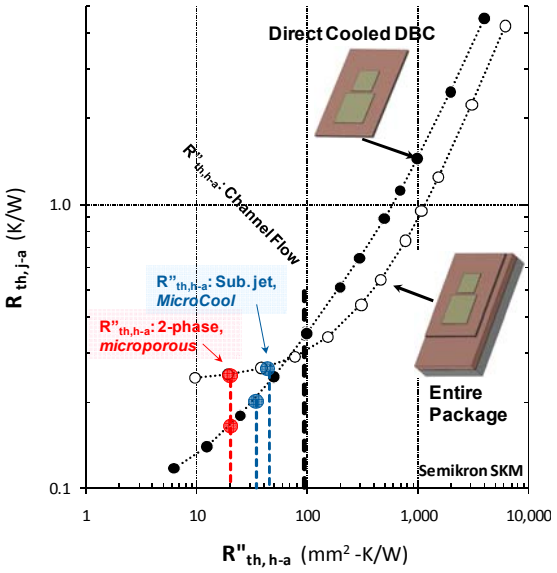

Fig. 26. Total thermal resistance as a function of the inverse of the convective coefficient.

Conclusions

Experiments were conducted to evaluate the use of enhanced surfaces as a means of enhancing heat transfer in both the single- and two-phase heat transfer regimes. Results demonstrate that surface enhancement techniques are a simple yet effective means of improving heat transfer efficiency that have the potential to increase the specific power and power density of automotive power electronics. Some of the major conclusions from this project are presented below.

Single-Phase Heat Transfer

- Results indicate that the enhanced surfaces tested would not be effective at enhancing heat transfer if utilized in channel flow within relatively large passages at velocities less than 2 m/s.
- In the free jet impingement configuration, the copper microporous coating (3M) produced the greatest heat transfer enhancement— about 130%.
- In the submerged jet impingement configuration, the MicroCool finned surface (Wolverine Tube, Inc.) produced the greatest heat transfer enhancement—about 100%.

Two-Phase Heat Transfer:

- The copper microporous coating (3M) increased nucleate boiling heat transfer rates by 100%–500% and increased the CHF by 7%–20% in pool boiling and spray impingement boiling configurations.
- The 20-μm-long copper nanowire coating (University of Colorado at Boulder) provided an ~100% increase in heat transfer coefficients and an ~5% increase in the CHF.

Publications

1. Thiagarajan, S. J., Narumanchi, S., King, C., Wang, W., and Yang, R., 2010, "Enhancement of Heat Transfer with Pool and Spray Impingement Boiling on Microporous and Nanowire Surface Coatings," Proc. 14th International Heat Transfer Conference IHTC-14, Washington, DC, USA.

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5.3 Electric Motor Thermal Management

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Objectives

The Thermal Management of Advanced Power Electronics and Electric Motors (APEEM) activity under the U.S. Department of Energy's (DOE) Vehicle Technologies Program (VTP) seeks to develop power electronics and electric machine technology that meets specific research and development technical targets. Meeting these targets is necessary to achieve widespread commercialization of eco-friendly advanced vehicle technologies, which include hybrid electric, plug-in hybrid electric, electric, and fuel cell vehicles. By commercializing these advanced vehicle technologies, the United States can reduce the amount of petroleum used in transportation.

The technical targets that researchers are addressing allow for smaller component volumes, lower costs, and lower weights without sacrificing performance or reliability. Thermal management plays an important role in the cost, weight, volume, and robustness of electric drive systems. For this reason, the APEEM activity has developed an active research and development effort for thermal management of power electronics. With the transition to more electrically dominant vehicle propulsion systems comes an increase in the importance of thermal management of electric machines. Thermal constraints are a primary limitation on the ultimate performance of electric machines, and there is a direct trade-off between thermal management and over sizing of electric machines to operate within the thermal constraints.

The goal of this research project is to characterize the current state of thermal management technologies for electric traction-drive machines and quantify the impact of thermal management on the performance of electric machines. The ultimate goal is to identify areas for improvement or identify knowledge gaps that would benefit from additional research. The research objectives are summarized as follows:

- Establish a foundation on which to evaluate potential improvements to electric machine thermal management.
- Identify where additional research into thermal management of electric machines could significantly improve the performance characteristics of electric machines relative to the APEEM technology targets [1].
- Identify areas of application for improved thermal management technologies.

Approach

The work for FY 2010 is summarized as follows:

- Research current electric machine thermal management methods used in automotive applications.

- Review techniques to quantify the heat load distribution of electric machines within the winding, stator, and rotor. Select critical operating points and begin development of methods for quantifying heat loads to support thermal analysis of electric machines that are compatible with widely available commercial software tools.
- Identify methods for utilizing finite element analysis (FEA) methods as applied to loss prediction and thermal response of electric machines.
- Research methods available within the published literature for developing reduced order lumped parameter thermal models for electric machines.

Major Accomplishments

The key accomplishments for FY 2010 included a thorough review of the current state-of-the-art of thermal management technologies as applied to electric traction drive machines for automotive applications. In FY 2010 we developed a collaboration with the University of Wisconsin – Madison to initiate this task. The collaboration accomplished the following:

- Performed a literature review of technical publications including journal papers, conference papers, and patents describing current cooling methods used in electric machines as applied to automotive applications.
- Searched existing publications describing current modeling tools to predict the thermal performance of electric machines.
- Reviewed methods for FEA as applied to electromagnetic and thermal analysis.
- Investigated approaches to develop reduced order or lumped parameter loss and thermal models for electric machines.
- Initiated efforts to begin development of models for loss prediction within electric machines and the thermal response as applied to interior permanent magnet machines.
- Identified areas for future contributions to the existing knowledge base related to electric machine thermal management.

Future Direction

Future work will apply the knowledge gained through FY 2010 to develop the necessary analytical methods to evaluate alternative thermal management technologies. Specifically, next year will focus on:

- Developing analytical methods compatible with commercial software tools to quantify heat load distributions for selected critical operating conditions.
- Creating an interior permanent magnet (IPM) machine thermal model and gain confidence in the model to initiate sensitivity analysis of alternative cooling methods.
- Building a lumped parameter modeling approach for the thermal response of IPM electric machines.
- Applying analysis to the development of promising cooling technologies as applied to electric machines.
- Expanding work and methods to other machine types consistent with electric machine research within the APEEM activity.

Technical Discussion

The ability to remove heat from the electric machine poses one of the major constraints on the designer's ability to achieve higher machine power density values. For this reason, with the support of DOE, NREL initiated in FY 2010 an investigation into the potential opportunities of improved thermal management of electric machines. To support this effort, NREL partnered with the University of Wisconsin – Madison because of their recognized expertise in the design and analysis of electric machines. The work performed during FY 2010 was primarily to provide a solid foundation summarizing previously published

work related to electric machine thermal management. The goal was to provide a thermal researcher or engineer not skilled in the art of electric machine design with an introduction to thermal management challenges associated with electric machines. The work described in this summary report includes the following main areas of discussion:

- Review thermal impacts of different machine types.
- Discuss thermal interfaces and material properties for electric machines.
- Describe cooling technologies for electric machines used for traction drive applications in the automotive industry.
- Identify thermal issues for electric machines that warrant additional investigation.
- Review current modeling methods for electric machines for loss prediction and thermal analysis.

Electric Machine Review

The basic machine types covered in this project were IPM synchronous machines and induction machines. Another term sometimes applied to permanent magnet synchronous machines is "DC brushless" machines. Brush-type DC machines with commutators and permanent magnet fields are completely different types of machines. Brushed DC machines have been widely used for electric traction in the past and are still used today for niche applications. Brush-type DC machines are gradually disappearing from traction applications because of their lower efficiency and higher maintenance requirements associated with the brushes and commutators. IPM synchronous and induction machines are the dominant machines used for electric traction drives. There is no clear winner between them for hybrid-electric, electric, and fuel-cell vehicles. Most current hybrid and electric passenger vehicles use IPM machines, except for the Tesla Motors Roadster, which uses an induction machine. The General Motors EV1 and earlier models of the Chevrolet hybrid Silverado and GMC Sierra pickup trucks also used induction machines. When coupled with modern solid-state inverters, IPM and induction machines can provide attractive combinations of conflicting design goals such as high efficiency, high reliability, low maintenance, high power/torque density, wide constant-power speed range, and low vibration and acoustic noise.

Comparison of Machine Types

The fundamental difference between an IPM and an induction machine is the presence of permanent magnets built into an IPM machine's rotor. These magnets provide magnetic field excitation in the machine's air gap without electrical current. The magnets enable the IPM machines to achieve a higher torque density and higher efficiency as compared to other machine types. On the other hand, the permanent magnets deliver this magnetic excitation with a fixed amplitude that cannot be reduced for increased efficiency at low torque or during high-speed, field-weakening operation.

An induction machine's stator currents induce currents in the rotor bars that interact with the stator magnetic field to create torque. A portion of the stator current must be used to produce magnetic flux in the induction machine's air gap. The need to use stator current to produce the magnetic flux places the induction machine at a disadvantage when compared to permanent magnet synchronous machines for achieving maximum efficiency at rated power. However, the ability to control the stator current in an induction machine makes it possible to adjust the airgap magnetic flux amplitude. The flexibility to adjust the magnetic flux provides advantages for achieving maximum efficiency during part load operation [2]. Ultimately, the relative advantages and disadvantages of IPM machines and induction machines must be compared for every set of traction drive specifications to determine which one is the better choice for particular applications.

There is also interest in other types of electric machines for traction applications, such as the switched reluctance (SR) machine. Although there are no current production passenger vehicles that use SR

machines in their traction drives, a couple large manufacturers of construction equipment, including Caterpillar and LeTourneau, have adopted the SR machine in some models of their earth-moving equipment. SR machines are appealing choices for this special class of traction application because they have rugged rotors. Also, some of the known limitations of SR machines, including higher torque ripple and acoustic noise, are not as problematic in earth-moving equipment as they would be in passenger vehicles.

Tables 1 and 2 summarize the relative advantages and disadvantages of permanent magnet machines and induction machines. In addition to the items listed, there are a number of concerns about the supply and prices of rare-earth permanent magnet materials. An example is dysprosium. Dysprosium is a metal used to improve the high-temperature magnetic properties of NdFeB magnets, and it has tended to have particularly high and volatile pricing. This is one area in which the thermal management of permanent magnet machines may be able to impact the cost of permanent magnet machines.

Table 4. Advantages and disadvantages of permanent magnet machines

Advantages	Disadvantages
• Higher torque and power density. • Higher efficiency than induction machines at medium to higher loads. • Lower rotor losses result in lower rotor cooling requirements. • Rotor magnetic saliency in IPM machines makes them better candidates for sensing rotor position at zero speed.	• Field strength of magnets cannot be adjusted, requiring special machine and controller designs for high-speed, flux-weakening operation. • Cost and availability concerns related to high-strength rare-earth magnets. • Permanent magnet performance generally decreases with increasing temperature. • Permanent magnets are susceptible to demagnetization due to overheating and electrical faults.

Table 5. Advantages and disadvantages of induction machines

Advantages	Disadvantages
• Ability to adjust stator flux amplitude using stator currents can be used to boost machine efficiency under partial load conditions. • Absence of permanent magnets eliminates associated concerns about magnet cost and availability. • Rotors are rugged and can tolerate higher temperatures due to absence of magnets.	• Torque cannot be produced without rotor currents that generate losses and heat. • High-efficiency induction machines require special rotor designs using copper that raises machine cost and reduces robustness. • Rotor losses increase with rotor temperature. • Detecting rotor position at zero speed without encoder or resolver is difficult when maximum starting torque is required.

Winding Structures and Impacts on Motor Cooling

The stators for induction machines and IPM machines are very similar with the exception of concentrated-winding permanent magnet machine stators that are not normally used for induction machines. For example, Remy International, Inc.'s line of high-voltage hairpin machines for hybrid and electric vehicles is designed to use the same stator with both permanent magnet and induction rotors available as options [3, 4]. For this reason, improvements related to stator cooling for distributed winding machines would be relevant to permanent magnet machines and induction machines.

Distributed windings have advantages and disadvantages compared to concentrated machine windings. For example, distributed windings increase the mass of the machine because of the significant amount of copper in the end windings. The end windings also increase the volume needed for the machine. Advantages and disadvantages of distributed windings relative to concentrated windings in items related to thermal management are listed in Table 3. As listed in Table 3, concentrated windings produce

increased losses within the rotor and magnets. Depending on the form factor of the machine (stack length), the increase in rotor losses could present challenges related to extracting the heat from the magnet and rotor.

Table 6. Advantages and disadvantages of distributed windings relative to concentrated windings related to thermal management

Advantages	Disadvantages
• Lower rotor losses • Increased end winding area that is available for cooling • Lower losses in magnet material	• Increased copper conduction losses due to longer distances current must travel

Machine Thermal Interfaces and Material Properties

To support subsequent development of thermal models, an understanding of the material options, uses, and properties utilized in commercial automotive traction drive system was required. As with power semiconductor packaging, thermal interfaces within electrical machines are a critical component of heat removal. A brief discussion of thermal interfaces is included below. In addition, a discussion of relevant thermal properties in relation to materials used for electric machine construction and cooling is highlighted.

Critical Thermal Interfaces

A number of thermal interfaces exist in the construction of electric machines. Interfaces related to stacked laminations, the stator to housing assembly, and the winding slot are described below. These thermal interfaces have a significant impact on the thermal management of electric machines, and the thermal contact resistance is difficult to quantify because of manufacturing variability.

Lamination Thermal Interface

The thermal conductivity of steel laminations used within the stator and rotor is anisotropic because heat conducted normal to the plane of the laminations needs to be conducted across each interlamination gap. Heat conducted parallel to the plane of laminations does not cross the interface boundaries. For thermal conduction in directions parallel to the laminations' surfaces, thermal conductivity can be estimated as a weighted average of the two materials' thermal conductivity as listed in Equation 1.

$$k_{th} = k_1 \, p_1 + k_2 \, p_2 \tag{1}$$

The average thermal conductivity of the combined lamination and interlamination gaps is k_{th}, k_1 is the thermal conductivity of the steel lamination material, and p_1 is the fractional portion (dimensionless) of the overall lamination stack made of up by the lamination steel. The term k_2 is the thermal conductivity of the coating material or inter-laminar gap material such as air or enamel, and p_2 is the fractional portion of the stack made up of the gap. The result is nearly the same as the product of the lamination steel's thermal conductivity and the stacking factor (usually in the range of 0.95 to 0.99). The thermal conductivity parallel to the laminations' planes will be only slightly less than the steel's thermal conductivity [5].

The thermal conductivity across the laminations is more complicated than thermal conductivity parallel to laminations, especially for lamination stacks that are not vacuum impregnated or otherwise glued together creating continuous and predictable thermal conductance between laminations. The average cross-lamination thermal conductivity varies with:

- Thickness of individual laminations
- Lamination surface finish details such as roughness and burrs

- Type and thickness of inter-laminar filling materials
- Lamination stack clamping force and variation in clamping pressure

There has been some literature published on thermal conductivity of stacked laminations. However, there is some scatter in the published thermal conductivity values for lamination stacks, and it can be necessary to test specific cases to be sure of accurate and relevant data. Figure 1a shows the thermal contact resistance per joint, providing an initial estimate into the thermal contact resistance of stacked laminations. The importance of the lamination contact resistance is shown in Figure 1b. Figure 1b shows that the contact resistance accounts for over 80% of the overall thermal resistance through the lamination.

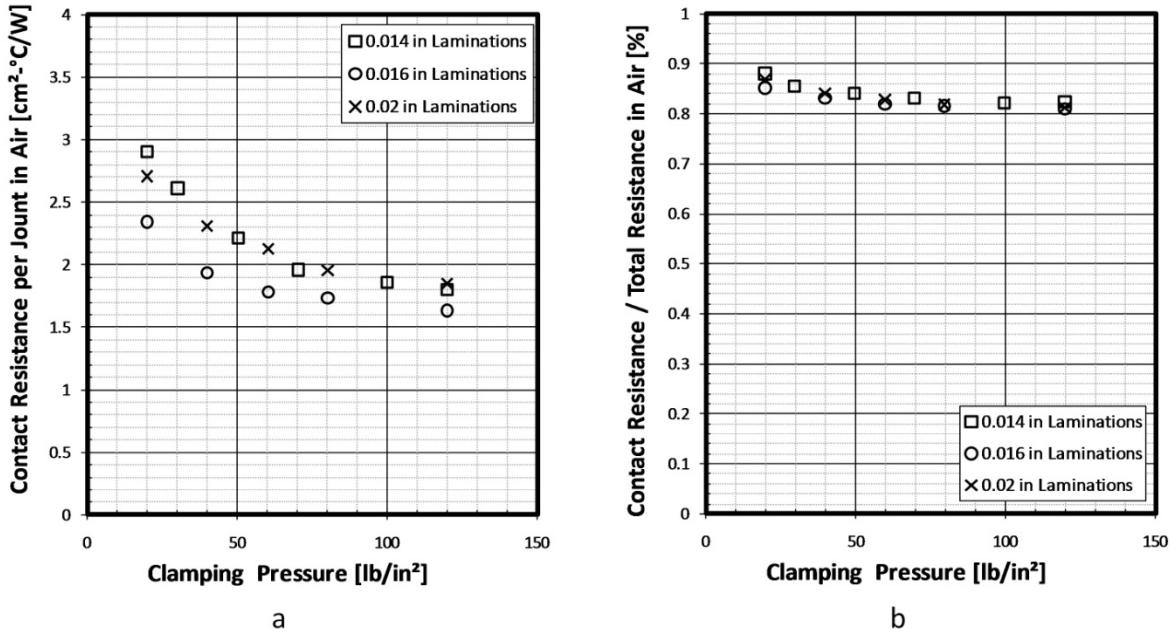

Fig. 27. Thermal contact resistance across laminations, extracted from [6]: (a) Thermal contact resistance per joint for stacked laminations; (b) Ratio of total lamination stack resistance due to contact resistance.

It is interesting to note the similarity in the contact resistance per joint for laminations of different thickness as seen in Figure 1. Figure 1 highlights one of the tradeoffs associated with designing machines where the axial heat conduction through the rotor is important. Using thinner laminations enables the designer to reduce eddy-current losses, especially at higher frequencies. However, the stack with thinner laminations will generally have increased overall thermal resistance in the axial direction because of the increased number of lamination interfaces. Another thermal design conflict arises when a designer seeks to lower the eddy current losses by increasing the lamination steel silicon content because the electrical steel's thermal conductivity tends to decrease as the silicon content increases (Table 5).

The importance of axial heat conduction through the laminations applies to a range of machine configurations. For distributed winding IPM machines, the axial heat conduction can be especially important for machines with longer aspect ratios that require a longer axial heat flow path. It also applies to IPM machines with concentrated stator windings, which tend to have a somewhat higher proportion of their losses in the rotor than distributed-winding machines. The discussion applies less to induction machines since their rotors have good axial heat transfer through the squirrel-cage rotor bar.

Case-to-Stator Thermal Interface

Thermal conduction across interfaces between solids can be the most limiting thermal resistance in some types of machines, and it is also one of the most variable in terms of machine-to-machine variation. For example, another critical thermal resistance is the interface between the stator laminations and the motor housing or case. The previous discussion of cross-lamination thermal resistance does not transfer to the thermal interface between the stator lamination stack and a shrink-fit machine housing. The relatively uniform flatness and surface finish of reasonably high-quality stacked laminations leads to fairly consistent cross-lamination thermal conductivity even if the clamping pressure varies, as seen in Figure 1a.

Totally enclosed fan-cooled (TEFC) machines usually have finned jackets that are shrunk-fit around the lamination stacks. Most of the machine's dissipated heat must cross the thermal interface between the lamination stack and the motor housing or jacket before the heat can be dissipated through the fins. Table 4 lists sample values for metal to metal thermal contact resistance. As can be seen there is a large variation that is possible. One additional challenge is the potential difference in thermal expansion between stator laminations and the housing, which can lead to an increase in the interface resistance as the gap increases with higher temperature

Table 7. Sample solid-to-solid thermal contact resistance values

Condition	Contact Resistance [mm²-K/W]
Iron – Aluminum [7]	25-250
Aluminum – Aluminum with Air [8]	275

Winding Slot Thermal Resistance

Another important thermal interface is the interface between the windings in the stator slots and the stator laminations [7]. A discussion of modeling approaches for the winding to stator lamination interface in found in [9]. The paper by Jih lists an approximation for the axial or out-of-plane thermal conductivity of the material within the stator slot (Equation 2). The parameter k_{eff} is the overall effective axial thermal conductivity of the bulk material, where k and A correspond to each of the respective material thermal conductivities and areas. A_{tot} is the total slot cross section area. The overall effective in-plane thermal conductivity can be obtained through finite element analysis (FEA) of the real materials within the stator slot [9].

$$k_{eff} = k_{cu}\frac{A_{cu}}{A_{tot}} + k_{coat}\frac{A_{coat}}{A_{tot}} + k_{resin}\frac{A_{resin}}{A_{tot}}k_{paper}\frac{A_{paper}}{A_{tot}} \quad (2)$$

Stanton proposes two alternative methods for estimating the thermal resistance between the winding and stator lamination [7]. One method attempts to correlate the effective in-plate thermal conductivity to the stator slot filling factor. With this method a range of 0.06 W/m-K to 0.09 W/m-K is listed for the in-plane thermal conductivity. The other approach approximates the slot with a series of layered windings. More details related to this approach are available in [7].

Electric Machine Thermal Properties

To support the development of thermal models for electric machines, an effort was made to collect representative thermal properties of materials used in electric machine design. The listed materials and properties are not assumed to be an exhaustive list, but it is an attempt to provide the thermal design engineer and overview of representative materials.

Table 5 presents some of the key material properties for selected motor related materials. The range shown for the thermal conductivity of steel reflects the decrease in electrical steel's thermal conductivity with increasing silicon content, as discussed in [7]. Silicon is commonly added to electrical steels used in electric machines in order to increase its electrical resistivity, which, in turn, decreases the steel's eddy current losses especially at high excitation frequencies and high speed. However, steel's thermal conductivity also decreases with increasing silicon content. The data for epoxy is from [10] and properties for sintered NdFeB rare-earth permanent-magnet material are from [11]. The properties for the wire coating and insulation paper are taken from [9].

The cross-lamination average thermal conductivity values for the laminations shown in Table 5 were calculated assuming the laminations were glued together with continuous contact assuming a thermal conductivity of 0.15 W/m-K and 0.6 W/m-K for the epoxy. Another approach to estimate the cross lamination thermal conductivity is also listed in Table 5 as "Across Laminations (alternate method without epoxy fill)." This method represents laminations that are stacked and compressed but not glued together. This method, used by Hsu [12], yields similar results to the data reported by Williams [6].

Table 8. Solid material properties for selected materials

Material	Specific Heat	Density	Thermal Conductivity
	[J/kg-K]	[kg/m^3]	[W/m-K]
Low-carbon Steel	481	7849	55
Lo-carbon Steel, 2.5% Si	480	7825	30
Lo-carbon Steel, 5% Si	480	7800	17
Epoxy	1660	1200	0.15
Along Laminations (Epoxy fill with k=0.15 W/m-K)	540	7517	53.3
Across Laminations (Epoxy fill with k=0.15 W/m-K)	540	7517	5.6
Epoxy	1660	1200	0.6
Along Laminations (Epoxy fill with k=0.6 W/m-K)	596	7201	53.4
Across Laminations (Epoxy fill with k=0.6 W/m-K)	596	7201	14.8
Across Laminations (alternate method without epoxy fill)	596	7201	1.7
NdFeB (Sintered)	450	7500	7
Wire Coating (Mylar)	1172	1390	0.155
Insulation Paper Liner	1660	1250	0.144

The range of cross-lamination thermal conductivity values between 1.7 and 14.8 W/m-K (Table 5) represents real variation in the cross-lamination thermal conductivity of manufactured machines. While this variation causes complications for the machine thermal analysis, there is evidence that the variation of the cross-lamination thermal conductivity among "identical" machines units produced using the same automated manufacturing equipment is relatively modest.

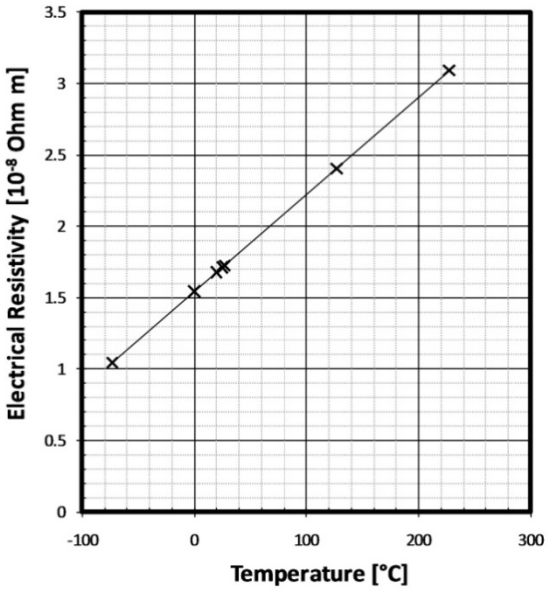

Fig. 28. Electric resistivity vs. temperature for pure copper [13]

In addition to the thermal properties, the electrical properties of some materials are important when evaluating the thermal characteristics of electric machines. For example, the electrical resistivity of copper varies significantly over the full operating temperature range expected in an electric vehicle application. Figure 2 shows the variation of electrical resistivity for pure copper over a range of temperatures [13]. Using the data shown in Figure 2, the electrical resistivity of copper ranges between 1.41×10^{-8} and 2.9×10^{-8} at –20°C and 200°C, respectively. This represents almost a factor of 2 increase in thermal resistance. The change in thermal resistance for a given operating temperature leads to changes in loss density such as variation in conduction losses within windings. It also changes the electric machine's electromagnetic dynamics as discussed in [14]. The interaction between the machine's electromagnetic performance and thermal performance highlights the need to understand the thermal characteristics of electric machines. It also demonstrates why coupling between electromagnetic and thermal analysis is important.

Several coolant fluids are used in automotive applications for cooling electric machines. Common fluids include air, water–ethylene glycol mixtures, and transmission oil. Fluid properties are not included in this summary report, but the following references were used for the fluid properties. Air properties were based on tabulated data commonly available in fluids and heat transfer text books such as those by Incropera and Munson [8, 15]. Water–ethylene glycol fluid properties were based on correlations provided by Alshamani [16]. Properties for automatic transmission fluids were obtained from data from Kemp and James [17] and Maranville et al. [18].

Review of Current Cooling Technologies

A number of different cooling techniques are currently used for thermal management of electric machines. A thorough review is not possible in this summary report, but a summary of the two most common methods are described along with advantages and disadvantages. A machine design often has more than one cooling technique used in combination with others. The cooling techniques highlighted below include:

- Air cooling with natural or forced convection
- Single-phase liquid cooling with water–ethylene glycol or transmission oil.

Air Cooling

Two common forms of air cooling in use for automotive applications include totally enclosed non-ventilated (TENV) systems and TEFC systems. An example of a machine that relies solely on a TENV system is the Honda mild hybrid system. The Honda parallel hybrid systems have a high ratio of peak power to average power, where most of the operation is at low power. The TENV offers a simple, compact, and lightweight system. A schematic of the machine is seen in [19]. The air-cooled system for the Tesla Motors Roadster is an example of a TEFC system. As a full electric vehicle, the Tesla system must be capable of removing higher heat loads. To accomplish this, the Tesla induction motor is surrounded by a dense arrangement of cooling fins that are designed to extract heat from the stator. Photos of the Tesla system are available in [20].

The benefits of air cooling are primarily associated with its simplicity because there are no liquids to pump, seal, and maintain. This can be an advantage to vehicle applications that do not already have other liquid cooling loops. The major limitation of air cooling is the lower heat transfer capability. Air cooling results in a higher machine mass to deliver the same output power. Advantages and disadvantages of air cooling for electric machines is summarized in Table 6.

Table 9. Advantages and disadvantages of air cooling

Advantages	Disadvantages
• Simplicity compared to alternative cooling techniques • Low cost • Low maintenance • No liquid leaks	• Much lower heat transfer capacity per area or volume, requiring larger machine for same power rating • Potential for high pumping losses and acoustic noise • Filtering of the air may be required • Sensitive to ambient air temperature

Single-Phase Liquid Cooling

Common forms of single-phase liquid cooling include using water-ethylene glycol and transmission oil. Often both are used in a single liquid-cooled design. For example, oil is actively sprayed or passively slung within the machine housing to transfer heat away from the rotor and end windings, and a pumped water-ethylene glycol cooling loop is then used to transfer heat out of the system to a radiator. Cooling with water-ethylene glycol is an efficient way to transfer heat and dissipate heat via a radiator. However, its major disadvantages are that it has poor dielectric properties. Lindström models a liquid-cooled IPM machine [21], and Kral provides an example of a water-cooled induction machine [22].

In contrast, oil is more compatible for use inside machines. Oil cooling is used for rotors and end windings in a number of current production models of hybrid vehicles. It is most useful inside machine housings in locations where its dielectric strength is important, such as the cooling of the stator windings using either active spraying or passive slinging configurations. Examples of oil cooling include patents from Remy and GE [23, 24]. Other examples of liquid cooling using combinations of water-ethylene glycol and oil are included in the following reports [12, 25, 26]. The benefits and disadvantages of cooling with oil and water ethylene glycol are summarized in Tables 7 and 8.

Table 10. Advantages and disadvantages of oil cooling

Advantages	Disadvantages
• Raises achievable machine torque and power as compared to air cooling • Excellent dielectric properties • Effective for spray cooling of windings and ends of rotors • Common in automotive drives systems	• Potential for leaks • High viscosity causes higher pumping losses • Lower thermal conductivity as compared to water • Maintenance

Table 11. Advantages and disadvantages of water cooling

Advantages	Disadvantages
• Raises achievable machine torque and power as compared to air cooling. • Common in automotive drives systems	• Potential for leaks • Poor dielectric properties make it unacceptable for use inside the machine housing • Material compatibility • Maintenance

Critical Thermal Management Areas

The critical thermal paths for electric traction machines depend on the machine type, usage conditions, cooling methods, and manufacturing methods. However, some general statements can be made identifying the critical heat transfer paths for many of the electric traction machines. In general, a few of the critical heat transfer paths are among the following:

- Heat transfer from the copper conductors in the stator slots through their protective layers of electrical insulation into the stator core
- Heat transfer from the stator core into the stator housing, crossing the mechanical interface between the stack of steel laminations and the housing, which is often shrunk-fit onto the stator core
- Heat transfer from the copper conductors in the stator end windings through their protective layers of electrical insulation into the air cavities at the two ends of the stator core
- Heat transfer from the rotor magnets into the surrounding rotor core for IPM machines
- Heat transfer from the rotating rotor magnetic core into the shaft and beyond to the connected mechanical load or through the bearings into the stator housing.

It should also be noted that in some machines, the best heat transfer path out of the rotor is through the bearings. This places additional design constraints on the bearings. For example, in a design where maximum rotor temperatures are high (maximum rotor temperatures tend to be higher in induction and SR machines than in permanent magnet machines), the bearings and coolants might experience their peak temperature exposure during post-shutdown events due to heat conducted from a hot rotor.

Electric Machine Modeling Efforts

In addition to the above-mentioned work to collect and review published information associated with electric machine thermal management, efforts were also made in FY 2010 to review published techniques for modeling the thermal behavior of electric machines. A detailed review of this effort is excluded from this summary report, but the modeling work will be a primary focus through FY 2011. There are two different but related approaches to modeling losses and heat transfer in electric machines: lumped parameter equivalent circuit models, and FEA models. There are some effects that couple the electromagnetic and thermal analysis. For example, loss distributions affect temperature distribution. Since electrical conductivity, magnetic losses, and coolant heat transfer properties all vary significantly with temperature, there are cross-couplings between the electrical and thermal behavior. The modeling of these cross-coupled effects is an area of current research.

Conclusion

The goal of this research project is to improve thermal management of electric machines to impact the achievable continuous power density needed to meet the needs of more electrically dominant vehicle applications. To determine the impact of thermal management technologies the project is developing methods to link high-level program targets such as power density to meaningful thermal performance targets and motor cooling technologies. The result of the project will quantitatively highlight the impact of thermal management on electric machines and identify areas that would benefit from additional research.

To accomplish these objectives the work in FY 2010 focused on developing a collaboration with recognized experts in the design and analysis of electric machines to establish a foundation on which to build the necessary analysis capabilities. Efforts were made in FY 2010 to perform detailed literature searches including journal publications, conference papers, and patents describing current cooling methods used in automotive traction drive electric machines. In addition, work was performed to identify existing publications describing modeling tools to predict the thermal performance of electric machines. This included methods for FEA as applied to electromagnetic and thermal analysis. In addition to FEA methods, other approaches including reduced-order or lumped-parameter electric machine electrical and thermal models were investigated. The results of the work in FY 2010 identified areas for future contribution to the art of electric machine thermal management, and future efforts will focus on applying the knowledge gained during FY 2010 to develop the necessary analytical and experimental methods to evaluate new cooling technologies for electric machines.

Acknowledgements

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5.4 Power Electronics Thermal System Performance and Integration

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Objectives

Electric drive systems, which include electric machines and power electronics, are a key enabling technology for advanced vehicle propulsion systems that reduce the transportation sector's petroleum dependence. To have wide application, electric drive technologies must be economical in terms of cost, weight, and size while meeting performance and reliability expectations. The push to reduce the cost, weight, and size of critical electric drive components presents significant challenges related to thermal management and system integration. The integration of thermal management technologies with electric drive components must be done at a system level instead of as an afterthought at the end of the design process. The system approach requires a thorough understanding of the interactions between hardware design and thermal management technologies. This project will develop techniques to improve the integrated design of both hardware and thermal management technologies. The end result will facilitate the integration of advanced power electronics thermal management technologies into commercially viable advanced automotive systems, including hybrid electric, plug-in hybrid electric, electric, and fuel cell vehicles.

Approach

The Thermal Management of Advanced Power Electronics and Electric Motors (APEEM) activity in the Department of Energy's (DOE) Vehicle Technologies Program (VTP) is currently developing and assessing the performance of a suite of advanced thermal cooling technologies, including single-phase and two-phase jet impingement, air cooling, low thermal resistance insulated gate bipolar transistor (IGBT) structures, improved thermal interface materials, and direct-cooled substrates. In order to evaluate, design, and develop thermal cooling systems that enable commercially viable products, a systems approach is required that bridges the gap between the component thermal response characteristics and new or innovative cooling technologies. In FY 2010 this project focused on three areas:

- Apply the previously developed integrated thermal management technique [1] to a wide range of commercial modules and new concepts developed within the APEEM activity with collaboration from Oak Ridge National Laboratory (ORNL).
- Develop experimental capabilities to measure the thermal performance of power semiconductor packages with integrated cooling technologies and verify experimental setup with support from a power electronics industry partner.
- Develop in collaboration with ORNL component thermal models to aid in the complete system thermal analysis of electric drive systems. For FY 2010, the work focused on developing a general parametric 3D electro-thermal model for DC-link capacitor thermal analysis. The model will enable analysis of power electronics packaging design alternatives.

Major Accomplishments

The key accomplishments for FY 2010 included collaboration with industry, DOE laboratory partners, and internal NREL thermal research projects to bridge the gap between power electronics components and the application of thermal management technologies. The developed systems analysis methods will be utilized and applied within ongoing and new research efforts related to thermal management of power electronics. Significant accomplishments for FY 2010 are listed below, and additional details are provided in the technical discussion of this report.

- Expansion of package analysis capabilities to a wide range of package configurations to demonstrate the link between package design and cooling technology selection. This work was used during FY 2010 by NREL thermal management researchers to evaluate the potential impacts of new cooling technologies when applied to power semiconductor package cooling.
- Collaboration with ORNL to apply the integrated thermal analysis process to packages under development within the APEEM activity at ORNL. The work demonstrated how the process is a valuable tool for evaluating potential design questions related to package configuration and heat exchanger performance.
- Collaboration with an industry partner on the design and validation of experimental capabilities to measure the steady-state and transient thermal characteristics of power semiconductor packages with integrated cooling technologies. The test capabilities will be a valuable capability to allow NREL thermal management researchers to test new cooling technologies when applied to power semiconductor packages.
- Developed and completed initial validation of a general parametric three-dimensional cylindrical metalized film capacitor thermal model that accounts for: anisotropic conductivity and non-uniform heating in the windings, end spray, and the electrical connections. The work was performed in collaboration with ORNL.

Future Direction

Although the current project ends in FY 2010, the developed analytical and experimental capabilities will feed into FY 2011 research activities to link cooling technology developments to power semiconductor mechanical design characteristics. The capacitor thermal model development will transition into FY 2011 research activities in collaboration with ORNL. The effort will focus on the development of a model for a capacitor module for an electric traction drive system that will be validated using experimental data. The model will enable investigations into how thermal management of the capacitor can be combined with other vehicle thermal management systems.

Technical Discussion

The major accomplishments for FY 2010 are described in more detail in the following four sections.

- Integrated Package and Cooling Thermal Performance – Modeling
- APEEM Packaging Collaboration
- Integrated Package and Cooling Thermal Performance – Experimental Capabilities
- General Parametric Capacitor Thermal Model

Integrated Package and Cooling Thermal Performance – Modeling

This paper outlines a method for investigating the system-level integrated performance of power semiconductor package configurations and heat exchanger technologies. The work was presented at the IMAPS 2nd Advanced Technology Workshop on Automotive Microelectronics and Packaging [2] , and it was included in an FY 2010 milestone to DOE [3]. The technical details are summarized below to illustrate a method for evaluating the integrated thermal performance of both packaging and cooling.

Approach

A range of commercial power semiconductor package configurations were selected to demonstrate the flexibility of the approach and to provide insight to researchers into the interactions between cooling technology development and packaging. Each package consists of an IGBT and diode pair. The selected packages are illustrated in Figure 1, and they represent a range of packaging options and sizes. It should be noted that the packages represent a range of sizes, and the IGBT and diode die areas of each package are not consistent. Except for the package shown in Figure 1e, the basic package layer structure is illustrated in Figure 2 with specific layers listed in Table 1. Layers that are not included in the listed packages are highlighted as "NA." The layer properties (thickness and thermal conductivity) are shown in Table 1. The layer properties were kept consistent across package configurations except where noted. The metallization layers bonded to the substrate were also kept consistent across each package configuration except for the package shown in Figure 1e.

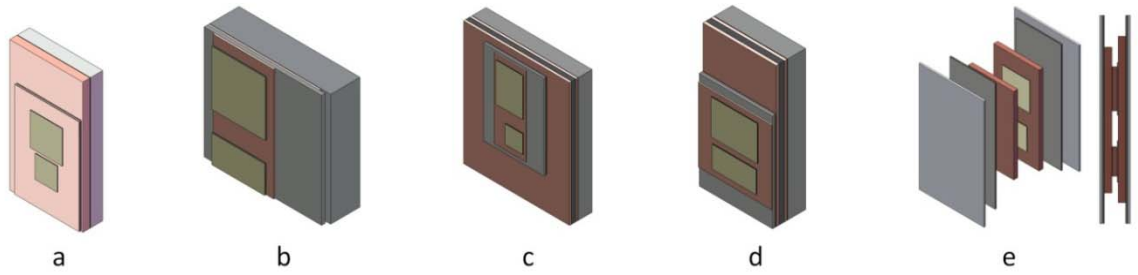

Fig. 29. Alternative package configurations for package thermal performance comparison. Configuration geometries are based on existing commercial packages: (a) Semikron SKM, (b) Semikron SKAI, (c) 2004 Prius, (d) 2007 Camry, (e) 2008 Lexus LS 600H.

Table 12. Package Layer Information

			Layer Properties		Package Configurations				
Layer	Layer		Layer Thickness [mm]	Layer Thermal Conductivity [W/m-K]	a	b	c	d	e
A	IGBT/Diode (Si)		0.12	92	x	x	x	x	See reference [4]
B	Solder		0.127	51	x	x	x	x	
C	Cu		0.25	394	x	x	x	x	
D	Substrate	AlN	0.64	140	NA	x	x	x	
		Al_2O_3	0.38	23	x	NA	NA	NA	
E	Cu		0.25	394	x	x	x	x	
F	Solder		0.127	51	x	NA	x	x	
G	Heat Spreader	Cu	3	394	x	NA	NA	NA	
		Cu-Mo-Cu	0.75-1.5-0.75	394-135-394	NA	NA	x	x	
H	TIM		0.1	1.5	x	x[a]	x	x	
I	Heat Sink		5	154	x	x	x	x	
			Cooled Surface Footprint Area: Ac [cm^2]		15.34	3.90	16.86	7.68	15.00[b]

Notes: [a] Modeled with a TIM (thermal interface material) of reduced thickness (0.05 mm).
[b] The list area is for one side, and it is the same for both surfaces on each side of package.

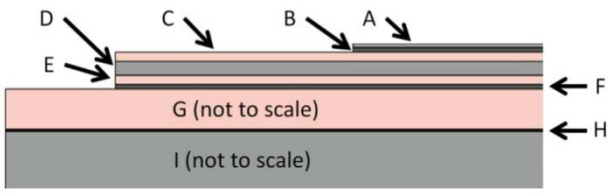

Fig. 30. Package material layer labels for Table 1

Results

A comparison of the listed packages from Figure 1 and Table 1 is shown in Figure 3. Figure 3a compares the total package thermal resistance ($R_{th,j-a}$) against the area-weighted heat exchanger thermal resistance ($R''_{th,h-a}$). The illustrated cooling performance bands for two-phase, forced liquid convection, and air-cooling are based on heat transfer coefficient values from Mudawar [4] and are included for reference. The listed total thermal resistance values of 0.454 K/W and 0.203 K/W are based on estimated single- and double-sided cooling, respectively [5, 6]. The values are included only as a reference to illustrate representative values. The figure shows the impact of double-sided cooling with the Lexus LS 600H package, while the other packages allow cooling on one side of the package. The footprint area of the package is also important. The SKAI module has a small footprint area and requires more aggressive cooling for equivalent performance. In comparison, the Prius package is more spread out with a larger footprint area for cooling. The larger footprint area enables less aggressive cooling for an equivalent thermal performance.

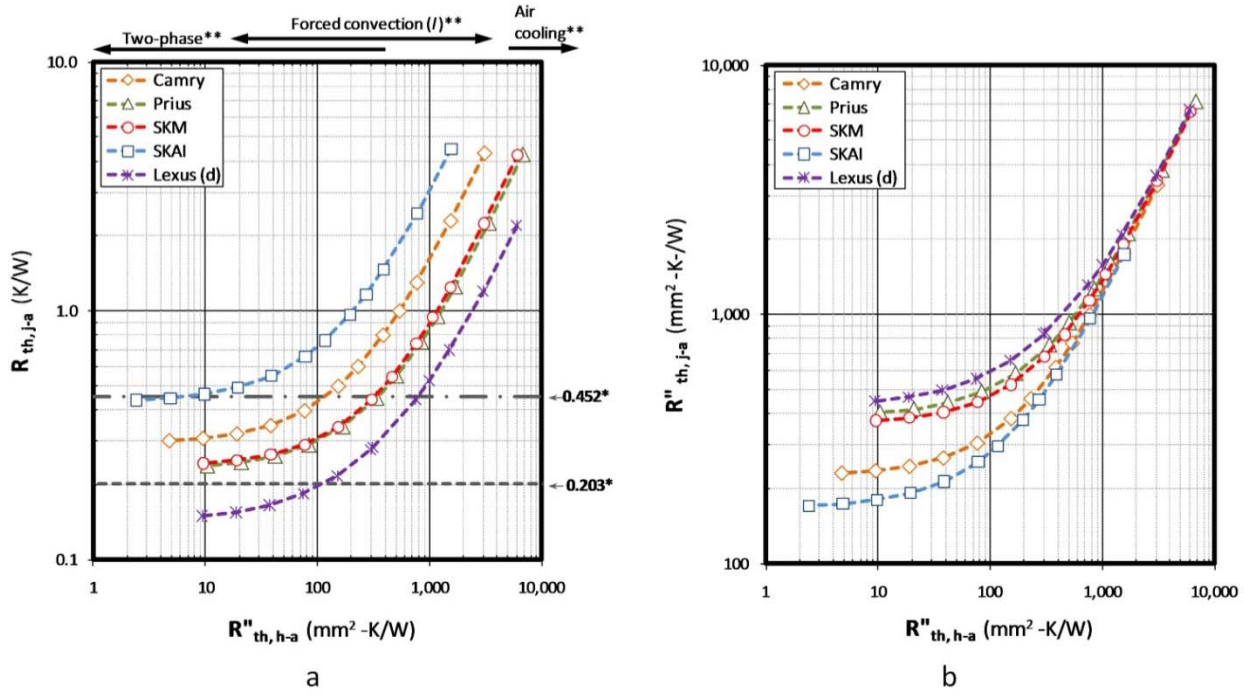

Fig. 31. Package configuration thermal performance. All packages are cooled on one side, except for the Lexus package. Cooling performance ranges are based on Mudawar [4]. (a) Junction to coolant thermal resistance; (b) Unit area junction to coolant thermal resistance.

Figure 3b shows the same data as Figure 3a, but the thermal performance metric is the total thermal resistance multiplied by the total cooled footprint area ($R''_{th,j-a}$). An interesting feature of the graph is seen as the cooling performance decreases. The package performance curves collapse onto a single line as the cooling becomes less aggressive. The results in Figure 3b illustrate how effective a particular packaging technology is at removing heat irrespective of the cooled footprint size. The curves in both Figure 3a and 3b flatten as the area-weighted heat exchanger thermal resistance ($R''_{th,h-a}$) decreases because of other thermal bottlenecks in the package, such as the thermal interface material (TIM). The flattening or leveling off of the curves indicates that further reductions in heat exchanger thermal resistance beyond this region have minimal effect on reducing the thermal resistance of the package.

The developed process can also be used to investigate potential package changes in terms of material selection and package structure. Figure 4 demonstrates the impact of a change in the substrate material for three alternative package configurations based on the Semikron SKM module from Figure 1. The three

package configurations include (1) the baseline configuration shown in Figure 1 and Table 1 with a TIM and aluminum heat sink, (2) a direct-cooled baseplate (DCB) configuration in which the TIM and aluminum heat sink are removed to enable direct cooling of the baseplate, and (3) a direct-cooled direct-bond-copper (DBC) (DCD) configuration in which the baseplate and solder layers are removed to cool the copper surface of the DBC directly. The DCD configuration shown in Figure 4 has a reduced cooling footprint area in comparison to the other packages. Each of the package configurations is evaluated with two substrate material options (viz. Al_2O_3 (0.38 mm) and AlN (0.64 mm)). The results in Figure 4 resemble those seen in Figure 3a. At higher $R''_{th,h-a}$ values, the package footprint plays the dominant role in distinguishing thermal performance. A key point to highlight is that as the cooling technology applied to a particular package improves (lower $R''_{th,h-a}$), the thermal characteristics of the package become more important. As the thermal performance of the heat exchanger improves, the trade-offs between package configuration (geometry and material selection) and cooling technology become apparent.

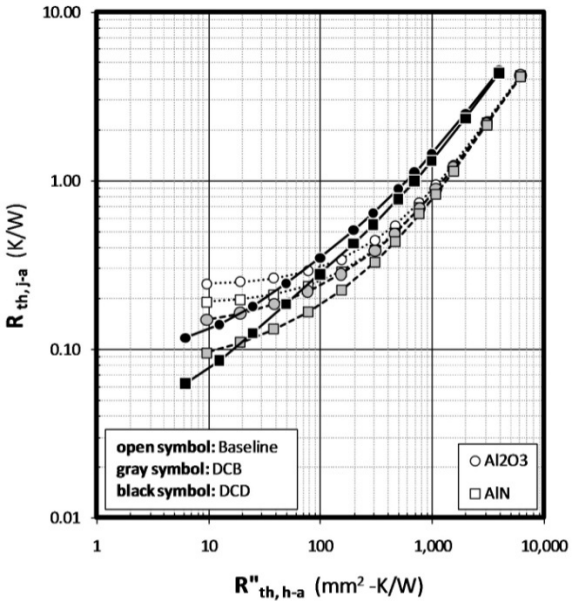

Fig. 32. Material impacts vs. package configuration based on the Semikron SKM package. DCB (direct-cooled baseplate) removes the TIM and aluminum heat exchanger. DCD (direct-cooled DBC) removes the TIM, aluminum heat sink, solder layer, and baseplate.

This work describes a method of integrating techniques for characterizing power semiconductor thermal performance and heat exchanger technologies. The methodology enables an analysis of the system performance and the trade-offs of the combined package and cooling system. It is important to note the importance of matching the heat exchanger thermal performance ($R_{th,h-a}$) with the package thermal performance. The optimal heat transfer mechanism is highly dependent on the package configuration; therefore, the package and heat exchanger need to be evaluated as an integrated system. The combined analysis ensures that one area of the thermal control system is not overdesigned, adding unnecessary cost, weight, and volume to the system.

APEEM Packaging Collaboration

With collaboration from ORNL, the developed process for evaluating the integrated package and heat exchanger thermal performance was applied to the direct-cooled substrate package concept developed at ORNL [3, 7]. Results from the developed parametric models were compared against simulation results from ORNL to verify the developed models. Once confidence in the models was obtained, the process for evaluating the integrated thermal performance was applied to a range of package concepts based on the direct-cooled design. The approach provides a method for comparing alternative package

configurations over a range of heat exchanger cooling performance values. The results illustrate the effects of package layout and material selection.

Approach

The approach followed in this work included three main steps. The first was the creation of parametric thermal models of the direct-cooled substrate package under development by ORNL. Representative heat exchanger boundary conditions were applied to the model based on simulation data provided by ORNL, and the results of the parametric model were compared against data provided by ORNL. Once confidence in the model was established, the next step applied the developed process for characterizing the integrated package and heat exchanger thermal performance on the ORNL direct-cooled substrate design. Finally, a range of alternative package modifications were selected to illustrate how the developed approach could be utilized to investigate modifications to the package design. The selected modifications include changes made by NREL to illustrate the process and requests from ORNL.

Results

Parametric Model Development and Verification

The analysis focused on two general package and cooling concepts developed at ORNL, as shown in Figure 5. In each configuration, the conventional metalized substrate and metal heat exchanger are removed. The silicon chips are soldered to a copper layer that is then attached to a ceramic substrate block. Coolant running directly through the substrate block provides cooling for the packages. Two different cooling arrangements were the focus of this work. The first, shown in Figure 5a, consisted of four circular coolant channels 9.8 mm in diameter. The second, shown in Figure 5b, consisted of an annulus 17.385 mm in diameter with a channel width of 5 mm. More details about the specific package designs can be found in the technical report by ORNL [7]. For this analysis, the diode locations were on the top and bottom of the images in Figure 1, while the IGBT locations were on the sides.

Fig. 33. Isometric view of package configurations with both cooling options: (a) Four-hole cooling design, (b) Annulus cooling design

The overall effective thermal resistance of the baseline heat exchanger design was calculated following the procedure outlined in [3]. The results are listed in Table 2 as applied to quarter sections of the models shown in Figure 5.

Table 13. Boundary Conditions

	4-Hole Design	Annulus Design
Cooled Surface Area (A_s) [mm^2]	923.63	819.25
Coolant Mass Flow into modeled section [kg/s]	6.616E-03	6.616E-03
UA_{eff} [W/K]	11.85	6.20
$R_{th,h-a}$ [K/W] (Effectiveness – NTU Method)	0.1068	0.1829
$R''_{th,h-a}$ [mm^2-K/W] (Effectiveness – NTU Method)	98.65	149.83

The results of the model verification showed that the peak IGBT and diode temperature of the parametric model were within 4% of the simulation results provided by ORNL. The difference between the model results was considered reasonable based on the different assumptions applied to the models. The results also verified the generalized effective heat exchanger performance values of the four-hole and annulus heat exchanger designs listed in Table 2.

Integrated Thermal Performance of ORNL Package Designs

The results of the thermal performance characterization performed on the baseline ORNL four-hole and annulus designs are shown in Figure 6. The intersection of the thermal performance curve with the calculated effective heat exchanger thermal resistance from Table 2 is highlighted in the figure. The thermal performances of the packages are similar to each other. The overall junction to ambient thermal resistance ($R_{th,j-a}$) for the four-hole design is slightly lower because the effective thermal resistance of the heat exchanger is slightly lower.

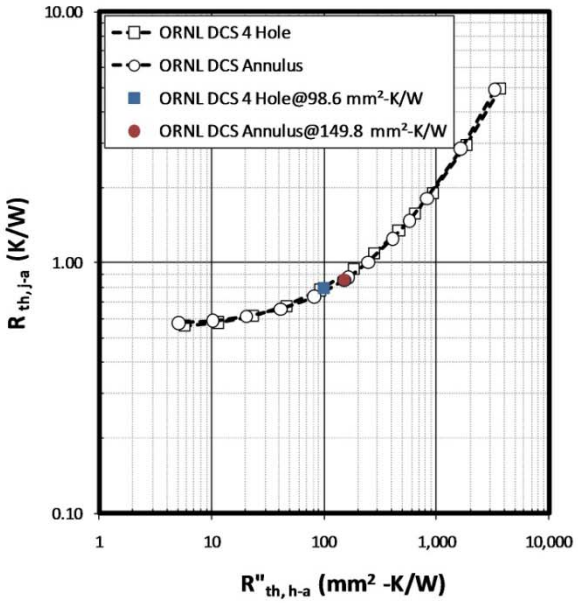

Fig. 34. Total thermal resistance thermal performance characterization of ORNL baseline 4-hole and annulus package designs

Package Modifications

To illustrate how the developed process can be used to evaluate alternative package configurations, variations were made to the original package design. In the modified packages, the ceramic substrate heat exchanger was replaced with an aluminum heat exchanger of the same shape as the original annulus design by ORNL. The IGBT and diode devices were mounted to standard metalized substrates. A variable thermal interface was also created between the substrate metallization layer and the aluminum heat sink. The variable thermal interface allows for variation in thickness and thermal conductivity. Table 3 shows the material properties for the alternative configurations. Additional details related to the package geometry are available in NREL's DOE milestone report [3].

Table 14. Thermal Performance Metrics of Alternative Configurations

Configuration ID	A1	A2	B1	B2	C1	C2
Substrate	Al_2O_3	Al_2O_3	AlN	AlN	AlN	AlN
Metallization	Cu	Cu	Cu	Cu	Al	Al
Thermal Interface Resistance [mm²-K/W]	2.5	66.7	2.5	66.7	2.5	66.7

The package thermal characterization curves for the alternative annulus configurations are summarized in Figure 7. The curves illustrate the relative impact of the different package options. Comparing figures 7a 7b shows the impact of the thermal interface resistance. The lines within each graph highlight the impact of changing either the substrate material or the metallization material. For example, the impact of switching from copper to aluminum for the metallization layer appears to be larger for the package with the higher thermal resistance interface material, as shown in Figure 7b. The difference may be due to the impact of thermal spreading prior to a high thermal resistance interface.

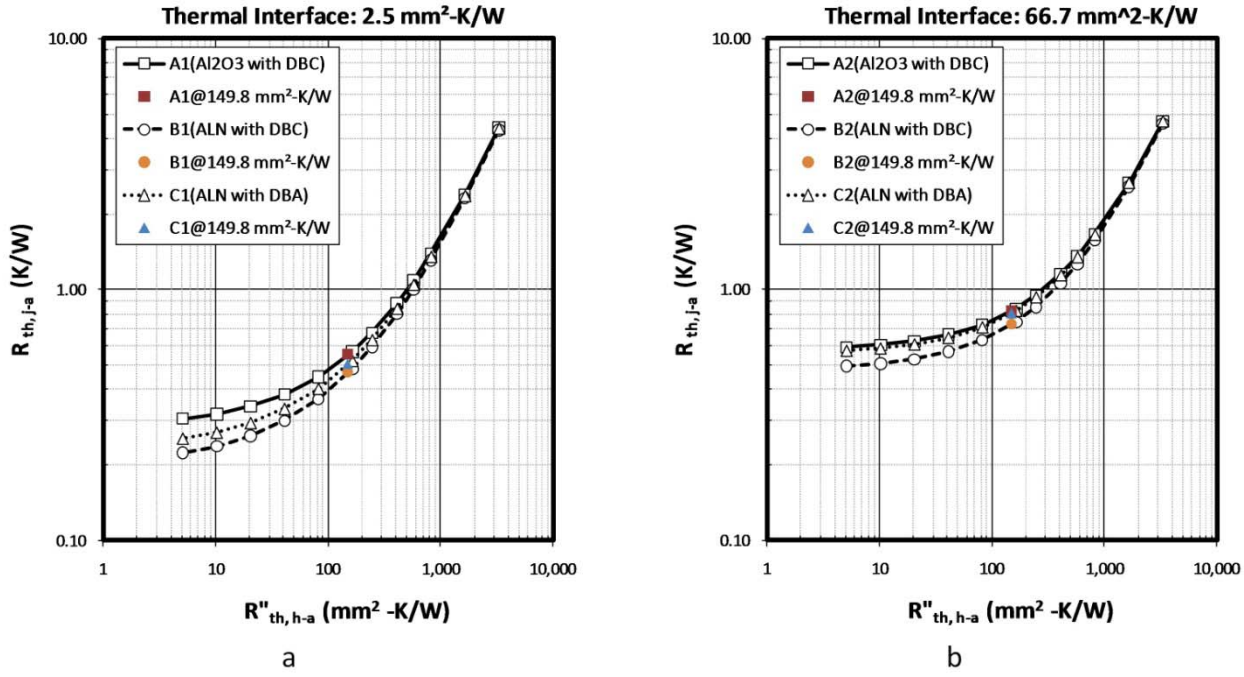

Fig. 35. Total thermal resistance thermal performance characterization of modified annulus package design: (a) Low thermal interface resistance, (b) High thermal interface resistance

The work with ORNL demonstrated the method of integrating techniques for characterizing power semiconductor thermal performance and heat exchanger technologies. The approach was applied to a new packaging concept developed as part of the APEEM activity within the Vehicle Technologies Program at the Department of Energy. The methodology enables an analysis of the system performance and the trade-offs of the combined package and cooling system. To illustrate the application of the work, the analysis was also extended to additional package configurations based on the annulus design developed by ORNL. The additional package configurations included options requested by ORNL.

Integrated Package and Cooling Thermal Performance – Experimental Capabilities

To support the modeling efforts related to evaluating the integrated package and cooling thermal performance, new experimental capabilities were added in FY 2010 to experimentally characterize the thermal performance of power semiconductor packages with integrated cooling technologies. The experimental capabilities were developed in collaboration with an industry partner in an effort to verify the test hardware. The diagram in Figure 8 describes the test setup, which is capable of transient and steady-state thermal characterization. The setup was used in FY 2010 to begin experimental tests of package designs with new or innovative cooling technologies. Figure 9 illustrates a sample power semiconductor packages under test.

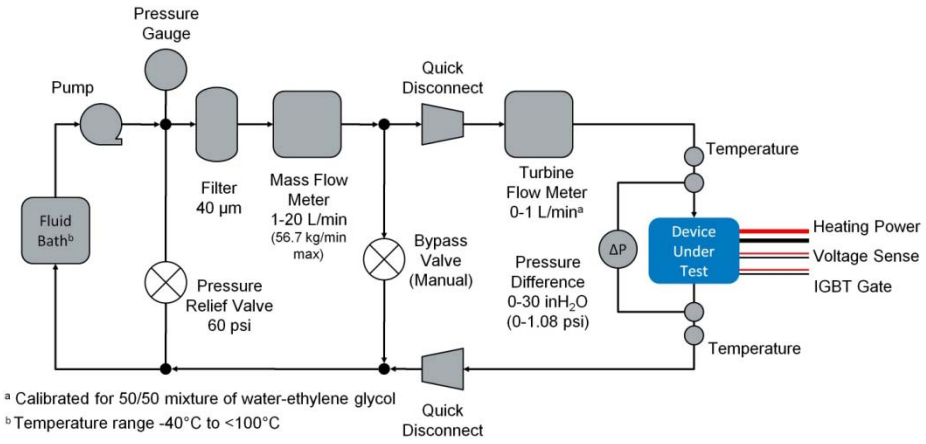

Fig. 36. Integrated power semiconductor and cooling technology thermal characterization hardware diagram

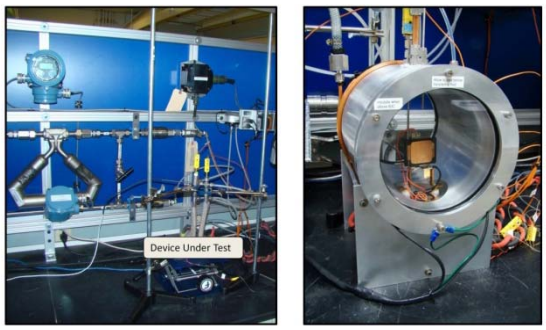

Fig. 37. Sample power semiconductor packages under test

Capacitor Thermal Model

DC-link capacitors comprise 20%–31% of inverter volume and weight in some current hybrid designs [8, 9]. The volume and weight of these capacitors is influenced by their thermal performance and environment. DC-link capacitor ripple current ratings for a given design are strongly dependent on the thermal behavior, with maximum ripple current decreasing with increasing device temperature. Increasing current load increases heat generation of the capacitor, leading to increased temperatures. Depending on severity, elevated temperatures can result in decreased life or sudden failure. Additionally, the thermal management system associated with the capacitor further increases the weight and volume of the system. The goal of this work is to develop a general parametric DC-link capacitor thermal model to evaluate thermal performance of power electronics packaging design alternatives. This model can be used to explore thermal system-level design trade-offs, including capacitor configuration, heat generation/ESR (equivalent series resistance), heat transfer approaches, materials, and connector configurations. This analysis will increase understanding of how thermal performance of DC-link capacitors impacts design and identifies opportunities for reduction of system cost, volume, and weight.

To achieve this goal, a general three-dimensional parametric capacitor model was developed that captures the important thermal characteristics including: anisotropic properties, non-uniform heat generation, and the influence of electrical connections. Modeling DC-link capacitors requires addressing multi-scale behavior spanning over seven orders of magnitude in length scale, from nanometers to centimeters. To accomplish this, a finite element analysis (FEA) model was developed in ANSYS to handle the larger scales, while the smaller scales are treated with simplified analytical solutions coupled to the FEA model.

While there are several possible technologies, metalized film capacitors are currently the most common for hybrid/electric vehicle applications. These capacitors store energy using charge separation between two conductors that sandwich a dielectric. The dialectic is typically on the order of microns thick, while the conductive metal film that is deposited on the dielectric is on the order of nanometers thick. The layers of wound capacitors are spirally wound around a core, forming a "jelly rolled" cylindrical structure. The wound structure will result in anisotropic conductivity, with the radial direction having layers in series and the axial and circumferential directions having layers in parallel. To address the nano- and micro-length scales of the windings, which determine bulk conductivity, an analytical resistance network model was used and applied as bulk anisotropic conductivity to the FEA model. The resistance network model was derived using a cylindrical element; however, it results in the equations shown in Figure 10 that agree with results derived for a flat wall element [10]. As a thought experiment, the conduction in the radial direction due to the spiral structure was included in the network. It was found that this quickly became insignificant with any distance traveled in the circumferential direction. The current approach currently excludes the contact resistance between layers, which has the potential to be significant.

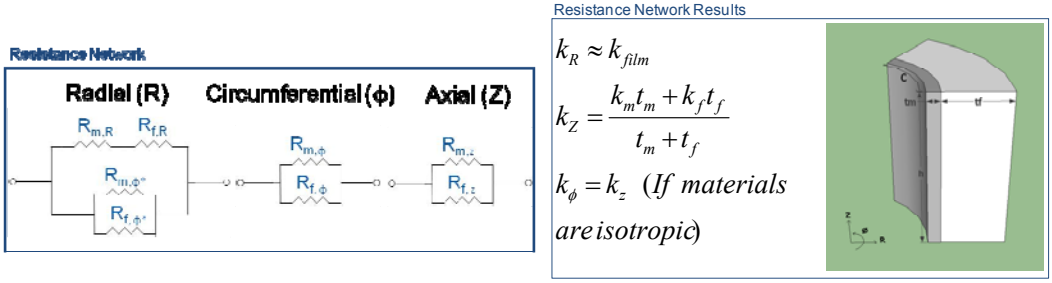

Fig. 38. Resistance network and resulting equations

Heat generation in a capacitor is dependent on the resistivity loss through the current path, resistivity in the end spray contact spots, and dielectric loss. The first mode is believed to be dominant under the conditions of interest, and the other two were considered negligible for this initial analysis. The heat generation in the windings of the capacitor also occurs in the nano-length scale metal layers. This scale is prohibitively small for a capacitor-sized FEA model, so once again an analytical solution was applied. At the free end of a capacitor electrode, the current will be zero. Moving away from the free end, the current will collect down the electrode until it is equal to the full current value at the connected end. Assuming the current collection is a linear process, the heat generation will be non-linear. Following a similar derivation approach to that of Qi and Boggs [11], a result was obtained agreeing with Hosking and Brubaker [12]. Since the two electrodes collect current in opposite directions, their volume-weighted average heat generation was used in the model. As shown in Figure 11, this results in a minimum heat generation in the center and a maximum heat generation at the two ends of the windings. Assuming that current and thus heat generation in the windings were independent of the radial direction, the heat was calculated and applied based on the axial position of each element centroid in the FEA model.

To form the electrical connections on the ends of each electrode and to collect the current, a metal end spray was added to the capacitor on each end. The larger-length-scale behavior of the end spray allowed this to be modeled with a simple analytical model and an FEA-based electrothermal model. The simple analytical model was derived for an axisymmetic circular connector with uniform current flux from the windings (consistent with the previous assumption that current is independent of the radial direction in the windings). This analytical model indicates that an optimal electrical connector radius exists where heat generation in the end spray in minimized. The optimal radius was verified by doing a parametric sweep of the electrical connector contact position. The analytical and numerical electrothermal heat generation models where shown to agree well for the simple axisymmetric end spray case, with the maximum

temperature agreeing to within 0.5% for a case study. The numerical electrothermal model, however, will give more flexibility in geometry and can be extended to handle the electrical connectors.

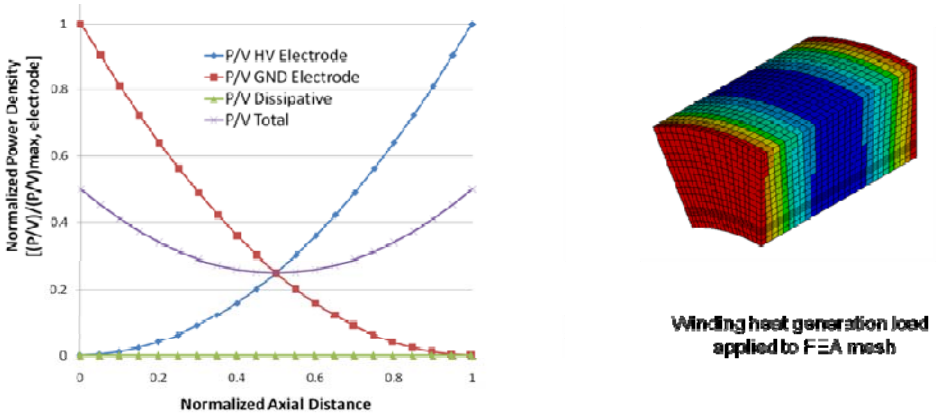

Fig. 39. Non-uniform heat generation in the capacitor windings

Initial validation of the model was done for an annular capacitor design. Experimental data were provided by ORNL. At the temperature locations provided, shown in Figure 12, the model agreed to within 0.5°C of the test data; however, incomplete information required estimation of some of the geometry, materials, and constructions. The validation is promising; however, considering these uncertainties, the results should be considered preliminary. Rather than do a full teardown of this capacitor to improve assumptions, a commercial vehicle DC-link capacitor module will be modeled next. The full model will be used to perform detailed validation and improvement of the model. Once validated, the module-level model will be used to investigate thermal management requirements and opportunities to reduce system cost, volume, and weight.

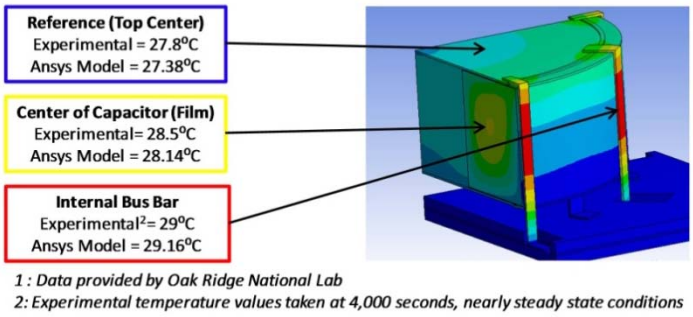

Fig. 40. Preliminary validation of DC-link capacitor thermal model

Conclusion

The objective of the thermal systems task is to facilitate the integration of advanced power electronic thermal management technologies into commercially viable advanced automotive systems. The design of a viable system requires understanding how the power electronics are used, how the environment in which they operate impacts thermal management, and how power semiconductor packaging and cooling impact performance. During FY 2010 we worked to collaborate with industry, DOE laboratory partners, and internal NREL thermal research projects to apply the developed system analysis capabilities related to thermal management of power electronics.

The method of integrating techniques for characterizing power semiconductor thermal performance and heat exchanger technologies was applied to a range of commercial modules. The results provide guidance for researches investigating new cooling technologies into what package configurations may be best able to work with the developed cooling technologies. The optimal heat transfer mechanism is highly dependent on the package configuration; therefore, the package and heat exchanger need to be evaluated as an integrated system. The combined analysis ensures that one area of the thermal control system is not overdesigned, adding unnecessary cost, weight, and volume to the system.

NREL worked with ORNL to apply the techniques for characterizing power semiconductor thermal performance and heat exchanger technologies to ORNL's new direct-cooled substrate design. The methodology enabled an analysis of the system performance and the trade-offs of the combined package and cooling system. The analysis was also extended to additional package configurations based on the annulus design developed by ORNL.

Other significant FY 2010 accomplishments support future thermal management projects into FY 2011. In collaboration with an industry partner, NREL developed experimental test capabilities to perform thermal characterization tests on integrated power semiconductor and cooling systems. This will support the testing of new cooling technologies as applied to power semiconductor packages. In addition, NREL worked with ORNL to validate a general parametric three-dimensional capacitor thermal model to enable future thermal investigations related to power electronics packaging.

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Kirk Lowe and Randy Wiles of ORNL

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5.5 Thermal Control of PHEV/EV Charging Systems

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Objectives

Multiple charging options exist for plug-in hybrid electric vehicles (PHEVs) and electric vehicles (EVs). Options range from high-power off-vehicle rapid charge stations, in-vehicle chargers with dedicated charging systems, and in-vehicle charging systems integrated with existing power electronics and electric machines. Despite the differences in charging configurations, thermal management is a common issue due to the power levels, limited vehicle package space, and net efficiency requirements. A challenge due to the wide range of applications is to match application-specific targets such as power density to cooling performance targets such as a heat exchanger thermal resistance. This project will look at merging power electronics charging configurations with thermal management technologies to enable robust cost-effective energy storage charging systems. Specifically, this project will investigate the potential application of alternative thermal management technologies to determine appropriate cooling technologies for charging applications.

Approach

The Thermal Management of Advanced Power Electronics and Electric Motors (APEEM) activity in the Department of Energy's (DOE) Vehicle Technologies Program (VTP) is currently developing a suite of advanced thermal cooling technologies and performance data, including single-phase and two-phase jet impingement, and air cooling. A significant challenge is matching the performance characteristics of a particular cooling technology to a specific APEEM technology application and the associated operating specifications. This year we worked to develop a target or specification cascading procedure that converts application-specific targets into thermal management performance targets. The link from application to thermal design targets provides researchers with an approach to evaluate new cooling developments. The process was developed to support the identification of cooling technologies for a range of electric vehicle support equipment (EVSE) options for vehicle charging. Specifically, this year focused in two areas:

- Develop a systems-target cascading process that links application specification goals (power, efficiency, size, temperature limits, etc.) to thermal design performance metrics that can be used by researchers of alternative cooling technologies
- Apply the developed approach to charging systems for PHEVs and EVs in collaboration with thermal researchers at NREL and PHEV researchers at Idaho National Laboratory (INL)

Major Accomplishments

The key accomplishment for FY 2010 included the following items.

- Expanded past systems analysis work at NREL to develop a process for matching application-specification targets to thermal design targets

- Applied the approach on a range of potential applications for PHEV and EV chargers
- Demonstrated application to a generalized cooling system utilizing a cold plate
  - Collaborated with INL to evaluate application data (efficiency and coolant temperature) of in-use PHEV charging systems
  - Worked with NREL's Air Cooling task to evaluate the use of air cooling for level one, two, and three charging applications
- Expanded analysis to high-power DC charging systems
  - Demonstrated the flexibility of the developed process to evaluate component specific cooling needs
  - Developed component loss models using manufacturer supplied data sheets and integrated model into the analysis process
  - Worked with NREL's Air Cooling task to evaluate the use of air cooling for high power DC charging applications

Future Direction

This project ends in fiscal year (FY) 2010, but the developed approach will continue to be used for future tasks at NREL to identify the relevant thermal management performance targets for specific applications. This work developed an approach for looking at a generalized cold plate and a DC-DC converter application as they relate to charging systems. This information will be used by NREL researchers to apply new developments related in cooling technologies to PHEV and EV charging systems. The approach will also be expanded as part of FY 2011 projects to include inverter applications for motor drives in support of NREL's Air Cooling task.

Technical Discussion

The technical discussion of the report is divided into three main sections. The first section describes the general process developed to convert application specifications such as power density to thermal performance metrics that can be used by researchers looking to apply new developments in cooling technologies. The final two sections demonstrate the application of the developed process to two different systems related to PHEV and EV chargers.

Target Cascade Process

As part of the APEEM activity at DOE, a number of specification goals or targets have been developed related to electric drive systems for vehicles [1]. The thermal management of electric drive components is a recognized challenge to the performance and reliability of the electric drive system. For this reason, the APEEM program supports ongoing research efforts into thermal management of electric drive components. However, it is a challenge to relate the high-level APEEM specification goals and targets to improvements in heat transfer technologies. For example, how does a power per size goal relate to a heat transfer coefficient? While no current APEEM goals or targets exist for charging systems, a similar question remains. What cooling technologies are needed to meet the wide range of charging systems? The overall thermal design depends on a number of factors that influence the overall system performance and cooling design. These factors can be grouped into four general categories, and examples are provided in Figure 1. The four areas include:

- Application Technical Specifications
- Package Mechanical Design
- Cooling Technology Selection
- Cooling Technology Balance of System

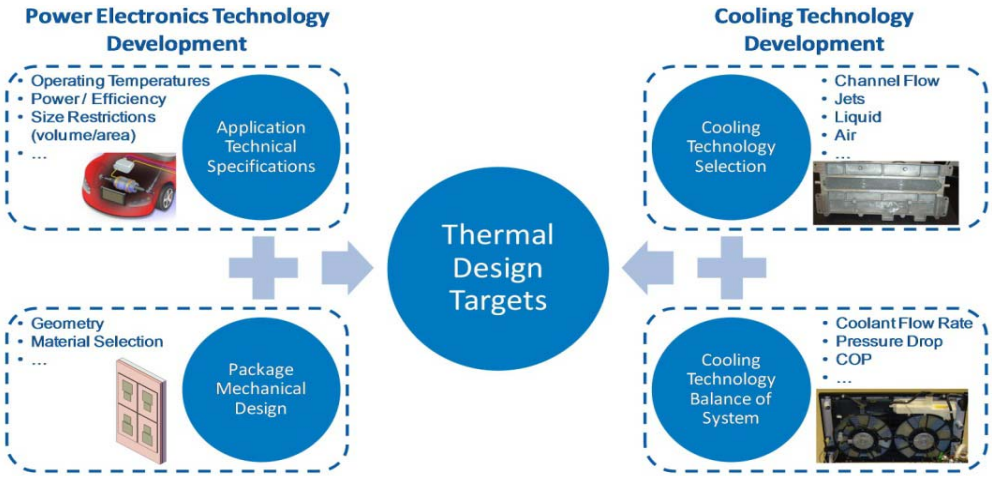

Fig. 41. Power electronics systems and integration focus areas

To meet the need to translate application specifications into thermal requirements, a process and capability were developed to link each of the four areas listed in Figure 1. All of the four areas above are significant design challenges within themselves, and when looked at together as an overall system a number of trade-offs are possible between different areas. A challenge is relating the application specifications to the thermal design targets that a thermal research engineer uses and understanding the potential system interactions. To match the application specifications to thermal design parameters a MATLAB-based system design program was developed to link each of the four areas described in Figure 1. The program enables design studies between multiple design parameters within each area. An example of the program flow is shown in Figure 2.

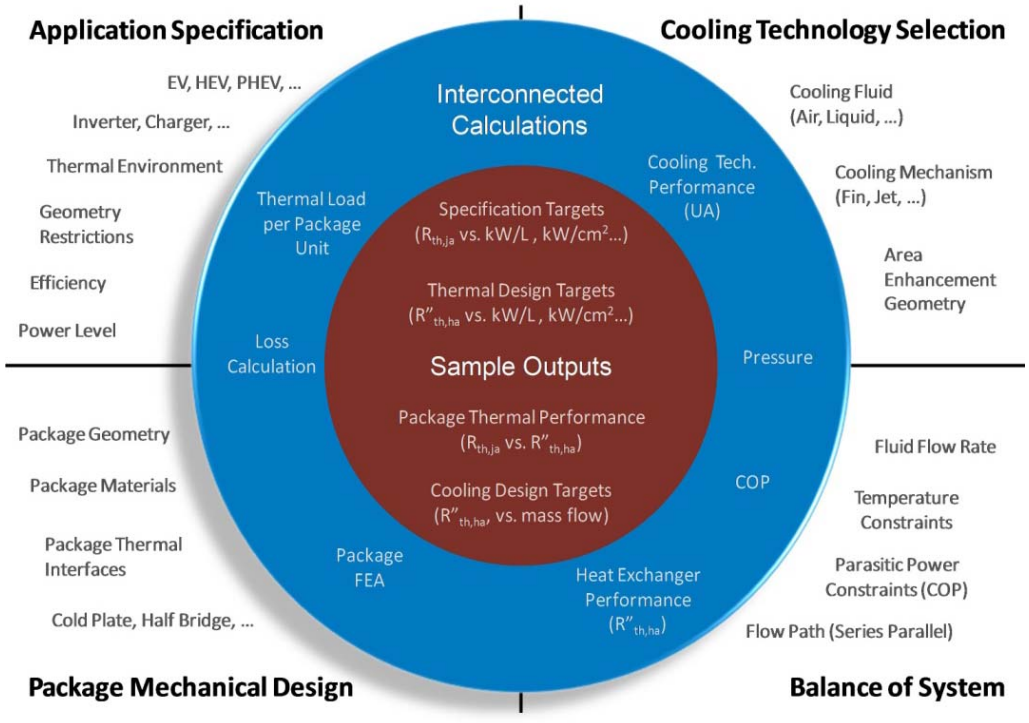

Fig. 42. Program flow

The four design areas from Figure 1 and 2 are linked together through interconnected calculations (shown in blue in Figure 2). The interconnected calculations enable design studies related to application specifications, package mechanical design, cooling technology selection, and cooling technology balance of system. The inputs to each area can be changed to match a specific application, perform sensitivity studies, or run design optimizations.

EVSE Demonstration Cases

The developed process was developed to support the investigation into thermal management of PHEV and EV charging systems. With this application in mind two test cases were developed to investigate the potential use of air cooling. While the cases were developed for charging applications with a focus on air cooling, the systems analysis program is flexible to enable studies of other applications or cooling technologies. This report will focus on the left side of the diagram in Figure 1 that translates the application specifications and mechanical design into thermal design targets. The right side of Figure 1 was developed in collaboration with NREL's Air Cooling research task, and the process is described in the Air Cooling annual report. Two examples of how the developed program was used to match cooling technology developments to charging systems are described below. The first case looks at the thermal requirements of using a cold plate to remove the entire heat load of a charging system. The second case looks at the thermal requirements of cooling the insulated gate bipolar transistor (IGBT) module used within a DC-DC converter for a high-power DC charger application.

Cold Plate Demonstration

The first application covers a generalized charging system that utilizes a cold plate to transfer heat from the charging components to the cooling system. The goal is to determine the needed cooling technology performance to meet the given application specifications. For this application it is assumed that all of the waste heat generated within the electrical components must be removed through the cold plate and cooling system. The application specifications include parameters related to the power level, charger efficiency, size (cold plate area), inlet coolant temperature, and allowable cold plate temperature. The final design would require more detailed analysis in terms of heat load locations, but the purpose of this analysis was to perform an initial screening to determine what cooling technologies could work for the given charging configurations. The work is summarized in three sections:

- Package Mechanical Design
- Application Technical Specifications
- Application Specific Thermal Design Targets

Package Mechanical Design

For the cold plate application, the package mechanical design consists of a simple metal plate made of either aluminum (Package 1) or copper (package 2). For this example, it is assumed that the heat is spread throughout the cold plate. The task is to relate the package design to thermal design metrics and cooling technology performance metrics. This process has been described in a previous paper related to power semiconductor cooling [2]. Figure 3 shows the thermal performance characteristics of the cold plate in terms of the peak surface temperature to ambient temperature thermal resistance ($R''_{th,ja}$) against the cooling technology performance values. In this work the cooling technology performance was characterized as the heat sink to ambient thermal resistance ($R''_{th,ha}$). More details related to the calculation of the heat exchanger thermal resistance can be found in [2] and NREL's Thermal System Integration and Performance FY2010 milestone report [3]. Figure 3 highlights the impact of a copper cold plate relative to the aluminum cold plate as the cooling technology becomes more aggressive. The cooling performance bands of alternative cooling methods shown in Figure 3 are taken from Mudawar [4], which are based on ranges for convection coefficients. It is expected that different area enhancement methods could significantly reduce the heat exchanger thermal resistance below what is shown in Figure 3.

However, it provides an interesting comparison of different cooling technologies. The focus of the work described in the following sections was on the aluminum cold plate.

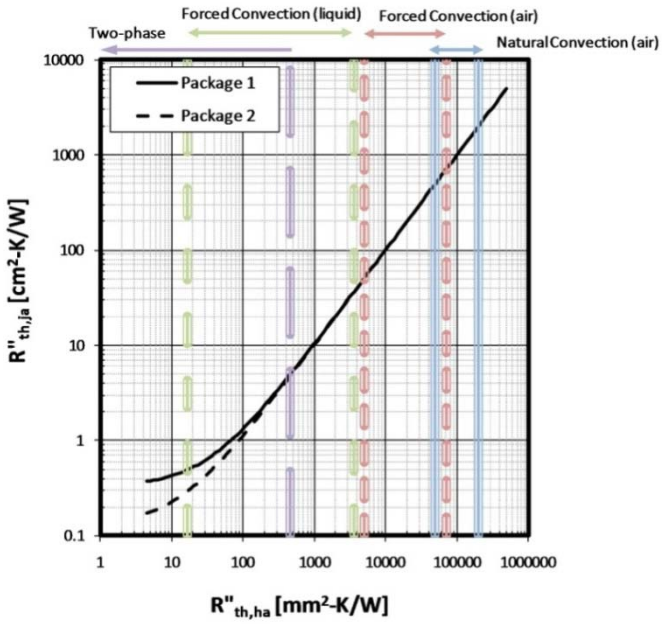

Fig. 43. Package mechanical design thermal performance. Cooling ranges based on heat transfer coefficients from Mudawar [4].

Application Technical Specifications

The application technical specifications determine the heat load and operating temperatures of the system as highlighted in Figure 1. The heat load of the charging application was based on the overall efficiency of the charging system. To determine realistic estimates for overall charging efficiency, NREL partnered with INL. As part of their work with the Vehicle Technologies Program in the Department of Energy, INL monitors and records data on a large fleet of PHEVs across the country. In support of this project, researchers at INL evaluated the charging data over a sample of vehicles and calculated the overall charging efficiency [5]. A graph from their report showing the charging efficiency distribution is shown in Figure 4a. Based on INL's analysis, an efficiency of 85% was used to estimate the heat loads for the results summarized in this report. However, within the program a range of efficiency numbers were included to see the impact of variation of efficiency. INL also analyzed temperatures within the charging system. The distribution of inlet air temperature into the charger is shown in Figure 4b. For the results in this report, an inlet air temperature of 40°C was used. As seen in Figure 4b, this covers the majority of the sampled data collected and analyzed by INL.

The application targets of power level, efficiency, and allowable temperature were translated into targets for total thermal resistance between the cold plate peak temperature and inlet coolant temperature ($R''_{th,ja}$). The black lines shown in Figure 5a show the maximum allowable total thermal resistance ($R''_{th,ja}$) for a given power rating, size, and allowable temperature rise (ΔT). The vertical double lines illustrate the relevant ranges for the different charge levels for areas between 300 cm^2 and 900 cm^2. The heat loads are based on an efficiency of 85% as discussed previously. The power levels for the charging configurations are based on standard level one, two, and three charging systems [6].

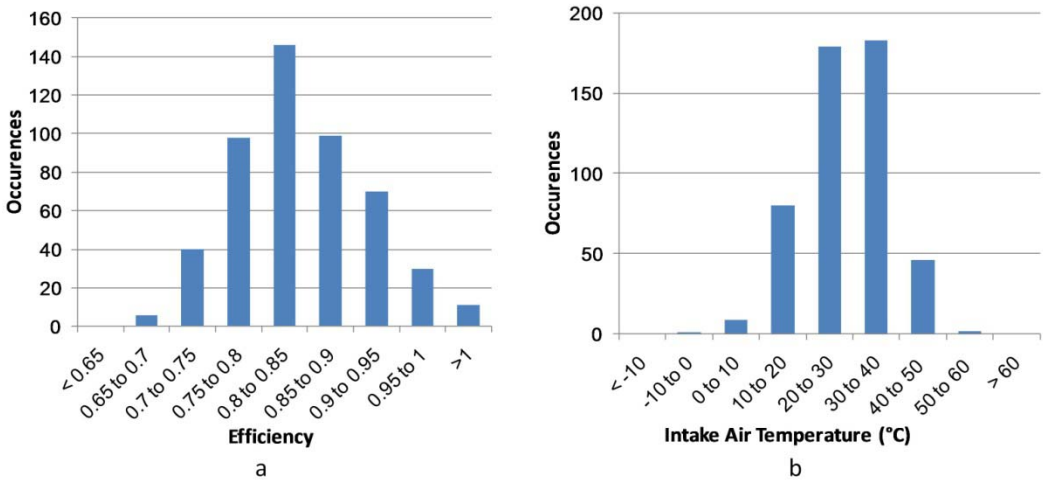

Fig. 44. INL charger analysis [5] (a) Efficiency, (b) Inlet air temperature

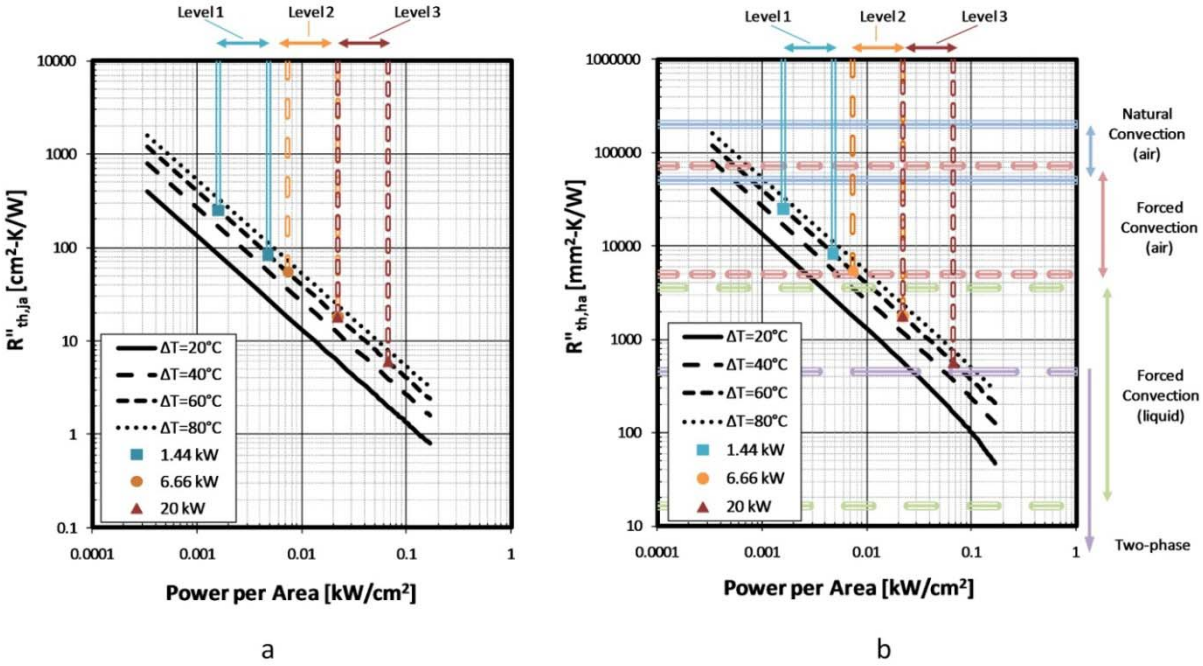

Fig. 45. (a) Impact of application technical specifications on thermal performance requirements with level 1, 2, and 3 charge levels highlighted, (b) Application technical specification linked to thermal design targets with cooling ranges highlighted. Cooling ranges based on Mudawar [4] for convection coefficients (surface enhancements would reduce the effective thermal resistance).

Application Specific Thermal Design Targets

After translating the mechanical design thermal performance and the application specifications into a common thermal performance target ($R''_{th,ja}$), it is possible to combine the results to match cooling technologies to application specifications. The results are shown in Figure 5b. The black lines in Figure 5b show the maximum allowable heat exchanger performance ($R''_{th,ha}$) that is capable of meeting the desired application targets in terms of power, area, and temperature. The vertical lines in Figure 5b are carried over from Figure 5a to highlight where the specific charger levels fall on the graph. The horizontal

lines are from Figure 3, and they represent the range of heat transfer coefficients of different cooling technologies [4]. As mentioned previously the highlighted thermal resistances based on convection coefficient would decrease as area enhancements are included.

As part of NREL's air cooling efforts, initial models for air cooling were incorporated into the modeling process. The air cooling models bring into the systems model the elements related to the items shown on the right of Figure 1. More information on how the cooling technologies are incorporated into the model is included in NREL's Air Cooling report. A sample of two conventional fin designs that meet the level 1 and level 2 application targets with the smaller area are shown in Figure 6. The solid horizontal lines represent the thermal resistance of a heat exchanger based on the listed fin geometries. The level 1 charger with the smaller fin assumes a flow rate of 30 L/s of air. The level 2 charger result with the larger fin assumes an air flow rate of 45 L/s. The horizontal dashed line is included to represent preliminary estimates for forced convection cooling using air with area enhancements. However, the thermal resistance could decrease, and it involves a tradeoff between multiple design factors. The ability to push this resistance lower is a significant aspect of NREL's Air Cooling effort, and the developed systems modeling approach will allow researchers to evaluate the impact of cooling improvements related to real applications. The primary point of Figure 6 in terms of PHEV and EV chargers is that air cooling appears to be a viable solution for even higher power charging systems.

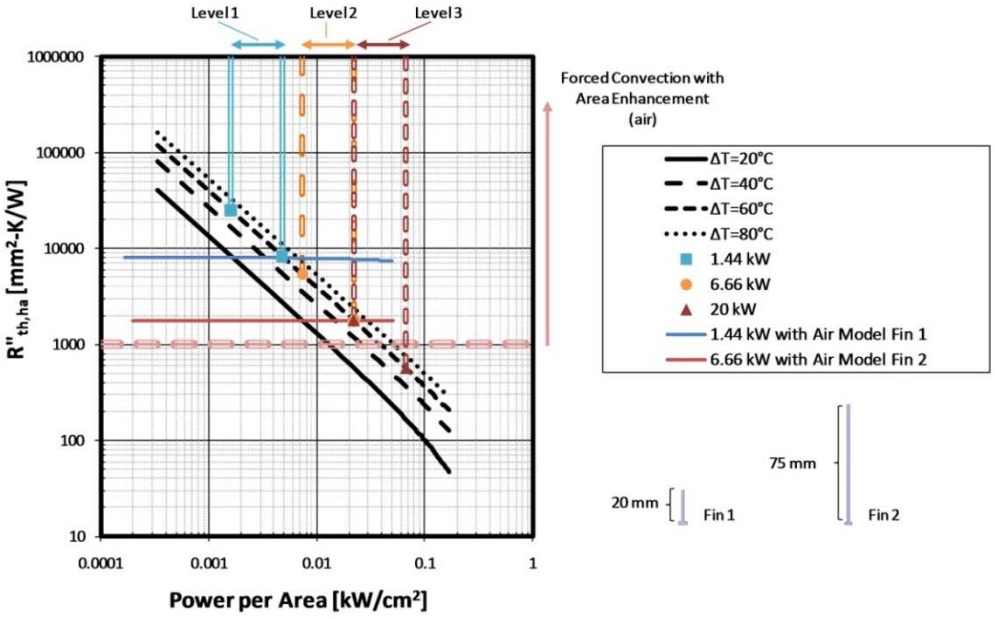

Fig. 46. Application technical specification linked to thermal design targets with air cooling range with area enhancement

DC-DC Converter Application

Instead of focusing on the full charging system, a second approach was used to demonstrate the flexibility of the developed systems analysis approach to look at cooling of certain components. The program was used to evaluate the ability of using air cooling to cool IGBT modules used within a DC-DC converter for a high power DC charging application. The DC-DC converter is configured to operate as a buck converter to convert a high voltage from a DC charge source into a lower voltage compatible with a particular energy storage or battery technology on a vehicle. The inductor and capacitor sizes were based on the Toyota Camry DC-DC converter [7] because it was assumed that the system would have similar power and performance requirements because of the interface to the battery. The high voltage input was fixed at 400 V, and the switching frequency was fixed at 10 kHz. The power level was also fixed at 20 kW. While

these parameters were fixed in this analysis, the program does have the capability include a range of values to perform desired sensitivity studies. The following summary of the work follows the same process as described above.

- Package Mechanical Design
- Application Technical Specifications
- Application Specific Thermal Design Targets

Package Mechanical Design

For the DC-DC converter application, the package thermal performance is based on an actual IGBT module as shown in Figures 7a and 7b. A large and a small heat exchanger area package were selected to illustrate the impact of increasing the available heat exchanger base footprint area. The thermal performance of each package was determined through finite element analysis of a single IGBT/diode pair as shown in Figure 7. The layer properties match previously published reports [3, 8]. Because the focus was on IGBT heating, heat was only applied to the IGBT in the finite element analysis. However, the analysis could be repeated to represent diode heating. The process follows the previously developed and published process developed as part of NREL's Power Electronic System Performance and Integration research effort [2, 3, 8].

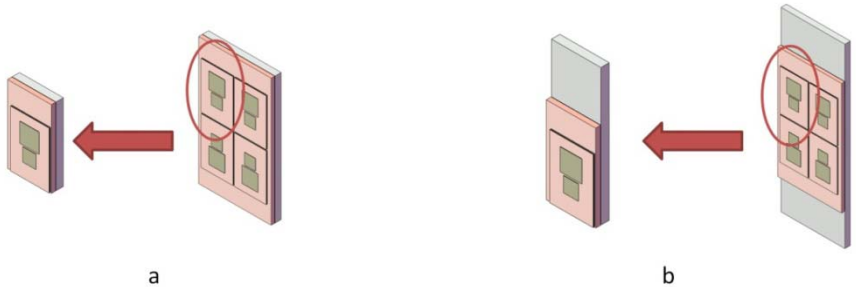

Fig. 47. Package geometry configurations. (a) Small heat sink area (15.34 cm^2); (b) Large or extended heat sink area (24.19 cm^2).

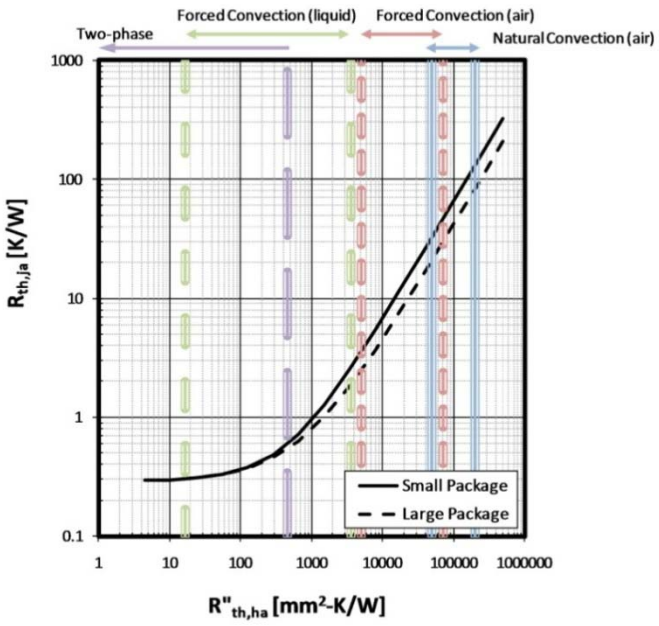

Fig. 48. Package mechanical design thermal performance. Cooling bands based on convection coefficients from Mudawar [4].

Figure 8 shows the thermal performance characteristics of the power semiconductor package with IGBT heating. The thermal performance is illustrated in terms of the peak IGBT temperature to inlet coolant temperature ($R_{th,ja}$) against the cooling technology performance values ($R''_{th,ha}$). Figure 8 shows that the impact of the large package design is more apparent for higher heat exchanger resistance values. As with Figure 3, the cooling performance bands of alternative cooling methods shown in Figure 8 are taken from Mudawar [4] which are based on ranges for convection coefficient. As discussed previously, it is expected that different area enhancement methods could significantly reduce the heat exchanger thermal resistance below what is shown in Figure 8.

Application Technical Specifications

As with the cold plate application, the application technical specifications determine the heat load and operating temperatures of the system as highlighted in Figure 1. The heat load was calculated based on an average loss model that accounts for the current ripple through the inductor of the DC-DC converter [9], the switching frequency, input voltage, switching duty cycle (D), and component specific parameters as supplied by power semiconductor suppliers. A detailed description of the loss model is beyond the scope of this summary report, but the loss results of the average model were compared against a more detailed MATLAB/Simulink based model that included the switching of the IGBT devices. A comparison between the two models was performed over a range of operating conditions and data sheet parameter values from different suppliers. The intent is not to compare the suppliers' components but to provide different inputs into the model for validation. A summary of the comparison results are shown in Figures 9a and 9b. As seen in Figure 9, there is close agreement between the average loss model results and the more detailed Simulink switching model.

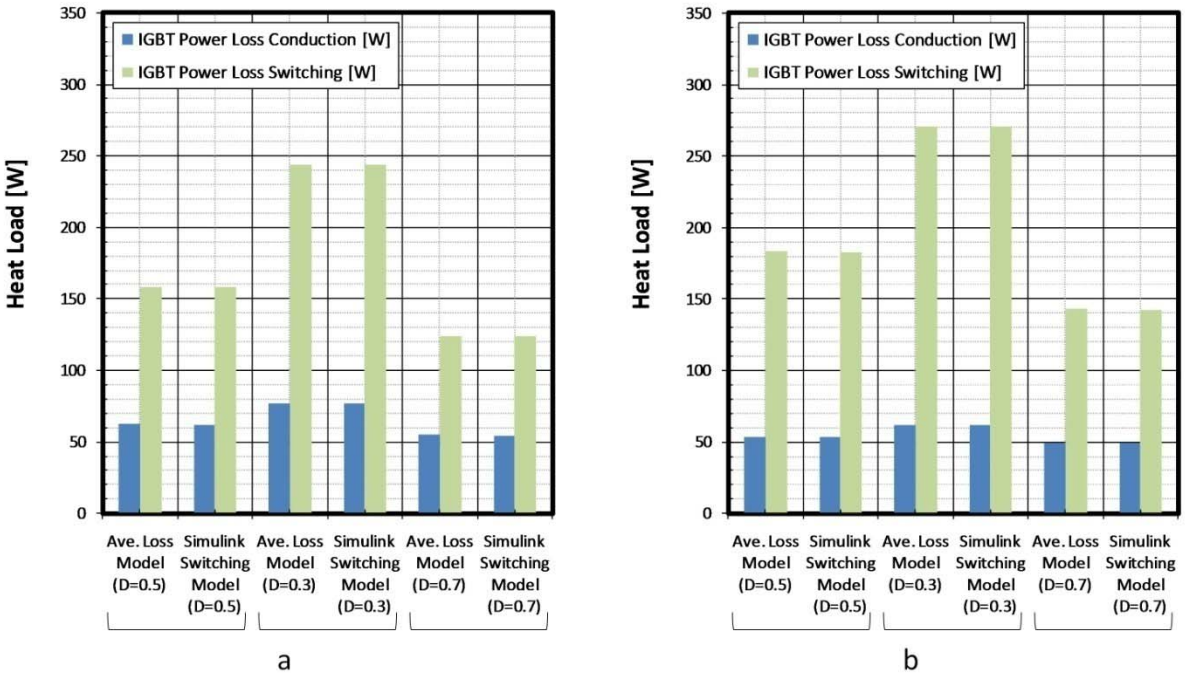

Fig. 49. Loss model comparison based on data sheet values from two IGBT modules operating at 20 kW with input voltage of 400 V, switching frequency of 10 kHz, and a range of duty cycles (D). (a) Semikron SKM 300GB128D; (b) Infineon FS450R12KE3.

The application specifications or targets in Table 1 were translated into targets for total thermal resistance between the peak IGBT temperature and inlet coolant temperature ($R_{th,ja}$). The package specific lines

shown in Figure 10 show the maximum allowable total thermal resistance ($R_{th,ja}$) for the listed specifications in Table 1. The vertical double lines illustrate the relevant ranges for the power to area ratio depending on the number of component modules that are placed in parallel to share the electrical load.

Table 15: Application Specifications for Figure 10

Parameter	Value
Power [kW]	20
Input Voltage [V]	400
Output Voltage [V]	200
Switching Frequency [kHz]	10
Peak junction temperature [°C]	125
Inlet coolant temperature [°C]	40
Component modules in parallel	1, 2, 3
Heat exchanger base footprint area [cm^2]	15.34 (small), 24.19 (large)
Component data sheet parameters	SKM 300GB128D

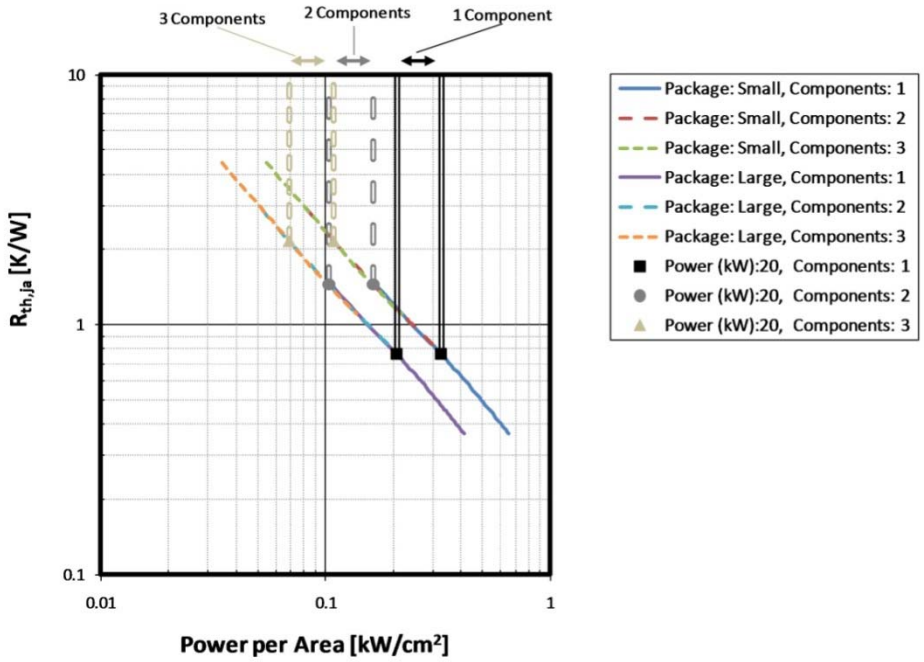

Fig. 50. Application technical specifications with variable number of components in parallel with application ranges highlighted

Application Specific Thermal Design Targets

After translating the mechanical design thermal performance and the application specifications into a common thermal performance target ($R_{th,ja}$) it is possible to combine the results to match cooling technologies to application specifications. The results are shown in Figure 11. The curves for the specified packages in Figure 11 show the maximum allowable heat exchanger performance ($R''_{th,ha}$) that is capable of meeting the desired application targets in terms of power, area, and temperature. The vertical lines in Figure 11 are carried over from Figure 10 to highlight the application range for the listed number of components placed in parallel to share the electrical load. Results similar to Figure 5b showing the impact of alternative cooling technologies could also be generated, but it is excluded because of the limited scope of this report.

As with the cold plate analysis, a primary emphasis of this work was to evaluate the potential of air cooling. More information on how the cooling technologies are incorporated into the model is included in NREL's Air Cooling report. An illustration of two conventional fin designs that meet the small package application specifications are shown in Figure 11. The solid horizontal lines represent the thermal resistance of a heat exchanger based on the listed fin geometries with an air flow rate of 50 L/s. The horizontal dashed line is included to represent initial estimates for forced convection cooling using air with area enhancements. The ability to push this resistance lower is a significant aspect of NREL's Air Cooling effort, and the developed systems modeling approach will allow researchers to evaluate the impact of cooling improvements related to real applications. The primary point of Figure 11 in terms of PHEV and EV chargers is that air cooling appears to be a viable solution for even higher power DC charging systems. This analysis would need to be extended to other critical components of the charging system.

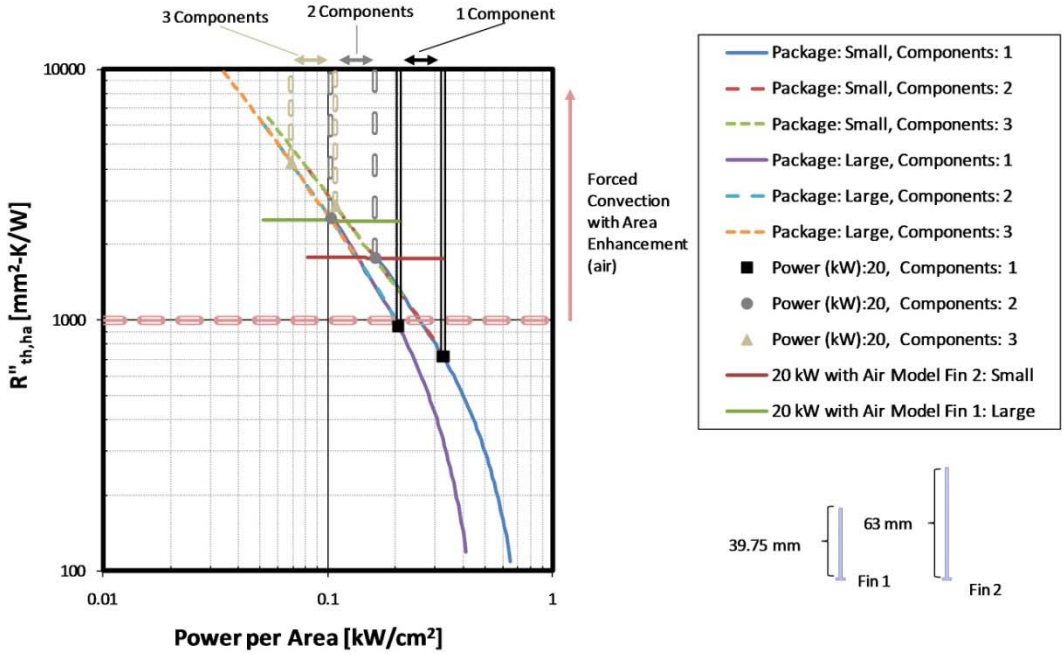

Fig. 51. Application technical specification linked to thermal design targets with air cooling

Conclusion

In FY 2010, we developed a flexible systems analysis process to match application specifications to thermal design targets. The approach was applied to a range of potential applications for PHEV and EV charging systems, with the goal of matching cooling technologies to charger applications. To include representative application specifications related to charger efficiency and inlet air temperatures, NREL collaborated with INL. INL provided analysis results of multiple charging events over a range of vehicles monitored as part of their activities supported by DOE. The results demonstrated that air cooling appears to be a viable option for even higher power rapid charging applications. The approach highlights the impact of potential improvements related to air cooling on overall application specifications.

Although the approach was designed to match cooling technologies to charging applications, the developed approach is flexible to include other power electronics applications. While this project ended in FY 2010 the developed methods will be used by researchers at NREL to link cooling technology developments to specific power electronics applications and operating specifications. The results of this analysis will provide guidance to thermal researchers. It will help researchers as they work to apply new

cooling technology developments to power electronics applications by matching cooling technologies to application specifications. The approach also enables higher level power electronics specifications related to power, efficiency, size, or temperature to be cascaded down to thermal performance metrics that can be understood by thermal researchers and engineers.

Acknowledgements

Coauthor:

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John Smart of Idaho National Laboratory

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5.6 Thermal Performance and Reliability of Bonded Interfaces

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Objectives

In automotive power electronics packages (e.g., insulated gate bipolar transistor [IGBT] packages), conventional thermal interface materials (TIMs) pose a bottleneck to heat removal. Due to advantages from a heat transfer and a packaging standpoint, there is an industry trend towards high thermal performance bonded interfaces. However, due to coefficient of thermal expansion (CTE) mismatches between materials/layers and resultant thermomechanical stresses, there could be voids and crack formations in these bonded interfaces, which poses a problem from a reliability standpoint. These cracks, voids, or delaminations manifest themselves in increased thermal resistance in the package, which again is a bottleneck to heat removal. Hence, the overall objective of this project is to investigate and improve the thermal performance and reliability of novel bonded interface materials for power electronics packaging applications. Specifically, the objectives for FY2010 were:

- Establish capabilities at NREL for synthesis and characterization of thermal performance and reliability of novel bonded interfaces for power electronics packages.
- Establish appropriate collaborations.
- Establish a procedure for estimating cycles to failure for novel bonded interface materials such as sintered micrometer and nanometer-sized silver particles, thermoplastic adhesives with embedded micrometer-sized carbon fibers, as well as lead-based and lead-free solders as a baseline.

Approach

- Establish various bonded interfaces between 50.8 mm x 50.8 mm cross-sectional area direct-bond-copper (DBC) and copper base plate samples. These interfaces will be based on sintered silver (micrometer and nanometer-sized particles), silver-indium paste, thermoplastics with embedded carbon fibers, lead-based and lead-free solder (as a baseline), and silver-filled adhesives.
- Perform thermal shock and thermal cycling on these samples (going from –40°C to 125°C) according to the Joint Electron Device Engineering Council (JEDEC) standards for up to 1,800 cycles as an upper limit. Monitor thermal resistance and perform acoustic microscopy and high-potential tests on these samples after select number of cycles.
- Perform mechanical tests on the select bonded interface samples to obtain information on stress versus strain relationship for the bonded material. In conjunction with modeling, this will ultimately help in establishing strain energy density versus cycles to failure curves for the different bonded interfaces.

- Change synthesis parameters to obtain improved thermal performance and reliability for the novel bonded interfaces under investigation.

Major Accomplishments

- We enhanced NREL testing capabilities through the acquisition of equipment such as a thermal shock chamber, a benchtop environmental chamber for thermal cycling, a hot press for synthesis of various types of bonded interfaces, a high-potential tester for characterizing dielectric strength of layers, and modified measuring blocks for the NREL ASTM steady-state apparatus for thermal resistance measurements. Approval has also been received for acquiring a C-mode scanning acoustic microscope (C-SAM) in FY2011.
- We established a subcontract with Virginia Tech to investigate thermal performance and reliability of bonded interfaces based on their nanosilver paste.
- DBC samples from Curamik (50.8 x 50.8 x 1.24 mm) and copper base plate (50.8 x 50.8 x 5 mm) samples were purchased or fabricated. All bonded interfaces will be studied between these two layers, which are coated with silver to improve bonding. All the interface materials mentioned in the section above for establishing the bonded interface were also acquired.

Future Direction

The following activities are envisioned for this project for FY2011 and FY2012.

- Synthesize and characterize the various bonded interfaces mentioned in the Approach section. In conjunction with modeling (finite element analysis) and incorporating suitable constitutive models for novel bonded interface materials, obtain information on cycles-to-failure for these interfaces.
- Expand the experiments and modeling to include other coatings on the DBC and base plate (gold), other substrates (DBC based on aluminum oxide or silicon nitride as opposed to aluminum nitride, or even direct-bond-aluminum [DBA]), and other base plates (aluminum, aluminum-silicon-carbide [AlSiC]).

Technical Discussion

Background

In a power electronics module, a semiconductor chip is typically attached by solder to a DBC ceramic substrate for electrical isolation purposes. This substrate is then mounted on to a base plate, typically copper or aluminum, which is then attached to a heat sink. A cross-section of a typical power electronics package is shown in Fig. 52 [1].

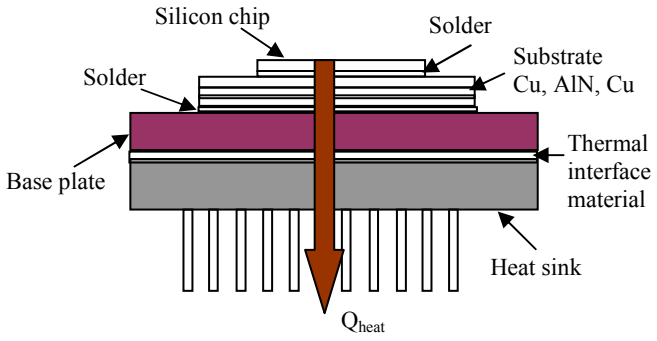

Fig. 52. A typical power electronics package

A CTE mismatch between the ceramic substrate and the copper base plate can cause crack initiation and propagation in the joining solder layer. Lead-based solders have predominantly been used in electronics

packaging; however, due to environmental reasons, there is a drive towards lead-free solutions. Lead-free solders are prone to thermomechanical reliability issues. Hence, alternative bonding techniques to solder are being developed to increase the thermomechanical reliability of this joint through the use of newer materials, such as thermoplastics with embedded carbon fibers and sintered silver micro- and nano-particles. While more common lead-based and lead-free solder materials have been analyzed to develop thermal fatigue cycles-to-failure predictions, little information is available for the more recently developed sintered and thermoplastic materials.

Previous work at NREL [1, 2] has focused on establishing a consistent, objective, and high-accuracy database via the ASTM steady-state approach 3 on the thermal performance of conventional as well as novel thermal interface materials. The conventional materials include greases, gels, phase-change materials, and filler pads. It was concluded that none of the conventional materials met the thermal performance specifications of 5 mm^2K/W thermal resistance for a 100 micrometers bondline thickness. Due to the promise of bonded interface materials, work at NREL is now focused on developing an objective and consistent story on the thermal performance and reliability of bonded interface materials. Conclusions on thermal performance and reliability from this effort will directly aid industry partners in making product development decisions. The testing procedure and laboratory equipment are described below.

Materials and Sample Synthesis

NREL has selected the following bonded interface materials for thermal performance and reliability testing:

- Kester Sn63/Pb37 solder paste (conventional lead-based solder)
- Henkel Innolot LF318 and SAC 305 lead-free solder
- Haraeus C8829A silver paste (for sintered interface based on micrometer-sized silver particles)
- Nanoscale silver paste developed by Dr. G.Q. Lu's group at Virginia Tech (for sintered interface based on nanoscale silver particles)
- Silver-Indium paste developed at the University of Maryland
- Dow Corning® DA-6534 silver filled, heat-curable silicone adhesive
- Henkel Hysol CF3350 adhesive film
- Btech thermoplastic adhesive film with embedded carbon fibers.

Each bonding material will follow its prescribed attachment procedure to form a 50.8-mm x 50.8-mm area footprint assembly. The assembly consists of a 5-mm-thick copper base plate attached to a DBC substrate (1.24 mm thickness). Before assembly, the copper layers in the DBC substrate and the copper base plate were electroplated with a 0.2-µm-thick and 5-µm-thick layer of silver, respectively, to improve adhesion with the bonding materials. A bake test in an oven at 300°C for 30 minutes was performed on both the silver-coated DBC and base plate samples. The intent of the bake test was to ensure there was no diffusion of copper through the silver coating. Diffusion of copper through the silver coating can prevent good bonding because of oxidation of copper. A sample DBC substrate and base plate are shown in Fig. 53(a), while the stencil that will be used for printing pastes onto the DBC and base plates is shown in Figure 2(b).

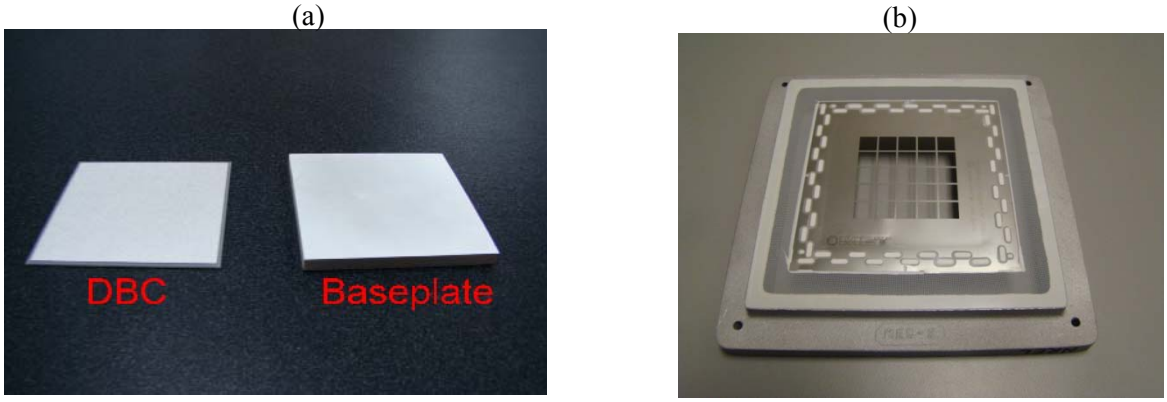

Fig. 53. (a) Sample DBC substrate and base plate, (b) Stencil for printing pastes

The bonding process for each interface material includes pressure and temperature requirements for optimal bond strength. NREL has developed a tabletop hot press for synthesizing test samples, as shown in Fig. 54. Two hot plates are positioned on either side of the sample to be bonded and are embedded with five 250-W cartridge heaters. Three heaters are inserted in the top hot plate and two in the bottom hot plate. A temperature controller adjusts the power of the heaters based upon the temperature measurement by a thermocouple located in the bottom hot plate. The test sample and hot plates are placed between layers of mica and cold plates (right side of Figure 3), and then inserted into an arbor press 4. Glycol-water (50-50% mix by volume) coolant is circulated within the cold plates to isolate the high bonding temperatures from the hydraulic piston and fluid. A screw jack is also placed between the hydraulic piston and top cold plate to provide fine adjustment to the applied bonding pressure. The pressure of the hydraulic fluid is electronically monitored to determine the force applied to the sample under bonding.

Bonded Interface Material Characterization

Degradation (e.g., cracks, voids) of the bonded interface can be nondestructively detected by several measurement techniques. After flaw initiation, the thermal and electrical performance of the sample assembly will degrade. Samples will be measured for initial performance and will subsequently be tested after a prescribed number of temperature cycles/shocks. NREL has previously developed a steady-state thermal resistance tester 1 based on ASTM test method D5470 3. The test setup is shown in Fig. 55, including an aluminum hot plate with embedded cartridge heaters and an aluminum cold plate with silicone oil circulating through it. Between the hot and cold plates are copper spreader blocks and copper metering blocks with embedded resistance temperature detectors (right side of Figure 4). For the bonded interface thermal performance and reliability testing, the metering blocks have been enlarged from 31.75-mm-diameter cylinders to 50.8-mm-square blocks to accommodate the larger square test samples.

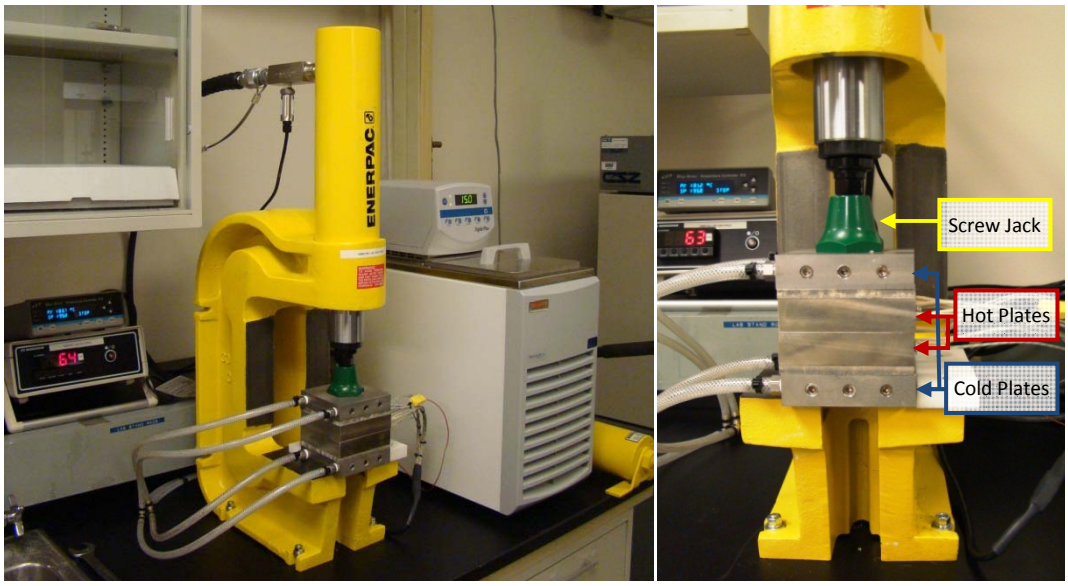

Fig. 54. NREL hot press

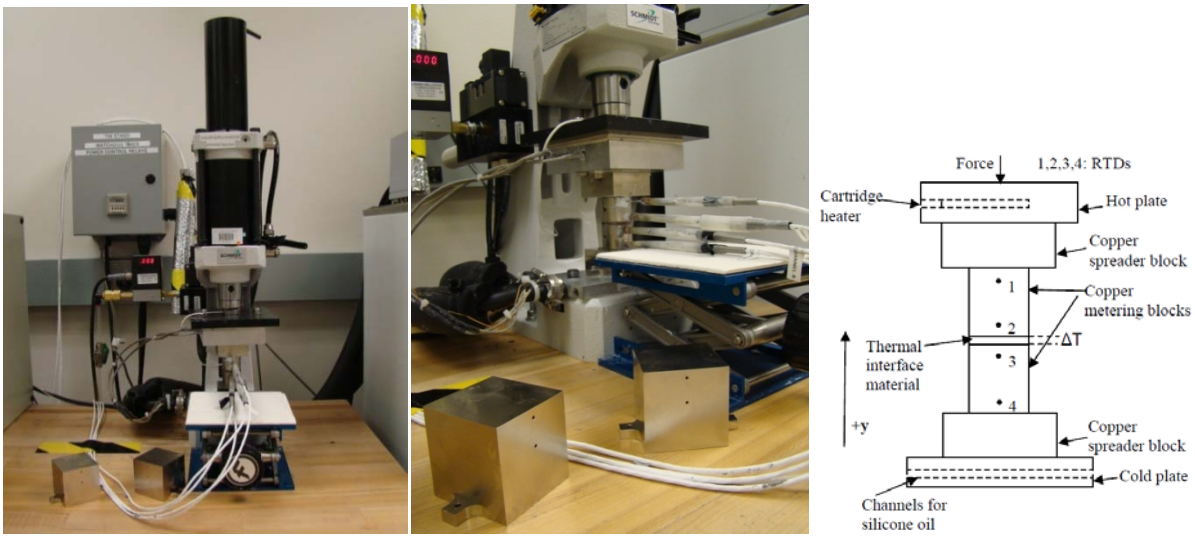

Fig. 55. Steady state thermal resistance tester (left), shown with modified 50.8 mm metering blocks (center) and as a schematic (right)

In addition to steady-state thermal resistance measurements, the electrical resistance of the samples will also be measured. In a high-potential (hipot) test, a high voltage is applied to an electronic device's current carrying components. The quality of the insulation in the device is determined by measuring its leakage current. Excessive leakage current indicates that dielectric breakdown in the insulation has occurred 5. NREL has constructed a dielectric resistance tester based on the hipot testing process to detect when a delamination, crack, or void in the DBC/base plate assembly has developed. A custom fixture contacts the top and bottom sides of a test sample and applies a standard test voltage. Leakage current exceeding a prescribed limit will indicate that damage has occurred within the sample. The dielectric tester is surrounded by an acrylic safety enclosure to protect the operator from the high voltages used during sample examination. The fixture and enclosure are pictured in Fig. 56. Additional nondestructive

investigation of the test samples will include the detection of cracks, voids, and delaminations by a C-mode scanning acoustic microscope.

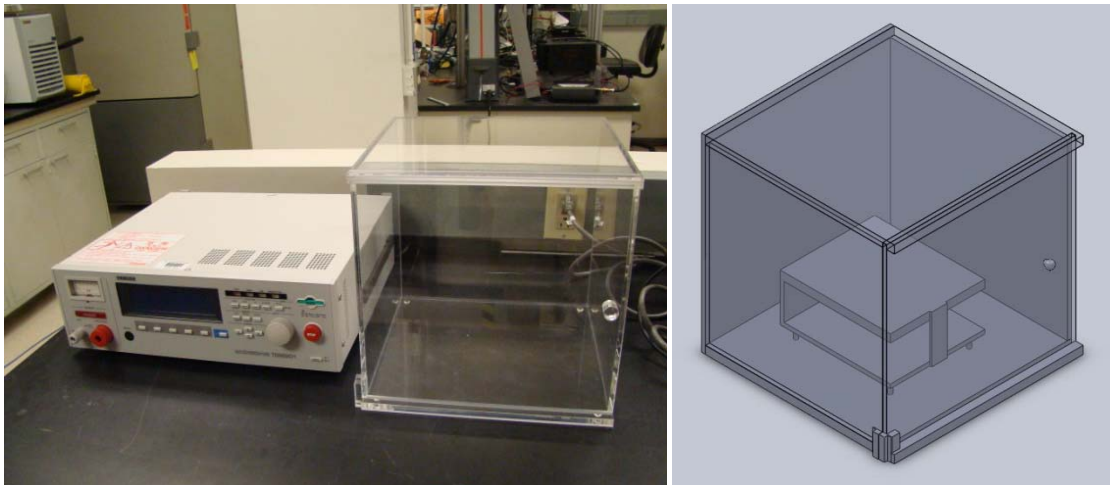

Fig. 56. Dielectric resistance tester.

Thermal Testing

In both physical testing and modeling, a "duty cycle" must be defined to induce failures in the samples under test (physically or mathematically). Generally speaking, there are three types of thermal duty cycles that can be used to create thermally induced stresses: a temperature cycle, a thermal shock cycle, and a power cycle. A temperature cycle specifies the temperatures to which a sample under test will be exposed, the durations of exposure, and the rate of change of temperature when the sample under test is brought to a new temperature set point. A thermal shock cycle is similar to a temperature cycle, but consists of rapid changes in the environmental temperature. Finally, a power cycle is created by heat dissipation in an actual electronics device to create realistic heat flow patterns and temperature distributions in a sample under test. Power cycling will not be conducted in our early bonded interface tests as there is no convenient way to include an electronic component such as an IGBT or diode onto the sample to create heat. Because the lifetimes of samples are too long to be tested in real time, accelerated test procedures must be employed to bring testing times down to a reasonable duration.

Joint or bond fatigue due to temperature cycling is dependent on several loading conditions. Acceleration factors for a test include the cycling temperature range, soak time, and ramp rate. Each factor affects the reliability of the bond; therefore, standards have been developed for specific test conditions. JEDEC Standard No. 22-A104D lists several test conditions suitable for electronics testing, with nominal minimum temperatures ranging from -65°C to 0°C and maximum temperatures ranging from 85°C to 150°C 6. Several authors specify JEDEC test condition G when subjecting their electronic test package samples to temperature cycling between –40°C and 125°C (see, for example, 7) while others cycle over the larger temperature range of –40°C and 150°C, following test condition M 9. NREL testing will follow JEDEC test condition G for cycling between –40°C and 125°C to evaluate the reliability of the bonded interfaces.

In addition to the temperature cycle range, JEDEC standard specifies the soak, or dwell, time. For electronic packages, the soak time is a period from 1 to 15 minutes at sample temperatures within a specified range of the nominal minimum and maximum temperatures. For component temperature cycling, a minimum soak time of 1 minute is specified. Solder fatigue and creep testing of

interconnections require longer soak times of 5 to 15 minutes 6. NREL testing will use a soak time of 10 minutes at maximum and minimum temperatures to follow JEDEC soak mode 3.

Ramp rates for thermal cycling must be sufficiently low to avoid transient thermal gradients in the test samples. To keep the temperature of the sample within a few degrees of ambient conditions, the JEDEC standard recommends that ramp rates remain under 15°C/min for any portion of the cycle with preference for lower rates of 10°–14°C/min. An alternative standard, IPC-SM-785 10, also defines a temperature cycle as a ramp rate less than 20°C/min. Higher ramp rates that exceed 30°C/min are considered thermal shock testing and will also be evaluated in our work. The Cincinnati Sub-Zero MicroClimate benchtop thermal test chamber and VTS Compact Thermal Shock Chamber will be used for sample testing and are shown in Fig. 57.

Fig. 57. CSZ MicroClimate (left) and VTS Compact Thermal Shock Chamber (right)

For an evaluation of the thermal cycling chamber (CSZ MicroClimate) to be used for testing, blocks of aluminum and copper with a total mass of approximately 1.2 kg were placed inside the chamber, and maximum chamber ramp rates were used. Cycling from –40°C to 125°C required approximately 30 minutes and cycling from 125°C to –40°C required 35 minutes, corresponding to ramp rates of 5.5°C/min and 4.7°C/min. The total cycle time in the test chamber was approximately 85 minutes, including 10-minute soak times at the temperature extremes.

Reliability Calculations

By developing a model that estimates the fatigue life of bonded interfaces during thermal cycling, prediction of crack/flaw initiation and/or propagation can be extended from the NREL test samples to power electronic devices of various geometries operating under different thermal cycle/shock profiles. Constitutive models can predict the stress-strain behavior of a bonded interface material caused by the CTE mismatch between the copper base plate and the ceramic substrate. The Anand viscoplastic law [11, 12] has been widely used in solder joint stress analysis 13 and has been incorporated into the ANSYS software package. Constant strain rate and temperature tests provide the experimental data that determine the nine material constants in the Anand model by curve fitting 14. The Anand model comprises the following plastic strain rate equation:

$$\dot{\varepsilon_p} = A\exp\left(-\frac{Q}{RT}\right)\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{1/m} \quad (1)$$

where:

σ = equivalent stress
s = deformation resistance
ξ = multiplier of stress
$\dot{\varepsilon}_p$ = inelastic strain rate
A = pre-exponential factor
Q = activation energy
R = universal gas constant
T = absolute temperature
m = strain rate sensitivity

The equivalent stress is defined as:

$$\sigma = cs; \quad c < 1 \tag{2}$$

where c is a function of temperature and strain rate by:

$$c = \frac{1}{\xi} \sinh^{-1} \left\{ \left[\frac{\dot{\varepsilon}_p}{A} \exp\left(\frac{Q}{RT}\right) \right]^m \right\} \tag{3}$$

An evolution equation of s is defined as:

$$\dot{s} = \left[h_0 \left| 1 - \frac{s}{s^*} \right|^a sign\left(1 - \frac{s}{s^*}\right) \right] \dot{\varepsilon}_p; \quad a \geq 1 \tag{4}$$

with:

$$s^* = \hat{s} \left[\frac{\dot{\varepsilon}_p}{A} \exp\left(\frac{Q}{RT}\right) \right]^n \tag{5}$$

where:

s^* = saturation value of s associated with a fixed temperature and strain rate
h_0 = hardening/ softening constant
a = strain rate sensitivity of hardening/ softening
$\hat{s}$ = coefficient
n = strain rate sensitivity for the saturation value of deformation resistance

With s_0 as the initial value of s, the nine material parameters of the Anand model, ξ, A, Q, m, h_0, a, $\hat{s}$, n, and s_0 can be determined by curve fitting to experimental data 14. These parameters can be used by the software package ANSYS to properly account for nonlinear material behavior of the bonded interface when a power electronics package under consideration is subjected to thermal cycling.

The experimental testing determines the number of accelerated thermal cycles required to cause failure in the NREL test samples. By simulating the sample geometry and accelerated thermal cycles in the ANSYS software, the strain energy density accumulation can be calculated in the bonded interface material for every thermal cycle. The summation of the strain energy density over the number of cycles needed for experimental failure yields the total energy dissipated in the interface before failure. Failure here is defined as the initiation of the crack or flaw, but could be extended to cases where the cracking or voiding covering certain area leads to a certain percentage increase in the thermal resistance of the sample. Lifetime estimation can be made for actual operation conditions by assuming the same total energy dissipation is required for failure. Several authors have used this method as an indicator of failure by thermal fatigue 13.

Summary of Procedure

The description in the preceding sections outlines the laboratory capabilities and modeling theory to obtain thermal reliability estimates for novel bonded interface materials. The process is summarized in Fig. 58 below.

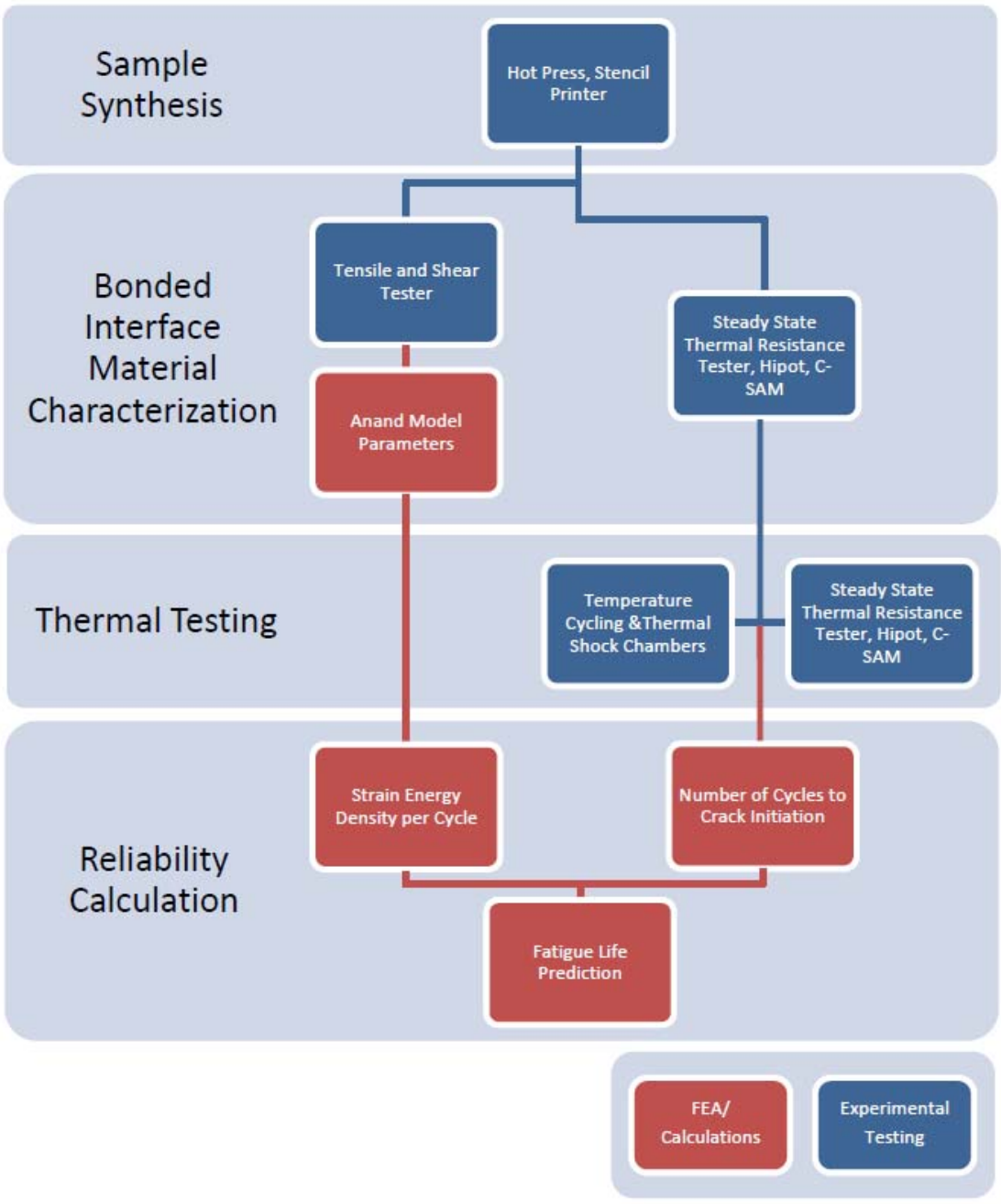

Fig. 58. Flowchart of bonded interface thermal reliability testing procedure

Conclusions

The work done in FY 2010 lays the groundwork for testing and analyzing the thermal performance and reliability of a number of bonded interface materials/technologies of strong interest in power electronics packaging applications. Significant experimental capabilities and collaborations have been established to synthesize, characterize, and model the thermal performance and reliability of a number of conventional (as a baseline) and novel bonded interface material technologies. Lessons learned from this study will also be used in improving process parameters for bonded interface synthesis using new materials such as sintered silver particles and thermoplastics with embedded carbon fibers.

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5.7 Thermal Stress & Reliability for Advanced Power Electronics & Electric Machines

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Objectives

The objective of this research activity is to develop and publish information related to validated physics-of-failure models for use by industry, academia, and the national laboratories in the evaluation and design of the next generation advanced power electronics modules that meet program targets for specific power, power density, and cost. A physics-of-failure model is capable of predicting the life of an engineering component with respect to some failure mechanism based on the material properties of the materials used for construction as well as the stress loading history of the component. A better understanding of the physics of failure can enable designers to reduce their system costs by reducing their design margins, increasing their operating margins, and enabling the use of new materials that provide better overall system benefits.

Our focus this year has been on bonded joints in power inverter modules and their related failure mechanisms. In fiscal year 2011, we plan to include an investigation of the physics of failure of electrical interconnects.

Approach

- Used a combination of analytical models (physics-based mathematical models), numerical models (based on the finite element method), and experimental testing to understand the physics of failure of bonded interfaces.
- Presented results at a FreedomCAR and Fuels Electrical and Electronics Technical Team meeting, the ASME International Mechanical Engineering Conference, and the 2009 IEEE Accelerated Stress Testing and Reliability Workshop for feedback.
- Technical approach:
- Conducted a comprehensive survey of analytical thermal stress models for bi-material and tri-material systems and implemented the models in Microsoft Excel.
- Compared the results of the finite element model prediction against the analytical models.
- Designed an experimental plan for bonded interface testing, planned equipment purchases, and set up laboratory experiments.
- Designed and analyzed a sample for testing bonded interface fatigue life.

Major Accomplishments

- Completed a comprehensive literature survey of analytical models of thermally induced stresses in bi-material and tri-material epitaxial (thin stacked plate) structures. These models are primarily in the elastic regime.
- Implemented analytical models from literature in a Microsoft Excel worksheet and added a user interface, a batch run system to perform design of experiments, and a Pareto chart output.
- Compared the outputs of a bi-material system implemented in a finite element analysis (FEA) software package with analytical results from the literature. We found good correspondence. A tri-material system has been similarly created although the comparison is less favorable—more work is needed.
- Modeling results from 2009 based on a Coffin-Manson fatigue model were presented to the FreedomCAR and Fuels Electrical and Electronics Technical Team, documented in a technical paper presented at the ASME International Mechanical Engineering Conference, and presented at the 2009 IEEE Accelerated Stress Testing and Reliability Workshop.

Future Direction

- Demonstrate correspondence between analytical tri-material system predictions and FEA.
- Use the Anand viscoplastic model for bonded interface materials in a bonded joint thermal stress FEA. Use technical literature and/or work with other national laboratories and research organizations to determine the material coefficients for the Anand model for novel bonded interface materials.
- Use techniques based on strain energy density or elastic/plastic/viscoplastic work partitioning per cycle to create empirical models that correlate damage rate with cycles to failure for novel bonded interface materials.
- Investigate the range of validity of the empirical models developed above, including whether they hold for the same materials in different form factors, the same materials with different surface coatings, the same materials with different processing parameters, etc.
- Because of the critical need to integrate experimental results into this modeling project, this project will be merged with the NREL project titled “Thermal Performance and Reliability of Bonded Interfaces” going forward.

Technical Discussion

Introduction

The objective of the thermal stress and reliability efforts at NREL is to publish and provide validated physics-of-failure model information and sufficient background to allow designers of next generation power electronics systems to investigate the use of novel bonded interface materials in the creation of systems that meet FreedomCAR and Fuels technical targets for cost, weight, efficiency, and volume while meeting requirements for life, safety, and customer acceptance.

Model validation is a key requirement for our efforts. As such, this project (which emphasizes modeling) is being merged with another NREL project (which emphasizes experiment) called “Thermal Performance and Reliability of Bonded Interfaces.” Future modeling efforts will appear in conjunction with the “Thermal Performance and Reliability of Bonded Interfaces” project. For this reason, work done in these two projects on specifying the duty cycle for testing is reported in the section “Thermal Testing” in the milestone report for the “Thermal Performance and Reliability of Bonded Interfaces” project.

Our approach is to develop validated physics-of-failure models by leveraging the strengths of analytical models in the literature, numerical solvers (primarily industry software packages using the finite element method), and experimental results. This technical discussion will focus on the progress made this year

with regard to development of a computer tool to run analytical thermal stress models that can be used to inform an FEA analysis and to do quick studies over a problem domain. We will also present comparisons made between FEA results and corresponding analytical models and progress made on combined electro-thermal-mechanical modeling for power modules.

Analytical Models

In this section, we will discuss various analytical models from the literature, their strengths and weaknesses, how results from the analytical models compare to each other as well as to similar results from a finite element code, and the next steps for both testing and analysis.
Analytical models based on physics and using simplifying mathematical assumptions are useful for quickly predicting thermally induced interfacial stresses in electronic packaging. The analytical models give guidance as to which engineering parameters (i.e., geometry, material properties, etc.) contribute most to an output stress of interest. They can also be used as a guideline to inform some FEA runs as to an expected result.

The analytical models for thermally induced stress can be generally categorized by the basic theories they are based upon: beam theory or theory of elasticity. We chose to concentrate on the models based on beam theory as they are more easily applied and equally valid. The assembly used for a bi-material model is shown in Figure 1. Figure 1 depicts two layered flat plates (shown on edge). The moments (M) and forces (F) at cross section, x, are shown. Figure 1(a) depicts the thicknesses (h) of each layer while Figure 1(b) shows the interfacial shearing stresses (τ) and peeling stresses (P) that arise at the interface. Figure 1(b) also indicates the total length of one plate as $2 \cdot L$ with L being the half-length of a layer. The shear stress occurs parallel to the bonded interface, and the peeling stress occurs normal to the bonded interface. The points of greatest stress are close to the edges of the bonded layers (but not directly at the edge).

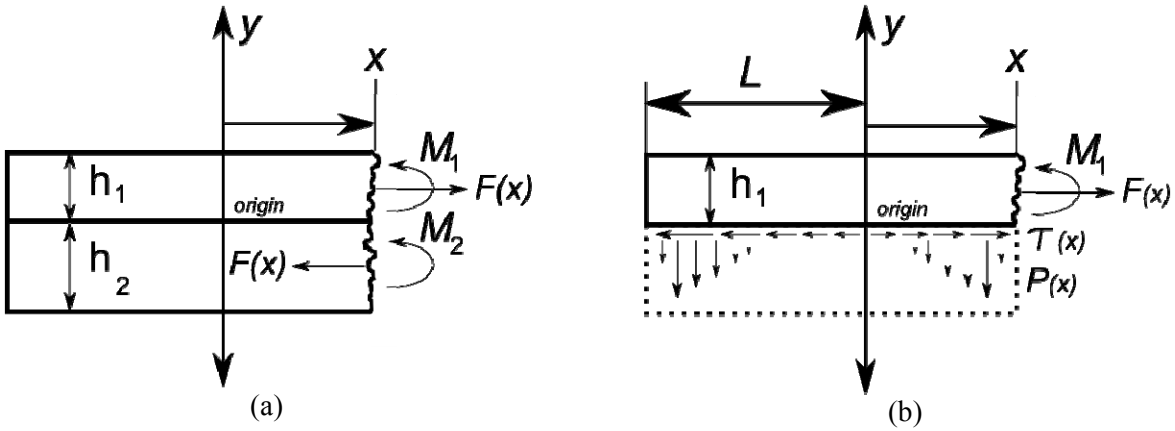


Fig. 1. Forces and moments in a bi-material assembly under thermally induced stress. (a) is the full assembly while (b) shows layer 1 with a ghosted (dashed) image of layer 2 and indicates the shearing forces that arise at the interface between layer 1 and 2

Limitations

Although analytical models have many benefits, they also have limitations and therefore must be used with care. Wang and Hsu [1] used a photoelastic method to determine experimentally the whole-field state of thermal stresses in bonded structures. A good match was found with FEA except in the vicinity of the edges. However, comparison with theoretical results indicated the theoretical methods oversimplify the state of stress and may need to be improved. Thus, the analytical models we present here are used only to provide directional indications and additional information for FEAs.

The analytical models for thermally induced stress that we found most useful to this project are based on beam theory. Within the beam theory context, each flat plate in a stack of bonded layers is assumed to be a thin "plate-like" beam. Thus, one limitation to the analytical models we reviewed is that the analysis is primarily in one dimension (along the length of this "beam"); a second dimension can be considered only in as much as plate-like beams are stacked one atop another. Therefore, two-dimensional and three-dimensional effects such as corner stresses are not captured.

A second limitation is that most of the models we reviewed assume materials remain in the linear elastic region throughout their life. However, real bonded interfaces may operate in not only the elastic regime, but also the plastic, and/or viscoplastic (creep) regime. Care will be needed when interpreting analytical model predictions if the material leaves the elastic region.

Another limitation of many analytical models is that they assume the temperature of the system is uniform across all materials. This is a good idealized approximation of the conditions within a thermal shock chamber where we intend to do testing. However, it is not a good recreation of the actual operating environment where we expect the temperature to be stratified from a hot semiconductor switch to a cooler heat sink.

Lastly, most published analytical models are limited to bi-material or tri-material assemblies whereas an actual inverter stack may consist of several individual layers. However, these simplified models are still appropriate for calculating stresses in a five-layer assembly if, for example, the direct bond copper (DBC) layer is seen as a single material, as shown in Figure 2.

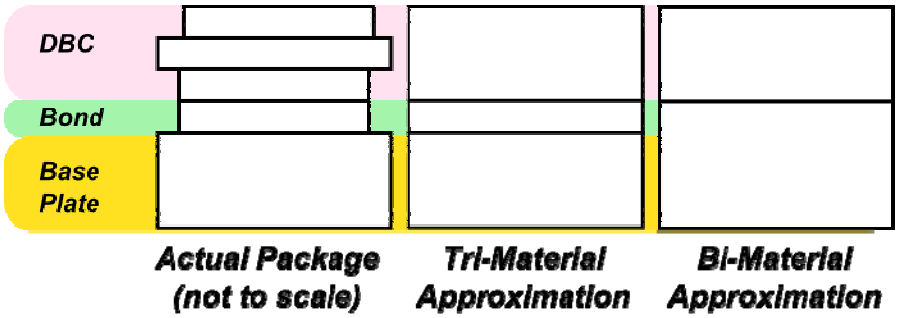


Fig. 2. Example bonded joint and depiction of a tri-material and bi-material approximation

A DBC (made up of three layers) can be replaced by a single layer with equivalent material properties: Young's modulus, Poisson's ratio, and coefficient of thermal expansion. For example, an equivalent Young's modulus can be derived using a weighted average based on layer thickness [2]. The calculation for the equivalent Young's modulus is displayed below:

(1)

Analytical Thermally Induced Stress Prediction Tool

In the next couple of sections, we will highlight a computer tool we constructed to automate the calculation of thermally induced stresses as predicted by several analytical models. The tool is written in Microsoft Excel. Here, we are particularly interested in predicting what the thermally induced stresses might be in test coupons consisting of a DBC (or DBA – direct bond aluminum) substrate bonded to a base plate. The test coupons will be used to characterize the cycle life of novel bonded interface materials during experiments planned for fiscal year 2011. Testing will reveal how different materials, loading conditions, and geometries affect cycles to failure. Analytical modeling can give us an initial feel for these anticipated results.

Analytical Model Predictions from Bi-Material and Tri-Material Models

For the results presented below, we will assume a test coupon consisting of a Si_3N_4 DBC bonded with a silver sintered attach material to a copper base plate and shall observe stresses at a temperature change of 190°C below the assumed stress-free bonding temperature of 150°C (i.e., at −40°C). There is nothing special about this example case other than it is one of many material combinations we could potentially examine in testing. We will use it here strictly to observe differences in model predictions for one case. The overall length of the assembly is taken to be 50.8 mm (2 inches). The material properties of the assembly are shown below in Table 1.

Table 1. Material Properties for Si_3N_4 DBC Substrate Sintered to a Copper Base Plate

Location	Thickness	Young's Modulus	Poisson's Ratio	Coefficient of Thermal Expansion
	(mm)	(GPa)	--	(ppm/°C)
DBC (equivalent properties)	0.920	153.57	0.30	16.6
Bonding Material	0.127	60.00	0.30	19.6
Base Plate	6.000	110.00	0.34	17.0

We used analytical models from the literature to predict both shearing and peeling stresses at the bonded interface of the example problem described above. Figure 3 shows how stresses vary across the length of a joint, L, as predicted by three bi-material thermally induced stress models: Suhir (1986) [3], Suhir (1989) [4], and Ru (2002) [5]. Results are reported as stress at the given normalized half-length or x/L; recall from Figure 1 that x is measured from the center of the assembly and the length of the assembly is 2·L. Shear stress is depicted in Figure 3(a) and peeling stress in Figure 3(b). The center of the joint would be where x/L equals 0.0, and the free edge of the joint is where x/L equals 1.0. The model by Suhir (1986) is elegant in its simplicity but does not correctly recreate the zero shear boundary condition. The Suhir (1989) model corrects for this using a high-order differential equation. Ru's model uses a lower order differential equation than the Suhir (1989) model and is able to capture the zero-longitudinal force and zero-shear stress boundary conditions at the free edge; however, Ru does not give a physical justification for his simplifying assumption. Peeling stress is given in Figure 3(b). There is a large discrepancy between the three models given for peeling stress in Figure 3(b). Unfortunately, we were unable to duplicate the results of the example problem from [4] using the closed form mathematical equations given in the paper. We were, however, able to duplicate the results of the example problem using equation 12 of [4], which relies upon the first and third derivatives of the shear stress (taken numerically). It is surprising to see that there is such a difference in the magnitude of peeling stress between the Suhir (1986) and Suhir (1989) models.

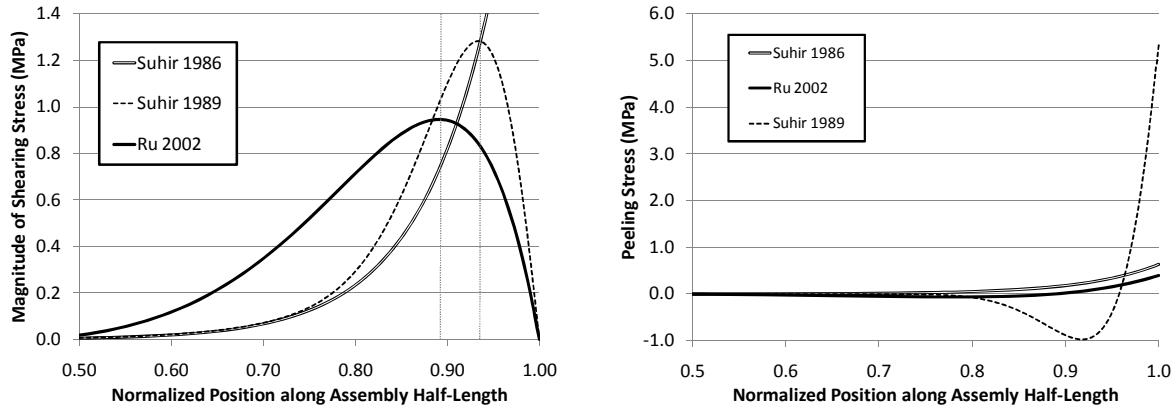


Fig. 3. Thermally induced stresses predicted in a bi-material assembly for (a) shear stress using the Ru (2002), Suhir (1986), and Suhir (1989) models and (b) peeling stress using the Ru (2002) model.

Figure 4 depicts the interfacial shearing stress from two analytical tri-material models: one from Schmidt (1999), [6], and one from Suhir (2001), [7]. In a tri-material approximation, the bonding material can be explicitly modeled which yields two interfaces where interfacial shear stresses can occur: at the interface between the DBC and the bonding material and at the interface between the bonding material and the base plate. Note that this model is similar to the Suhir (1986) model in that it does not incorporate a zero-shear stress boundary condition at the free edge.

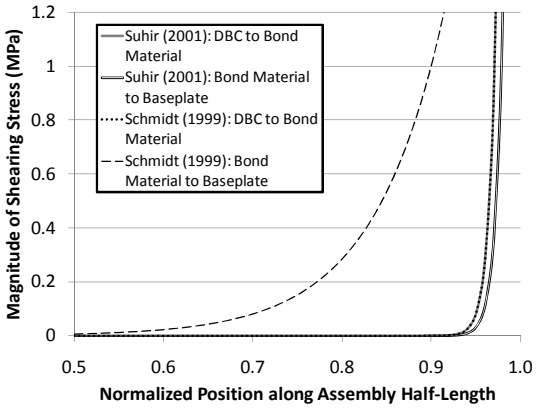


Fig. 4. Tri-material shear stress predicted using the Schmidt (1999) and Suhir (2001) models

A tri-material assembly introduces two interfacial boundaries: one from the DBC to the bonding material, and another from the bonding material to the base plate. Thus, for each model, there are two curves in Figure 4. The shear stress predicted between the DBC and bonding material is exactly the same for both the Suhir (2001) and Schmidt (1999) models; this is not surprising since both models derive from a common source. However, there is disagreement between the shearing stress predicted at the bonding material to base plate interface. Here, the Schmidt (1999) model prediction for stresses at the second interface corresponds closely to the Suhir (1986) prediction. According to both tri-material stress models, the act of explicitly simulating the bonding material indicates the potential for an interface with higher interfacial stress concentrations located closer to the free edge than is predicted by the bi-material models. Further work is needed to understand the tri-material physics and interpret their results.

Based on a comparison of models with each other and based on a review of experimental validation in the literature, the Suhir (1989) model appears to best represent the shearing and peeling stresses in a bi-material structure from the models reviewed. The models given in [3], [5], and [8] also appear to be useful in that they compare well with the Suhir (1989) model and are somewhat simpler. Similarly, of the tri-material models examined, we were only able to implement the Schmidt (1999) and Suhir (2001) models sufficiently such that they were able to duplicate example problems given by the authors. In a comparison of select analytical models with experimental results, Wang and Hsu [1] found the Suhir (1989) model to provide an "appropriate prediction of the interfacial peeling stress" but is "not quite correct" for the interfacial shearing stress. With respect to the Suhir (1986) model, Wang and Hsu found it had "shortcomings in prediction of the interfacial peeling stress" but that the interfacial shearing stress estimate was "rational."

Comparison to Finite Element Results

The ANSYS FEA software was used to compare the previously discussed analytical models to a numerical solution. For this example, we used the dimensions and material properties presented by Suhir [3]. In the example problem, elongated molybdenum and aluminum plates are perfectly bonded together to form a bi-material system. The system, initially at a stress free temperature is subjected to a uniform temperature change resulting in thermally induced stresses at the interfaces due to differences in the

coefficient of thermal expansion of the two materials. The material dimensions and material properties are summarized in Table 2 [3, 4].

Table 2. Material Properties and Dimensions Used in the ANSYS FEA Model

•	Aluminum	Molybdenum
Young's Modulus (GPa)	70.38	325
Poisson's Ratio	0.345	0.293
Coefficient of Thermal Expansion (ppm per °C)	23.3	4.9
Layer Height (mm)	2.5	
Layer Width (mm)	25.4	
Layer Length (mm)	50.8	
ΔT (°C)	240	

ANSYS version 12.1 was used to predict the stresses in the bi-metal model. ANSYS DesignModeler was used to build the geometries and assign material properties.

We took advantage of symmetry in both the longitudinal and lateral directions in the FEA model. We constrained one corner to have no rotational or linear movement while the remainder of the model was allowed to deform as a result of the coefficient of thermal expansion (CTE) mismatches and interfacial stresses. In order to simulate a 240°C change in temperature from a stress-free temperature condition, we found it necessary to set the reference temperature of the model to 0°C while the environment temperature was set to a magnitude of 240°C.

Shear and peeling stresses were compared between the Suhir's 1986 and 1989 analytical models and the numerical results.

Shear stress values were obtained along the interface between the bi-material structure at seven defined locations along the X-axis and mid-way across the Z-axis (see Figure 5). Results are shown in Table 3. Both the Suhir (1986) and FEA models fail to predict the zero shear stress condition at the free edge. Over the remainder of the body, the Suhir (1986) model compares well with the FEA as also observed by Wang and Hsu [1]. It is unknown if the location or value of the maximum shear stress predicted by the Suhir (1989) model is correct, although, interestingly, it is within about 10% of the FEA prediction at 95% of the normalized half length.

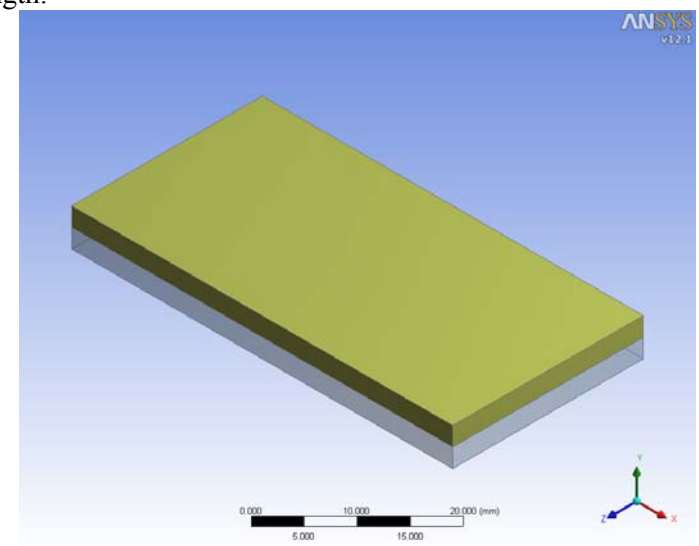


Fig. 5. FEA model of the bi-metal assembly from Suhir (1986)

Table 3. Comparison of the Predictions of Shear Stress Magnitude (MPa)

Normalized Position Along Assembly Half-Length	0.50	0.75	0.85	0.90	0.95	0.99	1.00
Suhir (1986) Model	0.04	2.48	13.50	31.52	73.61	145.06	171.87
Suhir (1989) Model	0.06	16.55	82.16	121.45	110.51	28.72	0.00
FEA	0.01	2.84	13.96	34.01	99.32	210.37	225.43

Peeling stresses are listed in Table 4. To determine peeling stress via FEA, values were averaged along the width of the sample at a given X location along the interface. For the analytical models, as noted previously, we were unable to predict peeling stress directly using the equations given in [4]. However, using equation 12 from [4], which involves the first and third derivatives of shear stress, we are able to reasonably duplicate the results presented in Figure 2 of the same paper. Those values are given in Table 4. Unfortunately, there does not seem to be good agreement between the FEA results and the analytical models for peeling stress although more investigation is needed.

Table 4. Comparison of the Predictions of Peeling Stress Magnitude (MPa)

Normalized Position Along Assembly Half-Length	0.50	0.75	0.85	0.90	0.95	0.99	1.00
Suhir (1986) Model	0.02	1.42	7.55	17.39	40.05	78.10	92.29
Suhir (1989) Model using equation 12 of [4] and numerical approximations of a first and third derivative	0.10	23.48	154.94	190.44	55.58	744.04	1010.67
FEA (at the interface)	6.92	10.73	22.34	28.23	16.77	173.94	394.64

Next Steps in Modeling and Simulation

Starting in FY2011, this task will be incorporated into the "Thermal Performance and Reliability of Bonded Interfaces" task. This offers an excellent opportunity to combine our modeling efforts with experimental testing. The algorithm for how we will combine test and simulation is depicted in Figure 6. For a set of bonded interface materials, we will choose a select number of variations. Parameters to vary include the substrate and/or substrate metallization layer materials (for example, direct bond copper or direct bond aluminum), base plate material, type of coatings used on the base plate and/or substrate, sample geometry, and thermal cycle. Because all of the stresses that arise from a bonded interface are driven by mismatch in the coefficient of thermal expansion, by varying each of these parameters, we create different strain energies inside the bonded interface material and at the interfaces between the bonding material and the substrate and base plate. Material properties for novel bonding materials not in the literature will be obtained through material properties testing at partner laboratories and/or at NREL.

We will use the finite element method and a constitutive model such as the Anand model [9-11] to predict the amount of strain energy accumulated per thermal cycle. This methodology has been pioneered elsewhere for solder materials [12, 13] although extensive data are not available for novel interface materials such as sintered joints. In parallel, actual thermal cycling will tell us how many cycles it takes to fail the given bonded joint variation. Failure can be defined with a criterion such as a given rise in bond thermal resistance or a given percentage of delamination. We can then plot the empirical relationship between the bonding material and the cycles it takes to fail. Such a relationship is useful to designers of advanced components in industry because they will be able to predict the life of the bonded interface for their unique application without having to engage in expensive and time-consuming accelerated life

testing—that is, if successful, life testing can be used as a validation tool as opposed to an analysis or design tool. Our next step is to create a parametric finite element model that uses the Anand model to predict the strain energy accumulated per cycle.

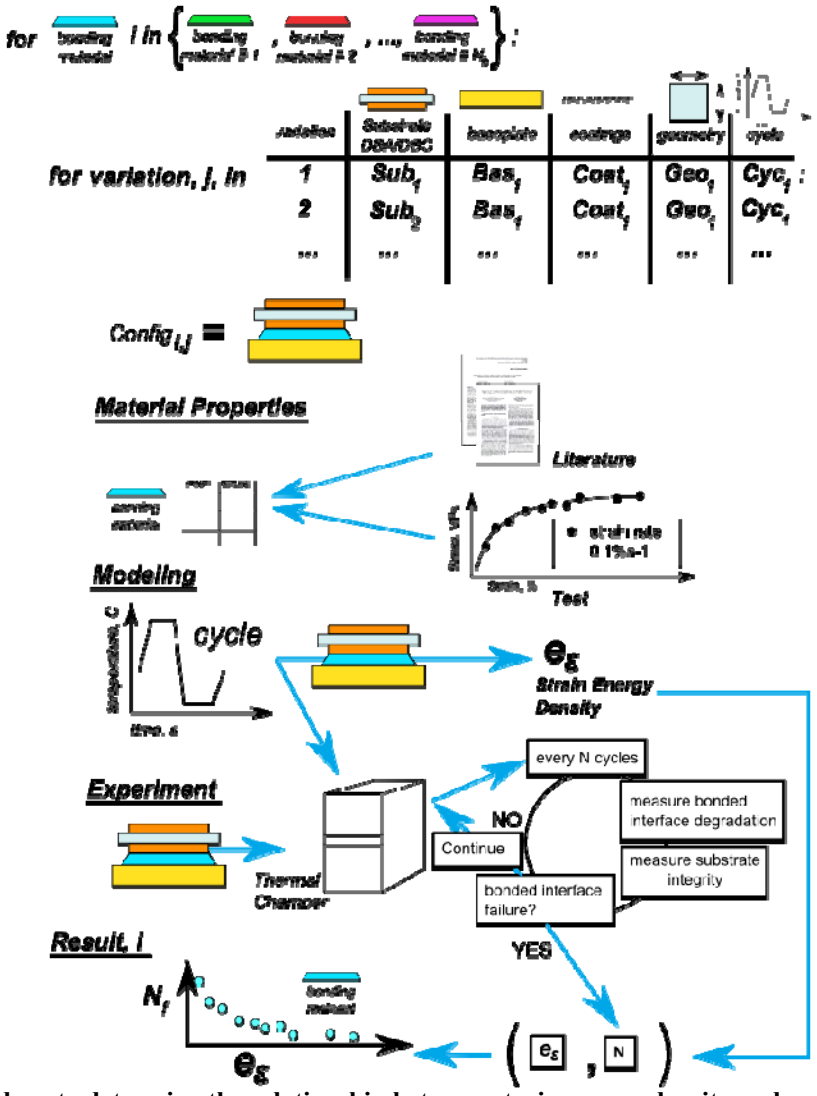


Fig. 6. Procedure to determine the relationship between strain energy density and cycles to failure

Electrothermomechanical Modeling of IGBT Modules

A critical element of the thermal stress and reliability effort has been the addition of thermomechanical fatigue models to the electrothermal modeling of power electronics. This work, which is being done as a collaborative effort between NIST, NREL, and the University of Maryland, has begun to introduce concepts of prognostics and health management into the reliability efforts being conducted as part of the APEEM program.

This work is prompted by reliability concerns that arise from the increased power density of modern power electronic modules. Though technological advances in chip design have improved the energy efficiency of devices, increased miniaturization of the devices and packages together with higher switching frequencies have led to power dissipation densities that are routinely in the range of 150-250 W/cm^2. Removing this heat requires enhanced single and two-phase cooling methods, such as those

described in other sections of this report. If the heat is not removed, the higher device junction temperatures that result when the device is powered will cause reduced device performance and reliability. Furthermore, the higher temperatures and the wider temperature swings during power cycling will degrade the packaging materials leading to decreased durability for the entire module.

This effort focuses on modeling the degradation in the packaging materials as a function of temperature or power cycling and correlating/validating this modeling against measurements of degradation on actual power modules. To model the effect of aging and thermal cycling on the performance and durability of a power module, an electrothermal model is created. The power dissipation in the electrical components provide the heat for the thermal template input nodes, which can be used to determine the temperature cycling magnitude at each package layer, while the calculated junction temperature can, in turn, be used to determine the electrical parameters of the device. Then thermomechanical stress modeling is conducted using University of Maryland physics-of-failure models to assess degradation in the package structure as a function of cycling. This degradation manifests as an increase in the thermal resistance of the damaged layer. The simulated junction temperature rise resulting from increased thermal resistance is then validated against actual junction temperatures measured after temperature cycling using unique NIST variable speed thermal stress and monitoring techniques, including transient thermal imaging (TTI) and high speed temperature sensitive parameter (TSP) measurement. The high speed temperature sensitive parameter measurement method uses the dependence of Vgs on temperature to determine the junction temperature of a device subjected to a power pulse. The Vgs values are calibrated against temperature by heating an unpowered device to known temperatures using a hot plate and then using a small test pulse to measure Vgs at that temperature. This calibration curve can then be used to infer the junction temperature from the Vgs value measured when a larger power pulse is used to heat the device.

The temperature cycling is conducted according to an accelerated testing protocol developed as part of this program. Also C-SAM, SEM, and X-ray images of the package are used to correlate the physical attach damage to the measured temperature increase. Finally, the higher junction temperature rise will then be used to determine the heating and cooling of the device during the next round of power cycling, as well as to serve as a monitor for the health of the packaged device.

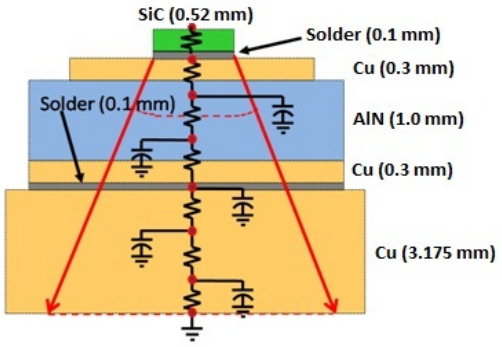


Fig. 7. Outline of electrothermal model for the SiC MOSFET in the Co-Pack Module

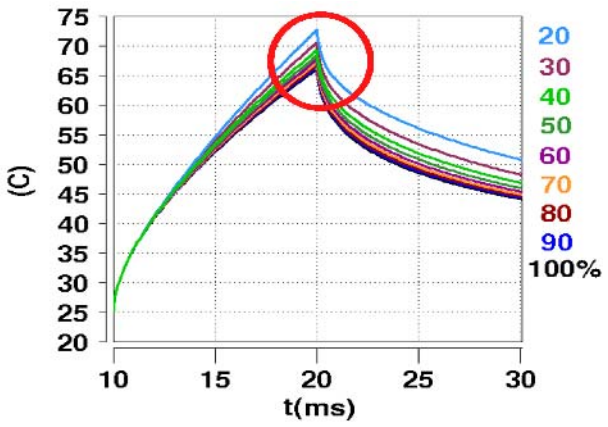


Fig. 8. Effect of die attach thermal conductivity level on junction temperature

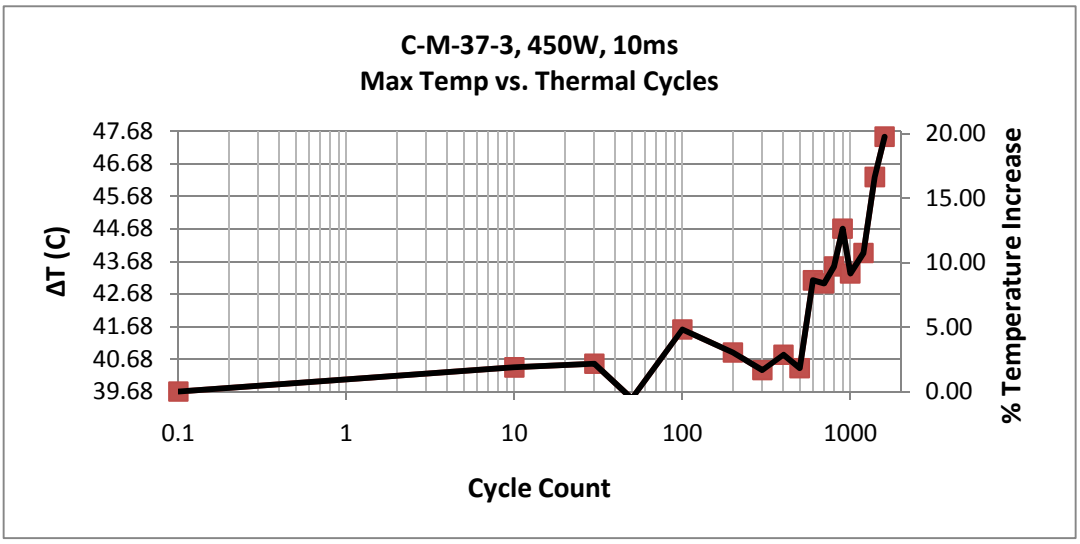
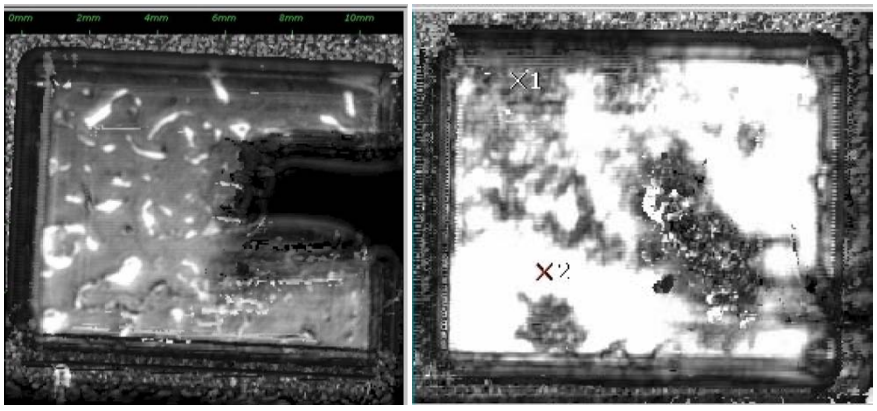


Fig. 9. Increase in ΔT_j resulting from thermal cycle damage to the module

As an example of this work, an electrothermal model was created for the Co-pack IGBT module, shown in Figure 7. Electrothermal modeling is used to predict the increase in junction temperature that occurs with decrease in the thermal conductivity of the die attach from 100% to 20% of its initial value as shown in Figure 8. This module was then cycled from 25°C to 200°C with a 10 minute hold at 200°C, a 5 min ramp up and a 5 min ramp down using the NIST variable speed thermal test system. The increase in the junction temperature for a fixed power pulse is measured using the temperature sensitive parameter technique as a function of cycling and plotted in Figure 9. This plot shows a significant increase in the change in junction temperature from 39.7°C to 47.7°C for the device subjected to a 450 W, 10 ms pulse after 1500 cycles, indicating significant damage in the die attach.

By correlating the measured change in temperature to the change in temperature resulting from an increase in the thermal resistivity of the die attach, one can model the increase in the resistivity of the die attach as a function of cycling. It was seen that a fivefold increase in thermal resistance was necessary to produce the 8°C change in ΔT_j observed in the measurements. Confirmation that the degradation causing this effect was concentrated in the die attach is provided by the C-SAM photographs in Figure 10.



(a) *(b)*

Fig. 10. Comparison of die attach delamination (shown as white areas) under the diode for a Co-Pack sample that underwent a) 0 cycles and b) 1500 cycles from 25°C to 200°C.

This work will continue into the next year as part of the "Thermal Performance and Reliability of Bonded Interfaces" project, where direct measurements of the increase of thermal resistance in attach materials as a function of thermal cycling damage will be used to generate, calibrate, and validate degradation models.

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