

# Study on PID resistance of HIT® PV modules

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#### Motivation

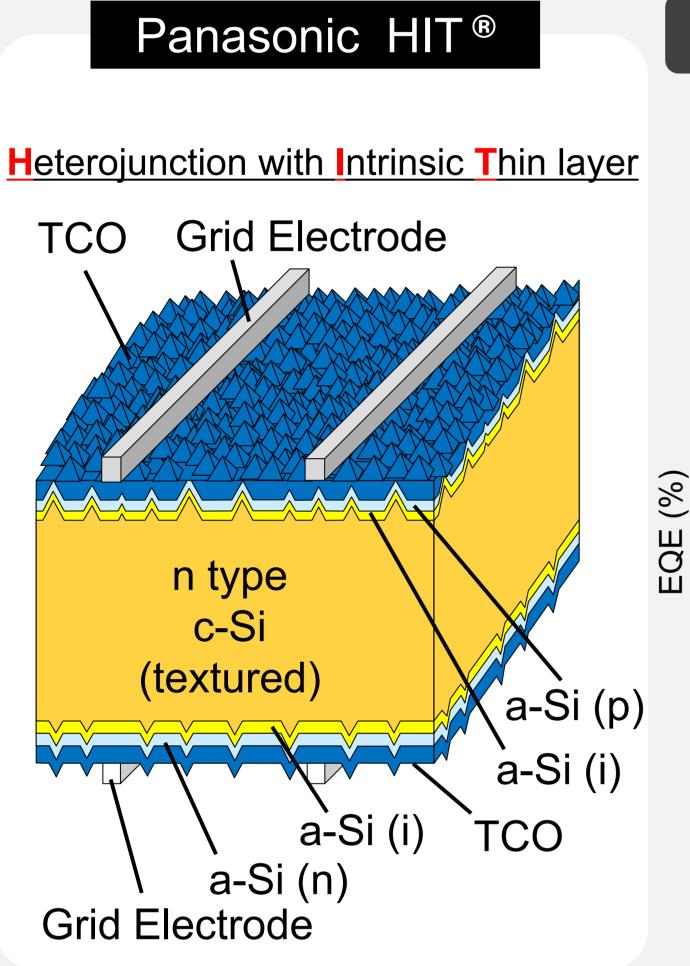
- 1. For increasing request in reliability, it is important to demonstrate that high-efficiency HIT module shows high PID resistance as originally designed.
- 2. For customer benefit, we aim for increasing high efficiency and reliability at the same time to maximize the lifetime power generation.

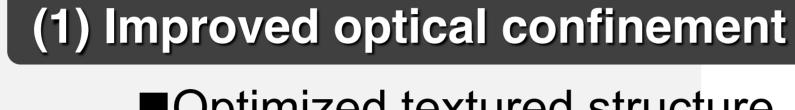
## Conclusion

- 1. All HIT PV modules have exhibited no sign of degradation under several PID tests.
- 2. Surface layer of HIT cell is TCO without insulating layer which does not cause accumulation of charges.
- 3. No incidences of PID have been reported from the European, U.S. or Japanese markets.

These facts confirm the high quality and high reliability of HIT modules.

## Maximizing the advantages of the HIT structure





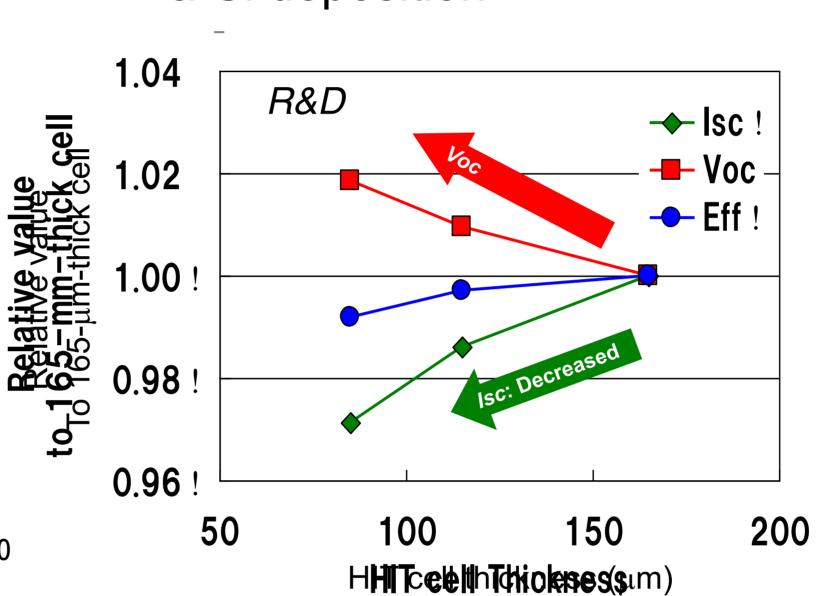
- ■Optimized textured structure ■High mobility TCO layer
- ■Wide gap a-Si layer
- 100.0 R&D 23.9% HIT (2012) 22.8% HIT 70.0 (2009)60.0 50.0 40.0 20.0 500 300 400 600

Wavelength (nm)

Improved Q.E. at shorter wavelengths

## (2) Improved heterostructure

- ■Clean Si surface
- ■Low damage, high quality a-Si deposition



Increased Voc can compensate for the drop in Isc

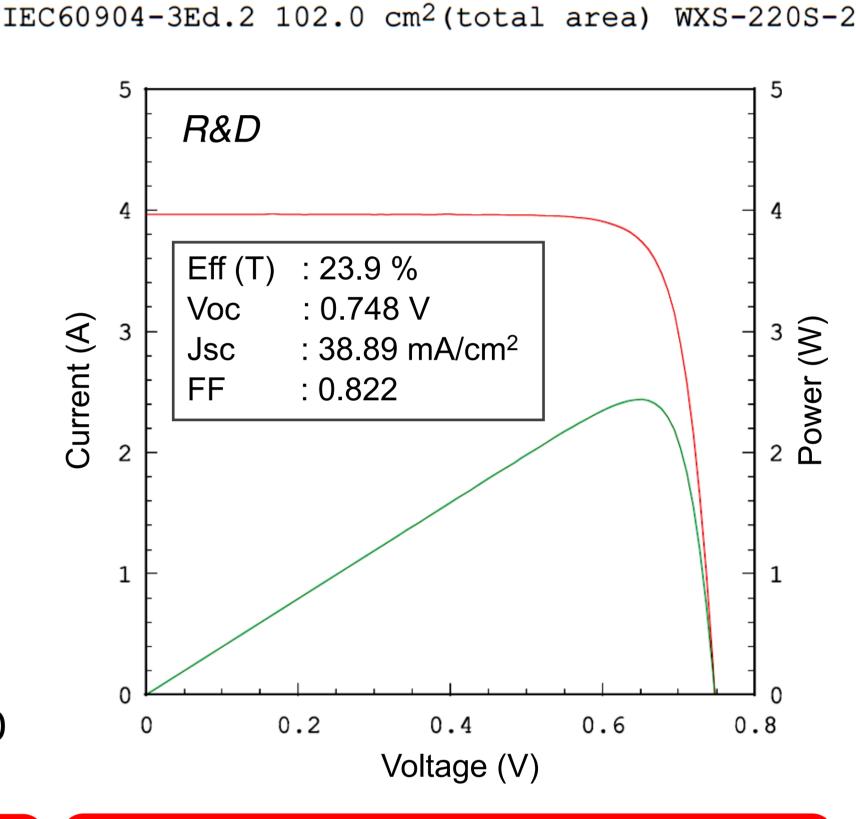
105

Degradation 6 0

Power

85

Results of PID test by Chemitox Inc.



I-V CURVE

23.9% efficiency with 98-µm thickness

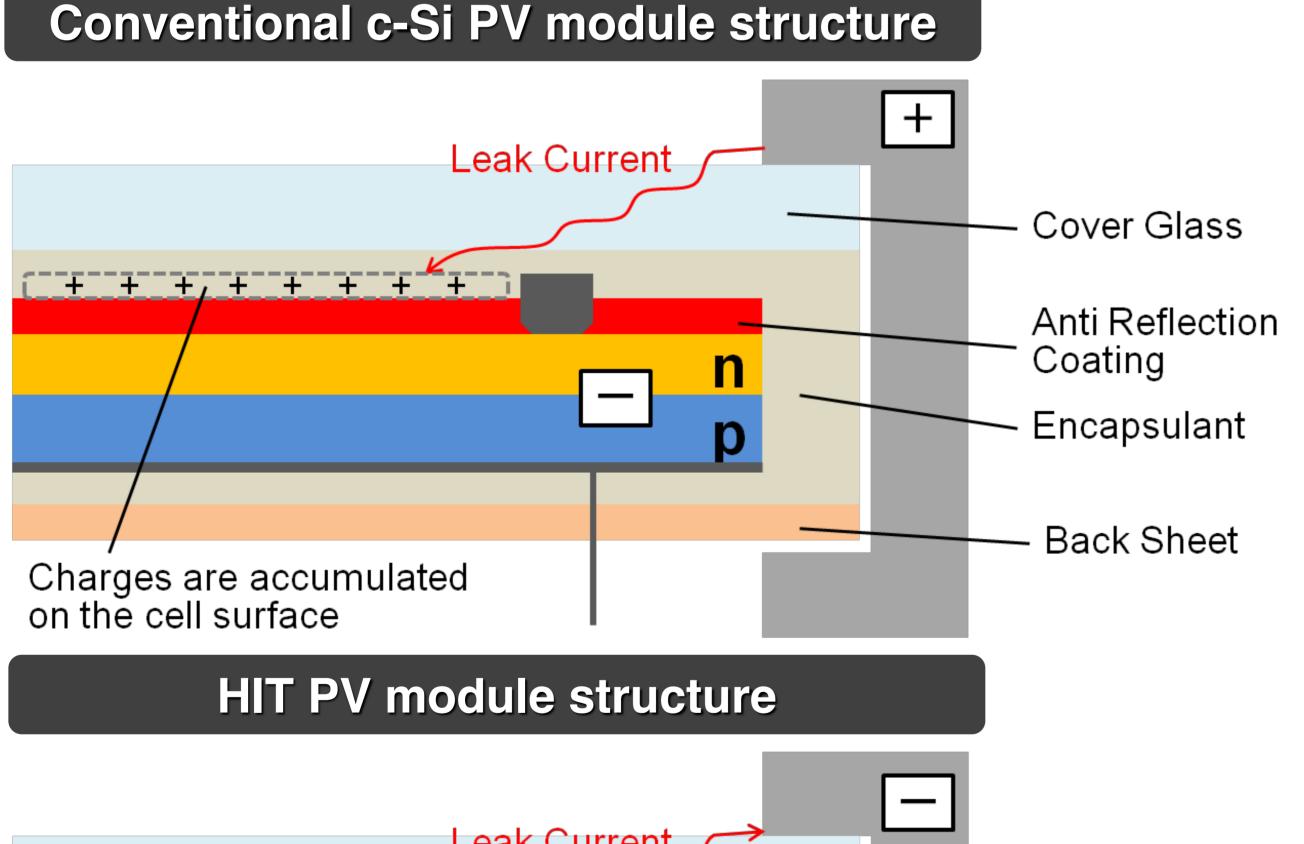
60°C 85%RH +1000V

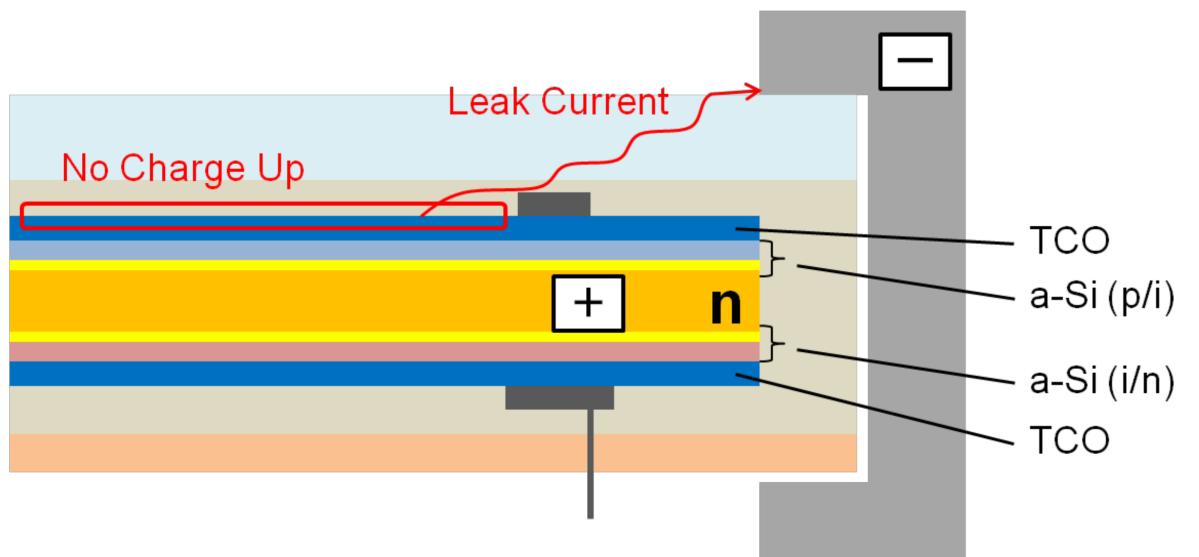
**VBHN240SJ01** 

**VBHN233SJ01** 

HIP-215NKH5

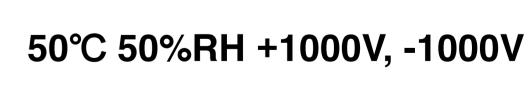
## PID resistance of HIT structure



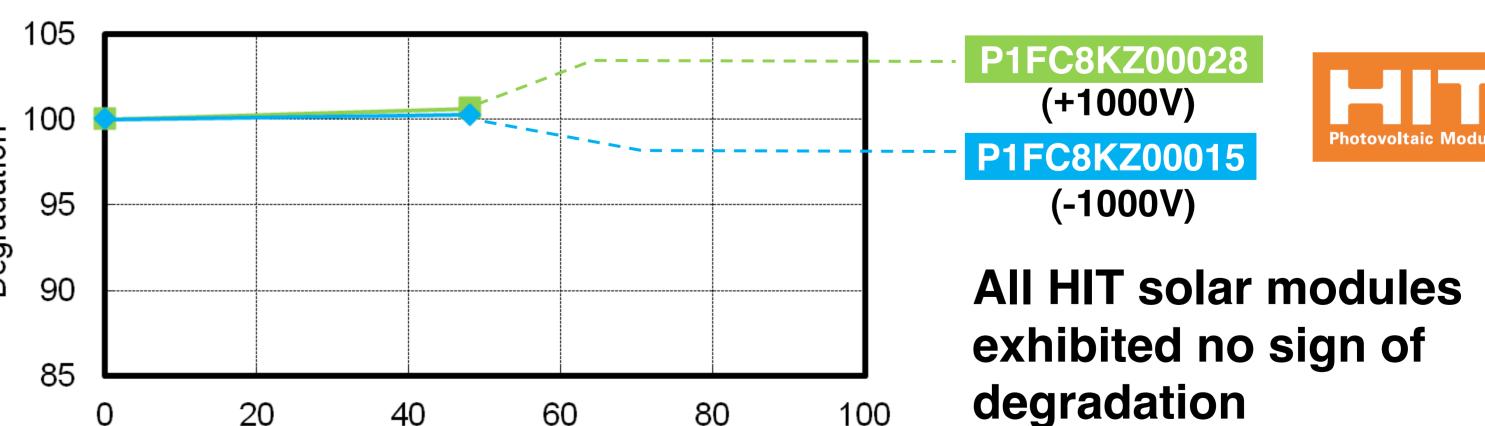


# Relative Max c-Si PV module A c-Si PV module B 70 20 100 60 Hours in Damp Heat Chamber Results of PID test by Fraunhofer CSP 105 Relative Max Power Degradation 100

Hours in Damp Heat Chamber



non-HIT



#### Conventional c-Si module structure

- (1) Front surface is covered with insulating anti-reflection coating.
- (2)Positive/negative charges are accumulated on the cell surface, that result in the power degradation.

#### HIT structure

- (1)Both surfaces are transparent conductive oxide (TCO) layers.
- (2) There is no insulating layer that accumulates electric charges under high-voltage biased condition.

### PID resistance of HIT PV modules is confirmed.